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19CSE211 Computer Organization and Architecture
Lab Handout - 4
Flipflops

Exercise Problems

1. Write a verilog code to implement positive edge triggered D flipflop

```
module dff(D, clk, Q);

input D, clk;
output Q;
reg Q;

always @(posedge clk)
begin
    Q = D;
end

endmodule
```

```
module dff_tb;

reg D, clk;
wire Q;

dff i1(D, clk, Q);

initial
begin
    D = 1'b0; clk=1'b0;
    $monitor("Time:%f, D=%b,
clk=%b, Q=%b", $time, D, clk, Q);
    #5 D = 1'b1; clk = 1'b1;
    #5 D = 1'b0; clk = 1'b0;
    #5 D = 1'b0; clk = 1'b1;
    #5 D = 1'b1; clk = 1'b1;
end

endmodule
```

2. Write a verilog code to implement negative edge triggered T flipflop

```
module tff(T, clk, Q,
reset);

input T, clk, reset;
output Q;
reg Q;

always @(negedge clk)
begin
    if (reset)
        Q = 0;
    else begin
        if(T)
            Q = ~Q;
        else
            Q = Q;
    end

end

endmodule
```

```
module tff_tb;

reg T, clk, reset;
wire Q;

tff i1(T, clk, Q, reset);

always #5 clk = ~clk;

initial
begin
    T = 1'b0; clk = 1'b0; reset =
1;
    $monitor("Time:%f, T=%b,
clk=%b, Q=%b", $time, T, clk, Q);
    #5 reset = 0;
    #5 T = 1'b1;
    #5 T = 1'b1;
    #5 T = 1'b1;
    #5 T = 1'b1;
    #5 $finish;
end

endmodule
```

3. Write a verilog code to implement positive edge triggered JK flipflop

```
module jk(J, K, clk, Q);

input J, K, clk;
output Q;
reg Q;

always @(posedge clk)
begin
    case ({J,K})
         2'b00 :  Q = Q;
         2'b01 :  Q = 0;
         2'b10 :  Q = 1;
         2'b11 :  Q = ~Q;
      endcase
end

endmodule
```

```
module jk_tb;

reg J, K, clk;
wire Q;

jk i1(J, K, clk, Q);

always #5 clk = ~clk;

initial
begin
    J = 1'b0; K = 1'b0; clk = 1'b0;
    $monitor ("Time:%f, J=%b, K=%b,
Q=%b",$time, J, K, Q);
    #5 J = 1'b0; K = 1'b1;
    #10 J = 1'b1; K = 1'b0;
    #10 J = 1'b1; K = 1'b1;
    #10 J = 1'b0; K = 1'b0;
    #10 $finish;
end
endmodule
```

Assignment

1. Write a verilog code to implement T flipflop using JK flipflop. Use the JK flipflop module in Q No.3.