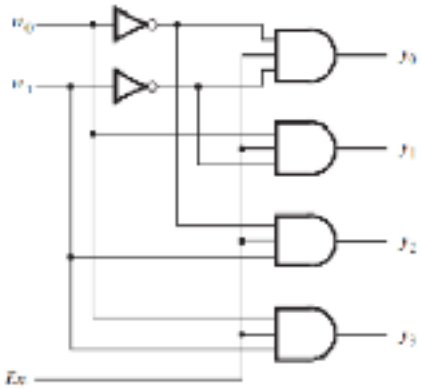
Amrita Vishwa Vidyapeetham
Amrita School of Engineering, Bangalore
Department of Computer Science and Engineering
19CSE211 Computer Organization and Architecture
Lab Handout - 6
Decoders and Encoders

Exercise Problems

1. Write a verilog code to implement 2:4 active high decoder using gate level modeling



```
module decoder2to4_gl(i0, i1, en, y0,
y1, y2, y3);
input i0, i1, en;
output y0, y1, y2, y3;
wire i0bar, i1bar;

not g1(i0bar, i0);
not g2(i1bar, i1);
and g3(y0, i0bar, i1bar, en);
and g4(y1, i0bar, i1, en);
and g5(y2, i0, i1bar, en);
and g6(y3, i0, i1, en);

endmodule
```

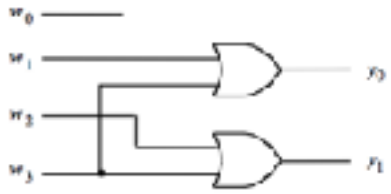
```
module decoder2to4_gl_tb;
reg i0, i1, en;
wire y0, y1, y2, y3;

decoder2to4_gl d1(i0, i1, en, y0, y1,
y2, y3);

initial
begin
     i0=1'b0; i1=1'b0; en=1'b0;
     $monitor("Time:%f, en=%b, i0=%b,
i1=%b, y0=%b, y1=%b, y2=%b, y3=%b",
$time, en, i0, i1, y0, y1, y2, y3);
     #5   en=1'b1; i0=1'b0; i1=1'b0;
     #5   en=1'b1; i0=1'b0; i1=1'b1;
     #5   en=1'b1; i0=1'b1; i1=1'b0;
     #5   en=1'b1; i0=1'b1; i1=1'b1;
     #5   en=1'b0; i0=1'b1; i1=1'b1;
end

endmodule
```

2. Write a verilog code to implement 4:2 encoder using data flow modeling



```
module encoder4to2_dl(i0,
i1, i2, i3, y0, y1);

input i0, i1, i2, i3;
output y0, y1;

assign y0 = i1|i3;
assign y1 = i2|i3;

endmodule
```

```
module encoder4to2_dl_tb;

reg i0, i1, i2, i3;
wire y0, y1;

encoder4to2_dl e1(i0, i1, i2, i3,
y0, y1);

initial
begin
    i0=1'b0; i1=1'b0; i2=1'b0;
i3=1'b0;
    $monitor("Time:%f, i0=%b i1=%b
i2=%b i3=%b, y0=%b, y1=%b",
$time,i0, i1, i2, i3, y0, y1 );
    #5 i0=1'b0; i1=1'b0; i2=1'b0;
i3=1'b0;
    #5 i0=1'b1; i1=1'b0; i2=1'b0;
i3=1'b0;
    #5 i0=1'b0; i1=1'b1; i2=1'b0;
i3=1'b0;
    #5 i0=1'b0; i1=1'b0; i2=1'b1;
i3=1'b0;
    #5 i0=1'b0; i1=1'b0; i2=1'b0;
i3=1'b1;
end

endmodule
```

3. Implement Q.No 2 using array for ports.

```
module encoder4to2_dl(i,
y);

input [3:0] i;
output [1:0] y;

assign y[0] = i[1]|i[3];
assign y[1] = i[2]|i[3];

endmodule
```

```
module encoder4to2_dl_tb;

reg [3:0] i;
wire [1:0] y;

encoder4to2_dl e1(i, y);

initial
begin
    i = 4'b0000;
    $monitor("Time:%f, i=%4b,
y=%2b", $time,i, y );
    #5 i = 4'b0001;
    #5 i = 4'b0010;
    #5 i = 4'b0100;
    #5 i = 4'b1000;
end

endmodule
```

Assignment

1. Write a verilog code to implement an active low 2to4 decoder using data flow modeling
2. Write a verilog code to implement active high 3to8 decoder decoder using 2to4 decoder. Use module from Exercise Q. No. 1.
3. Write a verilog code to implement the following expression using active high 3to8 decoder. Use module from assignment Q. No. 2.

$$f_1(a, b, c) = \Sigma m\ (0,4,6,7)$$