NOTES

1) DO NOT POPULATE IS ABBREVIATED AS DNP.
2) NET NAMES ENDING IN "_N" INDICATE ACTIVE LOW LOGIC SIGNAL.
3) DIFFERENTIAL SIGNAL PAIRS ARE IDENTIFIED BY COMMON ROOT NET NAME ENDING IN "_DP" AND "_DN".

REVISION HISTORY

REV	DESCRIPTION	DATE
A	Skipped.	
B	Build 4 (DVT) changes roll driver outline so needed a new PWB & CCA part number Schematic reuses the Rev B 3DG-302-026 (Build 3, EVT) of the schematic	FEB 25 2015
C	Fix to PWB part number on schematic for DVT.	APRIL 16 2015
D	Remove Programming Header (J3) Bump PWB Rev	MAY 15 2015
E	Change J2's mfg part number to black version	MAY 26 2015

Table of Contents:

Connector List:
J1 = Control Flex Interface (pg 2)
J2 = Motor (pg 2)

Last Reference Designator				
C48	R47	Y1		
D1	SW1			
J2	TP19			
PWB1	U5			

Skipped Reference Designators			
C1-C2	TP11		
C20			
C22			
R30-R33			

RELATED DOCUMENTS

Assembly:	3DG-300-196
Fabrication:	3DG-301-197
Artwork:	3DG-301-197

Designer C. Hinkle, B. Anschutz

Cover Page

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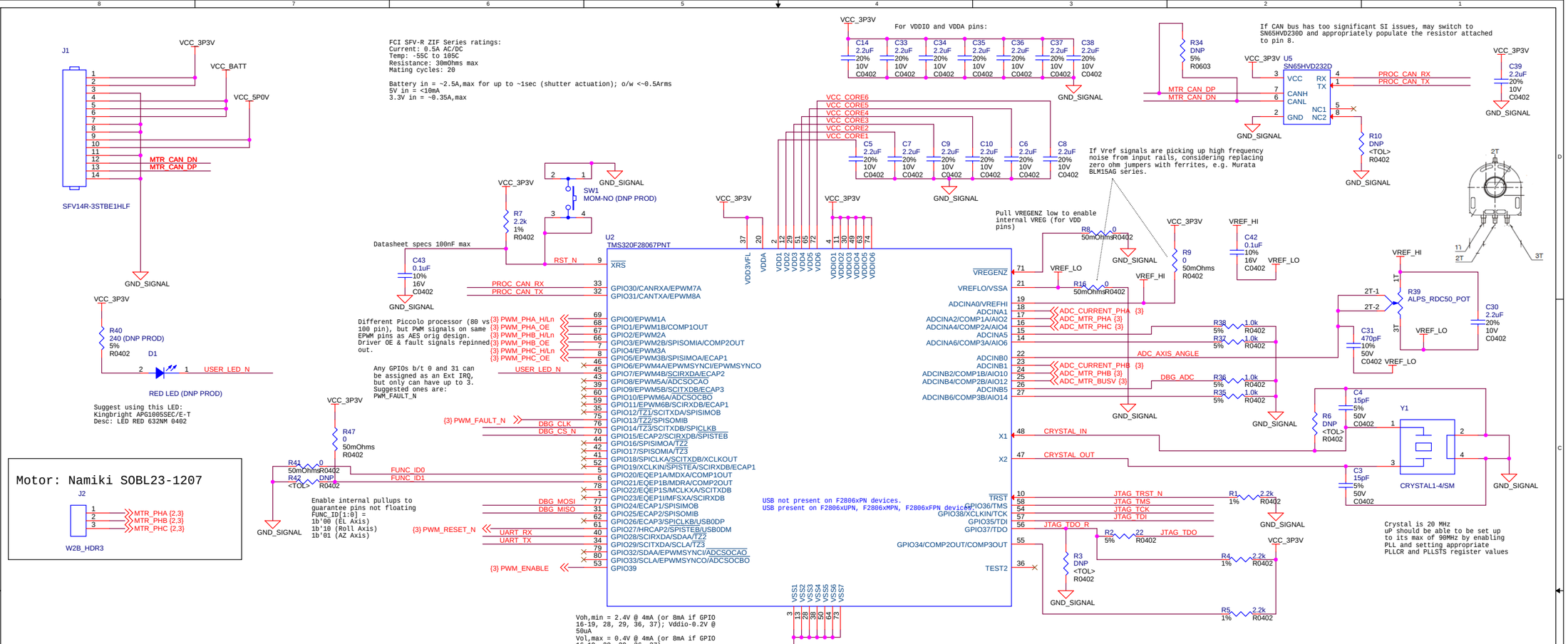


Table 6-1. Boot Mode Selection

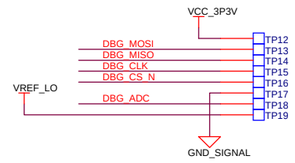
MODE	GPIO37/TDO	GPIO34/COMP2OUT/ COMP3OUT	$\overline{TRST}$	MODE
3	1	1	0	GetMode
2	1	0	0	Wait (see Section 6.1.11 for description)
1	0	1	0	SCI
0	0	0	0	Parallel IO
EMU	x	x	1	Emulation Boot

6.1.10.2 GetMode

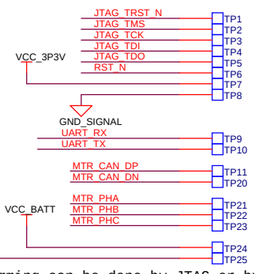
The default behavior of the *GetMode* option is to boot to flash. This behavior can be changed to another boot option by programming two locations in the OTP. If the content of either OTP location is invalid, then boot to flash is used. One of the following loaders can be specified: SCI, SPI, I^2C, CAN, or OTP.

Table 6-2. Peripheral Bootload Pins

BOOTLOADER	PERIPHERAL LOADER PINS
SCI	SCIRXDA (GPIO28) SCITXDA (GPIO29)
Parallel Boot	Data (GPIO31,30,5:0) 28x Control (AIO6) Host Control (AIO12)
SPI	SPISIMOA (GPIO16) SPISOMIA (GPIO17) SPICLKA (GPIO18) SPISTEA (GPIO19)
I^2C	SDAA (GPIO32) SCLA (GPIO33)
CAN	CANRXA (GPIO30) CANTXA (GPIO31)



NOTE: When the on-chip voltage regulator (VREG) is used, the GPIO19, GPIO34, GPIO35, GPIO36, GPIO37, and GPIO38 pins could glitch during power up. If this is unacceptable in an application, 1.8 V could be supplied externally. There is no power-sequencing requirement when using an external 1.8-V supply. However, if the 3.3-V transistors in the level-shifting output buffers of the I/O pins are powered prior to the 1.9-V transistors, it is possible for the output buffers to turn on, causing a glitch to occur on the pin during power up. To avoid this behavior, power the V_{DD} pins prior to or simultaneously with the V_{DDIO} pins, ensuring that the V_{DD} pins have reached 0.7 V before the V_{DDIO} pins reach 0.7 V.



Because of space constraints would like these pads on side 2.
* ~2mm circ pads on 0.1" centers for Solarbotic pogo pins
* ~3x1mm rect pads on 0.1" centers for Samtec SIB series (limited to 5, 10, 15, etc pin options)
* Assy shop ICT fixtures might allow for 35mil pads on maybe 50mil grid with 75-100mil being more likely
* Alternatively, may consider small pitch SMT header like 1.27mm parts from Sullins.

Flash Programming can be done by JTAG or by switching boot mode to SCI (UART I/F) from GetMode
Supported JTAG-based emulators - XDS510 class, XDS560 emulator, XDS100
Recommended serial port programmer utility - codeskin C2Prog

Processor

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Vccbat = 14.8V (14.4V min) - 16.8V (Ziad on 7/18)
Vccbat = 11V - 17V, including ripple (AES spec)

0.39ohms (at 1A and Tj=85C)
speculating 0.6 ohms at Tj=150C

Pcond,rms = 2 * ~rds(on),max * (Irms)^2
Design for Trms = 2mNm (sustained) or 20mNm (shutter actuation for <5sec)
Pcond,rms1 = 2 * 0.6ohms * (2mNm / 21.3mNm/A)^2 = 10mW
Pcond,rms2 = 2 * 0.6ohms * (20mNm / 21.3mNm/A)^2 = 1055mW
Pquies,max = 5mA * 15V = 74mW (includes PWM switching if <50kHz)
Pdiss,tot,rms,1 = 84mW (sustained)
Pdiss,tot,rms,2 = 1130mW (<5sec)
Thja = ~35C/W
Tj,shtdn,min = 150C
Tamb,max = 40C
Pmargin,rms,2 = (150C - 40C - 1.13W*35C/W) / 35C/W = 2.0W
% margin,rms = 180%
Device allows for Pmax,rms,nomargin = (150C - 40C) / 35C/W = 3.1W
Driver peak current (thermal limt) = sqrt(3.1W / (2 * 0.6 ohms)) = 1.61A
(so can't do peak torque for very long)
Driver max current = ~2.5A
Pcond,pk = 2 * 0.7ohms * (2.5A)^2 = ~8.8W
For Namiki motor = 53mNm (much higher than anticipated use)
    & 17.5V (so would actually be supply limited before motor driver limited)

THja = 35C/W
Assumes a JEDEC-standard, high-k (2s2p, 76.2mm x 114.3mm) board in natural convection (tested in ~1cu.ft. enclosure as long as Ta rise is < 110%*Ta,start) as per JESD51-7 and environment per JESD51-2A

Vsense calc
desire +/-3A over 0-3.3V
AD8210 has 20x gain
desire +/-3A over 0-0.165V
Rsense = 0.165V / 6A = 0.028 ohms

0.03 ohms closest available value
Csense range = 0.165V / 0.03 ohms = 5.5A = +/-2.75A
Pinst,max = 2.5A^2 * 0.03ohms = 0.19W
using 1/4W model

ADC is 12bits, so 4095 cnts over 5.5A = 1.34mA/LSB

Rds(on) output FETs probably ~0.3-0.6 ohms for operating temp & Vm over intended range
Hard current limit at 3A,min for >5us,typ (guaranteed operation up to 2.5A)

Vih,min = 2.2V
Vil,max = 0.7V

~100k internal pulldown on all 8 logic inputs

Change to ~550 ohms? Or SW cal'd to this phase lag?

VCC_5P0V
VCC_5P0V_FILT
R15 5% 62 R0402
C16 10uF 10% 25V C0805
GND_SIGNAL

VCC_BATT
C48 10uF 10% 25V C0805
C47 10uF 10% 25V C0805
C46 10uF 10% 25V C0805
C45 10uF 10% 25V C0805
C44 10uF 10% 25V C0805
C32 10uF 10% 25V C0805
C40 10uF 10% 25V C0805
C41 47nF 10% 100V C0603
GND_SIGNAL

C12 0.47uF 10% 6.3V C0402
GND_SIGNAL

U1 DRV8313PWPR
V3P3OUT
VCC_3P3V
R12 100k 5% R0402
{2} PWM_FAULT_N
R11 100k 5% R0402
R13 0 50mOhms R0402
R14 0 50mOhms R0402
GND_SIGNAL

{2} PWM_PHA_H/Ln
{2} PWM_PHA_OE
{2} PWM_PHB_H/Ln
{2} PWM_PHB_OE
{2} PWM_PHC_H/Ln
{2} PWM_PHC_OE
{2} PWM_RESET_N
{2} PWM_ENABLE

VCC_BATT
C13 0.1uF 10% 16V C0402
C11 0.01uF 5% 100V C0603
VM1 VM2 VCP CP1 CP2 OUT1 OUT2 OUT3 PGND1 PGND2 PGND3 NC
GND1 GND2 GND3 GND4 TPAD
GND_SIGNAL

VCC_BATT
R22 51k 1% R0402
R23 5.1k 1% R0402
C26 2.2uF 20% 10V C0402
ADC_MTR_BUSV {2}
GND_SIGNAL

VREF_HI VREF_LO
U3 AD8210YRZ
IN+ IN- VREF1 VREF2 V+ OUT NC GND
C21 47nF 10% 100V C0603
C15 0.1uF 10% 16V C0402
VCC_5P0V_FILT
IM_CURRENT_PHA
R21 1% 2.2k R0402
ADC_CURRENT_PHA {2}
C24 470pF 10% 50V C0402
VREF_LO
C17 2.2uF 20% 10V C0402
GND_SIGNAL
R46 10 1% R0402
R45 10 1% R0402
R17 1% 0.03 R0805
MTR_PHA {2,3}

VREF_HI VREF_LO
U4 AD8210YRZ
C23 47nF 10% 100V C0603
C18 0.1uF 10% 16V C0402
VCC_5P0V_FILT
IM_CURRENT_PHB
R20 1% 2.2k R0402
ADC_CURRENT_PHB {2}
C25 470pF 10% 50V C0402
VREF_LO
C19 2.2uF 20% 10V C0402
GND_SIGNAL
R43 10 1% R0402
R44 10 1% R0402
R18 1% 0.03 R0805
MTR_PHB {2}
R19 1% 0.03 R0805
MTR_PHC {2}

{2,3} MTR_PHA
R24 51k 1% R0402
R25 5.1k 1% R0402
C27 47nF 10% 10V C0402
ADC_MTR_PHC {2}
R26 51k 1% R0402
R27 5.1k 1% R0402
C28 47nF 10% 10V C0402
ADC_MTR_PHB {2}
R28 51k 1% R0402
R29 5.1k 1% R0402
C29 47nF 10% 10V C0402
ADC_MTR_PHA {2}
GND_SIGNAL

Motor Drive

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