NOTES

1) DO NOT POPULATE IS ABBREVIATED AS DNP.
2) NET NAMES ENDING IN "_N" INDICATE ACTIVE LOW LOGIC SIGNAL.
3) DIFFERENTIAL SIGNAL PAIRS ARE IDENTIFIED BY COMMON ROOT NET NAME ENDING IN "_DP" AND "_DN".

REVISION HISTORY

REV	DESCRIPTION	DATE
Prev A	Initial Gen 2 Prototype Design Release	DEC 23 2014
Prev B	Gen 2 Second Prototype Release Added R31, R44, U14, and changed U12 Moved R72 to different net Incorporated analog potentiometer into board Renamed board to be "Rigid-Flex" Deleted J8 Added R74, C81 Changed pullup voltage on R40 Added U15, R45, R46, R47, and C82	JAN 22 2015
A	New part numbers Added testpoints for CAN, Motor Phases, Battery and 5V power. Changed control flex connector	
B	Fix to PWB part number on schematic for DVT.	APRIL 16 2015
C	Added LDO for HB_INTR_N pull-up. Changed R72 to 10k pull-up. Changed U15 EN connection to HB_VON_3P3. Added pull-down to HB_VON_OUT	MAY 15 2015
D	J3 part number changed for black version	MAY 26 2015

Table of Contents:

Connector List:

J1 = n/a
J2 = n/a
J3 = Motor (pg 2)
J4 = Programming Header (pg 2)
J5 = n/a
J6 = GoPro HEROBus Interface (pg 4)
J7 = Control Flex Interface (pg 2)
J8 = deleted

PWB1

PWB Rev B

Last Reference Designator				
C82	PWB1	TP21		
D4	Q8	U15		
J8	R74	Y1		
L2	SW1			

Skipped Reference Designators			
C1-C14	J2	R1-R3	
C30	J5	R48	
D1	L1	TP11	
J1	Q1-Q6	U1-U3	

RELATED DOCUMENTS

Assembly:	3DG-300-236
Fabrication:	3DG-301-237
Artwork:	3DG-301-237

Designer C. HINKLE, B. ANSCHUTZ

Cover Page

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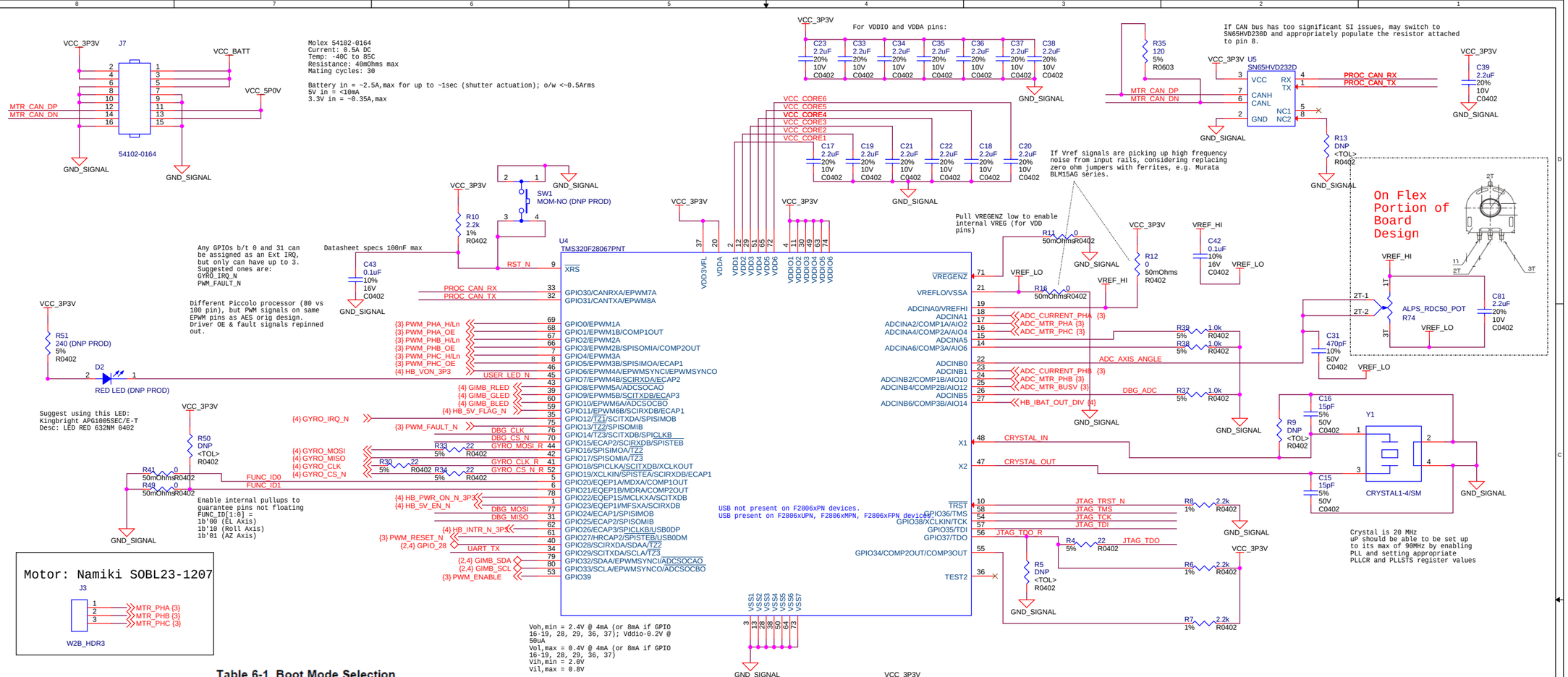


Table 6-1. Boot Mode Selection

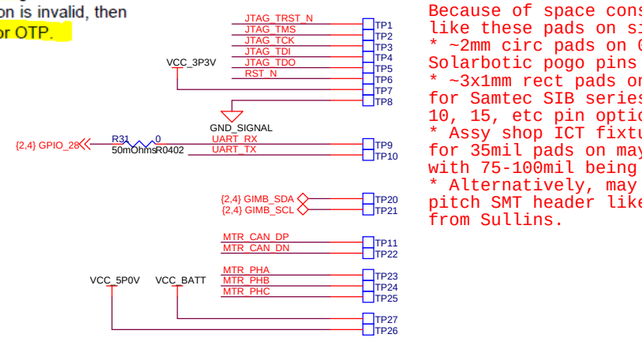
MODE	GPIO37/TDO	GPIO34/COMP2OUT/ COMP3OUT	$\overline{TRST}$	MODE
3	1	1	0	GetMode
2	1	0	0	Wait (see Section 6.1.11 for description)
1	0	1	0	SCI
0	0	0	0	Parallel IO
EMU	x	x	1	Emulation Boot

6.1.10.2 GetMode

The default behavior of the *GetMode* option is to boot to flash. This behavior can be changed to another boot option by programming two locations in the OTP. If the content of either OTP location is invalid, then boot to flash is used. One of the following loaders can be specified: SCI, SPI, I²C, CAN, or OTP.

Table 6-2. Peripheral Bootload Pins

BOOTLOADER	PERIPHERAL LOADER PINS
SCI	SCIRXDA (GPIO28) SCITXDA (GPIO29)
Parallel Boot	Data (GPIO31,30,5:0) 28x Control (AIO6) Host Control (AIO12)
SPI	SPISIMOA (GPIO16) SPISOMIA (GPIO17) SPICLKA (GPIO18) SPISTEA (GPIO19)
I²C	SDAA (GPIO32) SCLA (GPIO33)
CAN	CANRXA (GPIO30) CANTXA (GPIO31)



Because of space constraints would like these pads on side 2.
* ~2mm circ pads on 0.1" centers for Solarbotic pogo pins
* ~3x1mm rect pads on 0.1" centers for Samtec SIB series (limited to 5, 10, 15, etc pin options)
* Assy shop ICT fixtures might allow for 35mil pads on maybe 50mil grid with 75-100mil being more likely
* Alternatively, may consider small pitch SMT header like 1.27mm parts from Sullins.

Flash Programming can be done by JTAG or by switching boot mode to SCI (UART I/F) from GetMode
Supported JTAG-based emulators - XDS510 class, XDS560 emulator, XDS100
Recommended serial port programmer utility - codeskin C2Prog

NOTE: When the on-chip voltage regulator (VREG) is used, the GPIO19, GPIO34, GPIO35, GPIO36, GPIO37, and GPIO38 pins could glitch during power up. If this is unacceptable in an application, 1.8 V could be supplied externally. There is no power-sequencing requirement when using an external 1.8-V supply. However, if the 3.3-V transistors in the level-shifting output buffers of the I/O pins are powered prior to the 1.9-V transistors, it is possible for the output buffers to turn on, causing a glitch to occur on the pin during power up. To avoid this behavior, power the V_{DD} pins prior to or simultaneously with the V_{DDIO} pins, ensuring that the V_{DD} pins have reached 0.7 V before the V_{DDIO} pins reach 0.7 V.

Processor

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Vccbat = 14.8V (14.4V min) - 16.8V (Ziad on 7/18)
Vccbat = 11V - 17V, including ripple (AES spec)

0.39ohms (at 1A and Tj=85C)
speculating 0.6 ohms at Tj=150C

Pcond,rms = 2 * ~rds(on),max * (Irms)^2
Design for Trms = 2mNm (sustained) or 20mNm (shutter actuation for <5sec)
Pcond,rms1 = 2 * 0.6ohms * (2mNm / 21.3mNm/A)^2 = 10mW
Pcond,rms2 = 2 * 0.6ohms * (20mNm / 21.3mNm/A)^2 = 1055mW
Pquies,max = 5mA * 15V = 74mW (includes PWM switching if <50kHz)
Pdiss,tot,rms,1 = 84mW (sustained)
Pdiss,tot,rms,2 = 1130mW (<5sec)
Thja = ~35C/W
Tj,shtdn,min = 150C
Tamb,max = 40C
Pmargin,rms,2 = (150C - 40C - 1.13W*35C/W) / 35C/W = 2.0W
% margin,rms = 180%
Device allows for Pmax,rms,nomargin = (150C - 40C) / 35C/W = 3.1W
Driver peak current (thermal limt) = sqrt(3.1W / (2 * 0.6 ohms)) = 1.61A
(so can't do peak torque for very long)
Driver max current = ~2.5A
Pcond,pk = 2 * 0.7ohms * (2.5A)^2 = ~8.8W
For Namiki motor = 53mNm (much higher than anticipated use)
    & 17.5V (so would actually be supply limited before motor driver limited)

THja = 35C/W
Assumes a JEDEC-standard, high-k (2s2p, 76.2mm x 114.3mm) board in natural convection (tested in ~1cu.ft. enclosure as long as Ta rise is < 110%*Ta,start) as per JESD51-7 and environment per JESD51-2A

Vsense calc
desire +/-3A over 0-3.3V
AD8210 has 20x gain
desire +/-3A over 0-0.165V
Rsense = 0.165V / 6A = 0.028 ohms

0.03 ohms closest available value
Csense range = 0.165V / 0.03 ohms = 5.5A = +/-2.75A
Pinst,max = 2.5A^2 * 0.03ohms = 0.19W
using 1/4W model

ADC is 12bits, so 4095 cnts over 5.5A = 1.34mA/LSB

Rds(on) output FETs probably ~0.3-0.6 ohms for operating temp & Vm over intended range
Hard current limit at 3A,min for >5us,typ (guaranteed operation up to 2.5A)

Vih,min = 2.2V
Vil,max = 0.7V

~100k internal pulldown on all 8 logic inputs

Change to ~550 ohms?
Or SW cal'd to this phase lag?

VCC_5P0V
R19 62 5% R0402
VCC_5P0V_FILT
C28 10uF 10% 25V C0805
GND_SIGNAL

VCC_BATT
C57 10uF 10% 25V C0805
C56 10uF 10% 25V C0805
C55 10uF 10% 25V C0805
C54 10uF 10% 25V C0805
C53 10uF 10% 25V C0805
C58 10uF 10% 25V C0805
C49 10uF 10% 25V C0805
C50 47nF 10% 100V C0603
GND_SIGNAL

C25 0.47uF 10% 6.3V C0402
GND_SIGNAL

U6 DRV8313PWPR
VCC_BATT
C26 0.1uF 10% 16V C0402
15 V3P3OUT
4 VM1
11 VM2
3 VCP
1 CP1
2 CP2
C24 0.01uF 5% 100V C0603
5 OUT1
8 OUT2
9 OUT3
6 PGND1
7 PGND2
10 PGND3
21 NC
14 GND1
20 GND2
23 GND3
24 GND4
25 TPAD
GND_SIGNAL

VCC_3P3V
R15 100k 5% R0402
{2} PWM_FAULT_N
{2} PWM_PHA_H/Ln
{2} PWM_PHA_OE
{2} PWM_PHB_H/Ln
{2} PWM_PHB_OE
{2} PWM_PHC_H/Ln
{2} PWM_PHC_OE
{2} PWM_RESET_N
{2} PWM_ENABLE
27 IN1
26 EN1
25 IN2
24 EN2
23 IN3
22 EN3
16 RESET
17 SLEEP
18 FAULT

VCC_3P3V
R14 100k 5% R0402
R17 0 50mOhms R0402
R18 0 50mOhms R0402
19 COMPO
12 COMPP
13 COMPN
GND_SIGNAL

VREF_HI
VREF_LO
U7 AD8210YRZ
8 IN+
1 IN-
7 VREF1
3 VREF2
6 V+
5 OUT
4 NC
2 GND
VCC_5P0V_FILT
IM_CURRENT_PHA
R24 2.2k 1% R0402
ADC_CURRENT_PHA {2}
C27 0.1uF 10% 16V C0402
C29 2.2uF 20% 10V C0402
C45 470pF 10% 50V C0402
VREF_LO
GND_SIGNAL

C41 47nF 10% 100V C0603
R55 10 1% R0402
R54 10 1% R0402
R20 0.03 1% R0805
MTR_PHA {2,3}

U8 AD8210YRZ
VCC_5P0V_FILT
IM_CURRENT_PHB
R23 2.2k 1% R0402
ADC_CURRENT_PHB {2}
C32 0.1uF 10% 16V C0402
C40 2.2uF 20% 10V C0402
C46 470pF 10% 50V C0402
C44 47nF 10% 100V C0603
R52 10 1% R0402
R53 10 1% R0402
R21 0.03 1% R0805
R22 0.03 1% R0805
MTR_PHB {2}
MTR_PHC {2}

{2,3} MTR_PHA
R27 51k 1% R0402
R28 5.1k 1% R0402
ADC_MTR_PHC {2}
C48 47nF 10% 10V C0402
R29 51k 1% R0402
R56 5.1k 1% R0402
ADC_MTR_PHB {2}
C51 47nF 10% 10V C0402
R57 51k 1% R0402
R58 5.1k 1% R0402
ADC_MTR_PHA {2}
C52 47nF 10% 10V C0402
GND_SIGNAL

VCC_BATT
R25 51k 1% R0402
R26 5.1k 1% R0402
ADC_MTR_BUSV {2}
C47 2.2uF 20% 10V C0402
GND_SIGNAL

Motor Drive

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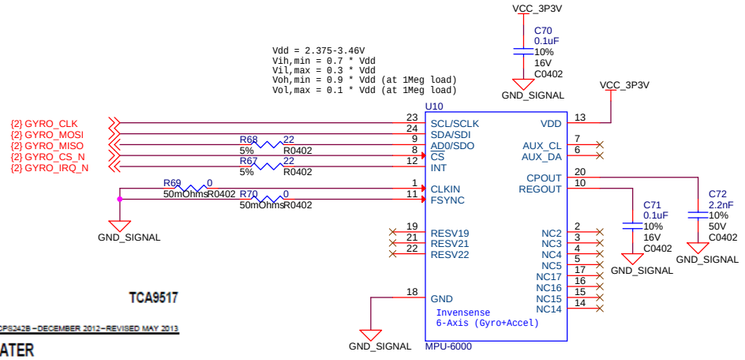
11.4.2 Exposed Die Pad Precautions

The MPU-60X0 has very low active and standby current consumption. The exposed die pad is not required for heat sinking, and should not be soldered to the PCB. Failure to adhere to this rule can induce performance changes due to package thermo-mechanical stress. There is no electrical connection between the pad and the CMOS.



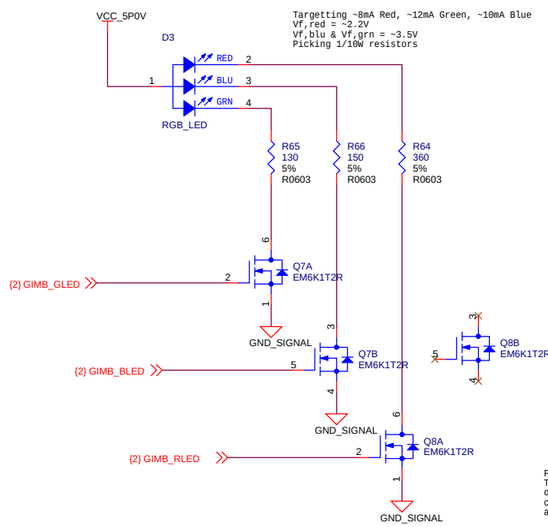
TCA9517

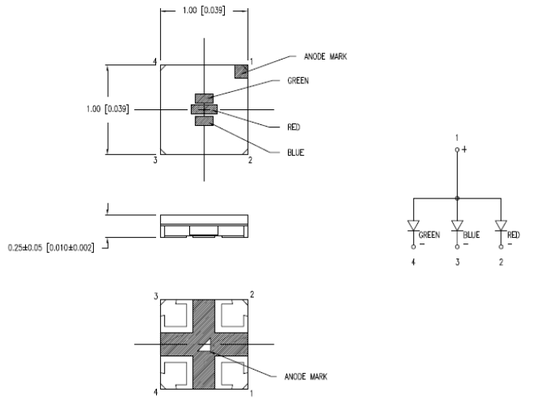
SCPS242B – DECEMBER 2012 – REVISED MAY 2013

I²C BUS REPEATER

Check for Samples: TCA9517

- 5.5-V Tolerant I²C and Enable Input Support Mixed-Mode Signal Operation
- Lockup-Free Operation
- Accommodates Standard Mode and Fast Mode I²C Devices and Multiple Masters
- Powered-Off High-Impedance I²C Pins



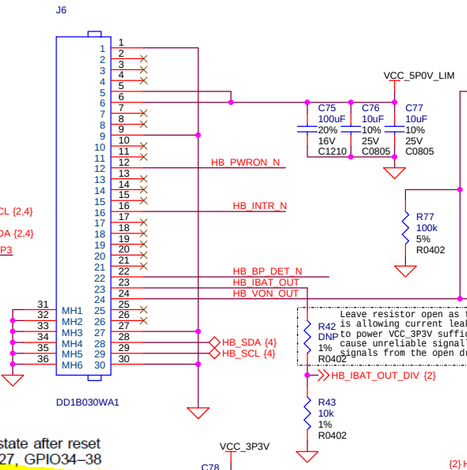


For HB_INTR_N, GoPro says:
This pin is weakly pulled up to 3.0V internally on the camera. Drive this pin using an open-collector driver in conjunction with an external 33kOhm pull-up resistor to 3.0V, but only after the camera has been turned on (to avoid input leakage currents into the camera). Refer to the circuit example above. Vil(min,max) = (0V, 0.7V). Vih(min,max) = (2.6V, 3.0V).

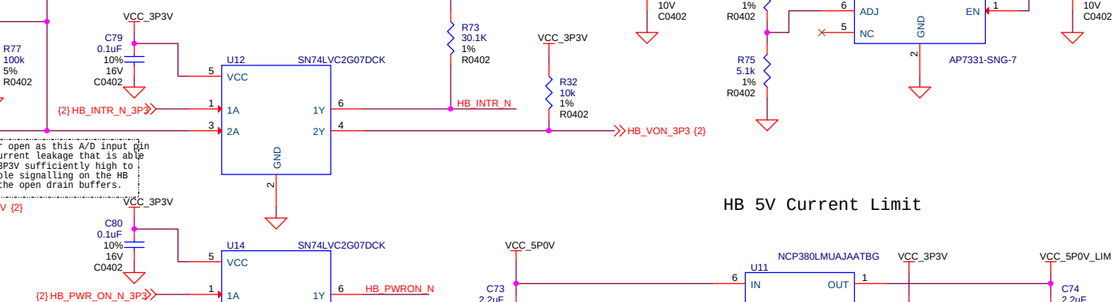
Circuit example uses a Zener to regulate HB_VON_OUT to 3V, but this requires too much current to keep Vz at 3V. Using LDO instead.

Output of LDO is centered at 2.76V, so we don't exceed Vih(max)=3.0V (assuming this is absolute/clamping max voltage)

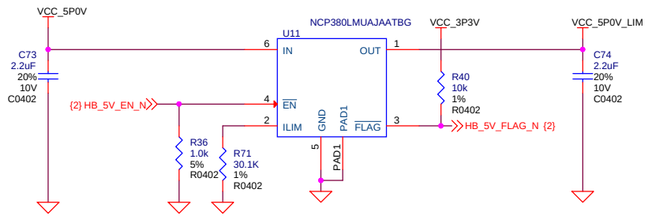
HeroBus Connector



HeroBus Open-Drain and Level Shift



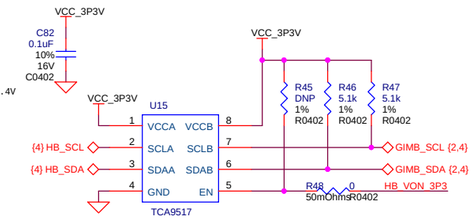
HB 5V Current Limit



TCA9517:
Vdd = 2.7-5.5V
Vih,min = 0.7 * Vdd
Vil,max (side A) = 0.3 * Vdd
Vol,max (side A) = 0.2V
Vil,max (aka Vilc, side B) = 0.4V
Vol,max (side B) = 0.6V

24LC00 EEPROM:
Vih,min = 0.7 * Vdd = ~2.4V
Vil,max = 0.3 * Vdd = ~0.98V
Vol,max = 0.4V @ <3mA

TMS320F2806x Piccolo uP:
Vih,min = 2V
Vil,max = 0.8V
Vol,max = 0.4V @ 4mA

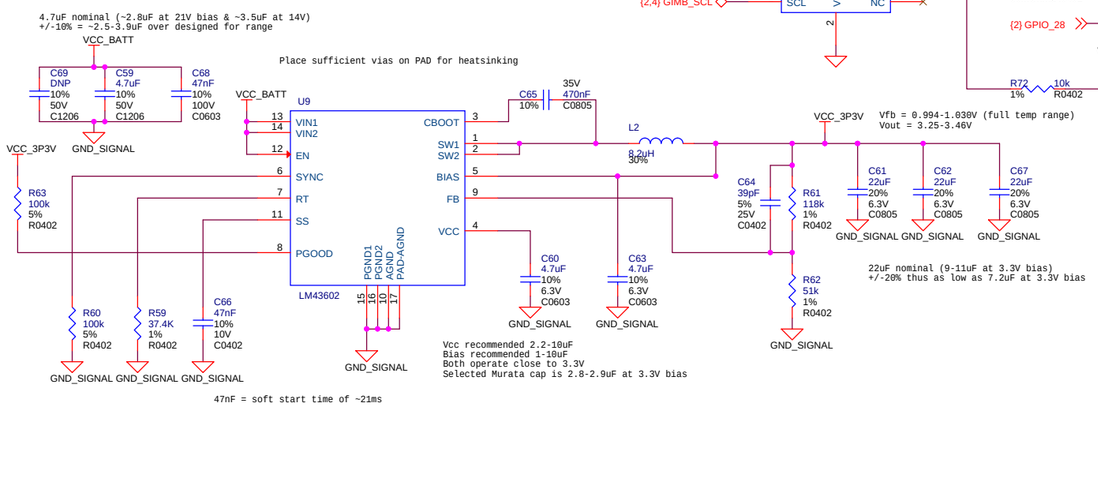


I2C buffer not for level translation but for:
1. High Iol,max (side A) spec of 6mA (>4mAmin in GoPro spec)
2. Low Vol,max (side A) spec of 0.2V (GoPro has no Vil,max spec)
3. Off isolation to Piccolo uP GPIOs when 3.3V not present but when GoPro on and installed in gimbal

EN connection prevents enabled U15 from pulling SCLB/SDAB low from floating SCLA/SDAA when GoPro isn't connected or isn't on.

Power Sequencing

There is no power sequencing requirement needed to ensure the device is in the proper state after reset or to prevent the I/Os from glitching during power up or power down (GPIO19, GPIO26–27, GPIO34–38 do not have glitch-free I/Os). No voltage larger than a diode drop (0.7 V) above V_{DDIO} should be applied to any digital pin (for analog pins, it is 0.7 V above V_{DDA}) prior to powering up the device. Voltages applied to pins on an unpowered device can bias internal p-n junctions in unintended ways and produce unpredictable results.



Misc

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