

HW6

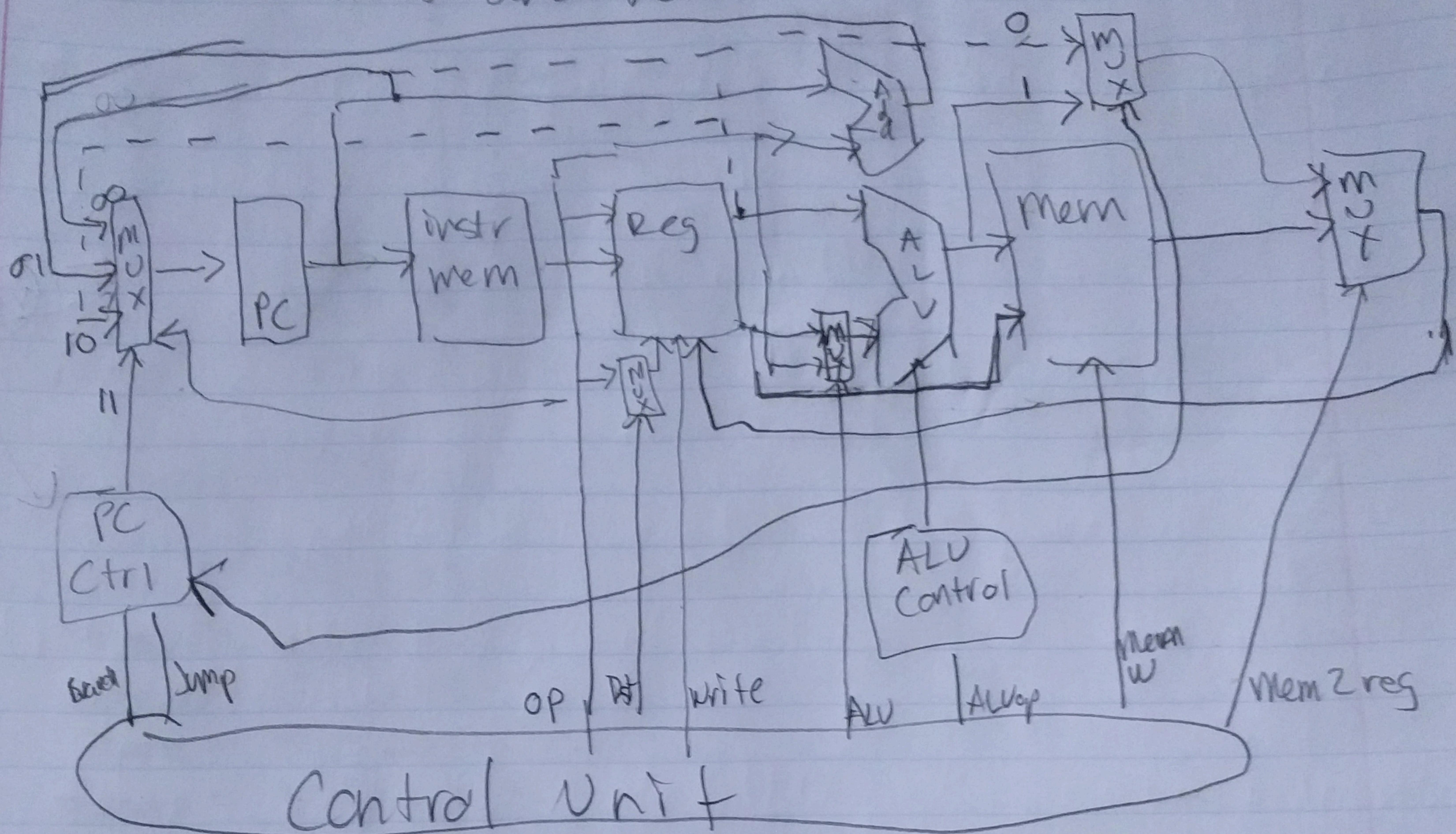
1. a.) No register can be written in the register file.
 - All R-type instructions that write to a destination/register
 - All I-type instrs with a destination register
- b.) RegDst stuck at rt, cant be rd
 - All R-type instrs with destination register, will write to other source reg rt
- c.) ALU is stuck having the second operand coming from the register.
 - All I-type instrs with an immediate constant
- d.) Value written to the register is always from ALU, cant be from memory.
 - Any of the load instrs
- e.) It wont indicate the presence of a branch instr.
 - All the branch instructions

HWP

- 2.
- a.) All instructions will write something into a register
 - Store, branch, and jump instructions wont work properly.
 - b.) RegDst stuck at rd, cant be rt.
 - All I-type instrs with a destination rt.
 - c.) ALU is stuck with its second operand being an immediate constant.
 - All R-type with a second source register,
 - d.) Value written to register is always from memory, cant be from ALU
 - Any Instr that use the ALU , ex. arithmetic instrs add, sub
 - e.) Thanks branch instr is always present.
 - All non-branch instructions

HW6

3. Dotted lines are new



$$.75 + .60 = 1.35$$

HWP

4. a.)

Instr Type	Instr Memory	Reg Read	ALU	Data Mem	Reg Write	Total
ALU	190	150	190		150	680
* & /	190	150	550		150	1040
Load	190	150	190	190	150	870
Store	190	150	190	190		720
Branch	190	150	190			530
Jump	190	150				340

$$\text{clk cycle} = 1040 \text{ ps}$$

$$\text{b.) ALU} = 4 \text{ cycles}$$

$$* \& / = 6 \text{ cycles}$$

$$\text{Load} = 5 \text{ cycles}$$

$$\text{Store} = 4 \text{ cycles}$$

$$\text{Branch} = 3 \text{ cycles}$$

$$\text{Jump} = 2 \text{ cycles}$$

$$\text{Avg} = .3(4) + .15(6) + .15(5) + .15(4) + .15(3) + .1(2) = 4.1$$

$$\text{Speedup} = \frac{1040}{200(4.1)} = 1.268$$