



TRABALHO #3: RELATÓRIO ULA

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Curso: Tecnologia em Análise e Desenvolvimento de Sistemas

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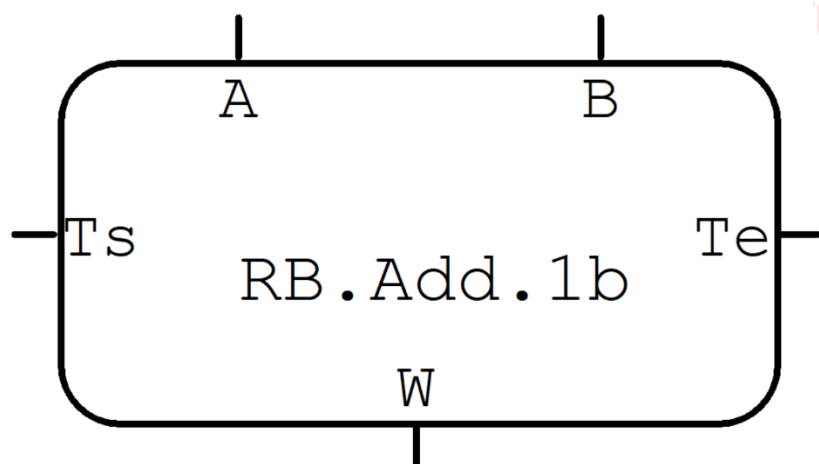
São José do Rio Preto, 24 de Maio de 2023.

Sumário

Somador 1 bit.....	1
a0 – ADD 1 bit.....	1
a1 – Tabela Verdade.....	1
a3 – Circuito Lógico	2
Somador 8 bits	3
b0 – ADD 8 bits	3
b1 – Tabela Verdade.....	3
b2 – Circuito Lógico	3
Buffer 8 bits	4
c0 – BUFFER 8 bits	4
c1 – Tabela Verdade	4
c2 – Circuito Lógico.....	4
Nand 8 bits	5
d0 – NAND 8 bits	5
d1 – Tabela Verdade.....	5
d2 – Circuito Lógico	5
Subtrator 1 bit	6
e0 – SUB 1 bit.....	6
e1 – Tabela Verdade	6
e2 – Circuito Lógico.....	7
Subtrator 8 bits.....	8
f0 – SUB 8 bits	8
f1 – Tabela Verdade	8
f2 – Circuito Lógico	8
Decode 2 bits	9
g0 – DECODE 2 bits	9
g1 – Tabela Verdade.....	9
g2 – Circuito Lógico	10
MUX 4x1	11
h0 – MUX 4x1	11
h1 – Tabela Verdade.....	11
h2 – Circuito Lógico	12
ULA 8 BITS	13
i0 – ULA 8 bits	13
i1 – Tabela Verdade.....	13
i2 – Circuito Lógico	14
Referências.....	14

Somador 1 bit

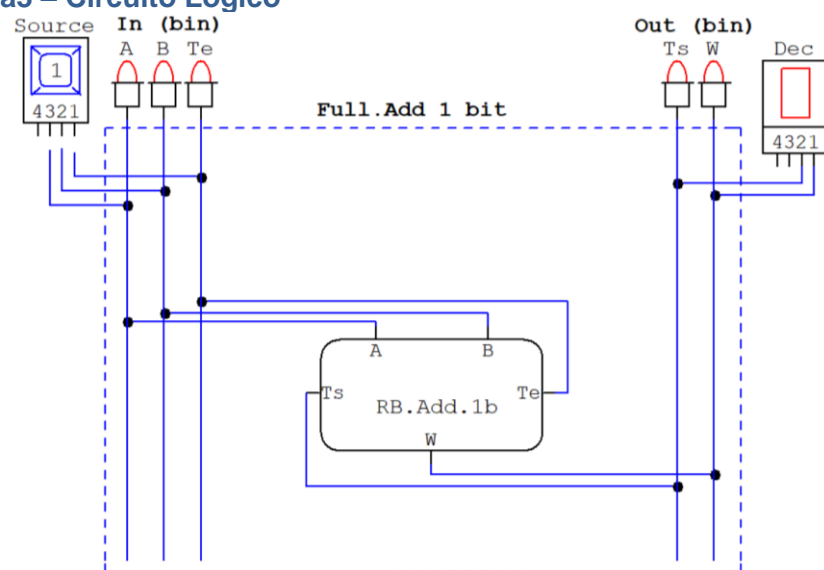
a0 – ADD 1 bit



a1 – Tabela Verdade

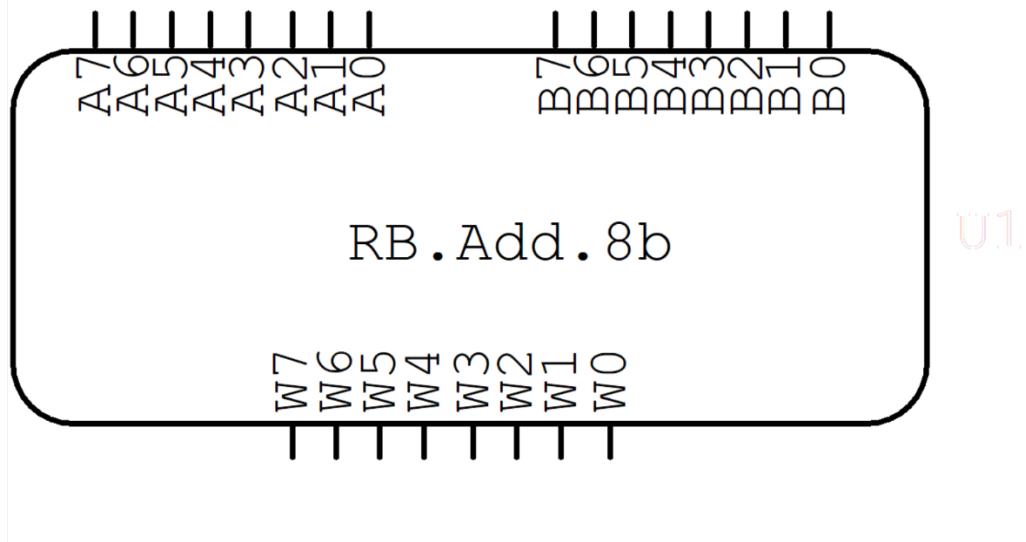
Dec	A	B	Te	Ts	W
0	0	0	0	0	0
1	0	0	1	0	1
2	0	1	0	0	1
3	0	1	1	1	0
4	1	0	0	0	1
5	1	0	1	1	0
6	1	1	0	1	0
7	1	1	1	1	1

a3 – Circuito Lógico

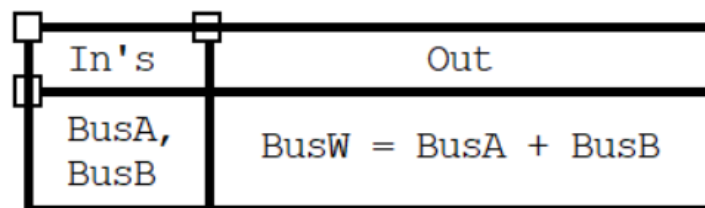


Somador 8 bits

b0 – ADD 8 bits

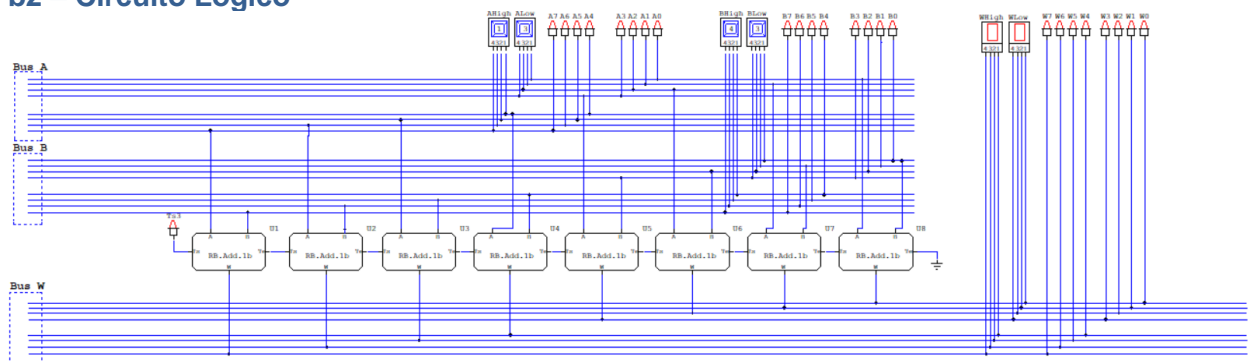


b1 – Tabela Verdade



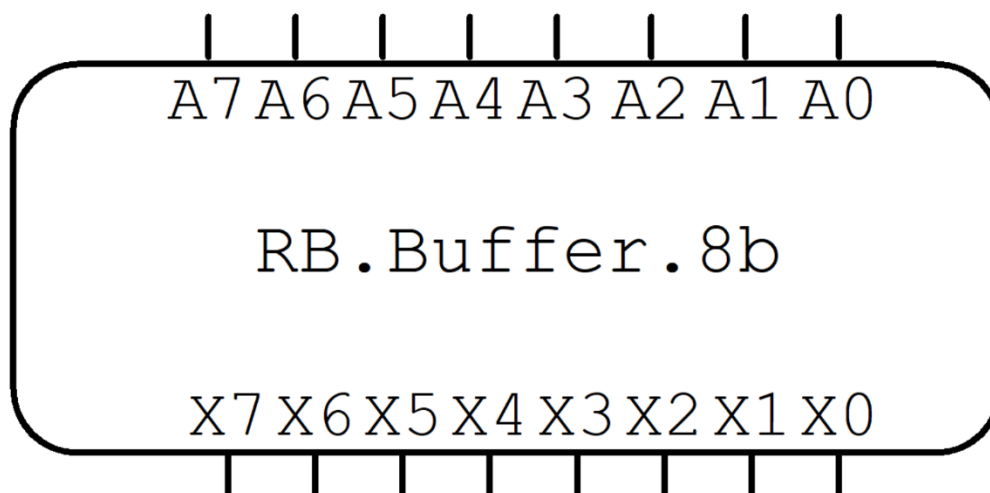
Aritmético

b2 – Circuito Lógico

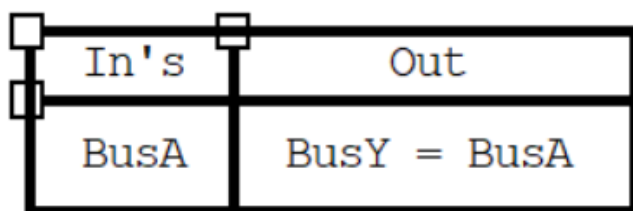


Buffer 8 bits

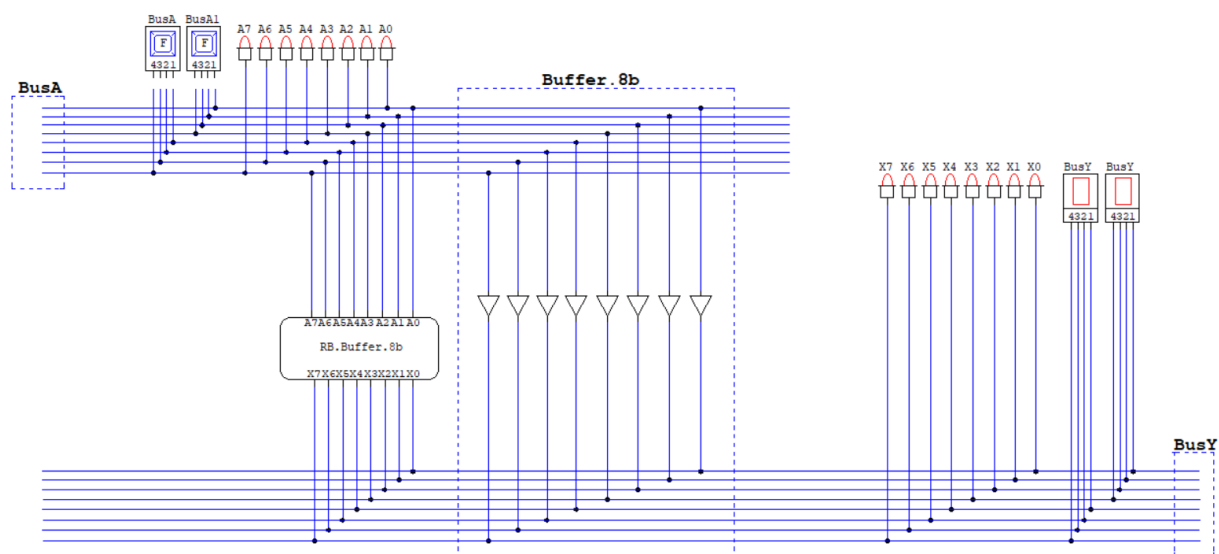
c0 – BUFFER 8 bits



c1 – Tabela Verdade

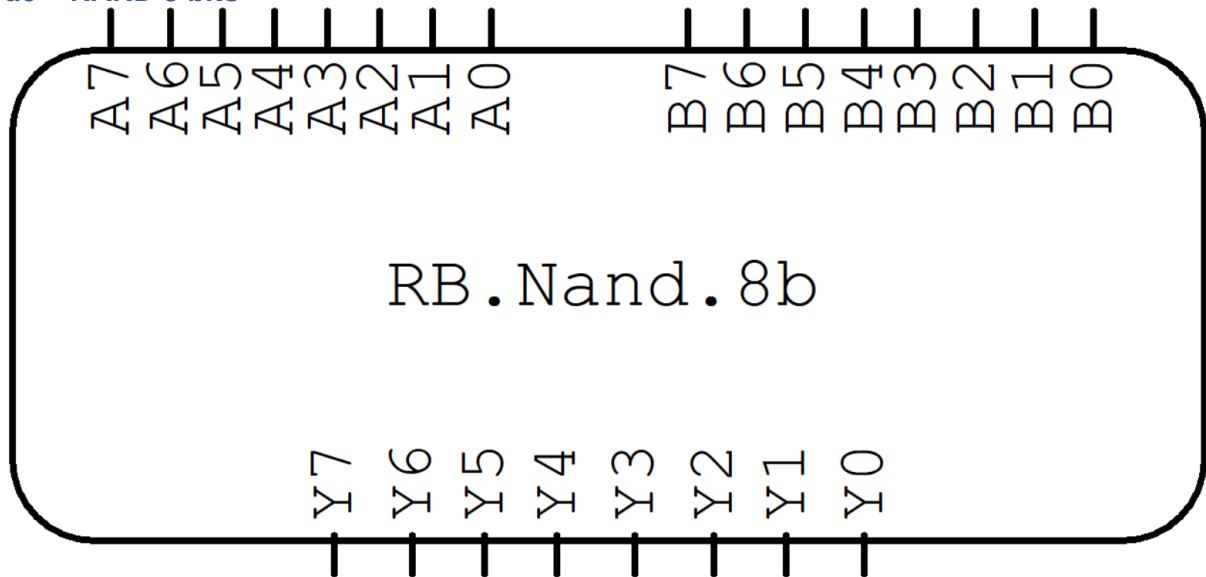


c2 – Circuito Lógico

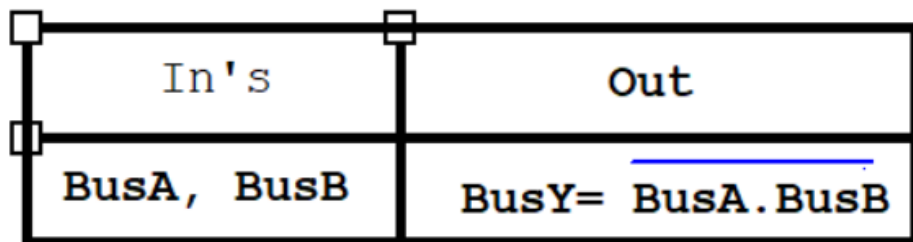


Nand 8 bits

d0 – NAND 8 bits

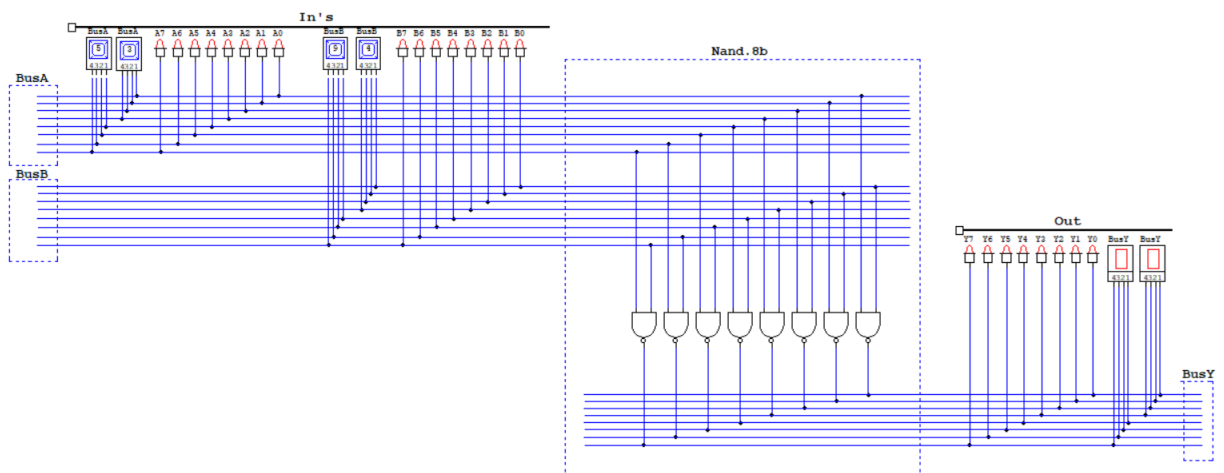


d1 – Tabela Verdade



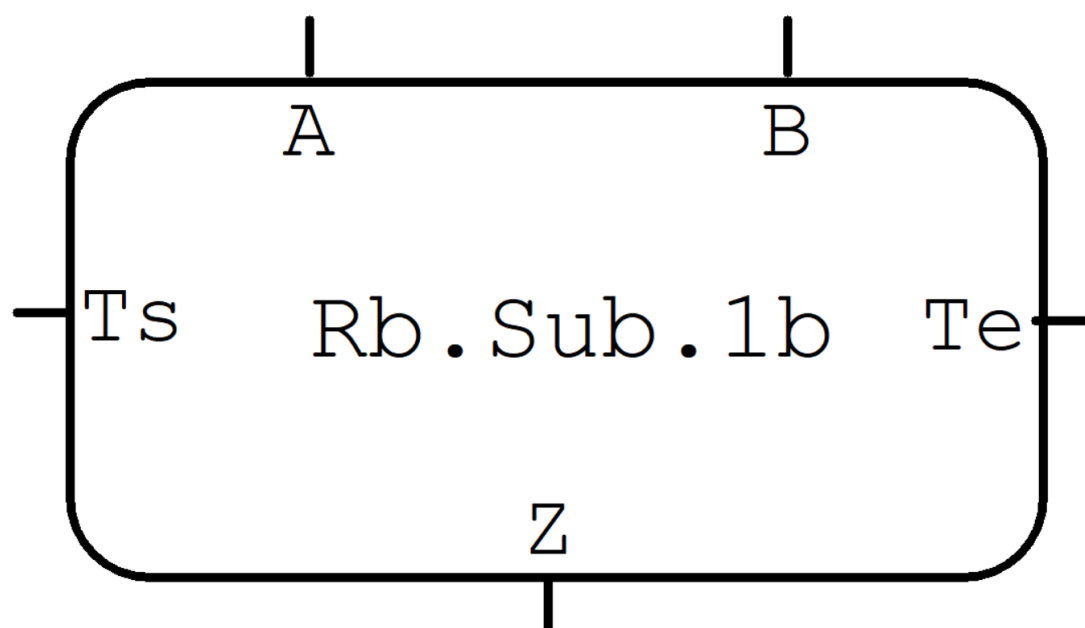
Aritmético

d2 – Circuito Lógico



Subtrator 1 bit

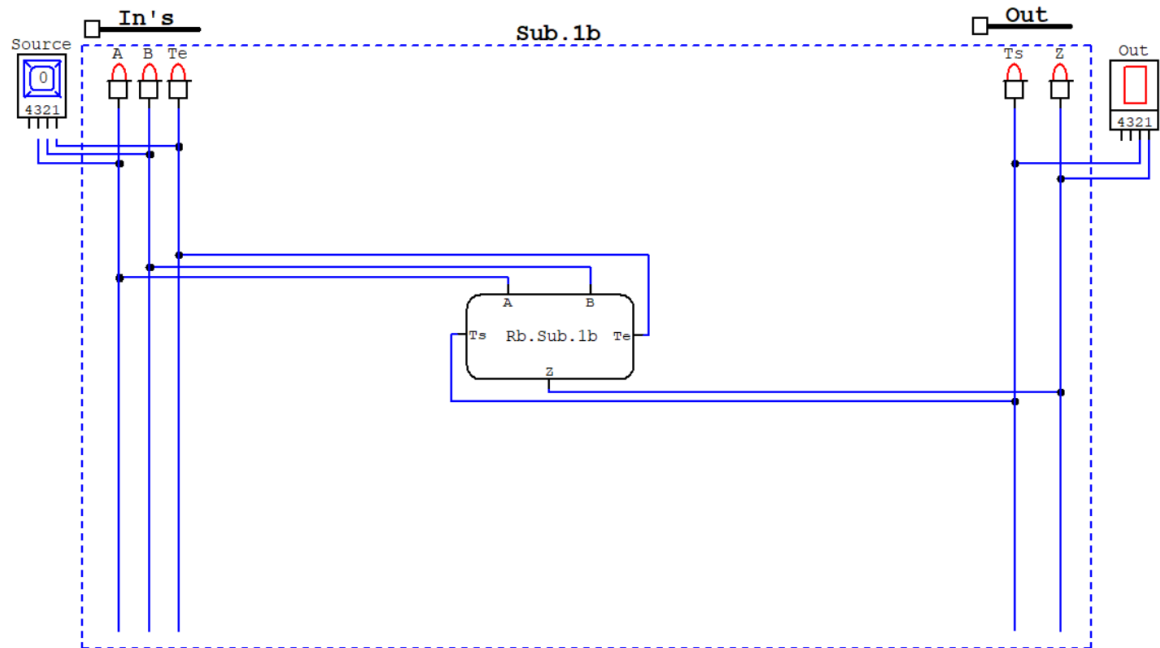
e0 – SUB 1 bit



e1 – Tabela Verdade

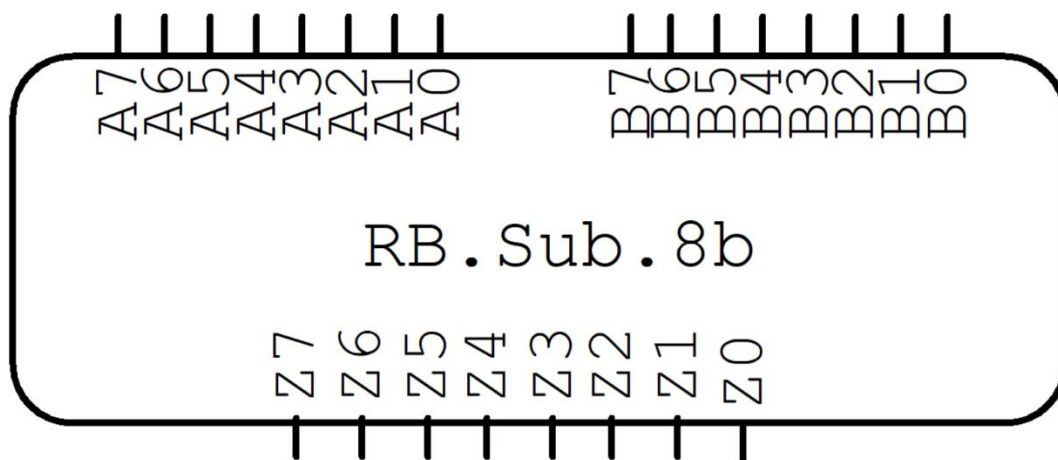
Dec	A	B	Te	Ts	Z
0	0	0	0	0	0
1	0	0	1	1	1
2	0	1	0	1	1
3	0	1	1	1	0
4	1	0	0	0	1
5	1	0	1	0	0
6	1	1	0	0	0
7	1	1	1	1	1

e2 – Circuito Lógico



Subtrator 8 bits

f0 – SUB 8 bits

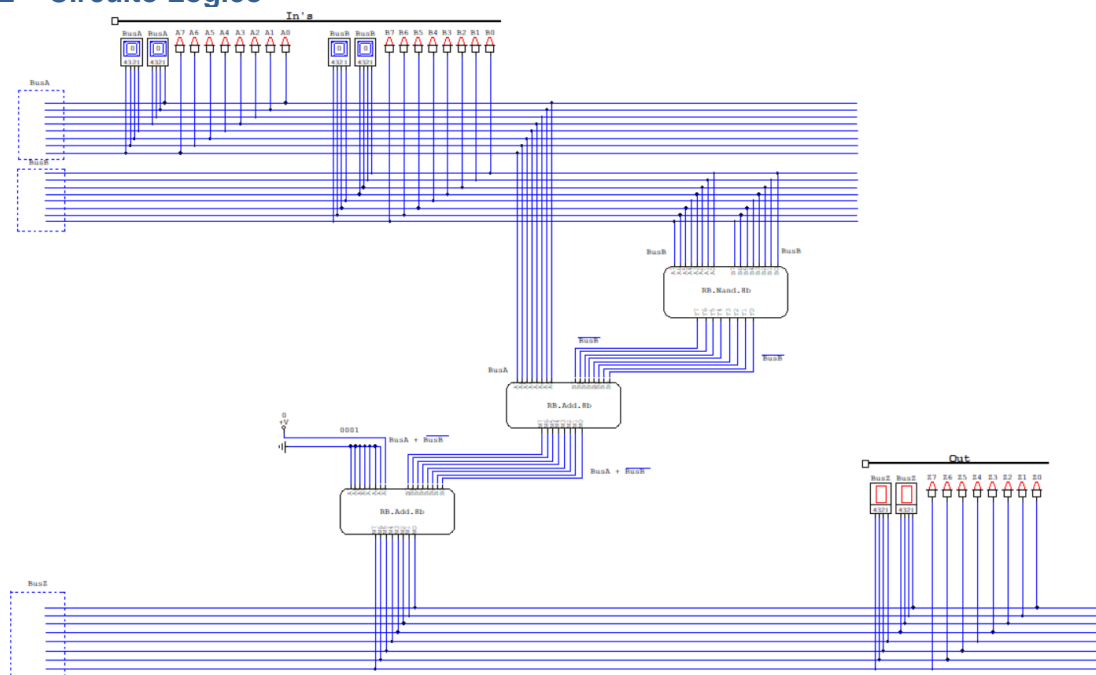


f1 – Tabela Verdade

In's	Out
BusA, BusB	$\text{BusZ} = \text{BusA} - \text{BusB}$

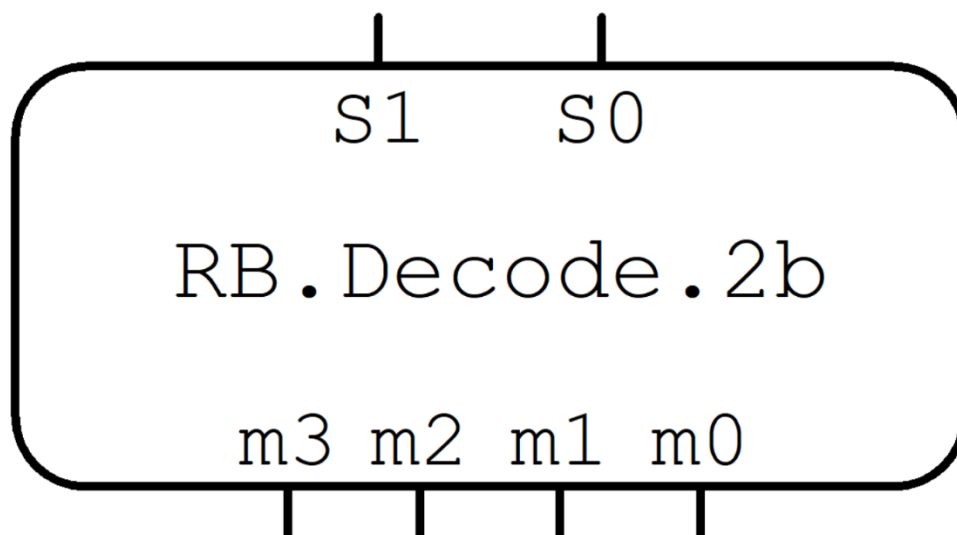
Aritmético

f2 – Circuito Lógico



Decode 2 bits

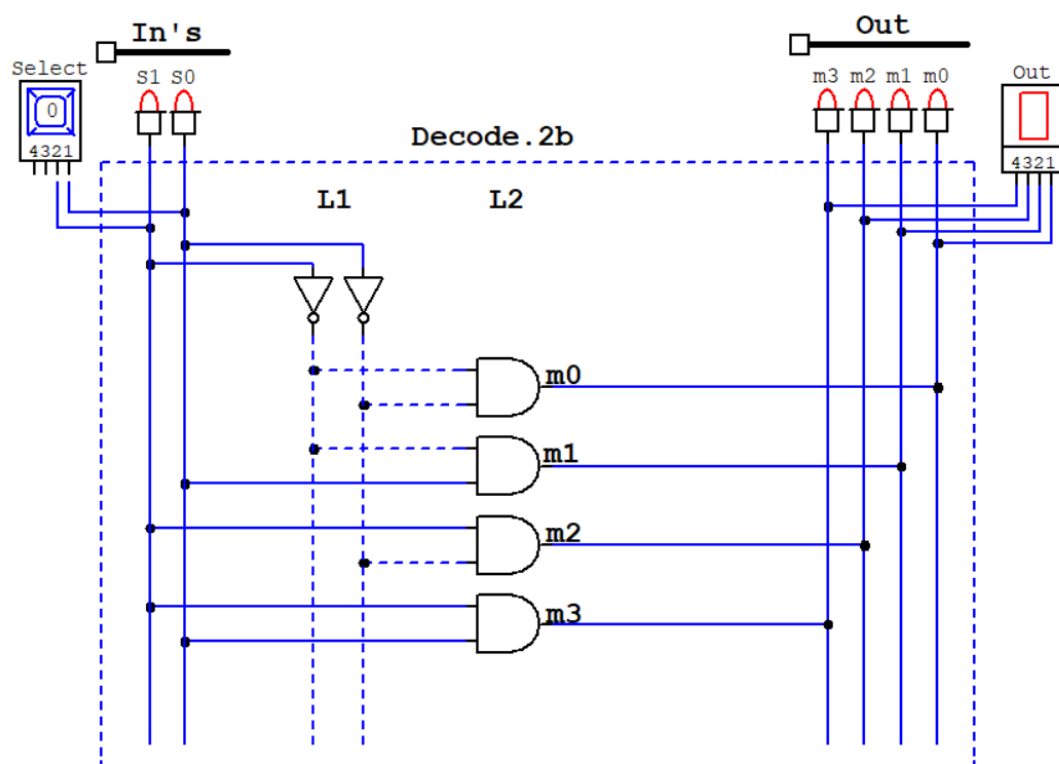
g0 – DECODE 2 bits



g1 – Tabela Verdade

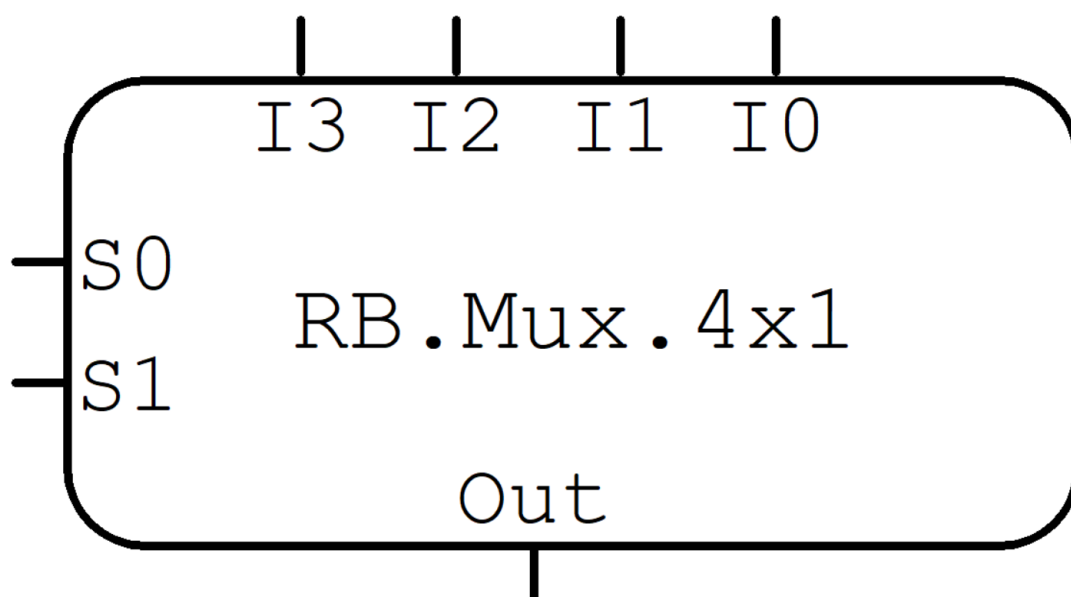
Dec	S1	S2	m0	m1	m2	m3
0	0	0	0	0	0	1
1	0	1	0	0	1	0
2	1	0	0	1	0	0
3	1	1	1	0	0	0

g2 – Circuito Lógico



MUX 4x1

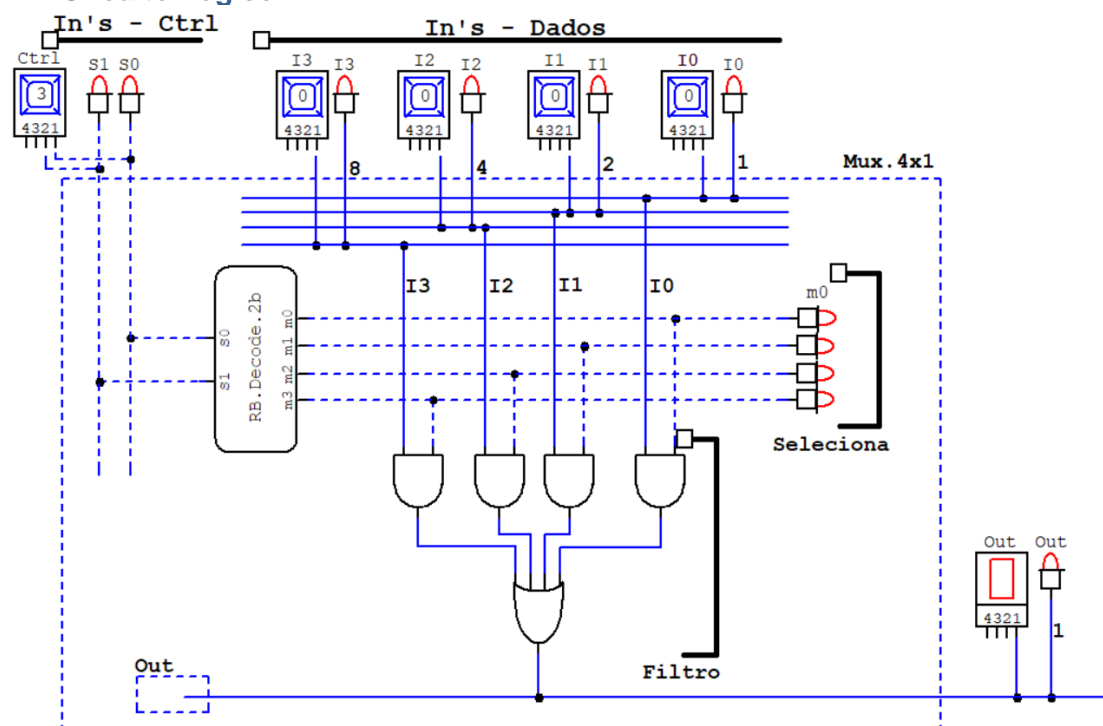
h0 – MUX 4x1



h1 – Tabela Verdade

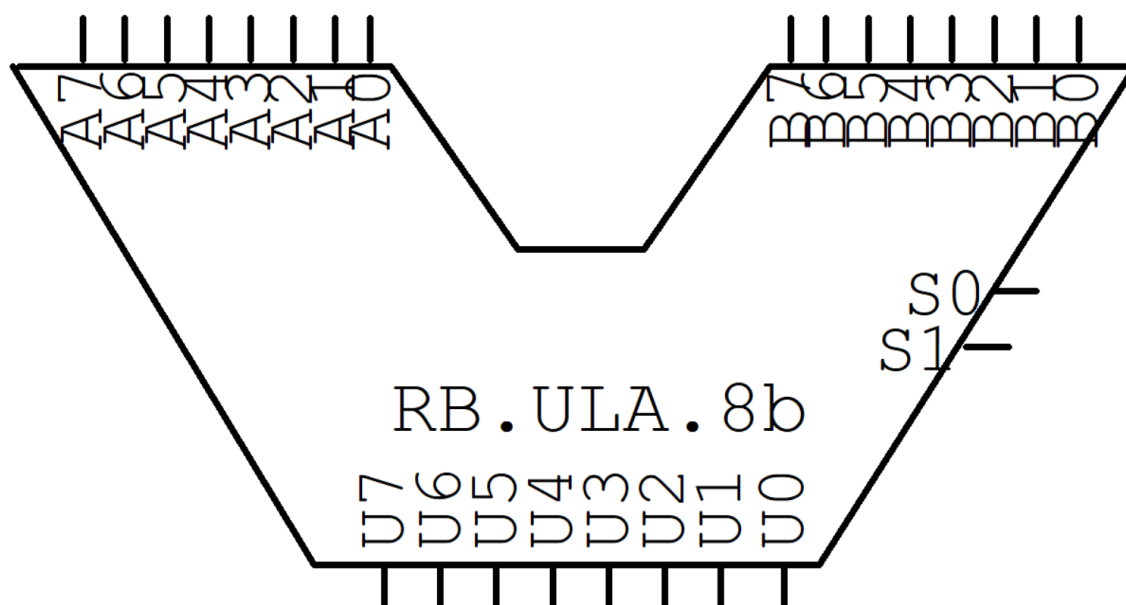
Dec	S1	S2	Out
0	0	0	I0
1	0	1	I1
2	1	0	I2
3	1	1	I3

h2 – Circuito Lógico



ULA 8 BITS

i0 – ULA 8 bits

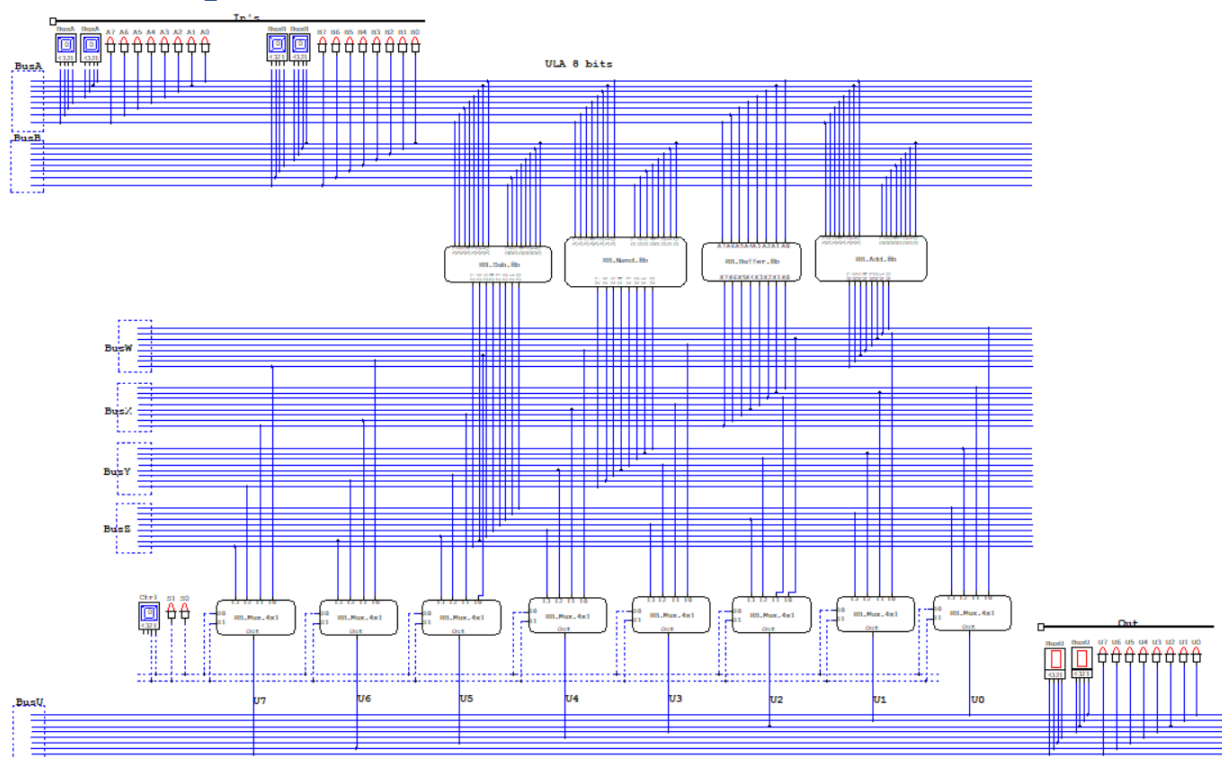


i1 – Tabela Verdade

Dec	S1	S2	Função	
0	0	0	BusA + BusB	Add
1	0	1	BusA	Buffer
2	1	0	BusA . BusB	Nand
3	1	1	BusA - BusB	Sub

Aritmético

i2 – Circuito Lógico



Referências

- Anotações das aulas