FIELD PROGRAMMABLE LOGIC ARRAY (16X48X8) 82S100 (T.S.)/82S101 (O.C.)

INTEGRATED FUSE LOGIC
SERIES 28

DESCRIPTION

The 82S100 (tri-state outputs) and the 82S101 (open collector outputs) are Bipolar Programmable Logic Arrays, containing 48 product terms (AND terms), and 8 sum terms (OR terms). Each OR term controls an output function which can be programmed either true active-high (Fp), or true active-low ($\overline{F}_p$). The true state of each output function is activated by any logical combination of 16-input variables, or their complements, up to 48 terms. Both devices are field programmable, which means that custom patterns are immediately available by following the fusing procedure outlined in this data sheet.

The 82S100 and 82S101 are fully TTL compatible, and include chip-enable control for expansion of input variables, and output inhibit. They feature either open collector or tri-state outputs for ease of expansion of product terms and application in bus-organized systems.

Both devices are available in commercial and military temperature ranges. For the commercial temperature range (0°C to +75°C) specify N82S100/101, F or N, and for the military temperature range (-55°C to +125° C) specify S82S100/101, F or G, I, R.

LOGIC FUNCTION

Typical Product Term:
$P_0 = I_0 \bullet I_1 \bullet \overline{I_2} \bullet I_5 \bullet \overline{I_{13}}$

Typical Output Functions: @ $\overline{CE} = 0$:
$F_0 = (P_0 + P_1 + P_2)$ @ L = Closed
$F_0 = (\overline{P_0} \bullet \overline{P_1} \bullet \overline{P_2})$ @ L = Open

NOTE

For each of the 8 outputs, either the function Fp (active-high) or $\overline{F}p$ (active low) is available, but not both. The required function polarity is programmed via link (L).

FEATURES

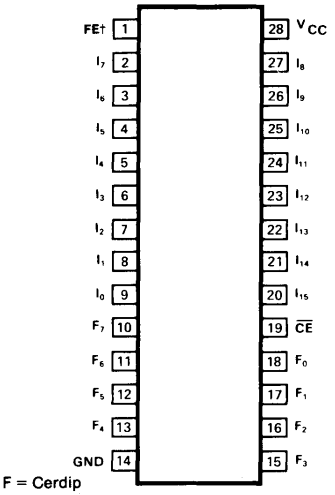
- **Field programmable (Ni-Cr link)**
- **Input variables: 16**
- **Output functions: 8**
- **Product terms: 48**
- **Address access time:**
  S82S100/101—80ns Max
  N82S100/101—50ns Max
- **Power dissipation: 600mW typ**
- **Input loading:**
  S82S100/101: −150μA Max
  N82S100/101: −100μA Max
- **Chip enable input**
- **Output option:**
  82S100: Tri-state
  82S101: Open collector
- **Output disable function:**
  Tri-state—Hi-Z
  Open collector—Hi

APPLICATIONS

- CRT display systems
- Random logic
- Code conversion
- Peripheral controllers
- Function generators
- Look-up and decision tables
- Microprogramming
- Address mapping
- Character generators
- Sequential controllers
- Data security encoders
- Fault detectors
- Frequency synthesizers

PIN CONFIGURATION

F,G,I,N,R PACKAGES

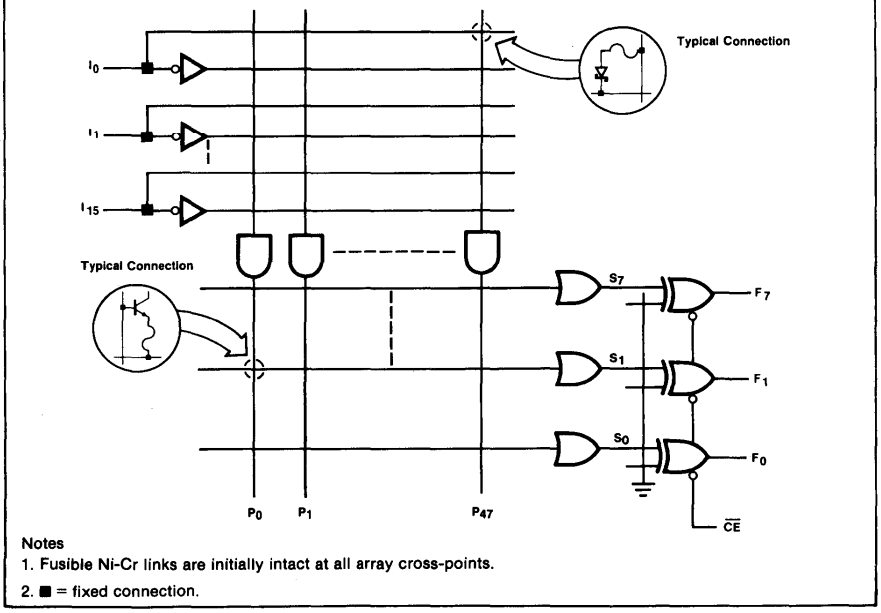


F = Cerdip
G = Leadless I = Ceramic N = Plastic
†Open or grounded during normal operation

TRUTH TABLE

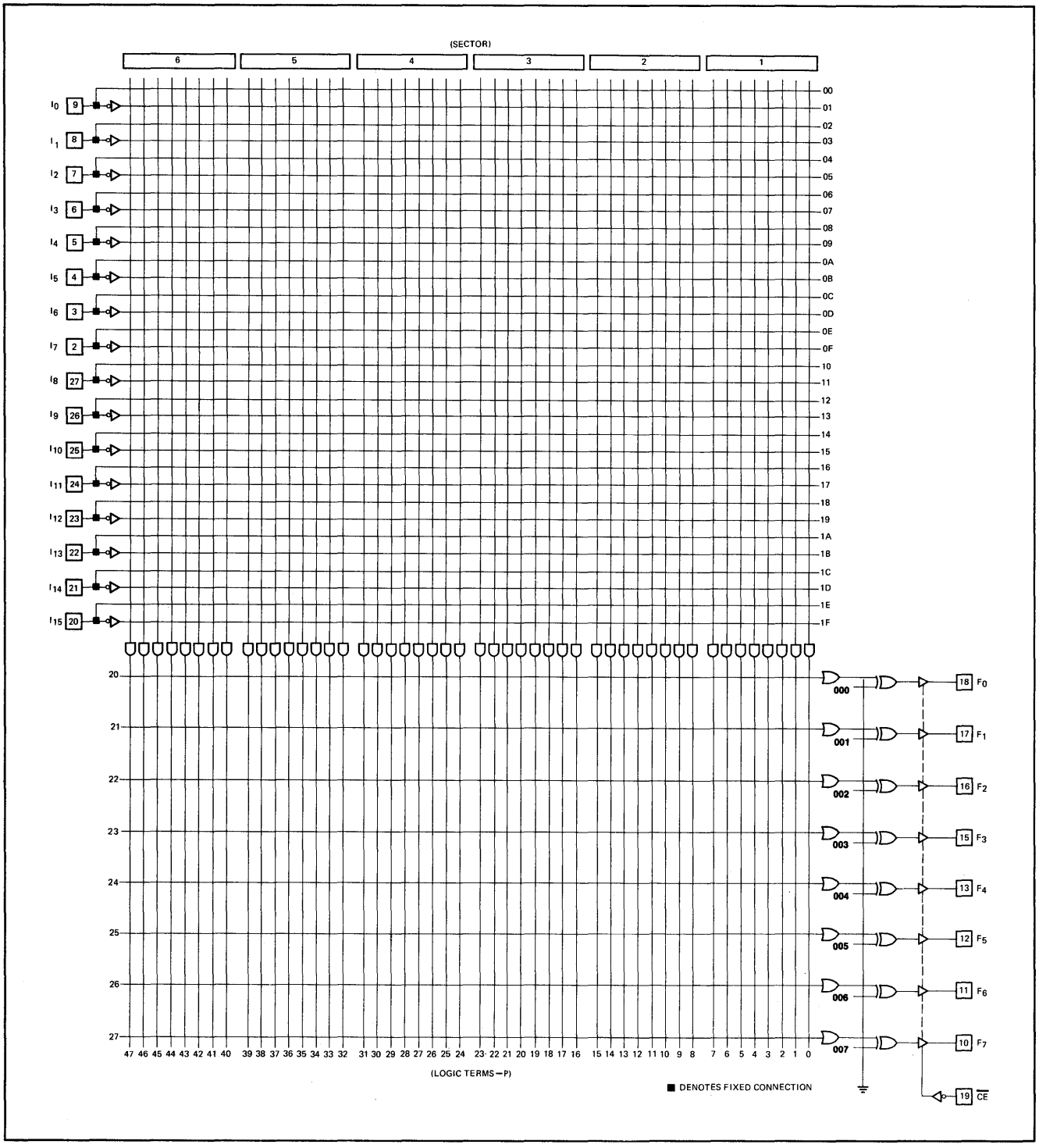
MODE	Pn	$\overline{CE}$	Sr ? f(Pn)	Fp	$\overline{F}_p$
Disabled (82S101)	X	1	X	1	1
Disabled (82S100)				Hi-Z	Hi-Z
Read	1	0	Yes	1	0
	0	0		0	1
	X	0	No	0	1

LOGIC DIAGRAM



Notes
1. Fusible Ni-Cr links are initially intact at all array cross-points.
2. ■ = fixed connection.

FPLA LOGIC DIAGRAM



FIELD PROGRAMMABLE LOGIC ARRAY (16X48X8) 82S100 (T.S.)/82S101 (O.C.)

INTEGRATED FUSE LOGIC
SERIES 28

ABSOLUTE MAXIMUM RATINGS[1]

PARAMETER		RATING Min	RATING Max	UNIT
V_{CC}	Supply voltage		+7	Vdc
V_{IN}	Input voltage		+5.5	Vdc
V_{OUT}	Output voltage		+5.5	Vdc
I_{IN}	Input currents	-30	+30	mA
I_{OUT}	Output currents		+100	mA
	Temperature range			°C
T_A	Operating			
	N82S100/101	0	+75	
	S82S100/101	-55	+125	
T_{STG}	Storage	-65	+150	

THERMAL RATINGS

TEMPERATURE	MILITARY	COMMERCIAL
Maximum junction	175°C	150°C
Maximum ambient	125°C	75°C
Allowable thermal rise ambient to junction	50°C	75°C

DC ELECTRICAL CHARACTERISTICS

N82S100/101: $0° \le T_A \le +75°C$, $4.75V \le V_{CC} \le 5.25V$
S82S100/101: $-55°C \le T_A \le +125°C$, $4.5V \le V_{CC} \le 5.5V$

PARAMETER		TEST CONDITIONS	N82S100/101 Min	N82S100/101 Typ[2]	N82S100/101 Max	S82S100/101 Min	S82S100/101 Typ[2]	S82S100/101 Max	UNIT
	Input voltage[3]								V
V_{IH}	**High**	V_{CC} = Max	2			2			
V_{IL}	**Low**	V_{CC} = Min			0.85			0.8	
V_{IC}	**Clamp[3,4]**	V_{CC} = Min, I_{IN} = -18mA		**-0.8**	-1.2		**-0.8**	-1.2	
	Output voltage	V_{CC} = Min							V
V_{OH}	**High (82S100)[3,5]**	I_{OH} = -2mA	2.4			2.4			
V_{OL}	**Low[3,6]**	I_{OL} = 9.6mA		**0.35**	0.45		**0.35**	0.50	
	Input current								µA
I_{IH}	High	V_{IN} = 5.5V		**<1**	25		**<1**	50	
I_{IL}	Low	V_{IN} = 0.45V		**-10**	-100		**-10**	-150	
	Output current	$\overline{CE}$ = High, V_{CC} = Max							
I_{OLK}	**Leakage[7]**	V_{OUT} = 5.5V		**1**	40		**1**	60	µA
$I_{O(OFF)}$	**Hi-Z state (82S100)[7]**	V_{OUT} = 5.5V		**1**	40		**1**	60	µA
		V_{OUT} = 0.45V		**-1**	-40		**-1**	-60	
I_{OS}	**Short circuit (82S100)[4,8]**	$\overline{CE}$ = Low, V_{OUT} = 0V	-20		-70	-15		-85	mA
I_{CC}	**V_{CC} supply current[9]**	V_{CC} = Max		**120**	170		**120**	180	mA
	Capacitance[7]	$\overline{CE}$ = High, V_{CC} = 5.0V							pF
C_{IN}	Input	V_{IN} = 2.0V		8			8		
C_{OUT}	Output	V_{OUT} = 2.0V		17			17		

AC ELECTRICAL CHARACTERISTICS

$R_1 = 470\Omega$, $R_2 = 1k\Omega$, $C_L = 30pF$
N82S100/101: $0°C \le T_A \le +75°C$, $4.75V \le V_{CC} \le 5.25V$
S82S100/101: $-55°C \le T_A \le +125°C$, $4.5V \le V_{CC} \le 5.5V$

PARAMETER		TO	FROM	N82S100/101 Min	N82S100/101 Typ[2]	N82S100/101 Max	S82S100/101 Min	S82S100/101 Typ[2]	S82S100/101 Max	UNIT
	Progagation delay									ns
T_{IA}	Input	Output	Input		**35**	50		**35**	80	
T_{CE}	Chip enable	Output	Chip enable		**15**	30		**15**	50	
	Disable time									ns
T_{CD}	Chip disable	Output	Chip enable		**15**	30		**15**	50	

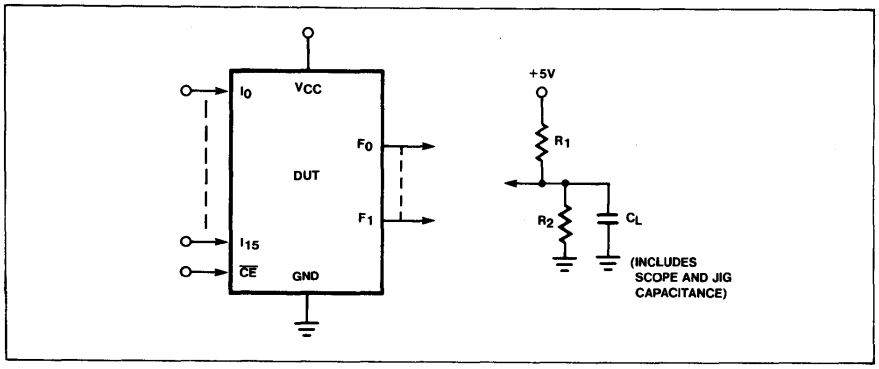
NOTES on following page.

FIELD PROGRAMMABLE LOGIC ARRAY (16X48X8) 82S100 (T.S.)82S101 (O.C.)

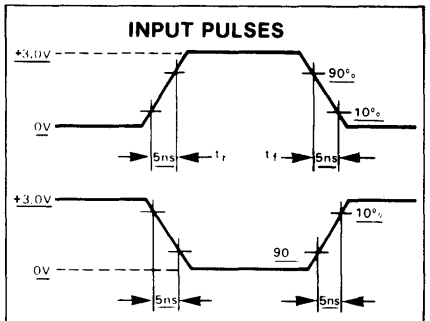
INTEGRATED FUSE LOGIC
SERIES 28

NOTES
1. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operation of the device specifications is not implied.
2. All voltage values are at V_{CC} = 5V, T_A = 25°C.
3. All voltage values are with respect to network ground terminal.
4. Test one at a time.
5. Measured with V_{IL} applied to $\overline{CE}$ and a logic high stored.
6. Measured with a programmed logic condition for which the output test is at a low logic level. Output sink current is applied thru a resistor to V_{CC}.
7. Measured with V_{IH} applied to $\overline{CE}$.
8. Duration of short circuit should not exceed 1 second.
9. I_{CC} is measured with the chip enable input grounded, all other inputs at 4.5V and the outputs open.

TEST LOAD CIRCUIT

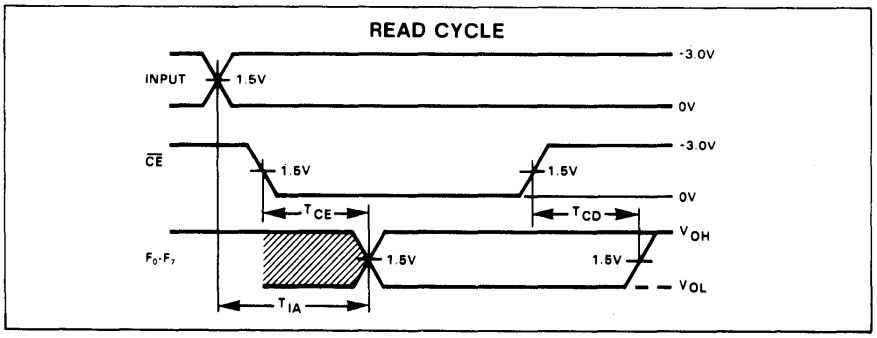


VOLTAGE WAVEFORM



Measurements: All circuit delays are measured at the +1.5V level of inputs and outputs.

TIMING DIAGRAM



TIMING DEFINITIONS

T_{CE} **Delay between beginning of Chip Enable low (with Input valid) and when Data Output becomes valid.**

T_{CD} Delay between when Chip Enable becomes high and Data Output is in off state (Hi-Z or high).

T_{IA} Delay between beginning of valid Input (with Chip Enable low) and when Data Output becomes valid.

VIRGIN DEVICE

The 82S100/101 are shipped in an unprogrammed state, characterized by:

1. All internal Ni-Cr links are intact.
2. Each product term (P-term) contains both true and complement values of every input variable I_m (P-terms always logically "false").
3. The "OR" Matrix contains all 48-P-terms.
4. The polarity of each output is set to active high (Fp function).
5. All outputs are at a low logic level.

RECOMMENDED PROGRAMMING PROCEDURE

To program each of 8 Boolean logic functions of 16 true or complement variables, including up to 48 P-terms, follow the Program/Verify procedures for the "AND" matrix, "OR" matrix, and output polarity outlined below. To maximize recovery from programming errors, leave all links in unused device areas intact.

SET-UP

Terminate all device outputs with a 10K resistor to +5V. Set GND (pin 14) to 0V.

Output Polarity

PROGRAM ACTIVE LOW ($\overline{Fp}$ FUNCTION)

Program output polarity before programming "AND" matrix and "OR" matrix. Program 1 output at the time. (L) links of unused outputs are not required to be fused.

1. Set FE (pin 1) to V_{FEL}.
2. Set V_{CC} (pin 28) to V_{CCL}.
3. Set $\overline{CE}$ (pin 19), and I_0 through I_{15} to V_{IH}.
4. Apply V_{OPH} to the appropriate output, and remove after a period t_p.
5. Repeat step 4 to program other outputs.

VERIFY OUTPUT POLARITY

1. Set FE (pin 1) to V_{FEL}; set V_{CC} (pin 28) to V_{CCS}.
2. Enable the chip by setting $\overline{CE}$ (pin 19) to V_{IL}.
3. Address a non-existent P-term by applying V_{IH} to all inputs I_0 through I_{15}.
4. Verify output polarity by sensing the logic state of outputs F_0 through F_7. All outputs at a high logic level are programmed active low (F_p function), while all outputs at a low logic level are programmed active high ($\overline{F_p}$ function).
5. Return V_{CC} to V_{CCP} or V_{CCL}.

"AND" Matrix

PROGRAM INPUT VARIABLE

Program one input at the time and one P-term at the time. All input variable links of unused P-terms are not required to be fused. However, unused input variables must be programmed as Don't Care for all programmed P-terms.

1. Set FE (pin 1) to V_{FEL}, and V_{CC} (pin 28) to V_{CCP}.
2. Disable all device outputs by setting $\overline{CE}$ (pin 19) to V_{IH}.
3. Disable all input variables by applying V_{IX} to inputs I_0 through I_{15}.
4. Address the P-term to be programmed (No. 0 through 47) by forcing the corresponding binary code on outputs F_0 through F_5 with F_0 as LSB. Use standard TTL logic levels V_{OHF} and V_{OLF}.
5a. If the P-term contains neither I_0 nor $\overline{I_0}$ (input is a Don't Care), fuse both I_0 and $\overline{I_0}$ links by executing both steps 5b and 5c, before continuing with step 7.
5b. If the P-term contains I_0, set to fuse the $\overline{I_0}$ link by lowering the input voltage at I_0 from V_{IX} to V_{IH}. Execute step 6.
5c. If the P-term contains $\overline{I_0}$, set to fuse the I_0 link by lowering the input voltage at I_0 from V_{IX} to V_{IL}. Execute step 6.
6a. After t_D delay, raise FE (pin 1) from V_{FEL} to V_{FEH}.
6b. After t_D delay, pulse the $\overline{CE}$ input from V_{IH} to V_{IX} for a period t_P.
6c. After t_D delay, return FE input to V_{FEL}.
7. Disable programmed input by returning I_0 to V_{IX}.
8. Repeat steps 5 through 7 for all other input variables.
9. Repeat steps 4 through 8 for all other P-terms.
10. Remove V_{IX} from all input variables.

VERIFY INPUT VARIABLE

1. Set FE (pin 1) to V_{FEL}; set V_{CC} (pin 28) to V_{CCP}.
2. Enable F_7 output by setting $\overline{CE}$ to V_{IX}.
3. Disable all input variables by applying V_{IX} to inputs I_0 through I_{15}.
4. Address the P-term to be verified (No. 0 through 47) by forcing the corresponding binary code on outputs F_0 through F_5.
5. Interrogate input variable I_0 as follows:
   A. Lower the input voltage at I_0 from V_{IX} to V_{IH}, and sense the logic state of output F_7.
   B. Lower the input voltage at I_0 from V_{IH} to V_{IL}, and sense the logic state output F_7.

The state of I_0 contained in the P-term is determined in accordance with the following truth table:

I_0	F_7	INPUT VARIABLE STATE CONTAINED IN P-TERM
0	1	$\overline{I_0}$
1	0	
0	0	I_0
1	1	
0	1	Don't Care
1	1	
0	0	(I_0), $(\overline{I_0})$
1	0	

Note that 2 tests are required to uniquely determine the state of the input variable contained in the P-term.

6. Disable verified input by returning I_0 to V_{IX}.
7. Repeat steps 5 and 6 for all other input variables.
8. Repeat steps 4 through 7 for all other P-terms.
9. Remove V_{IX} from all input variables.

"OR" MATRIX

PROGRAM PRODUCT TERM

Program one output at the time for one P-term at the time. All P_n links in the "OR" matrix corresponding to unused outputs and unused P-terms are not required to be fused.

1. Set FE (pin 1) to V_{FEL}.
2. Disable the chip by setting $\overline{CE}$ (pin 19) to V_{IH}.
3. After t_D delay, set V_{CC} (pin 28) to V_{CCS}, and inputs I_6 through I_{15} to V_{IH}, V_{IL}, or V_{IX}.
4. Address the P-term to be programmed (No. 0 through 47) by applying the corresponding binary code to input variables I_0 through I_5.
5a. If the P-term is contained in output function F_0 ($F_0 = 1$ or $\overline{F_0} = 0$), got to step 6, (fusing cycle not required).
5b. If the P-term is **not** contained in output function F_0 ($F_0 = 0$ or $\overline{F_0} = 1$), set to fuse the P_n link by forcing output F_0 to V_{OPF}.
6a. After t_D delay, raise FE (pin 1) from V_{FEL} to V_{FEH}.
6b. After t_D delay, pulse the $\overline{CE}$ input from V_{IH} to V_{IX} for a period t_P.
6c. After t_D delay, return FE input to V_{FEL}.
6d. After t_D delay, remove V_{OPF} from output F_0.
7. Repeat steps 5 and 6 for all other output functions.
8. Repeat steps 4 through 7 for all other P-terms.
9. Remove V_{CCS} from V_{CC}.

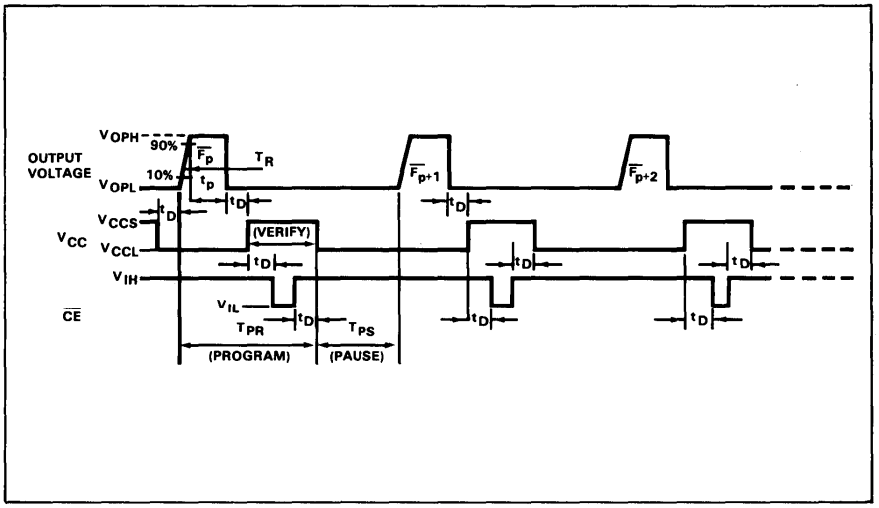
VERIFY PRODUCT TERM

1. Set FE (pin 1) to V_{FEL}.
2. Disable the chip by setting $\overline{CE}$ (pin 19) to V_{IH}.
3. After t_D delay, set V_{CC} (pin 28) to V_{CCS}, and inputs I_0 through I_{15} to V_{IH}, V_{IL}, or V_{IX}.
4. Address the P-term to be verified (No. 0 through 47) by applying the corresponding binary code to input variables I_0 through I_5.
5. After t_D delay, enable the chip by setting $\overline{CE}$ (pin 19) to V_{IL}.
6. To determine the status of the P_n link in the "OR" matrix for each output function F_p or $\overline{F_p}$, sense the state of outputs F_0 through F_7. The status of the link is given by the following truth table:

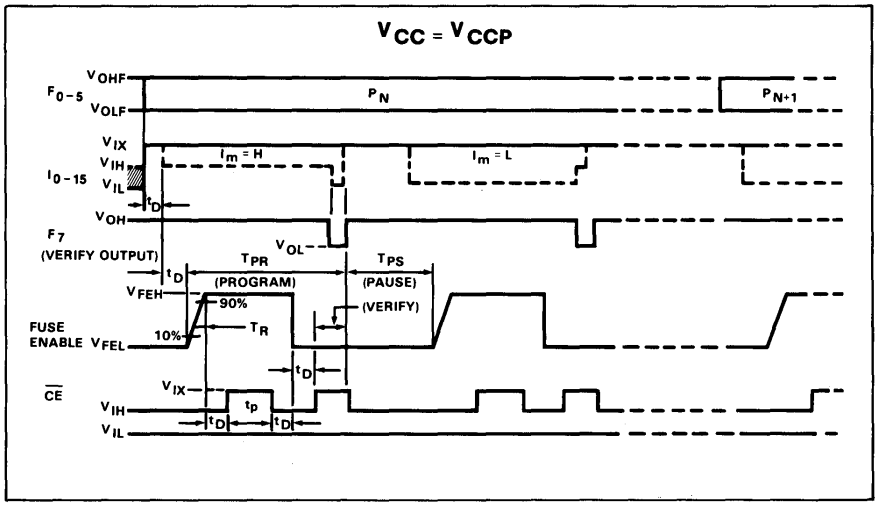
OUTPUT		P-TERM LINK
Active High (F_p)	Active Low ($\overline{F_p}$)	
0	1	Fused
1	0	Present

7. Repeat steps 4 through 6 for all other P-terms.
8. Remove V_{CCS} from V_{CC}.

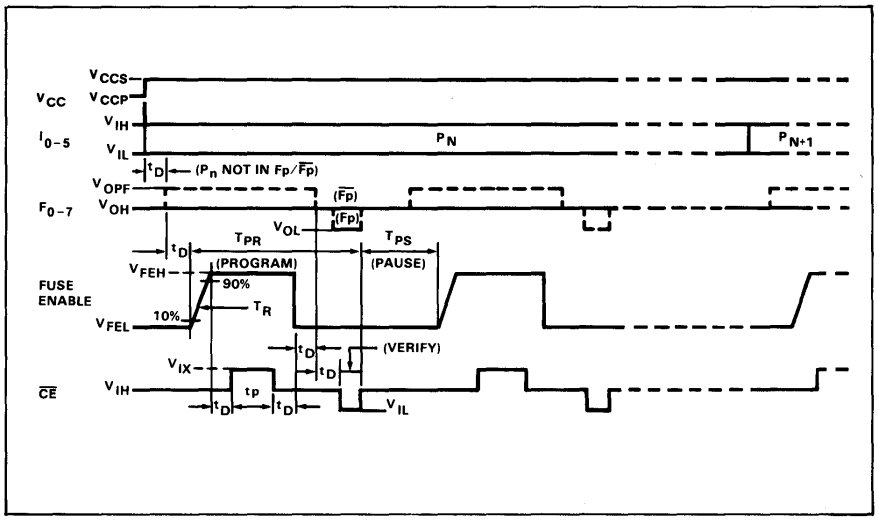
OUTPUT POLARITY PROGRAM-VERIFY SEQUENCE (TYPICAL)



"AND" MATRIX PROGRAM-VERIFY SEQUENCE (TYPICAL)



"OR" MATRIX PROGRAM-VERIFY SEQUENCE (TYPICAL)



PROGRAMMING SYSTEM SPECIFICATIONS[1] (T_A = +25°C)

PARAMETER		TEST CONDITIONS	LIMITS Min	LIMITS Typ	LIMITS Max	UNIT
V_{CCS}	V_{CC} supply (program/verify "OR", verify output polarity)[2]	I_{CCS} = 550mA, min, Transient or steady state	8.25	8.5	8.75	V
V_{CCL}	V_{CC} supply (program output polarity)		0	0.4	0.8	V
I_{CCS}	I_{CC} limit (program "OR")	V_{CCS} = +8.5 ± .25V	550		1,000	mA
	Output voltage					V
V_{OPH}	Program output polarity[3]	I_{OPH} = 300 ± 25mA	16.0	17.0	18.0	
V_{OPL}	Idle		0	0.4	0.8	
I_{OPH}	Output current limit (Program output polarity)	V_{OPH} = +17 ± 1V	275	300	325	mA
	Input voltage					V
V_{IH}	High		2.4		5.5	
V_{IL}	Low		0	0.4	0.8	
	Input current					µA
I_{IH}	High	V_{IH} = +5.5V			50	
I_{IL}	Low	V_{IL} = 0V			-500	
	Forced output voltage					V
V_{OHF}	High		2.4		5.5	
V_{OLF}	Low		0	0.4	0.8	
	Output current					
I_{OHF}	High	V_{OHF} = +5.5V			100	µA
I_{OLF}	Low	V_{OLF} = 0V			-1	mA
V_{IX}	$\overline{CE}$ program enable level		9.5	10	10.5	V
I_{IX1}	Input variables current	V_{IX} = +10V			10	mA
I_{IX2}	$\overline{CE}$ input current	V_{IX} = +10V			10	mA
V_{FEH}	FE supply (program)[3]	I_{FEH} = 300 ± 25mA, Transient or steady state	16.0	17.0	18.0	V
V_{FEL}	FE supply (idle)	I_{FEL} = -1mA, max	1.25	1.5	1.75	V
I_{FEH}	FE supply current limit	V_{FEH} = +17 ± 1V	275	300	325	mA
V_{CCP}	V_{CC} supply (program/verify "AND")	I_{CCP} = 550mA, min, Transient or steady state	4.75	5.0	5.25	V
I_{CCP}	I_{CC} limit (program "AND")	V_{CCP} = +5.0 ± .25V	550		1,000	mA
V_{OPF}	Forced output (program)		9.5	10	10.5	V
I_{OPF}	Output current (program)				10	mA
T_R	Output pulse rise time	10% to 90%	10		50	µs
t_P	$\overline{CE}$ programming pulse width		0.3	0.4	0.5	ms[5]
t_D	Pulse sequence delay		10			µs
T_{PR}	Programming time			0.6		ms
$\frac{T_{PR}}{T_{PR}+T_{PS}}$	Programming duty cycle				50	%
F_L	Fusing attempts per link				2	cycle
V_S	Verify threshold[4]		1.4	1.5	1.6	V

NOTES

1. These are specifications which a Programming System must satisy in order to be qualified by Signetics.
2. Bypass V_{CC} to GND with a 0.01µf capacitor to reduce voltage spikes.
3. Care should be taken to ensure that the voltage is maintained during the entire fusing cycle. The recommended supply is a constant current source clamped at the specified voltage limit.
4. V_S is the sensing threshold of the FPLA output voltage for a programmed link. It normally constitutes the reference voltage applied to a comparator circuit to verify a successful fusing attempt.
5. These are new limits resulting from device improvements, and which supersede, but do not obsolete the performance requirements of previously manufactured programming equipment.

FIELD PROGRAMMABLE LOGIC ARRAY (16X48X8) 82S100 (T.S.)82S101 (O.C.)

INTEGRATED FUSE LOGIC
SERIES 28

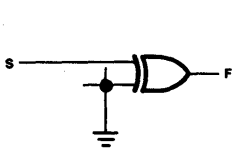
LOGIC PROGRAMMING

The FPLA can be programmed by means of Logic programming equipment.

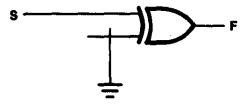
With Logic programming, the AND/OR/EX-OR gate input connections necessary to implement the desired logic function are coded directly from logic equations using the Program Table on the following page.

In this Table the logic state or action of variables I, P, and F, associated with each Sum Term S_r, is assigned a symbol which results in the proper fusing pattern of corresponding link pairs, defined as follows:

EX-OR ARRAY-(F)

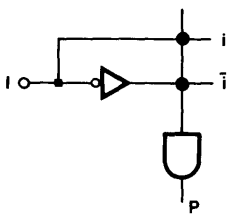


ACTIVE LEVEL	CODE
HIGH	H

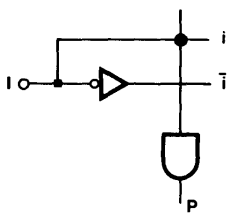


ACTIVE LEVEL	CODE
LOW	L

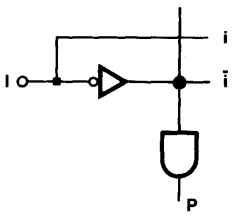
"AND" ARRAY - (I)



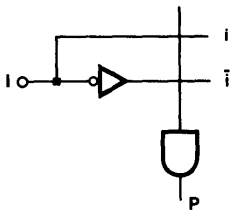
STATE	CODE
INACTIVE [1,2]	O



STATE	CODE
I	H

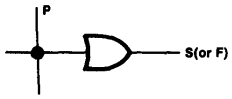


STATE	CODE
i	L

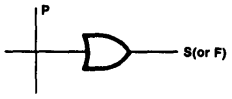


STATE	CODE
DON'T CARE	–

"OR" ARRAY - (F)



Pn STATUS	CODE
ACTIVE	A



Pn STATUS	CODE
INACTIVE	•

NOTES
1. This is the initial unprogrammed state of all link pairs. It is normally associated with all unused (inactive) AND gates P_n.
2. Any gate P_n will be unconditionally inhibited if any one of its (I) link pairs is left intact.

FIELD PROGRAMMABLE LOGIC ARRAY (16X48X8) 82S100 (T.S.)82S101 (O.C.)

INTEGRATED FUSE LOGIC
SERIES 28

FPLA PROGRAM TABLE (Logic)

PROGRAM TABLE ENTRIES

INPUT VARIABLE: Im (H); $\overline{Im}$ (L); Don't Care

OUTPUT FUNCTION: Prod. Term Present in F_P (A); Prod. Term Not Present in F_P (• (period)); — (dash)

OUTPUT ACTIVE LEVEL: Active High (H); Active Low (L)

NOTE: Enter (–) for unused inputs of used P-terms

NOTES:
1. Entries independent of output polarity
2. Enter (A) for unused outputs of used P-terms

NOTES
1. Polarity programmed once only
2. Enter (H) for all unused outputs

CUSTOMER NAME _____
PURCHASE ORDER # _____
SIGNETICS DEVICE # _____ CF (XXXX)
CUSTOMER SYMBOLIZED PART # _____
TOTAL NUMBER OF PARTS _____
PROGRAM TABLE # _____ REV ____ DATE ____

NO	PRODUCT TERM[1] INPUT VARIABLE[1] I15	I14	I13	I12	I11	I10	I9	I8	I7	I6	I5	I4	I3	I2	I1	I0	ACTIVE LEVEL[1] OUTPUT FUNCTION[1] O7	O6	O5	O4	O3	O2	O1	O0
0																								
1																								
2																								
3																								
4																								
5																								
6																								
7																								
8																								
9																								
10																								
11																								
12																								
13																								
14																								
15																								
16																								
17																								
18																								
19																								
20																								
21																								
22																								
23																								
24																								
25																								
26																								
27																								
28																								
29																								
30																								
31																								
32																								
33																								
34																								
35																								
36																								
37																								
38																								
39																								
40																								
41																								
42																								
43																								
44																								
45																								
46																								
47																								
PIN NO.	20	21	22	23	24	25	26	27	2	3	4	5	6	7	8	9	10	11	12	13	15	16	17	18
VARIABLE NAME																								

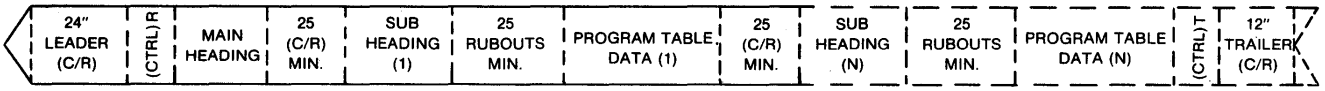
FIELD PROGRAMMABLE LOGIC ARRAY (16X48X8) 82S100 (T.S.)82S101 (O.C.)

INTEGRATED FUSE LOGIC
SERIES 28

TWX TAPE CODING

The FPLA Program Table can be sent to Signetics in ASCII code format via airmail using any type of 8-level tape (paper, mylar, fanfold, etc.), or via TWX: just dial (910) 339-9283, tell the operator to turn the paper puncher on, and acknowledge. At the end of transmission instruct the operator to send tape to Signetics Order Entry.

A number of Program Tables can be sequentially assembled on a continuous tape as follows, however limit tape length to a roll of 1.75 inch inside diameter, and 4.25 inch outside diameter:



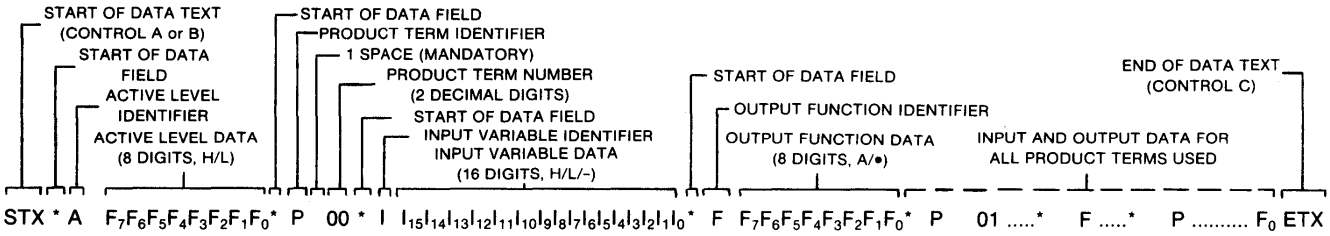
A. The MAIN HEADING at the beginning of tape includes the following information, with each entry preceded by a ($) character, whether used or not:

1. Customer Name _____
2. Customer TWX No. _____
3. Date _____
4. Purchase Order No. _____
5. Number of Program Tables _____
6. Total Number of Parts _____

B. Each SUB HEADING should contain specific information pertinent to each Program Table as follows, with each entry preceded by a ($) character, whether used or not:

1. Signetics Device No. _____
2. Program Table No. _____
3. Revision _____
4. Date _____
5. Customer Symbolized Part No. _____
6. Number of Parts _____

C. Program Table data blocks in Logic format are initiated with an STX character, and terminated with an ETX character. The body of the data consists of Output Active Level, Product Term, and Output Function information separated by appropriate identifiers in accordance with the following sequence:



Entries for the 3 Data Fields are determined in accordance with the following Table:

INPUT VARIABLE		
I_m	$\overline{I_m}$	Don't Care
H	L	— (dash)

NOTE
Enter (—) for unused inputs of used P-terms.

OUTPUT FUNCTION	
Product term present in Fp	Product term not present in Fp
A	• (period)

NOTES
1. Entries independent of output polarity.
2. Enter (A) for unused outputs of used P-terms.

OUTPUT ACTIVE LEVEL	
Active high	Active low
H	L

NOTES
1. Polarity programmed once only.
2. Enter (H) for all unused outputs.

Although the Product Term data are shown entered in sequence, this is not necessary. It is possible to input only one Product Term, if desired. Unused Product Terms require no entry. ETX signalling end of Program Table may occur with less than the maximum number of Product Terms entered.

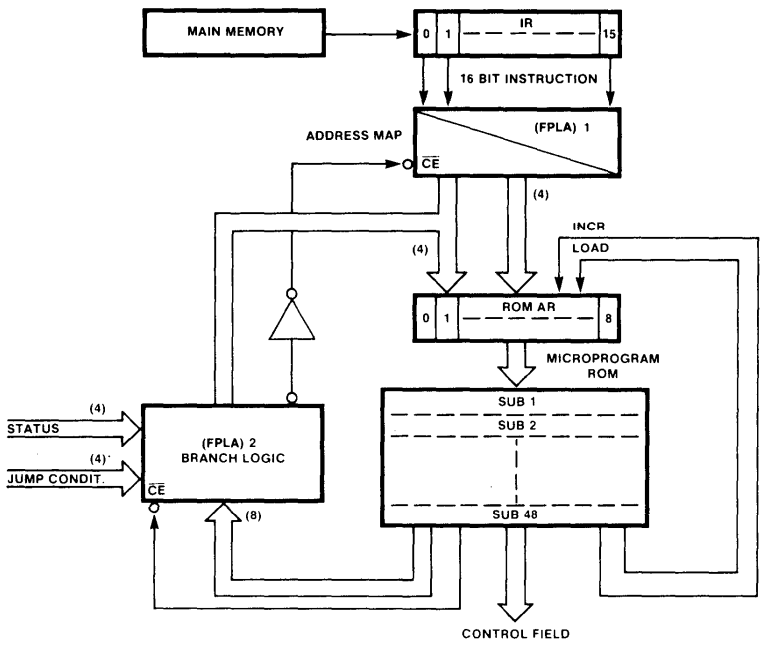
NOTES
1. Corrections to any entry can be made by backspace and rubout. However, limit consecutive rubouts to less than 25.
2. Terms can be re-entered any number of times. The last entry for a particular P-Term will be interpreted as valid data.
3. To facilitate an orderly Teletype print out, carriage returns, line feeds, spaces, rubouts etc. may be interspersed between data groups.
4. Comments are allowed between data fields, provided that an asterisk (*) is not used in any Heading or Comment entry.

FIELD PROGRAMMABLE LOGIC ARRAY (16X48X8) 82S100 (T.S.)82S101 (O.C.)

INTEGRATED FUSE LOGIC
SERIES 28

TYPICAL APPLICATIONS

SUBROUTINE ADDRESS MAP



SEQUENTIAL CONTROLLER