This project presents the implementation of a RISC-V soft-core processor on the Lattice iCEBreaker FPGA using only open-source tools. A soft-core processor is implemented using the FPGA’s programmable fabric, as opposed to hard-core processors which are fixed in silicon. The main objective was to demonstrate that a fully functional processor can be developed without relying on costly tools or proprietary IP. The entire design process was carried out using free and open-source software, including Yosys for synthesis, Nextpnr for place and route, Verilator for simulation, and GTKWave for waveform analysis. Two processor architectures were implemented: a multi-cycle design deployed on hardware, and a pipelined version simulated with hazard handling and branch prediction. To validate the processor’s functionality, a variety of C and assembly programs were compiled using the riscv32-unknown-elf-gcc toolchain and executed, including π digit calculation, Mandelbrot fractal visualization, and AES-128 encryption. This project demonstrates the feasibility and educational value of developing a complete RISC-V processor using a fully open-source workflow on accessible FPGA hardware, offering a transparent and low-cost alternative to traditional development methods.