

Tianyi Huang

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🎓 Computer Architecture · ✉ gwins777@qq.com · 🌐 github.com/Gwins7 · 🐙 Gwins7



M.S. Candidate at Center for Advanced Computer Systems, Institute of Computing Technology, Chinese Academy of Sciences (ICT, CAS), 2023. Research Direction: Computer Architecture Security and FPGA. Familiar with RISC-V Processor Architecture, Hardware Security Mechanisms, Agile Development Methods for Hardware, System Software, and FPGA HW/SW Co-Design. Participated in multiple research projects as a key member, such as the SmartNIC, Nanhu-VCU128 platform, and DASICS processor security mechanisms.

🎓 Education

2023.9 - 2026.6 | **ICT, CAS Computer Architecture Master** (Mentor: Prof. Mingyu Chen · GPA: 3.86 / 4)
2019.9 - 2023.6 | **University of CAS Computer Science Bachelor** (GPA: 3.80 / 4 · Rank: 15%)

🔧 Skill

Computer Arch.	Chisel agile hardware development on RISC-V processor mechanism design
FPGA	SoC design and optimization based on Xilinx FPGA
System software	OS Kernel (Linux) / Simulator (QEMU) development based on C
Dev Lang.	Chisel, (System)Verilog, C, RISC-V Assembly, Script (Vivado Tcl, Python, Makefile...)
English	IELTS Overall 7.5

🏆 Prize

ICT, CAS	Outstanding student of SKLP, ICT; Director's Excellence Award	2024
CSCC Com. Sys. Dev. Comp.	First Place in Second Prize, OS implementation track	2022
University of CAS	Outstanding student cadres	2020
University of CAS	Scholarship (Class: 2 First, 2 Second, 1 Third)	2019 - 2024

🔗 Project

DASICS	Lab Project	September 2023 - Present
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The processor in-process isolation protection mechanism includes CFI, DFI, syscall filter, etc., and realizes byte-granular permission protection by dividing regions

- Based on the RISC-V instruction set, implement the DASICS mechanism on the multi-generation architecture (Nanhu-V2, V3a, V5) of the NutShell sequential processor and the Xiangshan out-of-order processor, developed the corresponding software stack, and participated in and the tape-out project of Nanhu-V3a to obtain the actual chip
- Adapt and deploy DASICS systems on multiple FPGA platforms (Pynq Z2, VCU128, VCU1525, and S2C VU19P)
- Implement the DASICS mechanism on Penglai TEE on RISC-V to protect the TEE Enclave
- Carry out new DASICS functions and optimization designs, such as Bound compression, interoperability with MPK, etc., and participate in experimental testing and paper writing

Nanhu-VCU128 Platform	Lab Project	March 2024 - July 2024
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System Adaptation of the Nanhu Open Source High-Performance Processor Based on FPGA Platforms

- Deploy the Nanhu open-source RISC-V high-performance processor SoC on the Xilinx VCU128 development board.
- Optimize the SoC layout and timing, add external storage functionality (FMC-PCIe-SSD) and network functionality (RJ45 AXI-Ethernet).
- Perform software and hardware adaptation, successfully booted Ubuntu 22.04 LTS from SSD and achieved network connectivity.

An Agile Development Solution for High-Performance and Highly Scalable Smart NIC

- Based on the Xilinx ZU19EG FPGA, targeting CPU-Network scenarios with DPDK support for 100Gbps high-bandwidth transmission.
- Independently build the SoC framework using Chisel for agile development of functional modules.
- Pipeline processing of network packets with uniform pipeline-level interfaces to achieve high scalability.
- Support hardware functions include: TCP/IP checksum calculation, RSS load balancing, field comparison and search, regular expression matching, and AES encryption/decryption.

CCoreOS

Competition Project

March 2022 - July 2022

A Lightweight Operating System Kernel Written in C

- Developed for CSCC University Student Computer System Development Capability Competition (First Place in Second Prize, OS implementation track)
- Based on Kendryte K210 RISC-V development board
- The code is totally self-written with relatively complete operating system functions
- Using the riscv64-musl library, successfully ran user-level programs and tests like libc-test, busybox, lmbench, lua, binutils, and 7za.

Others

Other Projects

September 2023 - Present

- Participate in the design and technical support of the undergraduate operating system experimental course of the University of Chinese Academy of Sciences (based on NutShell on Pynq Z2 FPGA)

Participated paper

Jin, Y., Xu, Y., Yang, C., Wang, H., **Huang, T.**, Lu, T., & Chen, M. (2023). DASICS: Enhancing Memory Protection with Dynamic Compartmentalization. arXiv preprint arXiv:2310.06435.

Campus Activities

Class Propaganda Committee

September 2019 - June 2020

Officer, Outreach Department of the Student Union

September 2019 - June 2021