6.3. Externer Interrupt ATMEGA2560

Montag, 18. September 2017 11:10

Register EICRA (External Interrupt Control Register A)

3 2 1 Ext. Int. 0

	x	x	x	x	1	0	x	x
Bit	7	6	5	4	3	2	1	0
(0x69)	ISC31	ISC30	ISC21	ISC20	ISC11	ISC10	ISC01	ISC00
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial Value	0	0	0	0	0	0	0	0

Einstellung pos. od. neg. Flanke

2 Bits: ISC 1 0 ISC 1 1

Externer Interrupt 1

0	1	fallen
1	1	steig

z.B.: Externer Interrupt 2 auf steigende Flanke

Bits ISC20 und ISC21 setzen

Bit 4 Bit 5

Maske: 0011 0000 0x3

EICRA |= 0x30;

Register EIMSK (External Interrupt Mask Register)

	x	x	x	x	x	x	1	x
Bit	7	6	5	4	3	2	1	0
0x1D (0x3D)	INT7	INT6	INT5	INT4	INT3	INT2	INT1	INT0

Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial Value	0	0	0	0	0	0	0	0

Interrupt aktivieren

z.B.: Externen Interrupt 1 aktivieren

Bit INT1 setzen

```
EIMSK |= 0x02;
```

oder: `EIMSK |= (1<<INT1);`

Interrupts generell aktivieren:

```
#include <avr/interrupt.h>
sei();      // set enable interrupt → interrupts
cli();      // clear → interrupts deaktivieren
```

Interrupt Service Routine:

z.B.: Externer Interrupt 3

```
ISR(INT3_vect)
{
   ⋮
}
```