BENNETT UNIVERSITY
THE TIMES GROUP

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Department/ School: SCSET

END-TERM EXAMINATION, ODD SEMESTER DECEMBER 2023

COURSE CODE	**CSET-203**	**MAX. DURATION**	**2HRS**
COURSE NAME	**MICROPROCESSOR AND COMPUTER ARCHITECTURE**		
PROGRAM	**B.Tech.**	**TOTAL MARKS**	**35**

Mapping of Questions to Course and Program Outcomes										
Q.No.	A1	A2	A3	A4	A5	B1	B2	B3	B4	B5
CO	1	1	2	1	2	1	2	2	3	3
PO	1	1	1, 6	1	1, 6	1, 3	6	1	1, 6	1, 6
BTL*[1]	L1	L1	L2	L1	L3	L1	L5	L4	L4	L5

GENERAL INSTRUCTIONS: -

1. Do not write anything on the question paper except **name, enrolment number** and **department/school.**
2. Carrying mobile phones, smartwatches and any other non-permissible materials in the examination hall is an act of **UFM.**

COURSE INSTRUCTIONS:

a) **Be Precise in your writing**

SECTION A

Max Marks: 10

A1) Given multiplicand m=0101 1010 1110 1110 and multiplier n=0011 0101 1001 1100. Product $P = m \times n$ is obtained by multiplication of two numbers using the Booth's algorithm. Find out the number of total additions and subtractions performed to find the product. **(2 Marks)**

A2) List out the differences between direct mapping, associative mapping, and set associative Mapping. **(2 Marks)**

A3) A two way set associative cache consists of 128 lines, or slots, divided into several sets. Main memory contains 8K blocks of 256 words each. Write down the format of main memory addresses. **(2 Marks)**

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A4) Differentiate between CPU and Core in context with high end processors. **(2 Marks)**

A5) A device is constantly transferring the data with 40KBPS speed to memory using DMA. Assume that the transmission time to memory from IO once the data (4bytes) is ready is 10 microseconds. Compute the Percentage of time CPU is blocked due to:

(i) DMA in burst mode

(ii) DMA in Cycle stealing mode **(1+1= 2 Marks)**

SECTION B

Max Marks: 25

B1) Explain the architecture of DMA controller with an appropriate diagram. **(5 Marks)**

B2) State the contents of registers E, A, Q and SC during the process of multiplication of two binary numbers, 11111 (multiplicand) and 10101 (multiplier). (**Note**: The signs are not included.) **(5 Marks)**

B3) A DMA module is transferring 16-bit character in one cycle to the memory using cycle stealing. The process runs at 2 MHz clock frequency and DMA controller requires .25 processor cycles. Find the data transfer rate of the device. **(5 Marks)**

B4) We are given with 64K x 2 RAM Chips. Calculate the number of chips required to build 128KB RAM and size of the decoder if used. Draw the final designed circuit as well. **(2+1+2 =5 Marks)**

B5) Imagine a pipeline system that has four stages: instruction fetch (IF), instruction decodes (ID), execution (EX) and write back (WB). The following table illustrates the number of clock cycles needed for each instruction to finish each stage. Calculate the number of clock cycles and stall required to complete the instructions showing the machine cycle of all the instructions? **(5 Marks)**

Instructions	Instruction Fetch (IF)	Instruction Decode (ID)	Execution (EX)	Write Back (WB)
I_0	2	1	2	1
I_1	2	2	3	1
I_2	1	2	1	2
I_3	2	3	2	1
I_4	3	1	1	2

-ALL THE BEST-