Enrolment No: E22CSE0827 Name of Student: MADHAV GUPTA

Department/ School: SCSET

MID TERM EXAMINATION, ODD SEMESTER JULY 2023

COURSE CODE	CSET-203	MAX. DURATION	1 HR
COURSE NAME	Microprocessor and Computer Architecture		
PROGRAM	B.Tech	TOTAL MARKS	15

GENERAL INSTRUCTIONS: -

Mapping of Questions to Course and Program Outcomes										
Q.No.	Sec-1 1	Sec -1 2	Sec -1 3	Sec -2 1	Sec2 2	Sec-3 1	Sec -3 2	Sec -3 3	9	10
CO	CO1	CO2	CO1	CO2	CO2	CO1	CO1	CO2		
PO	PO1	PO2	PO2	PO3	PO5	PO1	PO1, PO2	PO1, PO2		

1. Do not write anything on the question paper except name, enrolment number and department/school.
2. Carrying mobile phone, smart watch and any other non-permissible materials in the examination hall is an act of UFM.

COURSE INSTRUCTIONS:

a) Be Precise in your writing.

b) Attempt all questions.

SECTION A

(1x3 = 3 Marks)

1) Perform (1FFF H - 2000 H) and tell the status of each flag used in 8086.

2) Consider a direct mapped cache of size 16 KB with block size 256 bytes. The size of main memory is 128 KB.

Find- (i) Physical Address (ii) Number of Tag Bits

3) Define and explain the concept of pipelining used in 8086 MPU.

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SECTION B

(3x2 = 6 Marks)

1) The 8-bit registers W, X, Y & Z are loaded with the value (F2) H, (FF) H, (B9) H and (EA)H respectively. Determine the register content after the execution of the following sequence of micro-operations sequentially.

(i) $W \leftarrow W + X, Y \leftarrow Y + Shl(Z)$

(ii) $Y \leftarrow Y \wedge Z, X \leftarrow X + 1.$

(iii) $W \leftarrow W - Y.$

(iv) $W \leftarrow Shr(X) \oplus Cir(Z)$

2) Which of the following options represents the correct matching?

Addressing Mode	Description
1. Immediate	A. the address field refers to the address of a word in the memory, which in-turn contains the address of the operand
2. Direct	B. the address field contains the address (in main memory) where the operand is stored
3. Indirect	C. operand value is present in the instruction itself (address field)
4. Register Direct	D. the address field of the operand is a register

(i) 1->A; 2->D; 3->C; 4->B

(ii) 1->C; 2->B; 3->D; 4->A

(iii) 1->C; 2->B; 3->A; 4->D

(iv) 1->A; 2->D; 3->B; 4->C

3) Draw and Explain the architecture of 8086 MPU in brief.

SECTION C

(2x3 = 6 Marks)

1) Use the Booth algorithm to multiply -54 (multiplicand) by 19 (multiplier), ~~where each number is represented using 6 bits.~~ Show the procedure in detail.

2) Consider a cache (M1) and memory (M2) hierarchy with the following characteristics:

M1 : 16 K words, 50 ns access time

M2 : 1 M words, 400 ns access time

Assume 8 words cache blocks and a set size of 256 words with set associative mapping.

(i) Show the mapping between M2 and M1.

(ii) Calculate the Effective Memory Access time with a cache hit ratio of h = .85.

-ALL THE BEST-