HEX-SIM: Evaluating Multi-modal Large Language Models on Multi-chiplet NPUs

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***Abstract*—Deep learning models are scaling in both parameters and modalities. Multi-modal large language models are increasingly used in robotic applications, driving the need for large-scale deep learning accelerators. Multi-chiplet heterogeneous neural network accelerators are an effective solution for today's multi-modal large language models. Different types of chiplets provide diverse functionalities, enabling large data storage, high on-chip bandwidth, and significant computing capability. While single-core or multi-core NPU accelerators can be validated through simulation, there is still a lack of software-level cycle-accurate simulators for multi-chiplet NPUs.**

In this work, we propose HEX-SIM, a configurable multi-chiplet deep learning accelerator simulator. HEX-SIM offers designers various macro architectures and system parameters to better evaluate accelerator designs. We conduct extensive simulation experiments using HEX-SIM, demonstrating the effects of parallelism, bandwidth, buffer size, and the number of computing engines on inference latency. These insights can significantly aid users in optimizing their designs. Our project code is open-sourced and available at https://github.com/jimrelief/HEX-SIM.

I. INTRODUCTION

Deep learning algorithms, as well as deep learning accelerators, are widely used in robotic applications [1–3]. Accurate simulation of deep learning accelerators's inference performance before deployment in real robots is crucial, as it helps estimate the performance and energy consumption of robots [4–6], which in turn determines the required computation resources. Researchers have also explored the development of deep learning accelerator simulators.

However, traditional deep learning accelerator simulators are no longer sufficient for simulating the inference procedures of current algorithms used in robotic applications due to two fundamental reasons. **Firstly, neural network models are progressing towards enhanced multi-modal capabilities and larger parameter size.** The models have evolved from single-modality, single-functionality networks, such as keyword spotting networks [7–9], natural language understanding [10–12], and object detection and classification [13–15], to multi-modality, end-to-end large language models like robotic transformer (RT) [16] and PaLM-E [17]. These networks are much larger and incorporate multiple types of layers. For example, PaLM-E includes both convolutional layers and transformers within a single network and contains billions of parameters. The existing simulators are inadequate in simulating multi-modal models and large-scale models effectively. **Secondly, as the scale and modalities of models increase, the scale and diversity of hardware are also expanding.** As the model size and modality increase, the hardware also scales. Deep learning accelerators have evolved from single-core [18–20] to multi-core [21–23] and further to multi-chiplet architectures [24–26]. The emerging chiplet-based DNN accelerator involves integrating multiple multi-core chiplets into a high-throughput, large chip using advanced packaging techniques. This introduces a distinct memory hierarchy and interconnect topology.

Despite extensive studies on multi-core and multi-chiplet Neural Processing Units (NPUs) [27], there is no existing complete simulator for multi-chiplet NPUs that can enable full-system simulation of the NPU, High Bandwidth Memory (HBM), and CPU. Evaluating multi-modality large language models on a multi-chiplet NPU faces two fundamental bottlenecks. Firstly, the complex memory hierarchy and data loading pose new challenges. Unlike SCALE-SIM [28] with a single on-chip buffer, a multi-chiplet NPU stores data across chiplets, multi-core NPUs, and individual cores, with multiple levels of on-chip buffers and off-chip DRAM. Secondly, large models exceed the memory capacity of a single NPU, and different scheduling and partitioning methods result in varied performance.

In this work, we design a cycle-accurate simulator for a multi-chiplet NPU, aiming to analyze and evaluate key parameters that impact resource allocation, performance, and

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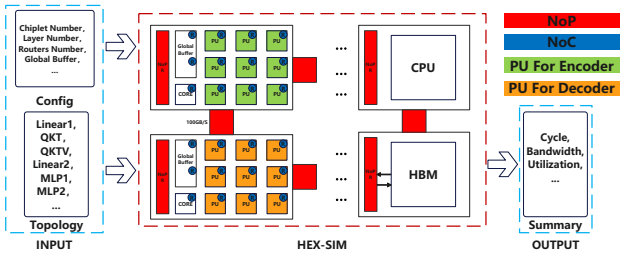


Fig. 1: Schematic depicting HEX-SIM

energy consumption. HEX-SIM establishes a basis architecture for a multi-chiplet integrated NPU and exposes various architectural details, including the number of chiplets, PUs, systolic array size, local buffer size, and system integration parameters like memory bandwidth at each level. Furthermore, HEX-SIM supports a wide range of workloads, especially multi-modality large language models used in robotic applications like robotic transformer and roboflamingo [29]. These models typically encode sensor inputs via convolutional neural networks and decode them into robot control instructions through transformer-based decoders. Even the smallest models have billions of parameters. In addition, HEX-SIM also supports other types of models, apart from the multimodal large language models used for robotic applications. Given the hardware parameters configuration file and workload configuration file, HEX-SIM reports the latency, utilization, SRAM access, and different levels of DRAM access. Fig. 1 shows the workflow of HEX-SIM.

Using HEX-SIM, we conduct a comprehensive analysis of the multi-chiplet NPU design space, uncovering key insights for hardware and software designers. These insights fall into three categories. First, we explore different model parallelism mechanisms, crucial as many large language models exceed single chiplet capacities. Second, we delve into hardware resource allocation for hybrid multi-chiplet NPUs running multi-modality large language models, highlighting performance variations with resource distribution changes. Lastly, we investigate memory size and bandwidth requirements across the memory hierarchy. The insights we propose using HEX-SIM are useful when designing a multi-chiplet NPU.

In summary, this paper makes the following contributions:

- We provide an open-source, cycle-accurate simulator for multi-chiplets NPUs.
- With the simulator, we evaluate multiple state-of-the-art multi-modality large language models used in the robotic domain and with different parallelism execution patterns.
- We provide insights on different trade-offs to help chip designers better allocate hardware resources.

The rest of the paper is organized as follows. We introduce the background and motivation of this paper in Sec. II. Sec. III describes detailed simulator design. Sec. IV evaluates multiple multi-modality large language models and uses HEX-SIM to highlight hardware design insights. Sec. V put this work in the context of related works and Sec. VII concludes the paper.

II. BACKGROUND

This paper is motivated by two trends in the domain of deep learning accelerators. Firstly, the integration of multiple chiplets has emerged as a promising approach for designing large-scale deep learning acceleration systems (Sec. II-A). Secondly, the accurate simulation of deep learning accelerator performance is crucial during the chip design process (Sec. II-B).

A. Large Scale Deep Learning Accelerators

Deep learning accelerators are growing larger as model sizes increase. There are two approaches to building large-scale neural network accelerators. The first approach is wafer-scale integration (WSI), which entails constructing a massive integrated deep-learning accelerator using an entire silicon wafer. For example, chip designers like Cerebras have developed a wafer-scale chip specifically designed to accelerate deep learning applications. This chip is $46225mm^2$ in size and boasts 900,000 cores [30]. However, this design approach comes with challenges related to chip yield and chip cost. The second approach is package-level multi-chiplet integration, which is a more cost-effective and widely adopted method. Each chiplet serves as a small building block designed and fabricated individually. These chiplets are then connected through a silicon interposer or an organic substrate, with efficient intra-package connection circuits also utilized [31].

The multi-chiplet NPU offers several benefits. Firstly, design and fabrication costs are significantly reduced due to the smaller size of chiplets compared to a large monolithic chip. Secondly, scalability is improved as different types of chiplets can be integrated into a single system. Multi-chiplet designs have already seen widespread use in CPUs [32] and GPUs [33]. Additionally, multi-chiplet NPUs have been a recent area of study [34].

However, due to the highly modular design approach, the chiplet-based accelerator introduces a vast design space that encompasses both architecture and workload mapping considerations. From the architecture perspective, the constraints imposed by chiplet sizes and the use of silicon interposers in 2.5D-based accelerators create a trade-off between resource allocations for chiplets and the package. Additionally, the choice of interconnection designs can significantly impact efficiency discrepancies. Designers are faced with higher demands when it comes to exploring architecture options.

B. Deep Learning Acceleration Simulation

Using a system architectural simulator for architecture simulation is considered an effective means for conducting architecture design. Compared to hardware-level simulation, software-level cycle-accurate architectural simulators can provide faster feedback to designers, enabling quicker iterations [35–37].

Researchers have studied software-level cycle-accurate architectural simulators for both single-core and multi-core NPUs, yielding valuable design insights. For instance, results from the single-core simulator SCALE-SIM [28] indicate that no single data flow consistently outperforms others, with the

choice of data flow being tied to the size of the systolic array. mNPUsim [38] suggests that, given the same chip area, a multi-core NPU should incorporate more small-size systolic arrays rather than fewer large-size ones.

Building on the insights gained from previous examples, we introduce HEX-SIM, a cycle-accurate simulator for a multi-chiplet NPU. Our simulator considers diverse types of chiplets, non-uniform memory bandwidth, and varying model-to-chip mappings. Through this work, we aim to uncover valuable insights for designing multi-chiplet NPUs.

III. HEX-SIM DESIGN

In this section, we present our simulator design. We start by describing the architecture of the multi-chiplet NPU system (Sec. III-A). Next, we explain the parallelization of a multi-modal large language model on a multi-chiplet NPU and discuss how to calculate inference latency (Sec. III-B). Finally, we delve into the details of our simulator design (Sec. III-C).

A. Architecture of Multi-Chiplet NPU System

We illustrate the architecture of a basic multi-chiplet NPU in Fig. 2 [24]. This architecture comprises three layers: the chip layer, the chiplet layer, and the processing unit (PU) layer. When running a multi-modality large language model on a multi-chiplet NPU system, it requires at least four types of chiplets: CPU, High Bandwidth Memory (HBM), chiplets for vision encoding, and chiplets for decoding. The CPU dispatches instructions for inference globally, while HBM stores weights and inputs for the network. Given that most large language models in the robotic domain involve multiple modalities, we include two types of chiplets to meet these requirements. Each chiplet is interconnected through a network on package (NoP), with the maximum bandwidth determined by detailed interconnection technologies. In HEX-SIM, the number of CPUs, the number of other chiplets, and the communication bandwidth are configurable according to specific requirements.

Each chiplet designed for vision encoding and decoding is equipped with a local CPU, a global buffer (GB), and several processing units (PUs). These components are interconnected through a MESH topology network on chip (NoC). The maximum bandwidth of the NoC is determined by the design and is configurable. Additionally, the number and size of the PUs and the size of the GB are also configurable.

Each processing unit (PU) is a classic systolic array-based deep learning accelerator, with on-chip SRAM divided into an input buffer, a weight buffer, and an output buffer. The size of the systolic array and on-chip buffer, as well as the dataflow, are configurable. For instance, in our evaluation, PUs for vision encoding are equipped with a 768KB local buffer (LB) and a 16×16 systolic array, while PUs employed for decoding utilize a 1536KB LB and a 32×32 systolic array.

B. Modeling Multi-Chiplet NPU System

HEX-SIM offers cycle-accurate inference simulation for multi-chiplet NPUs, allowing users to validate and optimize their designs in the pre-silicon stage. To achieve this, HEX-SIM employs two accurate modeling approaches. Firstly, it accurately models computation and data flow, including data communication within the same level (e.g., between chiplets) and across different levels (e.g., between HBM chiplets and PUs inside another chiplet). Secondly, HEX-SIM models different types of model parallelism, as this is a fundamental principle when executing large language models.

Modeling Memory Hierarchy, Data Flow and Computation. Latency, utilization, SRAM access, and various levels of DRAM access are crucial parameters that indicate the effectiveness of a chip design, significantly influencing inference performance. We have identified that simulating a multi-chiplet NPU design begins with understanding its memory hierarchy details. Specifically, we accurately quantify the memory size, bandwidth and the data requirements for each layer. By combining these key parameters with data flow information and computations on each systolic array, HEX-SIM calculates the actual performance of a chip.

The memory architecture of a multi-chiplet NPU is categorized into three levels. Within each chip, one or multiple HBM chiplets store weights and inputs. Below the HBM chiplets is a global buffer (GB) located inside each chiplet, and below the GB, there is a local buffer (LB) inside each PU. These three levels of memory are interconnected in a strict dependency: LBs only read or write data to GBs, GBs read from HBM chiplets and write to LBs. We illustrate this hierarchy in Fig. 3.

In HEX-SIM, both GB and LB are modeled in a double-buffer fashion to hide the data communication latency during computation latency. However, due to workload variations and bandwidth differences between NoP and NoC, systolic arrays often need to stall while waiting for data preparation.

For accurate performance simulation, we initially determine the parallelization, which will be discussed later. Once the model parallelization topology is established, HEX-SIM generates a data stream containing the sizes of input and weight matrices for operations at the PU layer. By considering the size of data loaded from HBM to GB and from GB to LB, along with the predetermined data flow of each PU (e.g., input stationary, weight stationary, output stationary), the computation cycle of each systolic array can be simulated. Following the computation, partial sums or final outputs are aggregated back to the HBM chiplet.

In addition to latency, HEX-SIM also reports the average bandwidth of each layer, indicating the potential for improvement in interconnection technology within each layer, as well as the utilization rate of the systolic array. Breakdowns of each layer's data can also be reported upon user request. This information provides valuable insights during the chip design process.

The design principles of HEX-SIM enable not only hardware reconfiguration and expansion but also provide generalizability. Currently, we support four types of chiplets, with two dedicated to vision encoding and language model decoding. With the trend of increasing modalities used in large language models, HEX-SIM can be easily integrated with more types

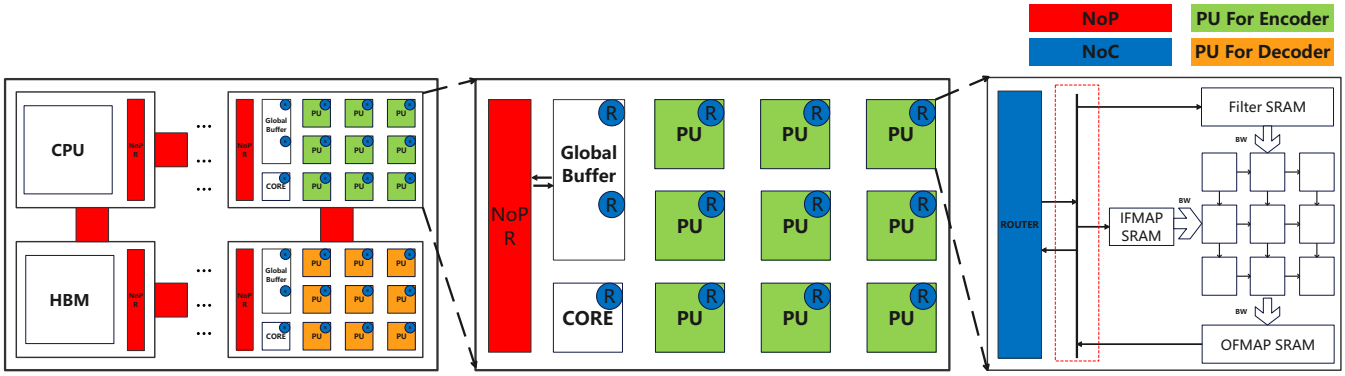


Fig. 2: Architecture of Multi-Chiplet NPU System. The chip consists of heterogeneous chiplets. Four chiplets are used in this work. Inside each chiplet, multiple PUs are connected through a NoC network. PU here means processing unit, each PU is a systolic array based deep learning accelerator. NoP means network on package, which is the connection between different chiplets, NoC means network on chip.

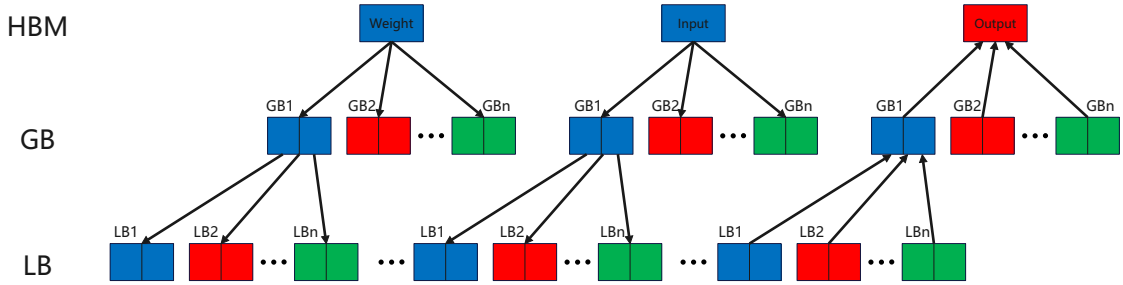


Fig. 3: Memory hierarchy modeling by HEX-SIM. HBM is used to store both weights, inputs and outputs. Each chiplet has its own global buffer (GB), each PU has its local buffer (LB).

of chiplets, such as chiplets for LiDAR processing and neural networks processing point cloud data.

Modeling Parallelism. Multi-chiplet NPUs offer abundant computational resources that enable users to employ various types of model-level parallelism [39], which is crucial for achieving real-time inference with large language models [40]. There are two main types of parallelism: layer-level parallelism, known as pipeline parallelism, and intra-layer parallelism, known as tensor parallelism [41, 42].

In HEX-SIM, we support both pipeline parallelism and two types of tensor parallelism: row parallelism and column parallelism. We explain how tensor parallelism operates in HEX-SIM, as it requires a customized data flow. The data flow for different types of tensor parallelism is illustrated in Fig. 4 and Fig. 5. In particular, the input matrix is denoted by X, the weight matrix by A, and the output matrix by Y.

In Fig. 4, we illustrate the workflow of row parallelism for large models in HEX-SIM. The input matrix is evenly split by column based on the number of chiplets corresponding to the type of the neural network, and similarly, the weight matrix is evenly split by row based on the number of chiplets. These segmented input matrices and weight matrices are transmitted to the chiplet layer through NoP. Within the chiplet layer, the input matrix and weight matrix are further divided

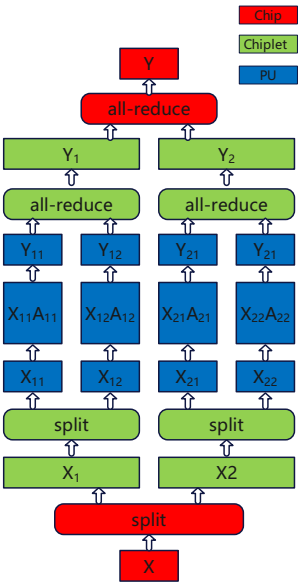


Fig. 4: Row Parallelism, where inputs and weights are distributed to different chiplets in a parallel way.

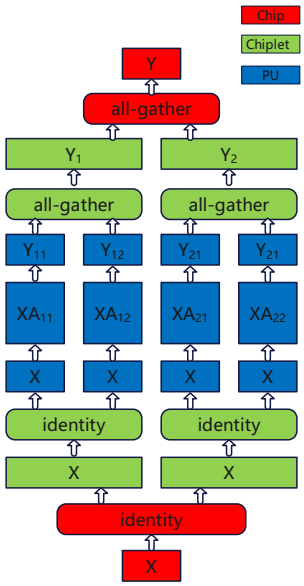


Fig. 5: Column Parallelism, where only weights are distributed to different chiplets in a parallel way.

uniformly based on the number of processing units (PUs) in the chiplet, and then transmitted to each PU through NoC. The input matrix and weight matrix in the PU layer undergo GEMM operations using a systolic array to produce the output matrix. The chiplet layer collects the output matrices from the PU layer through NoC for all-reduce operations. Finally, the output matrix is gathered from the chiplet layer through NoP in the chip layer, and an all-reduce operation is performed to obtain the final result of the GEMM calculation.

In Fig. 5, we depict the process of column parallelism in HEX-SIM. In the chip layer, the input matrix remains unsplit, while the weight matrix is evenly divided by columns based on the number of chiplets. These segmented weight matrices and the input matrix are then transmitted to the chiplet layer through NoP. Within the chiplet layer, the input matrix remains unchanged, while the weight matrix is segmented by column based on the number of processing units (PUs) in the chiplet. These segmented weight matrices are then transmitted to each PU through NoC. Similarly, in the PU layer, the output matrix is calculated using a systolic array. The chiplet layer collects the output matrix from the PU layer through NoC for all-gather operations. In the chip layer, the output matrix is gathered from the chiplet layer through NoP for all-gather operations to obtain the final GEMM calculation result.

The key distinction between column parallelism and row parallelism lies in the partitioning of the input matrix and weight matrix, as well as the aggregation of the output matrix. Row parallelism involves a finer granularity in matrix partitioning compared to column parallelism, resulting in lower computational requirements. However, row parallelism necessitates more complex all-reduce operations for the output matrix and demands a larger data output bandwidth during collection.

Overall, HEX-SIM supports two tensor parallel methods, which influence the GEMM computation of the systolic array in the final PU layer based on the selected parallel method. These different types of parallelism involve trade-offs in terms of inference latency, data movement, and even hardware design considerations, as we will further elaborate on in the evaluation.

C. Simulation Details

HEX-SIM takes both hardware configuration specifications and neural network topology as input for simulation. In this section, we discuss both inputs in detail.

1) Hardware Configuration: We provide an example of hardware configuration in Tbl. I. Since we are modeling a multi-chiplet NPU, users need to input parameters for each layer.

Chip Layer. At the chip layer, users need to specify three parameters: the number of chiplets used for vision encoding, the number of chiplets used for decoding, and the bandwidth of the connection between different chiplets.

Chiplet Layer. For each chiplet, we require information such as the type of chiplet, the number of router ports, the interconnection topology (e.g., mesh), the number of processing units (PUs), the bandwidth, and the size of the global buffer.

PU Layer. For each processing unit (PU), users need to provide the size of the systolic array, the size and partition of the on-chip buffer, the bandwidth, and the data flow. The type of PU should match the type of chiplet; in other words, if there are two types of chiplets in a chip, users should define PU information for both types.

Run Presets. In addition to the above information, users can also choose their preferred type of parallelism. Currently, we support both row and column parallelism, as well as pipeline parallelism.

2) Network Topology: In addition to hardware configuration, HEX-SIM also requires another configuration file describing the network topology. We provide an example of the network configuration in Tbl. II. The network is described in a layer-by-layer fashion, following a format that is similar to most DNN accelerator simulators. To ease the burden on users, we employ the same format for all layers, including convolutional layers and attention layers.

Meanwhile, HEX-SIM also supports mapping matrix operations from attention to the topology structure of convolution. For example, The GEMM operation of $m \times k$ and $k \times n$ can be mapped to a single channel $m \times k$ input matrix and n $1 \times k$

TABLE I: Hardware configuration, including modifiable specifications for chip layer, chiplet layer and PU layer and interconnections.

Package
Parallelism
Number of Encoder Chiplet
Number of Decoder Chiplet
Chiplet(Encoder)
Number of LAYER
Global Buffer Size(kB)
Routers per Global Buffer
Chiplet(Decoder)
Number of LAYER
Global Buffer Size(kB)
Routers per Global Buffer
PU(Encoder)
Array Size
IfmapSram(kB)
FilterSram(kB)
OfmapSram(kB)
Bandwidth
Dataflow
PU(Decoder)
Array Size
IfmapSram(kB)
FilterSram(kB)
OfmapSram(kB)
Bandwidth
Dataflow
Run Presets
Encoder Bandwidth
Decoder Bandwidth

TABLE II: Network topology, indicating the workloads that are running on HEX-SIM.

Parameter	Description
Layer Name	Defined tag
Input Height	Dimension of input matrix
Input Width	Dimension of input matrix
Filter height	Dimension of filter matrix
Filter Width	Dimension of filter matrix
Channels	Number of input channels
Num Filter	Number of filter
Strides	Strides in convolution

TABLE III: Validation, indicating the difference between the RTL computation cycle and HEX-SIM computation cycle.

Workload(matrix size)	RTL(cycle)	HEX-SIM (cycle)
10×10	72	72
20×20	82	82
30×30	92	92
40×40	204	204
50×50	224	224
60×60	244	244
70×70	396	396
80×80	426	426
90×90	456	456
100×100	648	648

convolution kernels when performing convolution with a stride of 1.

IV. EVALUATION

HEX-SIM opens up a huge design space for developing a multi-chiplet NPU. We describe the evaluation setup (sec:eval:set) and evaluate HEX-SIM in this section with two goals. First, we verified the correctness of HEX-SIM and evaluated the performance of different parallelisms given the same software and hardware (Sec. IV-C). We then explore the impact of varying important parameters in the hardware configurations and highlight the performance differences. We change the percentage of decoder chiplets (Sec. IV-E), number of PUs each chiplet owns, global buffer size (Sec. IV-F), and interconnection bandwidth (Sec. IV-G).

A. Validation

We validate HEX-SIM against an in-house RTL implementation of a real multi-chiplet system. We use matrix multiplication as the workload to test the inference cycles. The dataflow is in column parallelism. We have 4 chiplets, each with 2 PU inside. Network topology is mesh. As shown in Tbl. III, the figure the cycle counts obtained by both methods are in good agreement with each other.

B. Evaluation Setup

Software workloads setup. To evaluate HEX-SIM, we utilize three multi-modality large language models that are commonly employed in the robotic domain. Notice that although we mainly evaluate models that are widely used in the robotic domain, HEX-SIM can also serve as a versatile tool for simulating any multi-modality large language models.

- **Robotics Transformer (RT-1).** RT-1 [16] is one of the first several works training a transformer-based model to transfer knowledge from a large multi-modality dataset into downstream robot applications. It uses a neural network mixed with EfficientNet [43] to encode instruction and images and uses 8-layer Transformers [44] to decode robot actions.
- **RoboFlamingo (RF).** RF [29] is another vision language foundation model that can understand language instructions and perform accurate robot control. RF has achieved state-of-the-art performance on task-level manipulation tasks.
- **GR-1.** GR-1 [45] further enriches the type of tasks it allows the robot to execute. Both RF and GR-1 use Vision Transformer as encoders, with different network details. As for the decoder, they both use GPT-2.

Hardware setup. The chip we simulate in total has four different chiplets. We employ a RISC-V CPU for instruction dispatch, and a third-generation HBM is utilized for storing weights, inputs, and activations. For computing, we have two types of chiplets for encoding and decoding separately, each with 5 chiplets. The NoP bandwidth and NoC bandwidth are the same as the first multi-chiplet NPU Simba [24]. The bandwidth of HBM is extracted from its introduction paper [46].

For encoding, each chiplet has 16 PUs, a global buffer with a size to be 1536KB, and a RISC-V core [47]. Each PU is equipped with a 16×16 systolic array, and the size of the local buffer is 768KB evenly split for inputs, weights, and outputs.

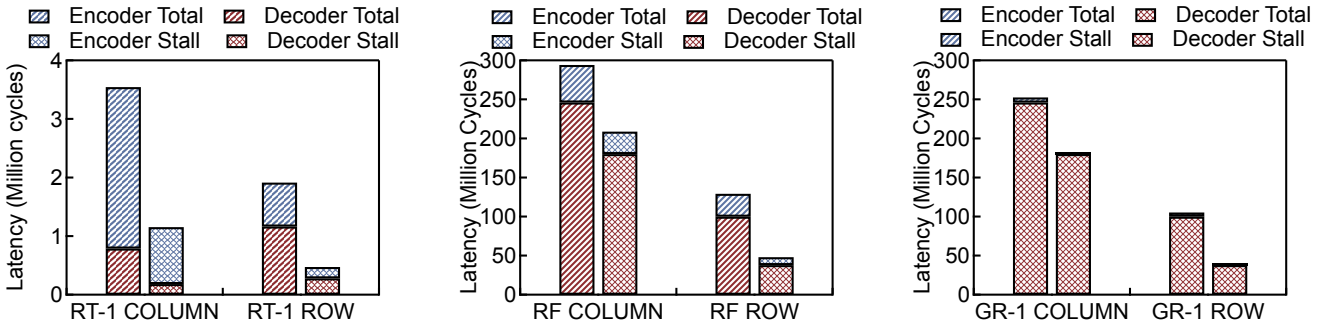
For decoding, each chiplet has 16 PUs, a global buffer with a size to be 3072KB, and a RISC-V core. Each PU is equipped with a 32×32 systolic array, and the size of the local buffer is 1536KB evenly split for inputs, weights, and outputs.

For the behavior of each systolic array, we use an RTL-validated single-core NPU simulation tool SCALE-SIM [28]. Although being cycle-accurate, the entire simulation runs fast. On average, we get the simulation results in around 6 hours running on an intel CORE i5-13600K.

C. Tensor Parallelism

As the scale of models continues to increase, the significance of large-scale multi-chiplet NPUs becomes more evident due to their potential for parallelism. We first compare total cycles consumed and stall cycles in Fig. 6. We find in all three cases, column parallelism costs longer latency compared to row parallelism. The difference in total cycles is 46.0%,56.1%, and 58.3%. Column parallelism also shows longer stall cycles. It stalls on average 281.7% longer compared to row parallelism.

Results suggest that in the workload we evaluate, row parallelism is a better choice compared to column parallelism. We find the key reason lies in the amount of data transmitted. In column parallelism, HEX-SIM only divides the number of filters, while in row parallelism, HEX-SIM divides the



(a) Inference latency of RT-1 with two different parallelisms.

(b) Inference latency of RoboFlamingo with two different parallelisms.

(c) Inference latency of RT-1 with two different parallelisms.

Fig. 6: Latency comparison on different tensor parallelisms. Both total cycles and stall cycles are reported.

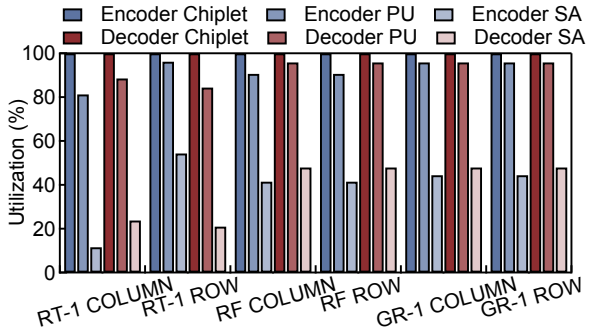


Fig. 7: Utilization for three levels of hardware, chiplet, PU, and systolic array (SA). Statistics of the encoder and decoder are shown separately.

number of channels in the input matrix and weight matrix, while large models usually have a large number of channels. This results in the input matrix size using column parallelism being N times larger than using row parallelism. Among them, N is the product of the number of chiplets and the number of PUs. However, row parallelism requires complex all-reduce operations on the output matrix and also requires a larger output bandwidth. This means when encountering neural networks with fewer channels and more filters, the effect of column parallelism is better than that of row parallelism. The reason is that on the one hand, the segmentation effect of column parallelism is greater than that of row parallelism, and on the other hand, the output bandwidth cannot meet the bandwidth required by row parallelism. Therefore, we believe that the choice of parallelism should be tailored to specific network types rather than adopting a fixed approach.

The utilization statistics support our findings. As shown in Fig. 7, both two parallelisms are having a high chiplet utilization. In all cases, the chiplet utilization is 100%, this means the scheduling works well and all the chiplets are used. PU utilization is also high. On average, the PU utilization is 91.3% for encoder stage and 92.6% for decoder stage. The utilization of PU is not perfect, as in some cases, there is no data scheduled on PU. In row parallelism, for example, weights are splited on the basis of channels, when the channels scheduled for each chiplet is smaller than the number of PUs, there will be idle PUs in this round of computation. We find this phenomenon is common in attention computation.

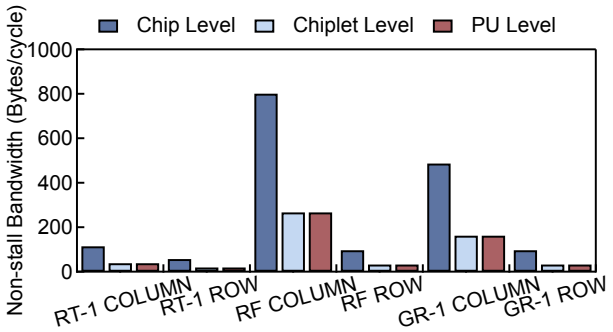
However, compared to the utilization of chiplets and PUs, the SA utilization is both in a relative low level. We witness an average utilization of 39.6% in encoder stage and a 35.4% in decoder stage, indicating that each systolic array is far from fully utilized. The reason is in two folds, first, the size of the matrix computation scheduled on each systolic array is usually smaller than the array size, even if we only use 16×16 and 32×32 MAC array. Second, the data communication rate can not catch up the computation speed. Thus, in many cases, the systolic array is stalled waiting to be fed with data.

Row parallelism is having a high utilization compared to column parallelism. The PU utilization of row parallelism is 4.9% higher compared to column parallelism, and the SA utilization is 10.1% higher. Both cases suggest that in the three networks we evaluate, row parallelism is a better topology as it significantly reduces the volum of data in communication. The results also validate that in row parallelism, the stall cycle is lower compared to the column parallelism.

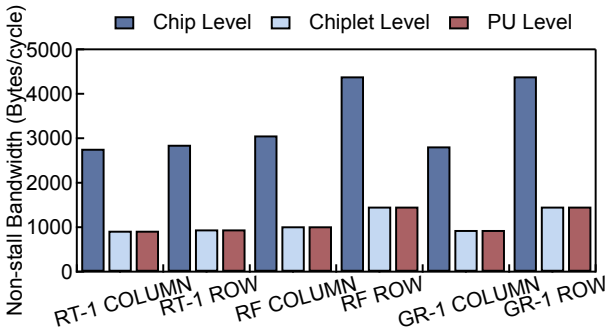
D. Non-stall Bandwidth

Stalling cycles take a significant amount of time. Our findings indicate that the primary reason for this is insufficient bandwidth. To demonstrate the bandwidth requirements for achieving non-stalling inference, we conducted an experiment. We show the results in Fig. 8 and separate the bandwidth requirements for input and output.

We can see that the minimum bandwidth for NoC to read and write LB is the same as the minimum bandwidth for LB to read and write systolic array, and the minimum read and write bandwidth for NoP to GB is three times that of NoC to LB. Meanwhile, the minimum write bandwidth required for RT-1 in row parallelism is 49.8% of the bandwidth in column parallelism. Similarly, the data for RF is 12.1% and GR-1 is 19.8%. In column parallelism, the minimum read bandwidth required for RT-1 is 96.9% when using row parallelism, RF is 69.8%, and GR-1 is 64.1%.

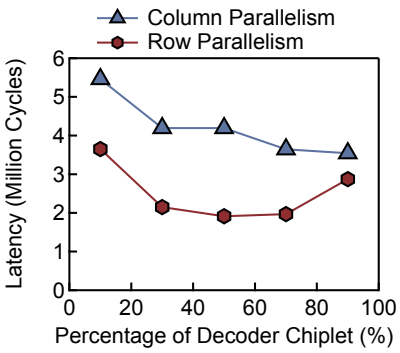


(a) Non-stall bandwidth requirements for data loading.

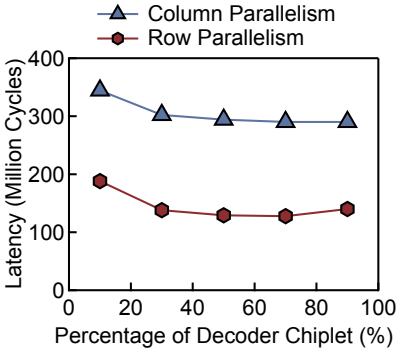


(b) Non-stall bandwidth requirements for data offloading.

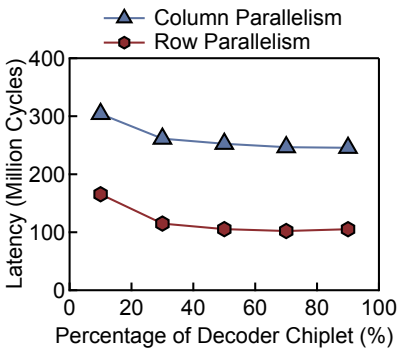
Fig. 8: Non-stall bandwidth requirements for input data loading and output data offloading.



(a) Inference latency change of RT-1 when the number of decoder chiplets change.



(b) Inference latency change of RoboFlamingo when the number of decoder chiplets changes.



(c) Inference latency change of GR-1 when the number of decoder chiplets changes.

Fig. 9: Latency changes when the percentage of decoder chiplet changes. X-axis means the percentage of decoder chiplets compared to total computing chiplets.

As we expected, at both read and write stage, the bandwidth requirements at chip layer is the highest. When gathering the output data, the non-stop bandwidth requirement reaches up to over 4000 Bytes per cycle, which is far beyond the upper bond of current technology. An effective way of lowering the burden on chip layer interconnection is to capture and utilize data locality more inside each chiplet.

E. Decoder Chiplet Scale

HEX-SIM provides simulation for heterogeneous multi-chiplet NPUs, which is a design trend, as robotic applications are using different sensor types. In our current evaluation, the encoder and decoder exhibit different chiplet designs. A natural design decision would be given the fixed chip area, increasing the scale of which type of chiplets would benefit the overall performance.

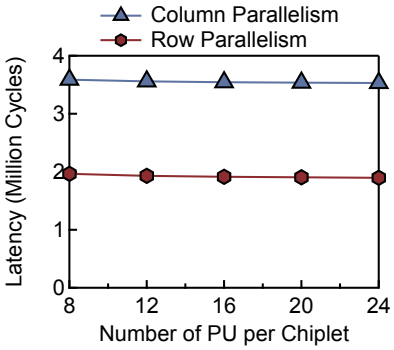
We gradually increase the number of decoder chiplets and re-run our simulation. We show the results in Fig. 9, where the x-axis represents the percentage of decoder chiplets used in total computing chiplets. Results show that the performance increase by 30.7% when the percentage of decoder chiplets increases from 10.0% to 70.0%. The performance improvement converges when further increasing resources on the decoder. For RT-1, further, increasing the percentage to 90.0% can even hurt the performance.

The result suggests that we use more chiplets for the decoder than for the encoder. The main reason for this is that the neural network in the decoder part has a larger number of parameters than the encoder part. The decoder parameters of RT-1, RF, and GR-1 account for 61.3%, 83.4%, and 94.7% respectively, so that the performance increases as the decoder ratio increases. Meanwhile, we also find that performance growth is slow when it accounts for 70.0% -90.0% of the total. This is because parallelism cannot be linearly increased based on the number of chiplets.

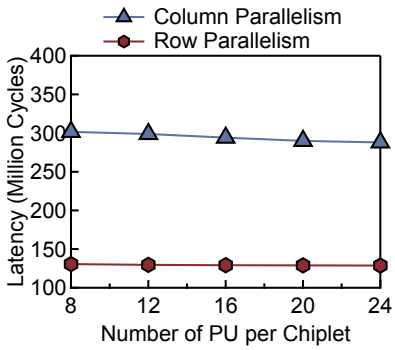
We find that in the case of RT-1, when the number of decoder chiplets exceeds 70% of the total chiplets, the runtime actually increases. This is because RT-1 is a relatively early model, with parameters in encoder and decoder to be the same. Thus, a fixed encoder decoder distribution may not be the optimal solution if runtime reconfiguration is possible.

F. PU Number and Global Buffer Size

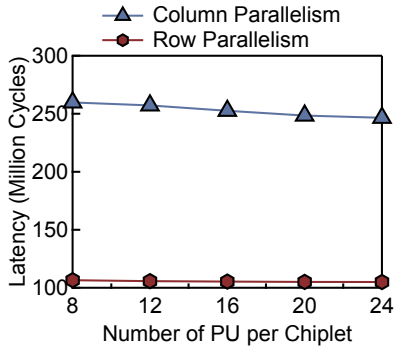
The number of PUs and size of the global buffer determines the computing capability of one single chiplet, yet stacking more computing and storage also increases the size of the chip. The stacked resources are wasted if not fully utilized. To evaluate the impact, we sweep the number of PUs and the size of global buffer.



(a) Inference latency of RT-1 when the number of PUs change.

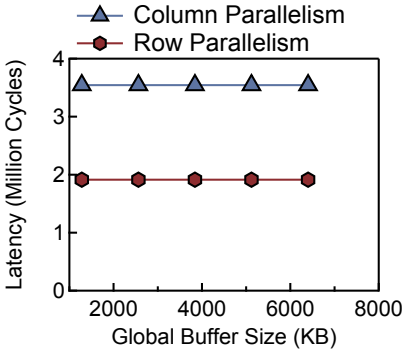


(b) Inference latency of RoboFlamingo when the number of PUs change.

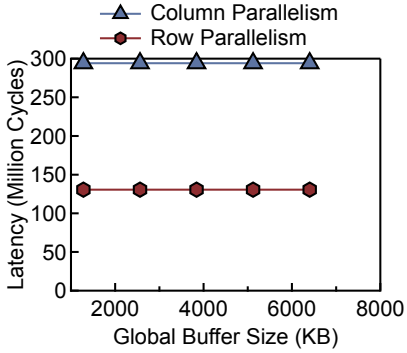


(c) Inference latency of RT-1 when the number of PUs change.

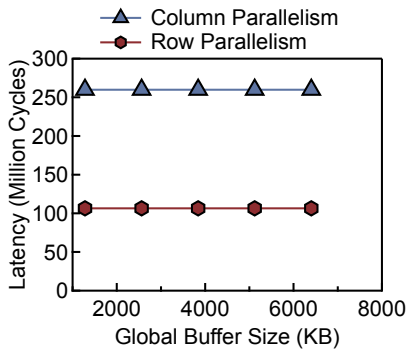
Fig. 10: Latency changes when the number of PUs changes. The X-axis means the number of PUs in one chiplet.



(a) Inference latency of RT-1 when global buffer size changes.



(b) Inference latency of RoboFlamingo when global buffer size changes.



(c) Inference latency of RT-1 when global buffer size changes.

Fig. 11: Latency changes when the size of the global buffer changes. X-axis means the size of the global buffer.

Fig. 10 shows the performance variation when increasing the number of PUs in one chiplet. We scale both encoder and decoder chiplets. When the number of PU in the chiplet increases by 4 each time, its average performance improves by 1.0%, 0.9%, 0.7%, and 0.4%. This is very obvious, the increase in PU has little effect on performance improvement, and the magnitude of performance improvement is gradually decreasing. The reason for this phenomenon is that the read and write bandwidth of GB is limited, and it cannot provide enough data for PU calculation. Moreover, the increase in PU cannot linearly improve parallelism, resulting in a smaller performance improvement.

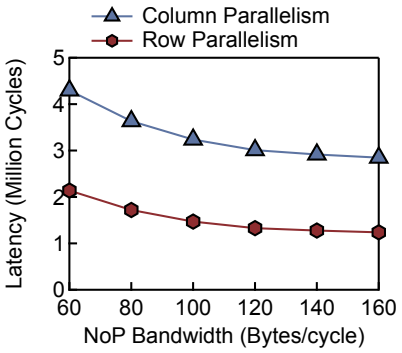
Fig. 11 shows the result on increasing the size of GB. We enlarge the GB size from 1280 KB to 6400 KB. Surprisingly, although the size of GB is increasing, performance has not been improved. This is because the GB read and write time is composed of non-stall time and stall time. The non-stall time for reading is obtained by dividing the transmitted data by the bandwidth, where the transmitted data and bandwidth do not change with the size of the GB. Then, the stall time is the difference between the division value of data and write bandwidth and the division value of data and read bandwidth. If the write bandwidth is greater than the read bandwidth, the stall time is 0. But in either case, the stall time is independent of the size of the GB. Thus, when the bandwidth is low, increasing the size of GB does not help.

G. Effect of NoP and NoC Bandwidth

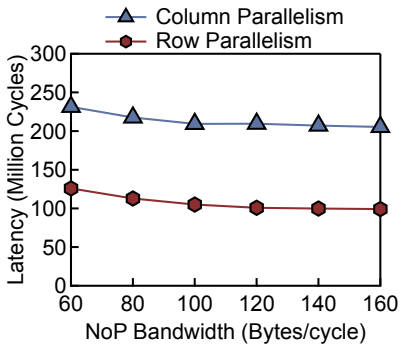
In the above subsections, we have observed that increasing the number of processing units (PUs) and the size of global buffers (GBs) does not have a significant impact on overall performance. We here further analyze the relationship between larger bandwidth with the performance. Notice that given the current technology, the NoP and NoC bandwidth we use in this evaluation may not be satisfied in real products, with some of the results being hypothetical. Therefore, these findings are intended to provide insights for chip designers rather than representing actual performance.

Fig. 12 shows the performance variation with increased NoP bandwidth. We tested the bandwidth of NoP from the 60 Bytes per CLK to 160 Bytes per CLK. The average performance improvements in each interval were 12.4%, 8.7%, 5.4%, 2.0%, and 1.5%, respectively. Performance does indeed increase with the increase of NoP bandwidth, yet the performance improvement is extremely limited when the NoP bandwidth exceeds 120 Bytes per CLK.

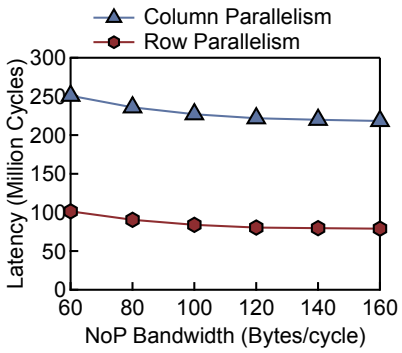
As shown in Fig. 13, similar to NoP bandwidth, increasing NoC bandwidth can also improve performance. We tested



(a) Inference latency of RT-1 when NoP bandwidth changes.

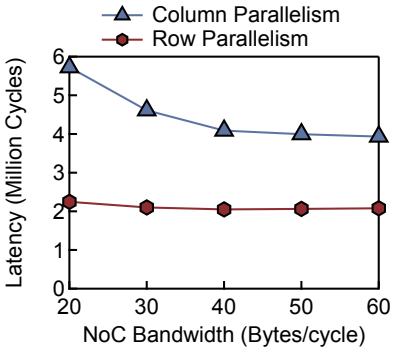


(b) Inference latency of RF when NoP bandwidth changes.

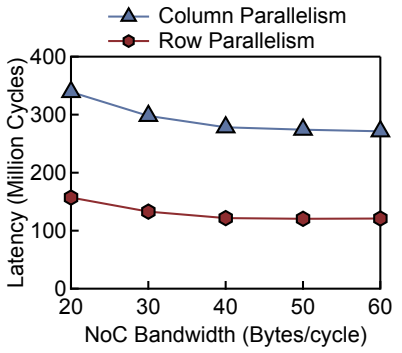


(c) Inference latency of GR-1 when NoP bandwidth changes.

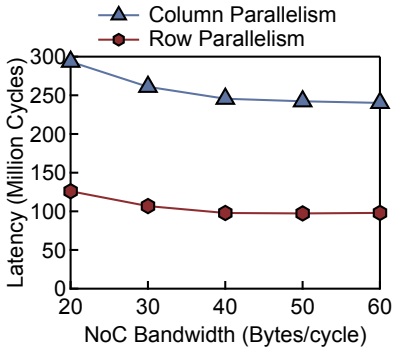
Fig. 12: Latency changes when the bandwidth of NoP changes.



(a) Inference latency of RT-1 when NoC bandwidth changes.



(b) Inference latency of RF when NoC bandwidth changes.



(c) Inference latency of GR-1 when NoC bandwidth changes.

Fig. 13: Latency changes when the bandwidth of NoC changes.

the NoC bandwidth range from 20 Bytes to 60 Bytes per CLK, with average performance improvements of 13.3%, 7.2%, 1.0%, and 0.3% for each interval, respectively. The improvements converge NoC bandwidth reaches 40 Bytes per CLK.

Both trends indicate that higher bandwidth NoP and NoC will provide sufficient data flow for the systolic array to perform calculations, and thus resulting in improved performance, particularly in scenarios with high data communication volume like column parallelism. The performance improvement gradually converges as the bandwidth of LB to SA does not scale with the bandwidth of NoP or NoC, the bottleneck thus transfer from data communication between chiplets and PUs to data communication inside PUs. However, we can still get the conclusions that improving bandwidth is the most effective approach of reducing runtime latency for a multi-chiplet NPU.

H. Real Hardware Evaluation

As shown in Tbl. IV, we simulate SIMBA, the first multi-chiplet NPU chip. We use all the parameters reported from SIMBA's original paper, which achieves a theoretical peak performance at 128 TOPS.

It is worth noting that the RF we selected has a larger number of model parameters in the encoder stage than GR1, but the actual inference performance of RF is slightly lower than that of GR1. This is because larger data volumes require higher bandwidth. Therefore, the actual inference performance of RF on SIMBA is lower than that of GR1.

TABLE IV: Real hardware evaluation, indicating the inference performance of different neural networks on Simba.

Network	Latency(ms)	Actural Performance(TOPS)
RT1	1.84	31.61
RF	183.60	56.85
GR1	157.48	58.12

V. Related Work

Multi-modality large language models for robotic applications. Using large models to control robots show great potentials in extending the usability of robots in complex tasks. Most state-of-the-art methods are applying multi-modal large language models in their solution. These large language models usually have multiple modalities such as vision and human language instructions and are consuming significant high inference latency [48–50]. Accelerating these multi-modality large language models is thus critical for real-time and low-power robotic applications [51].

Simulating performance of NPUs. Since NPUs have been widely used in data center and edge devices, simulating the

performance of different NPUs are proposed by the community. Tools like SCALE-SIM [28] first incorporate different data flows and provide cycle-accurate simulation for a single-core NPU and mNPUsim [38] further extend the simulating methodology to multi-core. SIAM [52] belongs to multi-chiplet simulation. However, SIAM only simulates in-memory computing (IMC) architectures. Our work provides the first multi-chiplet simulator for non-IMC architecture, which is still the major design methodology in most real-world products. To our knowledge, HEX-SIM provides the first cycle-accurate non-IMC architecture simulation tool for a heterogeneous multi-chiplet NPU.

Multi-chiplet chip design. Designing large monolithic chips to enhance chip performance has been a traditional approach to improving chip performance. However, larger die sizes of these chips can negatively impact yield and drive up costs. To address this, multi-chiplet chip design has been widely adopted in commercial products, such as AMD ZEN CPUs [53] and Radeon GPUs [54]. We have observed the same design methodology being utilized in NPU designs, such as Simba and Gemini [24, 55]. This emerging trend further motivates our work, with a particular focus on developing tools and simulations in this field.

VI. DISCUSSION

Chiplet has become an effective way of integrating heterogeneous chips into one computing system. In this work, we integrate four different chiplets to form an NPU to support the inference of multi-modal large language models that are widely adopted in the robotic domain.

We also support the flexibility for the users to integrate their own chiplets. To do so, users need to program a template file for the users to design their customized chiplet. The template file contains all needed parameters such as connectivity models, the number of PUs, the size of the global buffer, NoC bandwidth, and the hardware architecture of PUs. The type of PU needs to be within the current library we support, with detailed parameters such as the size of the systolic array, dataflow, the size of the local buffer, etc. If the users want to incorporate a chiplet out of our library, such as an in-memory computing unit, they can also be plugged in through an additional cycle-accurate simulator of the PU itself.

VII. CONCLUSION

Motivated by the increase of parameters and modality of neural networks, this work presents a cycle-accurate simulator for multi-chiplet NPUs. Using HEX-SIM, users can effectively test the performance and optimize their NPU designs. Through thorough evaluation using HEX-SIM on three state-of-the-arts multi-modality large language models, we find that the chiplets used for the decoder and interconnection bandwidth contribute most to performance improvements, while the size of global buffers and number of PUs are bounded by the above two parameters. The code is available at https://github.com/jimrelief/HEX-SIM.

VIII. ACKNOWLEDGMENTS

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