



# Gowin Software Quick Start Guide

SUG918-1.7.1E,2023-12-29

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## Revision History

Date	Version	Description
05/07/2020	1.0E	Initial version published.
09/07/2020	1.1E	<ul style="list-style-type: none"><li>● RTL schematic added.</li><li>● File encryption added.</li><li>● Tcl command added.</li></ul>
10/21/2020	1.1.1E	Use GowinSynthesis as an example to describe synthesis.
06/10/2021	1.2E	<ul style="list-style-type: none"><li>● Synplify Pro removed.</li><li>● MIPI IP in the design modified.</li></ul>
11/02/2021	1.3E	Some descriptions updated.
07/28/2022	1.4E	Modified the design to FIFO HS and updated the relevant descriptions.
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08/18/2023	1.6E	The descriptions of timing optimization removed.
11/30/2023	1.7E	<ul style="list-style-type: none"><li>● create_project, import_files, and run close commands added.</li><li>● Some screenshots in Chapter 3 Quick Start updated.</li></ul>
12/29/2023	1.7.1E	<ul style="list-style-type: none"><li>● The title of Figure 3-3 updated to FIFO HS Configuration.</li><li>● Minor description changes.</li></ul>

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# 1 About This Guide

## 1.1 Purpose

This manual uses FIFO HS as an example to introduce Gowin Software and aims to help you get familiar with the usage and improve the design efficiency.

## 1.2 Related Documents

You can find the related documents at [www.gowinsemi.com](http://www.gowinsemi.com):

- [SUG100, Gowin Software User Guide](#)
- [SUG935, Gowin Design Physical Constraints User Guide](#)
- [SUG101, Gowin Design Timing Constraints User Guide](#)
- [SUG114, Gowin Analyzer Oscilloscope User Guide](#)
- [SUG282, Gowin Power Analyzer User Guide](#)
- [SUG502, Gowin Programmer User Guide](#)
- [SUG550, GowinSynthesis User Guide](#)
- [SUG755, Gowin HDL Schematic Viewer User Guide](#)
- [SUG1018, Arora V Design Physical Constraints User Guide](#)

## 1.3 Terminology and Abbreviations

Table 1-1 shows the abbreviations and terminology used in this manual.

**Table 1-1 Terminology and Abbreviations**

Terminology and Abbreviations	Meaning
AO Core	Analysis Oscilloscope Core
BSRAM	Block Static Random Access Memory
DFF	D Flip-Flop
FloorPlanner	FloorPlanner
GAO	Gowin Analyzer Oscilloscope
GPA	Gowin Power Analyzer

Terminology and Abbreviations	Meaning
I/O	Input/Output
IP Core	Intellectual Property Core
PnR	Place & Route
RTL	Register Transfer Level

## 1.4 Support and Feedback

Gowin Semiconductor provides customers with comprehensive technical support. If you have any questions, comments, or suggestions, please feel free to contact us directly by the following ways.

Website: [www.gowinsemi.com](http://www.gowinsemi.com)

E-mail: [support@gowinsemi.com](mailto:support@gowinsemi.com)

# 2 Introduction

## 2.1 Design Flow Introduction

Gowin Software is available in Windows and Linux. It supports GUI running mode and commands running mode. Take the GUI running mode in Windows and FIFO HS design as an instance to introduce quick start of Gowin Software.

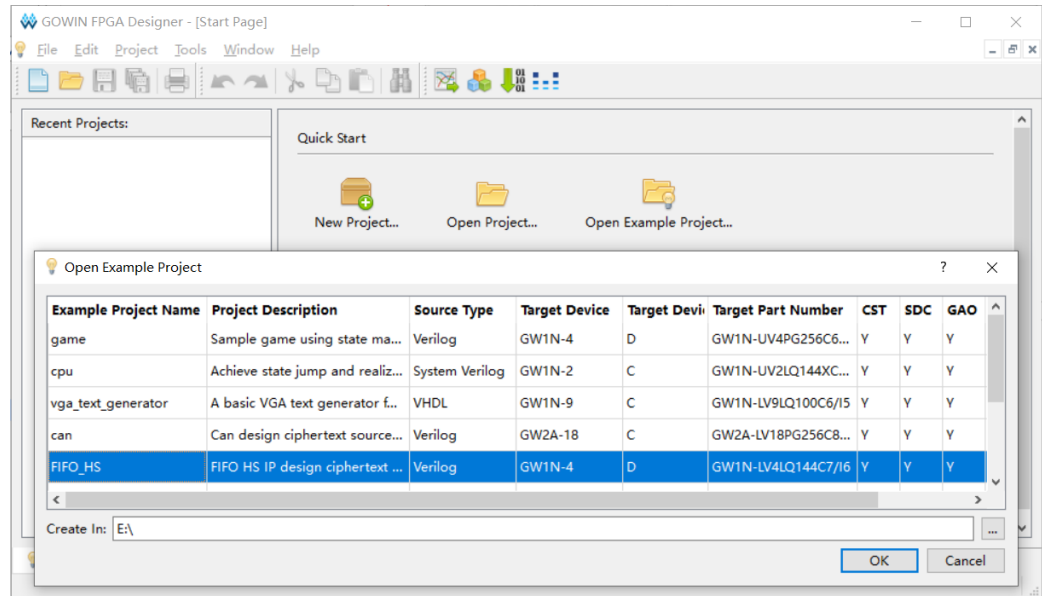
The design uses FloorPlanner to add physical constraints, uses Timing Constraints Editor to add timing constraints, uses GAO to add GAO config file and to capture data, GPA to add GPA config file, and Programmer to download bitstream.

## 2.2 Quick Started Design Introduction

FIFO HS IP can complete the data transmission and buffering with different bit widths in the asynchronous clock domain, and configure different output control signals and data structures according to your requirements.

The whole design provides clock for FIFO HS through port, provides reset signal, enable signal and input data through logic, and finally uses GAO to collect data to verify the correctness of FIFO HS.

The design has been added to the sample project FIFO\_HS, which can be quickly created by clicking "Start Page > Open Example Project...", as shown in Figure 2-1. Creating a project through the example will skip the previous steps and go directly to placement and routing, and the subsequent process. If you want to be familiar with the use of Gowin Software step by step, you can operate according to the guidelines in the document. The source files, constraint files and configuration files involved in the design are consistent with those in the sample project. You can save the files in the sample project for later use.

**Figure 2-1 Open Example Project**

# 3 Quick Start

## 3.1 Create a New Project

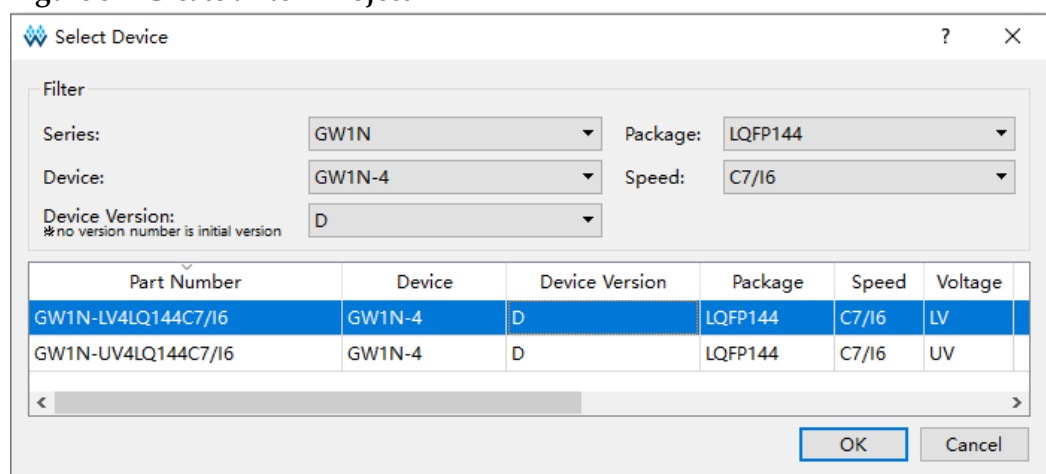
### 3.1.1 Create a New Project

Open Gowin Software and click "Start Page > Quick Start > New Project" to create a new project named as FIFO\_HS. The device selected is as shown in Figure 3-1.

- Series: GW1N
- Device: GW1N-4
- Device Version: D
- Package: LQFP144
- Speed: C7/I6
- Part Number: GW1N-LV4LQ144C7/I6

Click "Next" until the project creation completed. For the details, please refer to [SUG100, Gowin Software User Guide](#).





**Figure 3-1 Create a New Project**



After the project is created, the impl and src folders are generated under the project creation path, as shown in Figure 3-2. impl contains

synthesis and PnR files and src contains the source files.

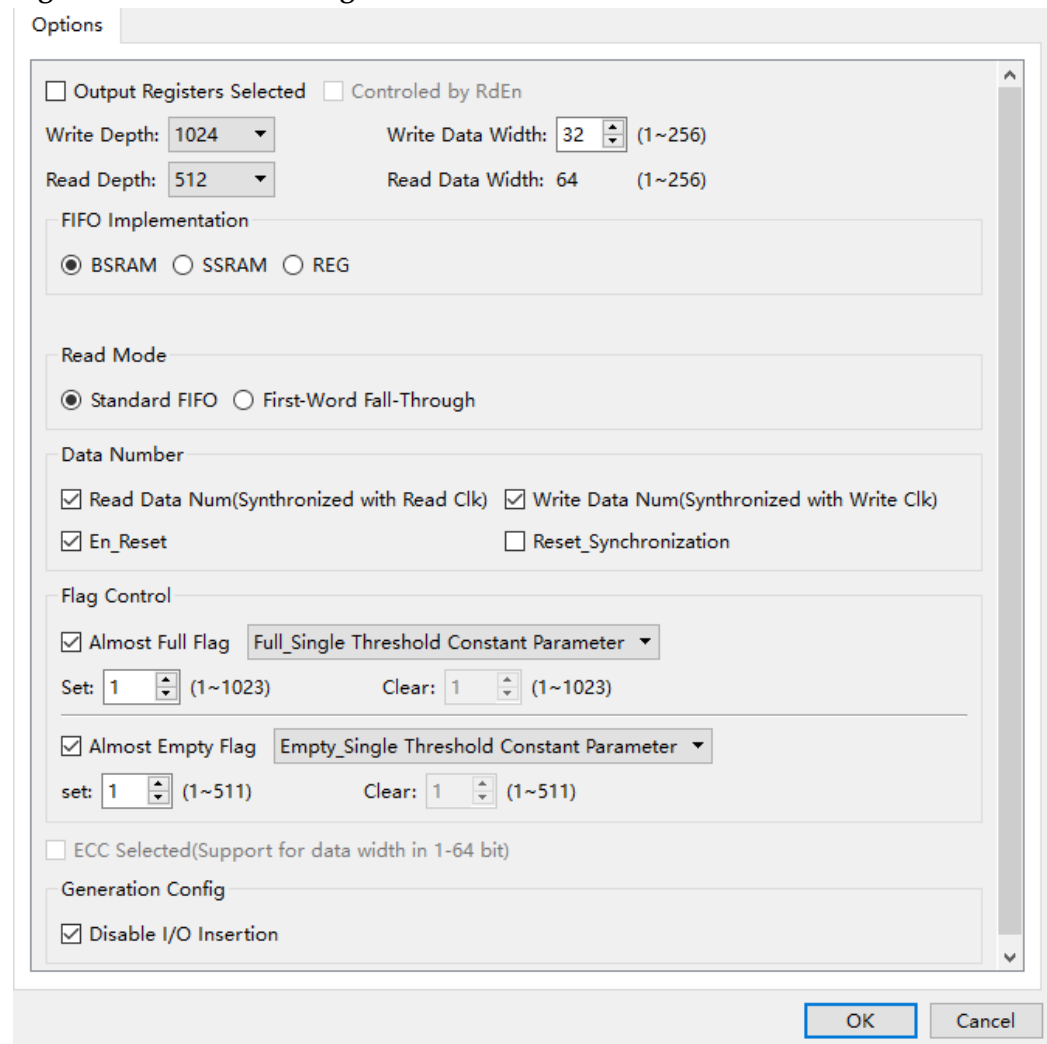
**Figure 3-2 Project Directory**

Name	Date modified	Type	Size
 impl	5/31/2022 15:54	File folder	
 src	5/31/2022 15:54	File folder	
 FIFO_HS.gprj	5/31/2022 15:43	GPRJ File	1 KB
 FIFO_HS.gprj.user	5/31/2022 15:51	USER File	4 KB

### 3.1.2 Generate FIFO HS IP

Click "Tools > IP Core Generator" to open the IP Core Generator window. Double-click "Memory Control > FIFO > FIFO HS" to open the IP Customization dialog box to configure as required. The FIFO HS configuration in this design is shown in Figure 3-3. Then click "OK" to generate FIFO HS IP.

**Figure 3-3 FIFO HS Configuration**



The image shows the 'FIFO HS Configuration' dialog box with the 'Options' tab selected. The configuration is as follows:

- ☐ Output Registers Selected ☐ Controlled by RdEn
- Write Depth: 1024 (dropdown) Write Data Width: 32 (dropdown, range 1~256)
- Read Depth: 512 (dropdown) Read Data Width: 64 (dropdown, range 1~256)
- FIFO Implementation: ☒ BSRAM ☐ SSRAM ☐ REG
- Read Mode: ☒ Standard FIFO ☐ First-Word Fall-Through
- Data Number:
  - ☒ Read Data Num(Synthonized with Read Clk) ☒ Write Data Num(Synthonized with Write Clk)
  - ☒ En\_Reset ☐ Reset\_Synchronization
- Flag Control:
  - ☒ Almost Full Flag: Full\_Single Threshold Constant Parameter (dropdown)
    - Set: 1 (dropdown, range 1~1023) Clear: 1 (dropdown, range 1~1023)
  - ☒ Almost Empty Flag: Empty\_Single Threshold Constant Parameter (dropdown)
    - set: 1 (dropdown, range 1~511) Clear: 1 (dropdown, range 1~511)
- ☐ ECC Selected(Support for data width in 1-64 bit)
- Generation Config:
  - ☒ Disable I/O Insertion

At the bottom right, there are 'OK' and 'Cancel' buttons.

After generation, IP design files and simulation files are generated under the IP creation path, as shown in Figure 3-4.

- .v file is an IP design file, encrypted.
- \_tmp.v is an IP design template file.
- .vo file is an IP simulation model file, unencrypted.
- .ipc file is an IP configuration file. The user can load the file to modify the configuration.
- temp contains the files required to generate the IP.
- The doc, model, sim, and tb contain the simulation files: readme text, simulation model, simulation script, and testbench.

**Note!**

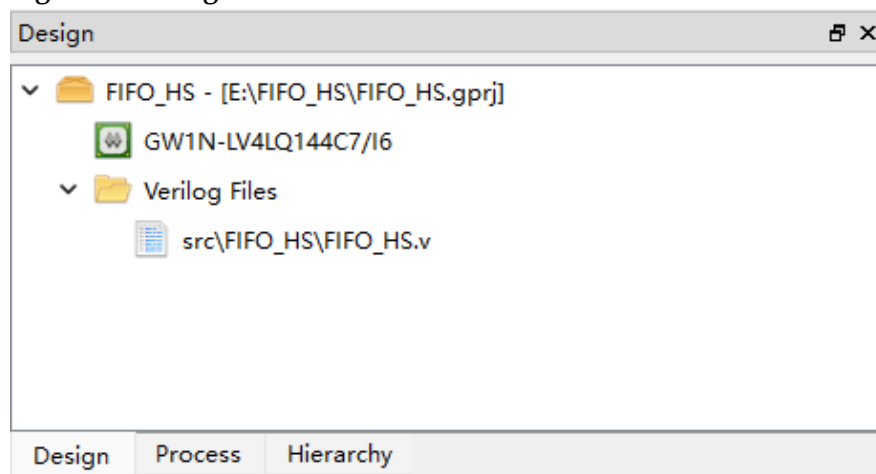
- For Gowin Software 1.9.8.06 and later versions, if VHDL is selected as the Language during IP generation, .vho file will be generated under the IP creation path, which is an IP simulation model file in plaintext.
- At present, for some IPs, the created path still generates doc, model, sim, and tb folders, indicating readme text, simulation model, simulation script, and testbench simulation file. The IP directory is subject to IP Core Generator in use.

**Figure 3-4 FIFO HS IP Directory**

Name	Date modified	Type	Size
temp	5/31/2022 15:54	File folder	
FIFO_HS.ipc	5/30/2022 16:59	IPC File	1 KB
FIFO_HS.v	5/30/2022 16:59	V File	59 KB
FIFO_HS.vo	5/30/2022 16:59	VO File	60 KB
FIFO_HS_tmp.v	5/30/2022 16:59	V File	1 KB

After FIFO HS IP is generated, the Design window is as shown in Figure 3-5.

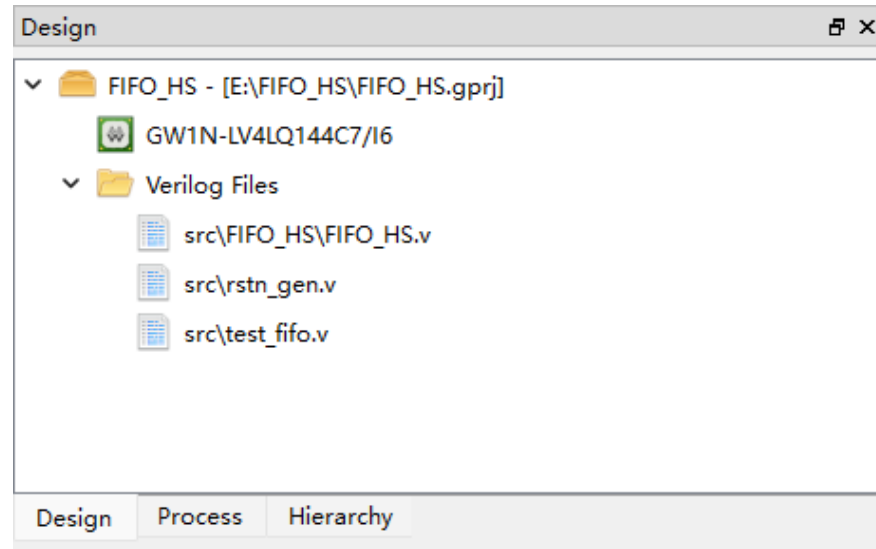
**Figure 3-5 Design Window**



### 3.1.3 Load File

In order to test FIFO HS, some design files need to be loaded or created, as shown in Figure 3-6. For the steps to load files, you can see [Section 2.2 Quick Started Design Introduction](#).

Figure 3-6 Load Files



## 3.2 RTL Schematic

After the source file is loaded, you can view the RTL design schematic by clicking "Tools > Schematic Viewer > RTL Design Viewer" to help you better understand the RTL logic. For details, see [SUG755, Gowin HDL Schematic Viewer User Guide](#).

## 3.3 GAO Configuration

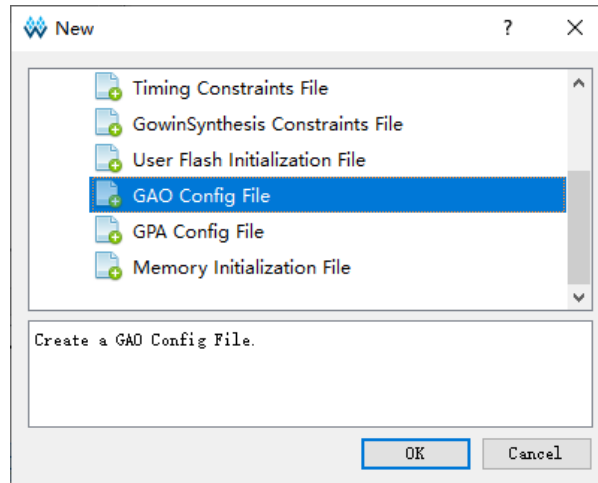
Gowin Software supports two signal capture sources: RTL-level signal capture and post-synthesis netlist-level signal capture; GAO config. file can be created after the source files are created or loaded at the RTL level, and GAO config. file can be created after the synthesis is completed at the post-synthesis netlist level. GAO config. file can be used to capture data and verify the the design. In addition, Gowin Software provides Standard Mode GAO and Lite Mode GAO. For the usage, see [SUG114, Gowin Analyzer Oscilloscope User Guide](#).

This design uses RTL-level signal capture and Standard Mode GAO as an instance.

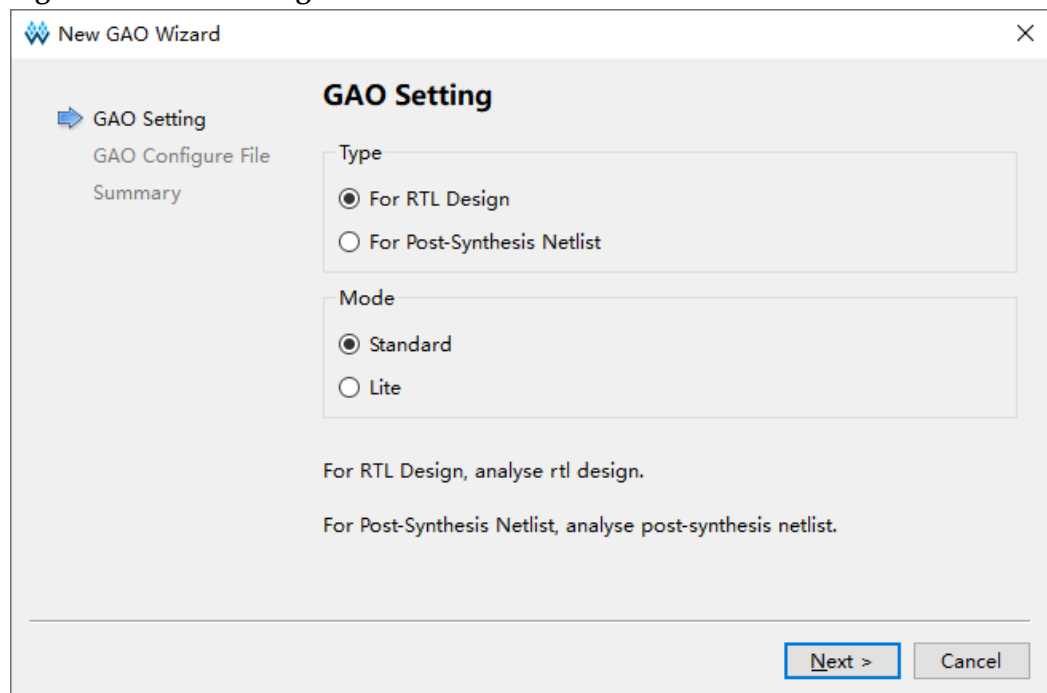
### 3.3.1 Create Standard Mode GAO Config File

Select "Design > New File..." to open "New" dialog box, and select "GAO Config File" in "New", as shown in Figure 3-7. Click "OK".



**Figure 3-7 Create GAO Config File**

Select "For RTL Design" in Type, and "Standard" in Mode, as shown in Figure 3-8. Click "Next". The file name is FIFO HS. Then click "Next" until finished.

**Figure 3-8 GAO Setting**

### 3.3.2 Configure Standard Mode GAO

After file created, you can configure the number of AO cores, trigger options and capture options. The trigger options include match unit, trigger port, match type and expressions; The capture options include sample clock, capture, capture utilization and capture signals. In this design the number of AO cores is 1 and the trigger options and capture options configuration are shown in Figure 3-9 and Figure 3-10.

**Figure 3-9 Trigger Options Configuration**

Match Unit	Trigger Port	Match Type	Function	Counter	Value
<input checked="" type="checkbox"/> M0	Trigger 0	Basic w/edges	==	Disabled	R
<input type="checkbox"/> M1	NONE	Basic	==	Disabled	
<input type="checkbox"/> M2	NONE	Basic	==	Disabled	
<input type="checkbox"/> M3	NONE	Basic	==	Disabled	
<input type="checkbox"/> M4	NONE	Basic	==	Disabled	
<input type="checkbox"/> M5	NONE	Basic	==	Disabled	
<input type="checkbox"/> M6	NONE	Basic	==	Disabled	
<input type="checkbox"/> M7	NONE	Basic	==	Disabled	
<input type="checkbox"/> M8	NONE	Basic	==	Disabled	
<input type="checkbox"/> M9	NONE	Basic	==	Disabled	
<input type="checkbox"/> M10	NONE	Basic	==	Disabled	

**Figure 3-10 Capture Options Configuration**

**Sample Clock**

Clock:  ...

Sample On: ☒ Rising ☐ Falling

**Capture**

Storage Size:

Windows Number:

Capture Amount:

GAO Implementation:

Trigger Position:

☐ Force Trigger by Falling Edge

**Capture Utilization**

BSRAM Usage : 6/10

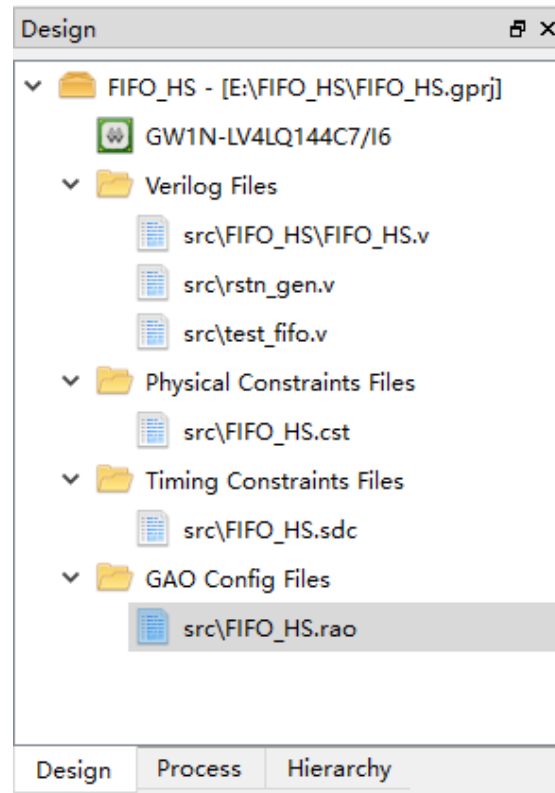
**Capture Signals**

Add Add From Trigger Remove

- rst\_n
- error
- w\_en
- > w\_data[15:0]
- r\_en
- > r\_data[31:0]

After configuration, click "Save" to finish and the design window is as shown in Figure 3-11.

Figure 3-11 GAO Config Files



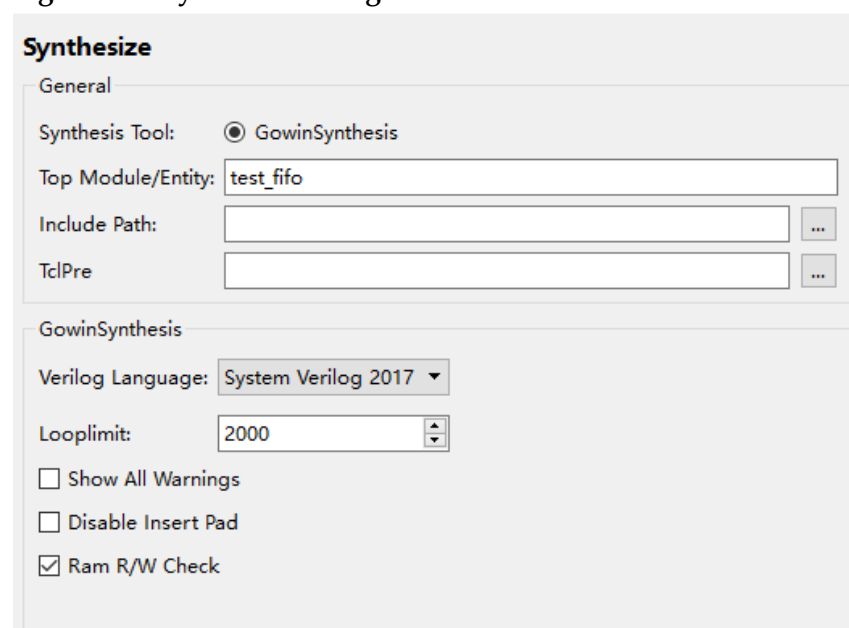
## 3.4 Use GowinSynthesis to Synthesize

### 3.4.1 Configuration

Select "Process > Synthesize (right-click) > Configuration" to open "Configuration" dialog box. For details, refer to [SUG550, GowinSynthesis User Guide](#).

The top module/entity is test\_fifo, as shown in Figure 3-12.

Figure 3-12 Synthesis Configuration



In addition, you can add some attributes and instructions to the source file to control synthesis. For the details, see [SUG550, GowinSynthesis User Guide](#). As shown in Figure 3-13, in this design, a specific net is retained without optimization during the synthesis by using the `/* synthesis syn_keep=1 */` attribute.

Figure 3-13 Attributes and Instructions of GowinSynthesis

```

67 reg [1:0] ALT_CNT_d;
68 reg [7:0] rand_num;
69 reg [9:0] rand_cnt;
70 reg [11:0] start_rdmck;
71 reg fifo_empty_d;
72 wire [WRSIZE-1:0] w_data_d/* synthesis syn_keep=1 */;
73 wire load;
74 wire [RDSIZE-1:0] r_data;
75 wire [WNSIZE:0] w_num;
76 wire [RNSIZE:0] r_num;
77 wire fifo_full;
78 wire fifo_empty;
79 wire fifo_alempy;
80 //test state machine

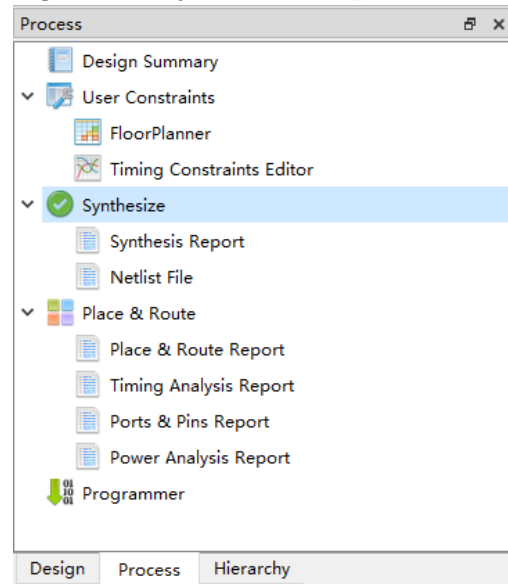
```

### 3.4.2 Synthesize

After synthesis configuration, you can start to synthesize.

Double-click "Synthesize" in Process window to synthesize, as shown in Figure 3-14. When the icon changes to "✔", you can double-click Synthesis Report to view the report and double-click Netlist File to view the netlist file.

Figure 3-14 Synthesis Completed



After synthesis, the gwsynthesis folder is generated under the \impl path. The folder contains all the files and folders generated in synthesis, as shown in Figure 3-15.

Figure 3-15 gwsynthesis Directory

Name	Date modified	Type	Size
RTL_GAO	5/31/2022 15:54	File folder	
FIFO_HS.log	5/31/2022 15:51	LOG File	6 KB
FIFO_HS.prj	5/31/2022 15:50	PRJ File	2 KB
FIFO_HS.vg	5/31/2022 15:51	VG File	454 KB
FIFO_HS_syn.rpt.html	5/31/2022 15:51	360 se HTML Doc...	29 KB
FIFO_HS_syn_resource.html	5/31/2022 15:51	360 se HTML Doc...	3 KB
FIFO_HS_syn_rsc.xml	5/31/2022 15:51	XML Document	1 KB

If the project contains the GAO config file, after PnR, RTL\_GAO folder is generated under the project creation path \impl\gwsynthesis, as shown in Figure 3-15, and this folder contains all the files generated by the RTL GAO synthesis as shown in Figure 3-16.

- ao\_0 contains the parameter files of the AO core.
- ao\_control contains the parameter files of the control AO core.
- gao.v is the netlist file GAO post-synthesis, encrypted.
- gw\_gao\_top.v is the top file of GAO, connecting ao, ao\_control and jtag modules.
- The other files are generated during GAO synthesis.

Figure 3-16 GAO Directory

Name	Date modified	Type	Size
ao_0	5/31/2022 15:54	File folder	
ao_control	5/31/2022 15:54	File folder	
gw_gao_top.v	5/31/2022 15:54	V File	6 KB

## 3.5 View Schematic Diagram of the Netlist after Synthesis

After completing the synthesis, you can view the schematic diagram of the entire design through the menu bar "Tools > Schematic Viewer > Post-Synthesis Netlist Viewer" to help you better understand the logic of the design after synthesis. For more details, see [SUG755-1.2.1E Gowin HDL Schematic Viewer User Guide](#).

## 3.6 Physical Constraints

After synthesis, you can use FloorPlanner or write manually to add physical constraints. In this design, FloorPlanner is selected. For more details, please refer to the [SUG935, Gowin Design Physical Constraints User Guide](#) and [SUG1018, Arora V Design Physical Constraints User Guide](#).

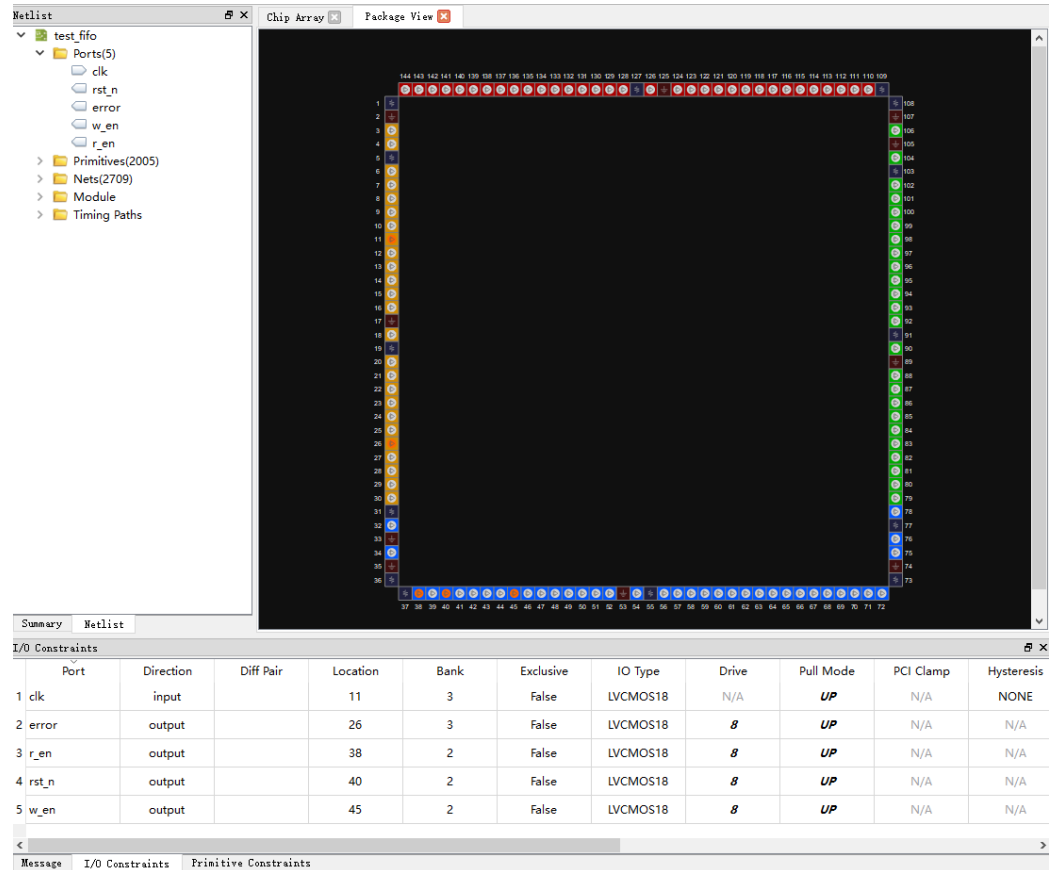
### 3.6.1 Create New Physical Constraints

Click "Process > User Constraints > FloorPlanner" to open

FloorPlanner, which supports I/O, Primitive, and Group physical constraints. This design only adds I/O constraints and uses it as an instance.

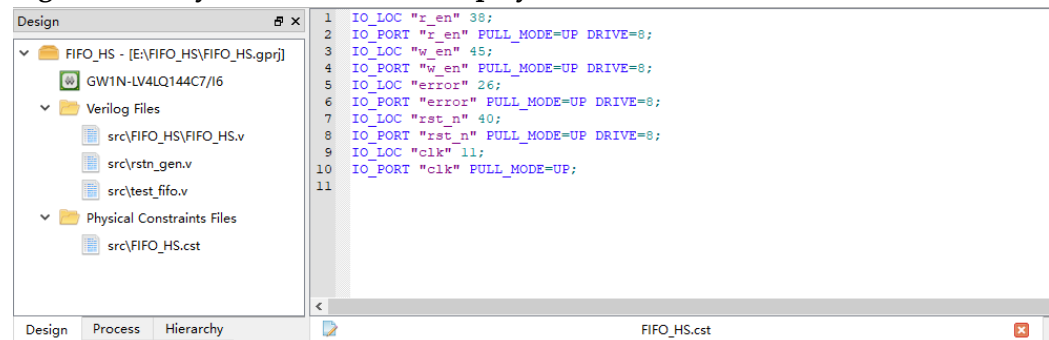
You can create I/O constraints in I/O Constraints window. Drag the port row to be constrained in the Netlist or I/O Constraints window to a specific location in the Package View or Chip Array view. After finished, the port location displays in the IOB, as shown in Figure 3-17.

**Figure 3-17 I/O Constraints**



After constraints finished, click "Save" to generate physical constraints files as shown in Figure 3-18.

**Figure 3-18 Physical Constraints Display**



In PnR, if there is no physical constraints file, the PnR will be automatically performed. If there is a physical constraint file, the PnR will

be performed according to the physical constraints file.

### 3.6.2 Modify Physical Constraints

After physical constraints files generated, you can modify the constraints by FloorPlanner. Click "Save" to finish.

## 3.7 Timing Constraint

After synthesis, you can use Timing Constraints Editor or write manually to add timing constraints. In this design, Timing Constraints Editor is selected. For more details, please refer to [SUG101, Gowin Design Timing Constraints Guide](#).

### 3.7.1 Create New Timing Constraints

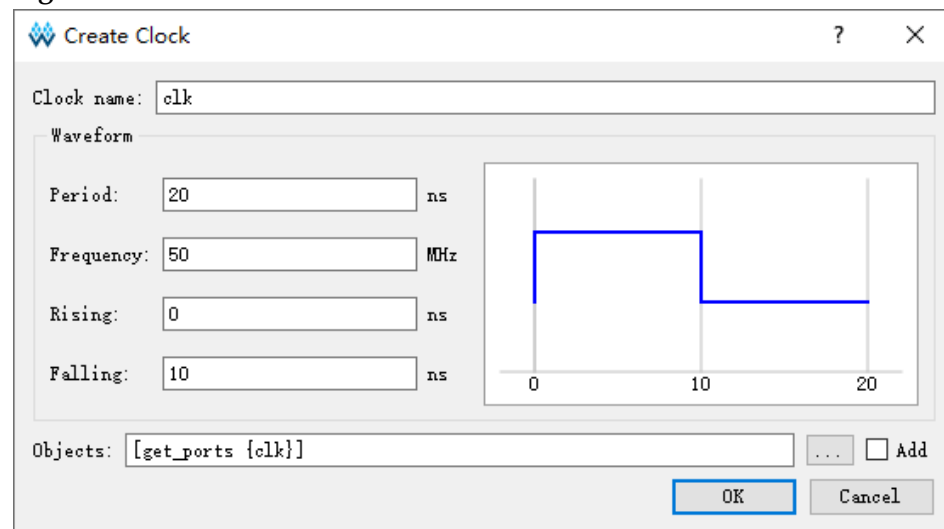
Click "Process > User Constraints > Timing Constrains Editor" to open Timing Constrains Editor, which supports clock, I/O and timing report constraints. This design adds clock and timing report constraints and uses them as instances.

#### Clock Constraints

Select "Clocks" under "Timing Constraints", right-click in the blank space on the right and select "Create Clock". This will open the "Create Clock" dialog, as shown in Figure 3-19. And create the following constraints:

- Clock name: clk
- Period: 20
- Frequency: 50
- Rising: 0
- Falling: 10
- Source Object: get\_ports {clk}

Figure 3-19 Clock Constraints



The design uses GAO, so the clock `tck_pad_i` is created in the same way as `clk`. The relationship between `clk` and `tck_pad_i` is an asynchronous clock. If you do not want to use Gowin Software to analyze this relationship, you can create a clock group constraint through the timing constraint editor.

### Timing Report Constraint

Select "Timing Constraints > Report > Report Timing", right-click in the blank space on the right and select "Create Report". In the popped-up "Report Timing" dialog, configure the parameters; the setup paths for `clk` to `clk` are reported, limiting the number of paths to 100, as shown in Figure 3-20.

**Figure 3-20 Timing Report Constraint**

**Report Timing**

**Clocks**

From clock:

To clock:

**Objects**

From:

Through:

To:

**Analysis Type**

☒ Setup ☐ Hold ☐ Recovery ☐ Removal

**Path**

Max Paths:  Min Logic Level:

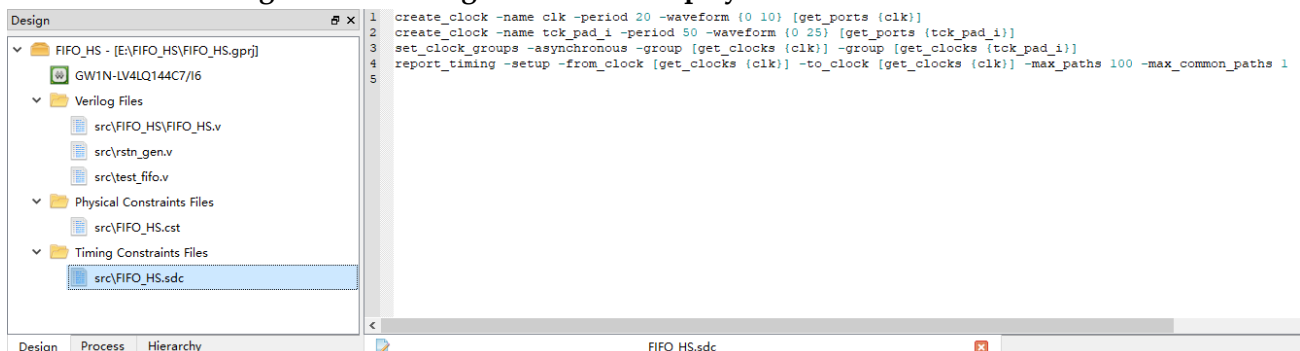
Max Common Paths:  Max Logic Level:

Module Instance:

OK Cancel

After constraints is finished, click "Save" to generate timing constraints, as shown in Figure 3-21.

**Figure 3-21 Timing Constraints Display**





In PnR, if there is no timing constraints file, the PnR will be automatically performed. If there is a timing constraint file, the PnR will be performed according to the timing constraints file.

### 3.7.2 Modify Timing Constraints

After timing constraints files are generated, you can modify the constraints by Timing Constraints Editor. Click "Save" to finish.

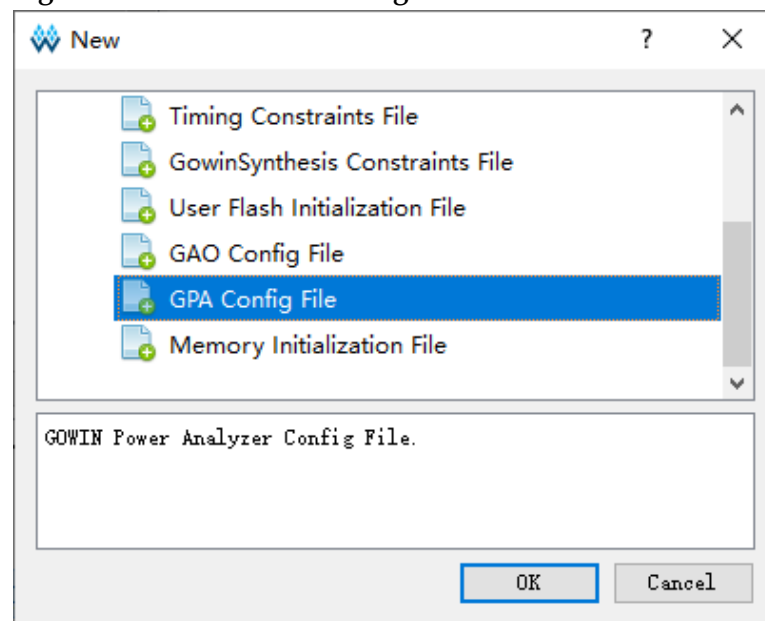
## 3.8 GPA Configuration

After synthesis, you can create a GPA config file to analyze power. For the usage, please refer to [SUG282, Gowin Power Analyzer User Guide](#).

### 3.8.1 Create GPA Config File

Select "Design > New File..." to open "New" dialog box, and select "GPA Config File" in "New", as shown in Figure 3-22. Click "OK". The file name is FIFO\_HS and the file is under src by default. Then click "OK" to finish.

Figure 3-22 Create GPA Config File



### 3.8.2 Configure GPA

After GPA config file is created, configure General Setting, Rate Setting and Clock Setting.

- General Setting includes the parameters of device, package, speed grade, temperature grade, thermal impedance, and voltage.
- Rate Setting is used to configure signal transition rate. You can set transition rate of IO or Net, or use the default value.
- Clock Setting is used to configure clock and enable features of BSRAM, I/O and DFF.

#### General Setting

In this design, the general setting is configured as follows: commercial temperature, 25°C ambient temperature, no heat sink, VCCX 3.3V and VCC 1.2V, as shown in Figure 3-23.

**Figure 3-23 General Setting Configuration**

The screenshot shows the 'General Setting' configuration window for the GPA tool. The window is divided into several sections:

- Operating Conditions:** Grade is set to 'COMMERCIAL' and Process is set to 'TYPICAL'.
- Environment:** Ambient Temperature is set to '25.000°C'. The 'Custom Theta JA' checkbox is checked, with a value of '25.000°C/W'.
- Heat Sink:** The 'None' radio button is selected. Other options include 'Low Profile', 'Medium Profile', 'High Profile', and 'Custom'. The 'Air-flow' is set to '0 (LFM)'. The 'Custom Theta SA' is set to '25.000°C/W'.
- Board Thermal Model:** The 'None' radio button is selected. Other options include 'Custom' and 'Typical'. The 'Board Temperature' is set to '25.000°C' with a range of '(-40°C-100°C)'. The 'Custom Theta JB' is set to '25.000°C/W'.
- Voltage:** VCC is set to '1.200V' and VCCX is set to '3.300V'.

The window title bar indicates the file name 'FIFO\_HS.gpa'.

### Rate Setting

In this design, the transition rate of clk is 50% and the remaining signals use the default value 12.5%, as shown in Figure 3-24.

**Figure 3-24 Rate Setting Configuration**

**General Setting** **Rate Setting** **Clock Setting**

**Net Rate**

☒ % ☐ transition/s + -

Name	Value
clk	50.00%

**VCD File**

Instance	File Name	File Type
----------	-----------	-----------

☐ Filter glitch on VCD file + -

**Default Rate Setting**

Default Rate used for IO input signals: 12.50 %

Default Rate used for remaining signals

Default Value: 12.50 %

FIFO\_HS.gpa

### Clock Setting

In this design, the clock is created in the timing analysis, and the rest are not set, as shown in Figure 3-25.

**Figure 3-25 Clock Setting Configuration**

**General Setting** **Rate Setting** **Clock Setting**

**Clock**

Global Enable: 100.00 + -

Clock Name	Clock Enable	Quad1	Quad2	Quad3	Quad4
clk	100				

**B-SRAM**

Clock Enable: 100.00 Read Probability: 100.00 Write Probability: 100.00 + -

Name	ClockA Enable	ReadA Probability	WriteA Probability	ClockB Enable	ReadB Probability	WriteB Probability
clk	100.00	100.00	100.00			

**IO**

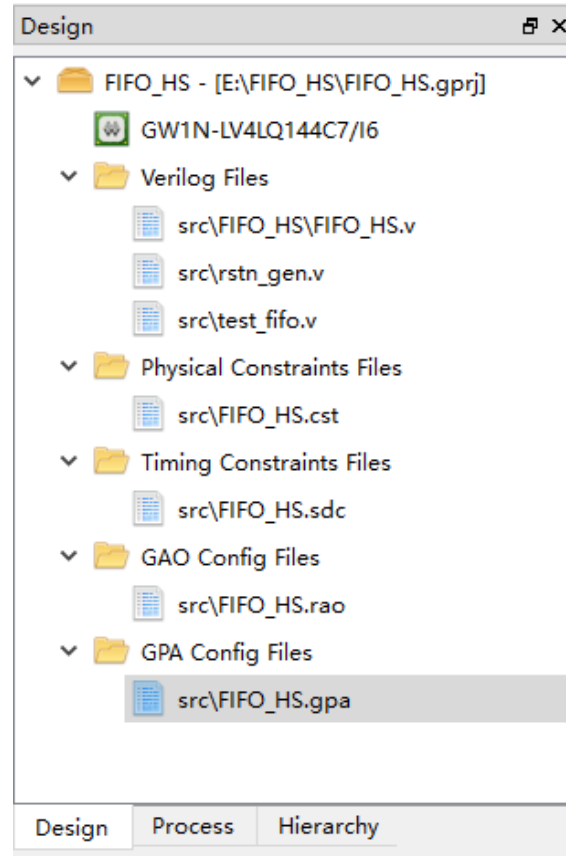
Name	Out Enable	Load Capacity
------	------------	---------------

**DFF**

Name	Value
------	-------

FIFO\_HS.gpa

After configuration, click "Save" to finish and the design window is as shown in Figure 3-26.

**Figure 3-26 GPA Config Files**

In PnR, if there is no GPA config file, the PnR will be automatically performed. If there is a GPA config file, the PnR will be performed according to the GPA config file.

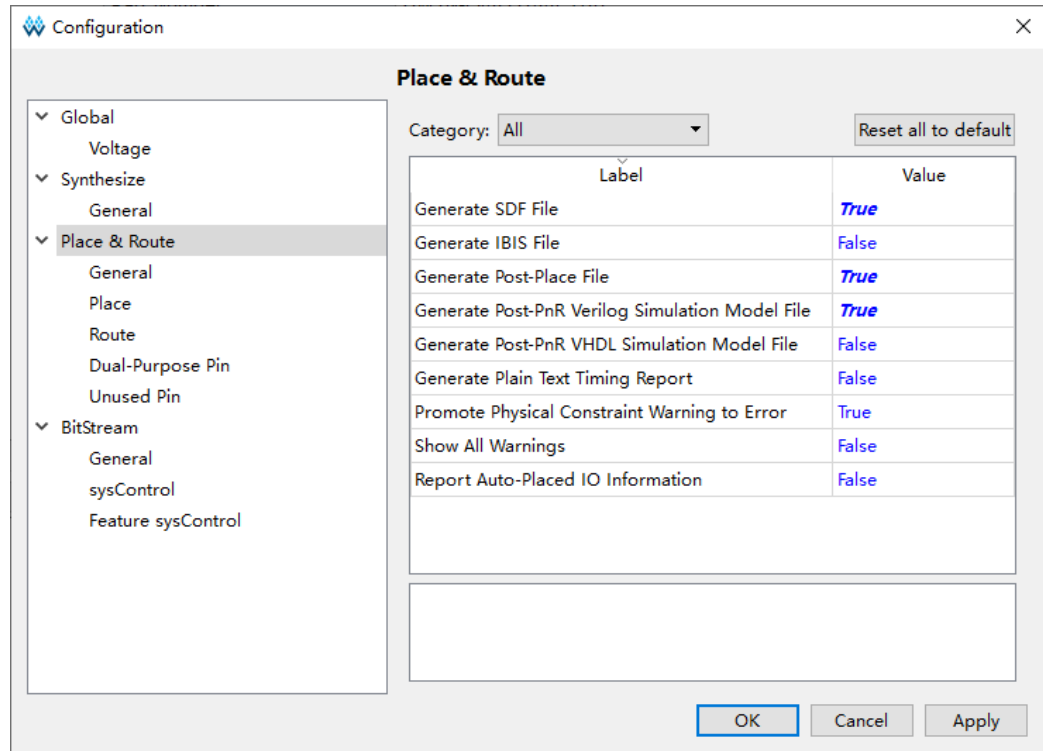
## 3.9 Place & Route

After synthesis and the creation of physical constraints files, timing constraints file, GPA config file as required, you can start PnR.

### 3.9.1 Configuration

Select "Process > Place & Route (right-click) > Configuration" to open "Configuration" dialog box to configure Place & Route and Bitstream. For the details, see [SUG100, Gowin Software User Guide](#).

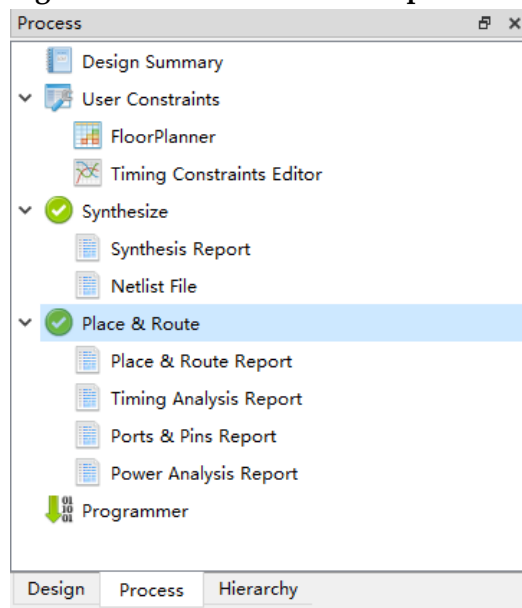
In this design, "Generate SDF File", "Generate Post-Place File" and "Generate Post-PNR Verilog Simulation Model File" in "General" option are configured to True. "Place output register to IOB" in "Place" option is configured to False, and the rest options use default values, as shown in Figure 3-27.

**Figure 3-27 Place & Route Configuration**

### 3.9.2 Run PnR

After configuration, you can run PnR.

















Double-click Place & Route in Process window to start PnR based on physical constraints and GAO configuration, start timing analysis based on timing constraints, and start power analysis based on power analysis configuration. After PnR, the icon before the Place & Route changes to "✔", as shown in Figure 3-28.

**Figure 3-28 Place & Route Completed**

After finishing PnR, the pnr folder is generated under the project

creation path \impl, as shown in Figure 3-29. The folder contains all the files generated in PnR, including the bitstream file, the netlist file after PnR, and the output reports. For the details, refer to [3.12 Output Files](#).

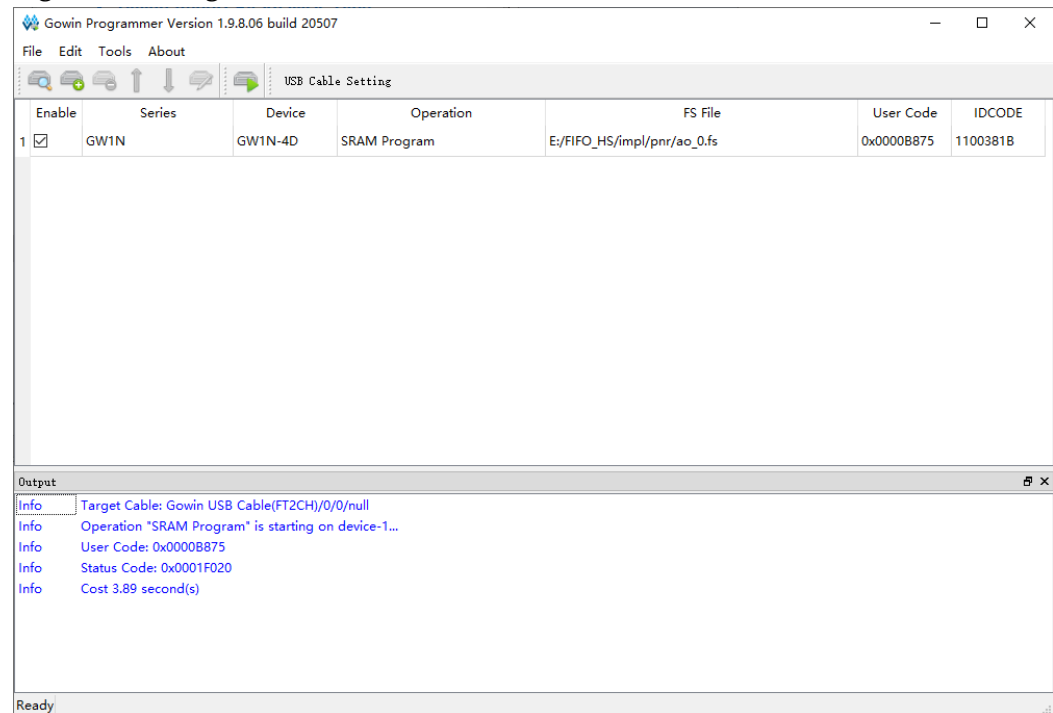
**Figure 3-29 PnR Directory**

Name	Date modified	Type	Size
 ao_0.fs	5/31/2022 15:51	FS File	1,732 KB
 cmd.do	5/31/2022 15:51	DO File	1 KB
 device.cfg	5/31/2022 15:51	CFG File	1 KB
 FIFO_HS.db	5/31/2022 15:51	Data Base File	43 KB
 FIFO_HS.log	5/31/2022 15:51	LOG File	2 KB
 FIFO_HS.pin.html	5/31/2022 15:51	360 se HTML Doc...	35 KB
 FIFO_HS.posp	5/31/2022 15:51	POSP File	1 KB
 FIFO_HS.power.html	5/31/2022 15:51	360 se HTML Doc...	8 KB
 FIFO_HS.rpt.html	5/31/2022 15:51	360 se HTML Doc...	40 KB
 FIFO_HS.rpt.txt	5/31/2022 15:51	TXT File	29 KB
 FIFO_HS.sdf	5/31/2022 15:51	SDF File	2,321 KB
 FIFO_HS.timing_paths	5/31/2022 15:51	TIMING_PATHS File	32 KB
 FIFO_HS.tr.html	5/31/2022 15:51	360 se HTML Doc...	1 KB
 FIFO_HS.vo	5/31/2022 15:51	VO File	561 KB
 FIFO_HS_tr_cata.html	5/31/2022 15:51	360 se HTML Doc...	8 KB
 FIFO_HS_tr_content.html	5/31/2022 15:51	360 se HTML Doc...	844 KB

## 3.10 Download Bitstream

Run Place & route to generate the bitstream file and download it with Programmer to verify the design. For the usage, please see [SUG502. Gowin Programmer User Guide](#).

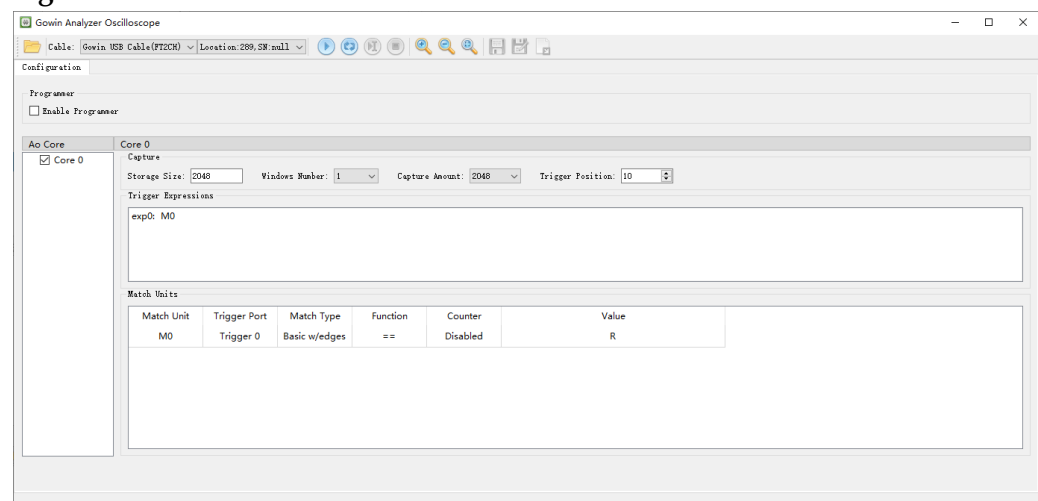
Select "Process > Program Device (double-click)" to open Programmer, and the programmer automatically identifies the bitstream file. After the development board is ready, click "Program/Configure" to download the bitstream to the development board. Figure 3-30 shows the completion of the bitstream download.

**Figure 3-30 Programmer**

## 3.11 GAO Captures Data

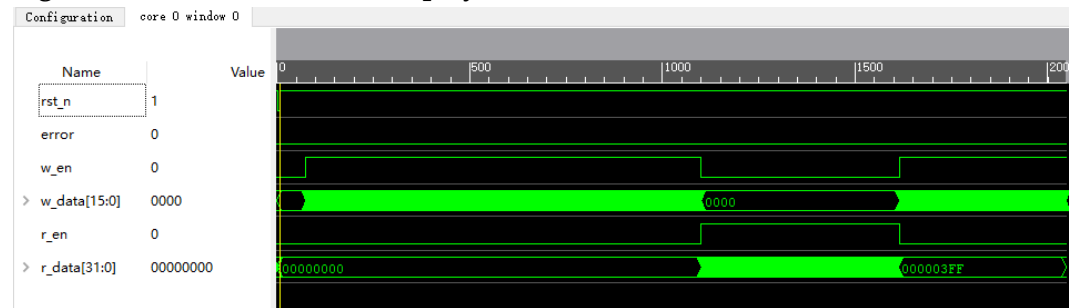
After the bitstream is downloaded, you can use GAO to verify the design. For the usage, refer to the [SUG114, Gowin Analyzer Oscilloscope User Guide](#).

Click the GAO icon in the Gowin Software toolbar to open the GAO interface, which automatically identifies the GAO config file, as shown in Figure 3-31.

**Figure 3-31 GAO Interface**

Click the Start icon in the GAO interface to capture data. After finishing capturing data, GAO interface generates a window to display the waveform, as shown in Figure 3-32. The window supports cursor, zoom-out and so on so as to facilitate you to analyze the data.

Figure 3-32 GAO Waveform Display



## 3.12 Output Files

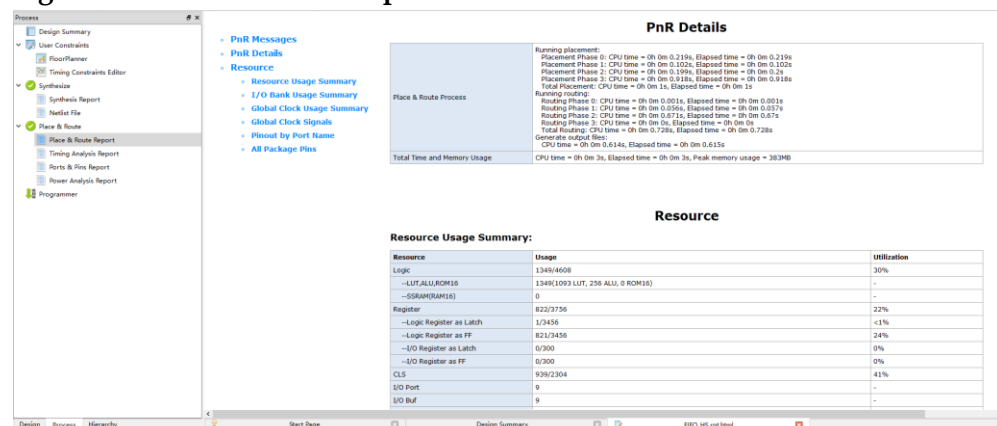
### 3.12.1 Place & Route Report

The Place & Route Report describes the resource, memory consumption, time consumption, etc. occupied by the user design, with the file extension name .rpt.html. Check the \*.rpt.html file for further details.

Double-click "Place & Route Report" in the Process window to open Place & Route report, as shown in Figure 3-33.

For the details, refer to 6.2 Place & Route Report of [SUG100 Gowin Software User Guide](#).

Figure 3-33 Place &amp; Route Report



### 3.12.2 Ports and Pins Report

The Ports and Pins Report is the ports and pins files after placement. It includes port types, attributes, and locations, etc. The generated file is saved with extension name .pin.html. Check the .pin.html file for further details.

Double-click Ports & Pins Report in the Process window to open Ports & Pins Report, as shown in Figure 3-34.

For the details, refer to 6.3 Ports & Pins Report of [SUG100, Gowin Software User Guide](#).



Figure 3-34 Ports &amp; Pins Report

**Pin Details**

Pinout by Port Name:

Port Name	Dir	Loc/Bank	Constraint	Dir	Site	IO Type	Drive	Pull Mode	PCI Clamp	Hysteresis	Open Drain	Vref	Single Resistor	Diff Resistor	Bank Vccio
clk		25/3	N	in	IOL11(A)	LVCN0518	NA	UP	ON	NONE	NA	NA	OFF	NA	
trst_pad_j		13/3	N	in	IOL10(A)	LVCN0518	NA	UP	ON	NONE	NA	NA	OFF	NA	
trst_pad_j		14/3	N	in	IOL10(B)	LVCN0518	NA	UP	ON	NONE	NA	NA	OFF	NA	
tdo_pad_j		16/3	N	in	IOL10(C)	LVCN0518	NA	UP	ON	NONE	NA	NA	OFF	NA	
rst_n		30/3	N	out	IOL15(B)	LVCN0518	8	UP	NA	NA	OFF	NA	OFF	NA	
error		116/0	N	out	IOT30(B)	LVCN0518	8	UP	NA	NA	OFF	NA	NA	NA	
w_en		57/2	N	out	IOL15(B)	LVCN0518	8	UP	NA	NA	OFF	NA	NA	NA	
r_en		138/0	N	out	IOT7(A)	LVCN0518	8	UP	NA	NA	OFF	NA	NA	NA	
tdo_pad_o		18/3	N	out	IOL10(E)	LVCN0518	8	UP	NA	NA	OFF	NA	OFF	NA	

**All Package Pins:**

Loc/Bank	Signal	Dir	Site	IO Type	Drive	Pull Mode	PCI Clamp	Hysteresis	Open Drain	Vref	Single Resistor	Diff Resistor	Bank Vccio
144/0	-	in	IOT2(B)	LVCN0518	NA	UP	ON	NONE	NA	NA	NA	NA	1.8
143/0	-	in	IOT2(B)	LVCN0518	NA	UP	ON	NONE	NA	NA	NA	NA	1.8
142/0	-	in	IOT4(A)	LVCN0518	NA	UP	ON	NONE	NA	NA	NA	NA	1.8
141/0	-	in	IOT4(B)	LVCN0518	NA	UP	ON	NONE	NA	NA	NA	NA	1.8
140/0	-	in	IOT9(A)	LVCN0518	NA	UP	ON	NONE	NA	NA	NA	NA	1.8
139/0	-	in	IOT9(B)	LVCN0518	NA	UP	ON	NONE	NA	NA	NA	NA	1.8
138/0	-	in	IOT7(A)	LVCN0518	8	UP	NA	NA	OFF	NA	NA	NA	1.8
137/0	-	in	IOT7(B)	LVCN0518	NA	UP	ON	NONE	NA	NA	NA	NA	1.8
136/0	-	in	IOT9(A)	LVCN0518	NA	UP	ON	NONE	NA	NA	NA	NA	1.8
135/0	-	in	IOT9(B)	LVCN0518	NA	UP	ON	NONE	NA	NA	NA	NA	1.8
134/0	-	in	IOT12(A)	LVCN0518	NA	UP	ON	NONE	NA	NA	NA	NA	1.8

### 3.12.3 Timing Report

The timing report includes setup check, hold check, recovery time check, removal time check, min. clock pulse check, max. fan out path, Place & Route congestion report, etc. by default. The timing report also includes the max. frequency report.

Double-click Timing Analysis Report in the Process window to open the timing analysis report for the project, as shown in Figure 3-35.

For the details, please refer to [SUG940, Gowin Design Timing Constraints User Guide](#).

Figure 3-35 Timing Report

**Timing Summaries**

**STA Tool Run Summary:**

Setup Delay Model	Slew 1.14V BSC C7/B6
Hold Delay Model	Fast 1.28V OC C7/B6
Numbers of Paths Analyzed	2275
Numbers of Endpoints Analyzed	2390
Numbers of Failing Endpoints	0
Numbers of Setup Violated Endpoints	0
Numbers of Hold Violated Endpoints	0

**Clock Summary:**

Clock Name	Type	Period	Frequency(MHz)	Rise	Fall	Source	Master	Objects
clk	Base	20.000	50.000	0.000	10.000			clk
trst_pad_j	Base	50.000	20.000	0.000	25.000			trst_pad_j
u_ifb_hn_top/ffs_int/wfull_val	Base	20.000	50.000	0.000	10.000			u_ifb_hn_top/ffs_int/wfull_val_v12F

**Max Frequency Summary:**

NO.	Clock Name	Constraint	Actual Fmax	Logic Level	Entity
1	clk	50.000(MHz)	79.105(MHz)	16	TOP
2	trst_pad_j	20.000(MHz)	99.675(MHz)	7	TOP

No timing paths to get frequency of u\_ifb\_hn\_top/ffs\_int/wfull\_val

**Total Negative Slack Summary:**

Clock Name	Analysis Type	Endpoints TNS	Number of Endpoints
clk	Setup	0.000	0
clk	Hold	0.000	0
trst_pad_j	Setup	0.000	0

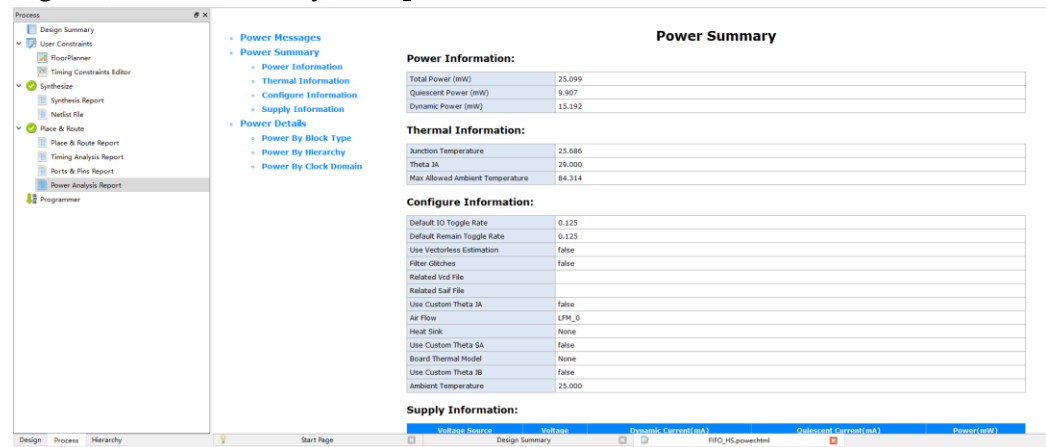
### 3.12.4 Power Analysis Report

The Power Analysis Report helps you evaluate the basic power consumption of your design.

Double-click Power Analysis Report in the Process window to open the power analysis report as shown in Figure 3-36.

For the details, please refer to chapter 4 Power Analysis Report of [SUG282, Gowin Power Analysis User Guide](#).

Figure 3-36 Power Analysis Report

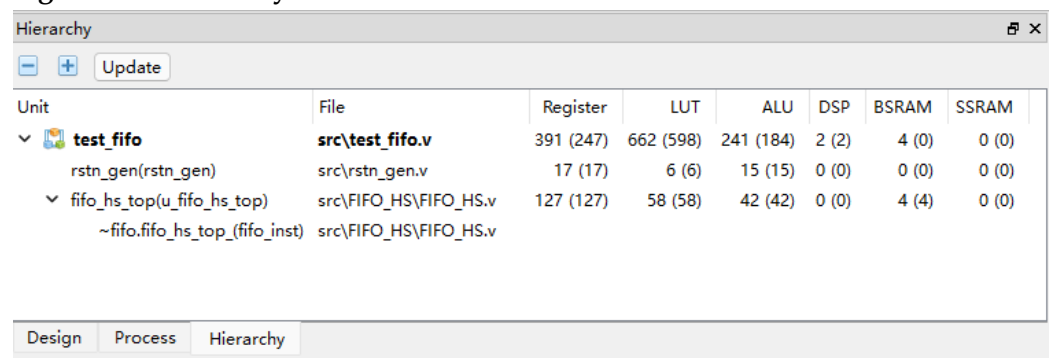


## 3.13 File Encryption

### 3.13.1 Source File Encryption

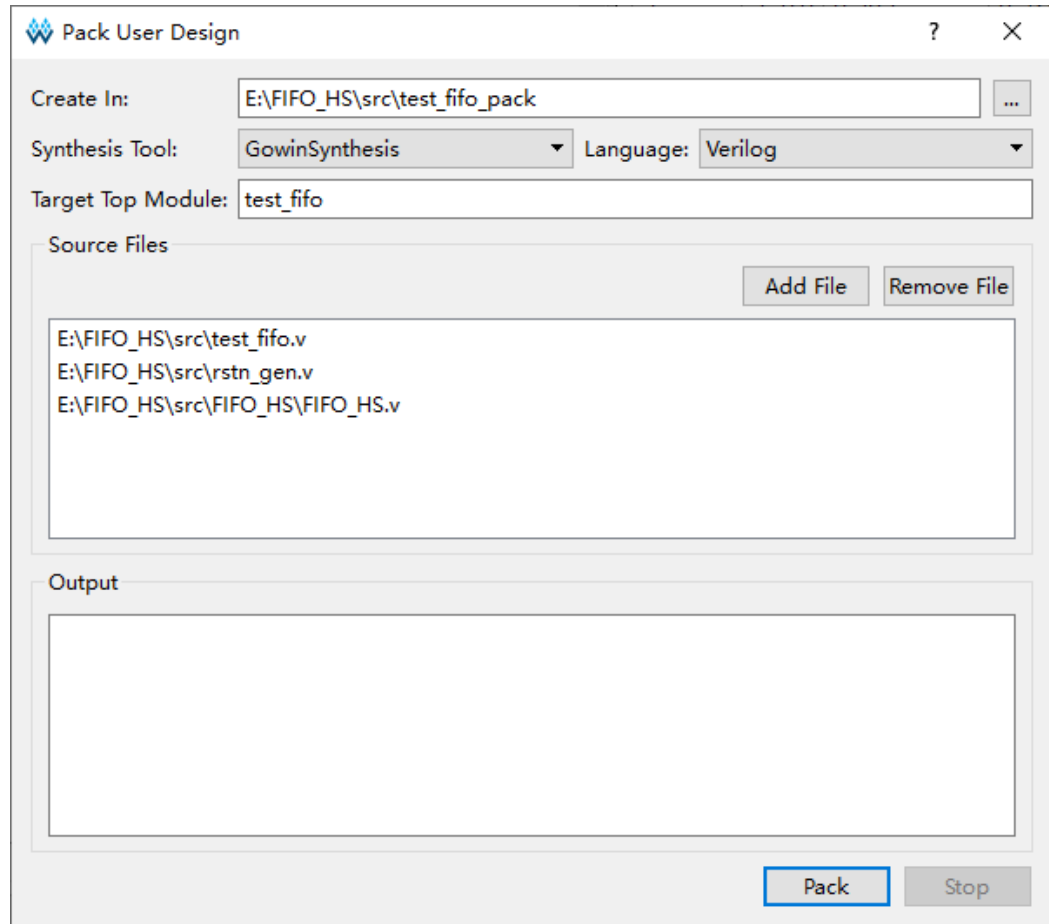
When you need to encrypt and protect source files, you can encrypt the selected module and its sub modules in Hierarchy window, as shown in Figure 3-37. For details, see [SUG100, Gowin Software User Guide](#).

Figure 3-37 Hierarchy Window



Take module test\_fifo as an example to introduce the file encryption.

You can right-click test\_fifo in the Hierarchy window and select "Pack User Design" in the right-click list to open the dialog box, as shown in Figure 3-38.

**Figure 3-38 Pack User Design Dialog Box**

Select test\_fifo as the top module. Click "Pack" to start encryption. The relevant information will be printed in the Output window.

After the encryption, two files are generated under the destination path (E:\FIFO\_HS\src\test\_fifo\_pack): test\_fifo\_gowin.vp and test\_fifo\_sim.v.

- test\_fifo\_gowin.vp: Encrypted files that can be used by others.
- test\_fifo\_sim.v: Flattened synthesized plaintext netlist file that can be used for simulation.

### 3.13.2 Simulation File Encryption

The simulation file provided by Gowin is plaintext. In order to protect the simulation file, it can be encrypted by using a third-party simulation software, such as Modelsim and VCS, and the license of the tool needs to be obtained. Here it uses test\_fifo\_sim.v as an example to introduce the encryption.

#### Encryption by Modelsim

When using Modelsim, the steps to encrypt the simulation file are as follows:

1. Add macro `protect and `endprotect before and after the encrypted in the simulation file test\_fifo\_sim.v.

2. Run command: `vlog +protect test_fifo_sim.v`.
3. After running the command, `test_fifo_sim.vp` is generated in the work library, which is the encrypted file of `test_fifo_sim.v` that can be used for Modelsim simulation.

### **Encryption by VCS**

When using VCS, the steps to encrypt the simulation file are as follows:

1. Add macro ``protect128` and ``endprotect128` before and after the encrypted in the simulation file `test_fifo_sim.v`.
2. Run command: `vcs +v2k -protect128 test_fifo_sim.v`.
3. After running the command, `test_fifo_sim.vp` is generated under the current path, which is the encrypted file of `test_fifo_sim.v` that can be used for VCS simulation.

# 4 Tcl

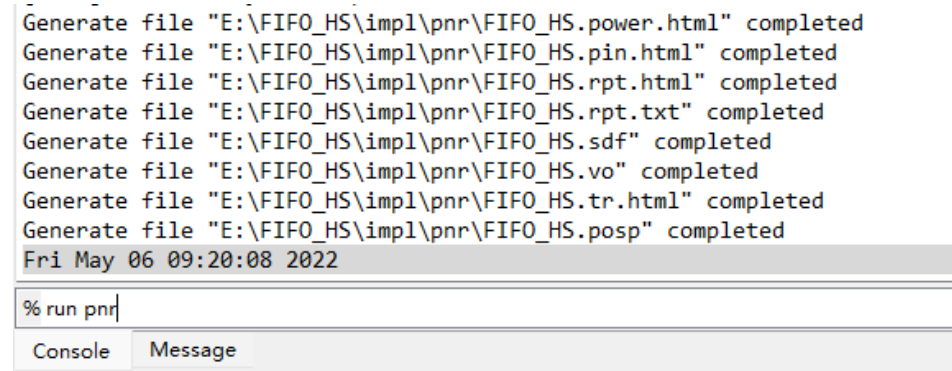
The previous chapters introduce the way to implement the entire design process by using GUI. Gowin Software also provides tcl commands for some settings. Take FIFO HS design in Windows as an example to introduce the usage of tcl commands. For the details, see Chapter 8 Tcl Commands of [SUG100, Gowin Software User Guide](#).

## 4.1 Tcl Execution

### 4.1.1 Tcl Editing Window

At the bottom of the Console page is the tcl editing window, where you can enter the tcl commands and press Enter to run, as shown in Figure 4-1.

**Figure 4-1 Tcl Editing Window**



```

Generate file "E:\FIFO_HS\impl\pnr\FIFO_HS.power.html" completed
Generate file "E:\FIFO_HS\impl\pnr\FIFO_HS.pin.html" completed
Generate file "E:\FIFO_HS\impl\pnr\FIFO_HS.rpt.html" completed
Generate file "E:\FIFO_HS\impl\pnr\FIFO_HS.rpt.txt" completed
Generate file "E:\FIFO_HS\impl\pnr\FIFO_HS.sdf" completed
Generate file "E:\FIFO_HS\impl\pnr\FIFO_HS.vo" completed
Generate file "E:\FIFO_HS\impl\pnr\FIFO_HS.tr.html" completed
Generate file "E:\FIFO_HS\impl\pnr\FIFO_HS.posp" completed
Fri May 06 09:20:08 2022
% run pnr|
  
```

Console Message

### 4.1.2 Tcl Command Line

Start command: `\x.x\IDE\bin\gw_sh.exe [script file]` under the installation directory

The First Way: enter `gw_sh.exe` to start. This mode executes in the same way as the Tcl editing window, executing tcl commands one by one, as shown in Figure 4-2.

**Figure 4-2 Tcl Command Line**

```
*** GOWIN Tcl Command Line Console ***
% add_file -type verilog "E:/FIFO_HS/src/test_fifo.v"
add new file: "E:/FIFO_HS/src/test_fifo.v"
% add_file -type verilog "E:/FIFO_HS/src/FIFO_HS/FIFO_HS.v"
add new file: "E:/FIFO_HS/src/FIFO_HS/FIFO_HS.v"
%
```

The Second Way: use gw\_sh.exe [script file] to execute the script file. Tcl script file can contain all the supported tcl commands, such as, device, design file, option, and run information, and tcl script file is shown in Figure 4-3. Tcl script file can be generated by handwriting or saveto command, but saveto command The tcl script file can be generated by hand or by saveto command, but the saveto command does not include the run command when generating the tcl script, so you can add the run command if needed.

**Figure 4-3 Tcl Script File**

```
1 add_file -type verilog "E:/FIFO_HS/src/FIFO_HS/FIFO_HS.v"
2 add_file -type verilog "E:/FIFO_HS/src/rstn_gen.v"
3 add_file -type verilog "E:/FIFO_HS/src/test_fifo.v"
4 add_file -type cst "E:/FIFO_HS/src/FIFO_HS.cst"
5 add_file -type sdc "E:/FIFO_HS/src/FIFO_HS.sdc"
6 add_file -type gao "E:/FIFO_HS/src/FIFO_HS.rao"
7 add_file -type gpa "E:/FIFO_HS/src/FIFO_HS.gpa"
8 set_device GW1N-LV4LQ144C7/I6 -device_version D
9 set_option -synthesis_tool gowinsynthesis
10 set_option -output_base_name FIFO_HS
11 set_option -top_module test_fifo
12 set_option -verilog_std sysv2017
13 set_option -gen_sdf 1
14 set_option -gen_posp 1
15 set_option -gen_verilog_sim_netlist 1
16 set_option -oreg_in_iob 0
17 set_option -bit_format txt
18 run all
```

## 4.2 Tcl Quick Start

As tcl command line executes in the same way as the Tcl editing window, the following uses tcl editing window as an example to introduce how to use it.

### 4.2.1 create\_project

create\_project is used to create a new project. -name is used to specify the name of the project to be created; -dir is used to specify the path where the project will be located; -pn is used to specify the Part Number, and -device\_version is used to specify the version of the device corresponding to the Part Number. The tcl command is implemented as follows:

```
create_project -name FIFO_HS_newPrj -dir D:/tcl_prj -pn
GW1N-LV4LQ144C7/I6 -device_version D
```

After executing this command, the project named FIFO\_HS\_newPrj with the device information GW1N-LV4LQ144C7/I6 will be created under the specified path and the project interface will pop up.

## 4.2.2 import\_files

`import_files` is used to copy files or directories to the current project path/src. `-file` is used to add one or more files to the project path/src. `-fileList` is used to specify a list file to be added to the project path under /src, and each line in the file represents a project file to be added. The tcl command is implemented as follows:

`import_files -fileList fileList.txt`; the contents of the `fileList.txt` file are:

```
E:/FIFO_HS/src/FIFO_HS.cst
E:/FIFO_HS/src/FIFO_HS.gpa
E:/FIFO_HS/src/FIFO_HS.rao
E:/FIFO_HS/src/FIFO_HS.sdc
E:/FIFO_HS/src/rstn_gen.v
E:/FIFO_HS/src/test_fifo.v
E:/FIFO_HS/src/FIFO_HS/FIFO_HS.v
```

After executing this command, it will copy the files in the `fileList` list to the current project path /src and add all the files under the path to the project.

## 4.2.3 rm\_file

`rm_file` is used to remove files. For example, use this tcl command to remove `rstn_gen.v` and `test_fifo.v` from the project. Use the tcl command to achieve the following:

Remove `rstn_gen.v` and `test_fifo.v`

```
rm_file src/rstn_gen.v src/test_fifo.v
```

After running the command, the Console will display the prompt for removing files, and these two files will be removed from the Design window.

## 4.2.4 add\_file

`add_file` is used to add files. Here it will use tcl to add the removed files `rstn_gen.v` and `test_fifo.v` to the project. Use the tcl command to achieve the following:

Add `rstn_gen.v` and `test_fifo.v`

```
add_file src/rstn_gen.v src/test_fifo.v
```

After running the command, the Console will display the prompt for adding files, and these two files will appear in the Design window.

## 4.2.5 set\_file\_enable

`set_file_enable` is used to set whether a file can be used. Here it will use tcl to set `test_fifo.v` disable/enable.

Modify `test_fifo.v` to disable

```
set_file_enable src/test_fifo.v false
```

After running the command, the Console will display the prompt for disabling the file and test\_fifo.v file is grayed out in Design window.

Modify test\_fifo.v to enable

```
set_file_enable src/test_fifo.v true
```

After running the command, the Console will display the prompt for enabling the file and test\_fifo.v file is available in Design window.

## 4.2.6 set\_option

set\_option is used to set options in the project. Here it will use tcl to configure synthesis and PnR.

- Select GowinSynthesis  
set\_option -synthesis\_tool gowinsynthesis
- Set TOP Module/Entity to test\_fifo  
set\_option -top\_module test\_fifo
- Set Generate SDF File to True  
set\_option -gen\_sdf 1
- Set Generate Post-Place File to True  
set\_option -gen\_posp 1
- Set Generate Post-PNR Verilog Simulation Model File to True  
set\_option -gen\_verilog\_sim\_netlist 1
- Set Place output register to IOB to False  
set\_option -oreg\_in\_job 0

## 4.2.7 run

Run is used to run a flow or all flows. Here it will use tcl to run synthesis and PnR flows.

- Run synthesis  
Run syn
- Run PnR  
Run pnr

## 4.2.8 set\_device

Set\_device is used to set the target device. Here it will use tcl to set GW1N-9 (C version), GW1N-LV9PG256C6/I5 as the target device.

Set GW1N-9 (C version), GW1N-LV9PG256C6/I5 as the target device.

```
Set_device GW1N-LV9PG256C6/I5 -device_version C
```

After running the command, the Console will display the device information.



## 4.2.9 saveto

saveto is used to save the current data to the tcl script, including device, design file, and options, but no run information. Save the data as fifo\_hs.tcl, and you can run with command line gw\_sh.exe fifo\_hs.tcl, as shown below.

Save the current data to fifo\_hs.tcl

```
saveto fifo_hs.tcl
```

After running the command, the fifo\_hs.tcl file is generated on the path where the project files are located.

## 4.2.10 run close

run close is used to close the current project. The tcl command is implemented as follows:

```
run close
```

After executing this command, the current project will be closed.

