ZHEJIANG UNIVERSITY COLLEGE OF INFORMATION SCIENCE AND ELECTRONICS ENGINEERING

HOMEWORK #8

Computer Organization and Design

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Major: Electronic Science and Technology

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Problem 1.

a Why is the cost of a page fault in virtual memory considered very high?
b What are the typical advantages of having larger page size?
c Write one advantage and one disadvantage of a virtually tagged cache?
d Which type of parallel computing architecture is no longer commonly encountered in machines today (MIMD, MISD, SIMD, SISD)?

Answer :

a The cost of a page fault in virtual memory is considered very high because it involves accessing the disk, which is significantly slower than accessing the main memory. This can lead to substantial delays in program execution.
b The typical advantages of having larger page size include reduced page table size and lower page fault rate, as more data can be transferred in a single page.
c One advantage of a virtually tagged cache is that it can reduce the cache access time since the virtual address is used directly. One disadvantage is that it can lead to issues with synonym problems, where different virtual addresses map to the same physical address.
d MISD (Multiple Instruction, Single Data) is the type of parallel computing architecture that is no longer commonly encountered in machines today.

Problem 2.

An important advantage of interrupts over polling is the ability of the processor to perform other tasks while waiting for communication from an I/O device. Suppose that a 2GHz processor needs to read 1000 bytes of data from a particular I/O device.

The I/O device supplies 1 bytes of data every 0.01ms. The code to process the 1000 bytes data and store it in a buffer takes 2000 cycles.

1. a.If the processor detects that a byte of data is ready through polling, and a polling iteration takes 40 cycles, how many cycles does the entire operation take?
2. b.If instead, the processor is interrupted when a byte is ready, and the processor spends the time between interrupts on another task, how many cycles of this other task can the processor complete while the I/O communication is taking place? The overhead for handling an interrupt is 100 cycles.

Answer : a. If the processor detects that a byte of data is ready through polling, and a polling iteration takes 40 cycles, the entire operation in polling takes $1000 \times 40 = 40000$ cycles. and process the 1000 bytes data and store it in a buffer takes 2000 cycles. So the total time in polling and processing is $40000 + 2000 = 42000$ cycles.

considering the the I/O device supplies 1 bytes of data every 0.01ms, the processor needs to poll during $1000 \times 0.01 = 10$ ms. So the total time in polling is 0.01s * 2GHz = 20,000,000 cycles. and the total time in processing is 2000 cycles. So the total time in polling and processing is $20,000,000 + 2000 = 20,002,000$ cycles.

b. the I/O device supplies 1 bytes of data every 0.01ms, the cycles needed to supply 1 byte of data is $0.01 \times 10^{-}3 \times 2 \times 10^{9} = 20000$ cycles. the interrupt overhead is 100 cycles, so 20000-100 = 19900 cycles can be used to process other tasks. the total time cycles of this other task can the processor complete while the I/O communication is taking place is $1000 \times 19900 = 19900000$ cycles.