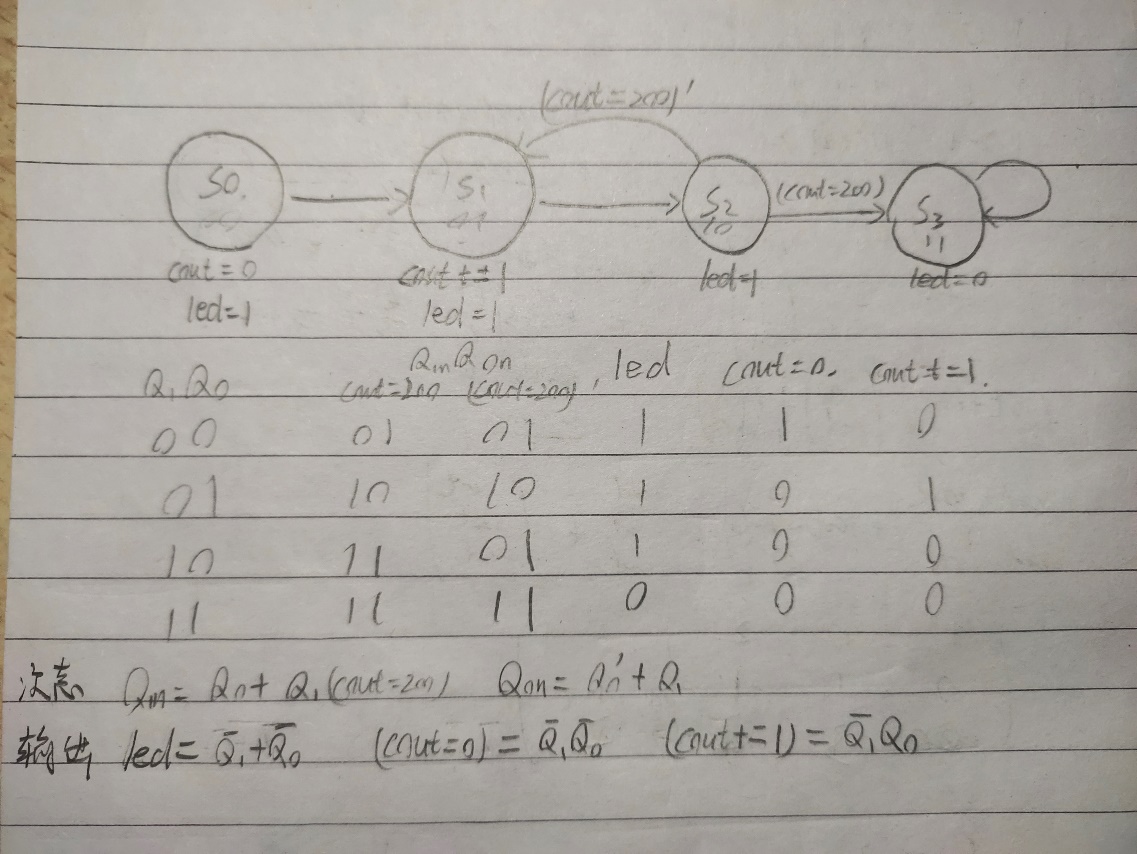
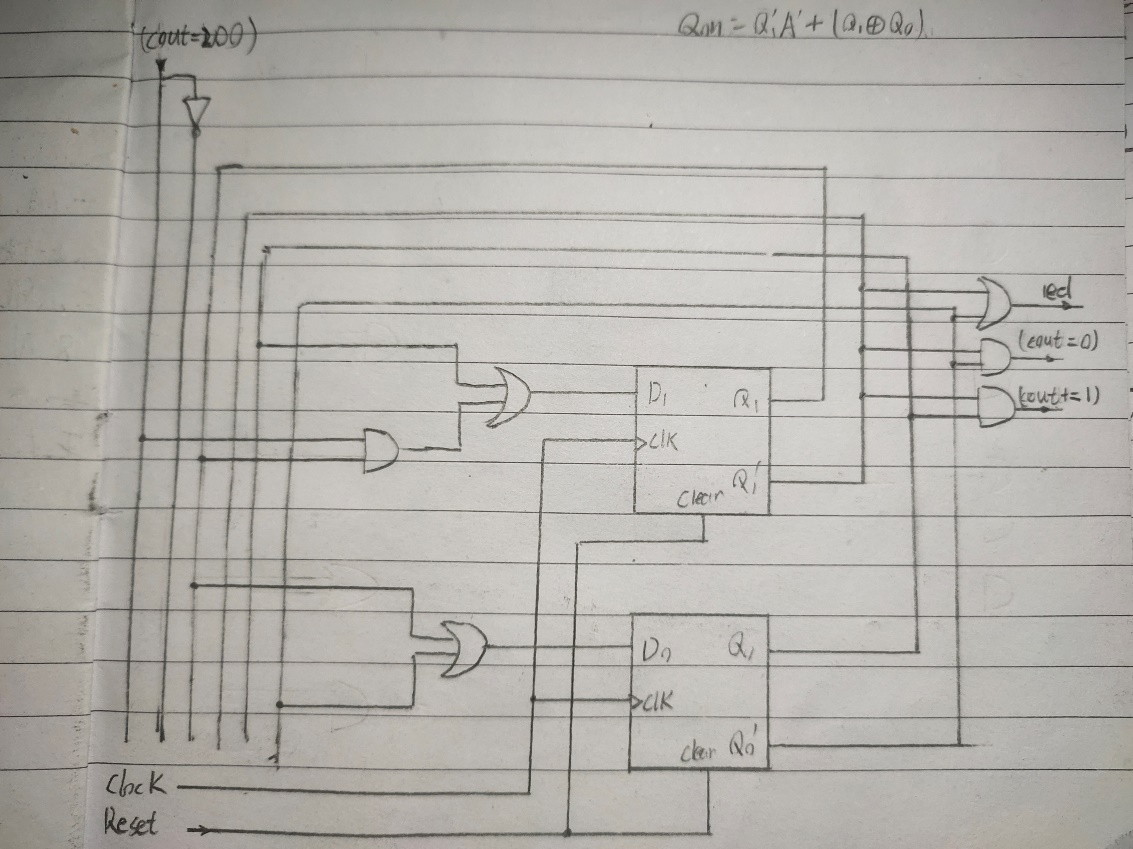
1)Construct a FSM circuit that will turn on a LED for 100 seconds and then turn it off. Assume that the input clock frequency is 4 Hz. This means that for every second, the FSM will go through four states. You cannot use a clock divider to slow down the clock. If you just use the number of states to do the delay, this will require 400 states. This will require too many flip-flops for drawing the circuit manually. So instead, you can use a counter to count how many times to loop around in a state before going on to the next state to get this time delay.

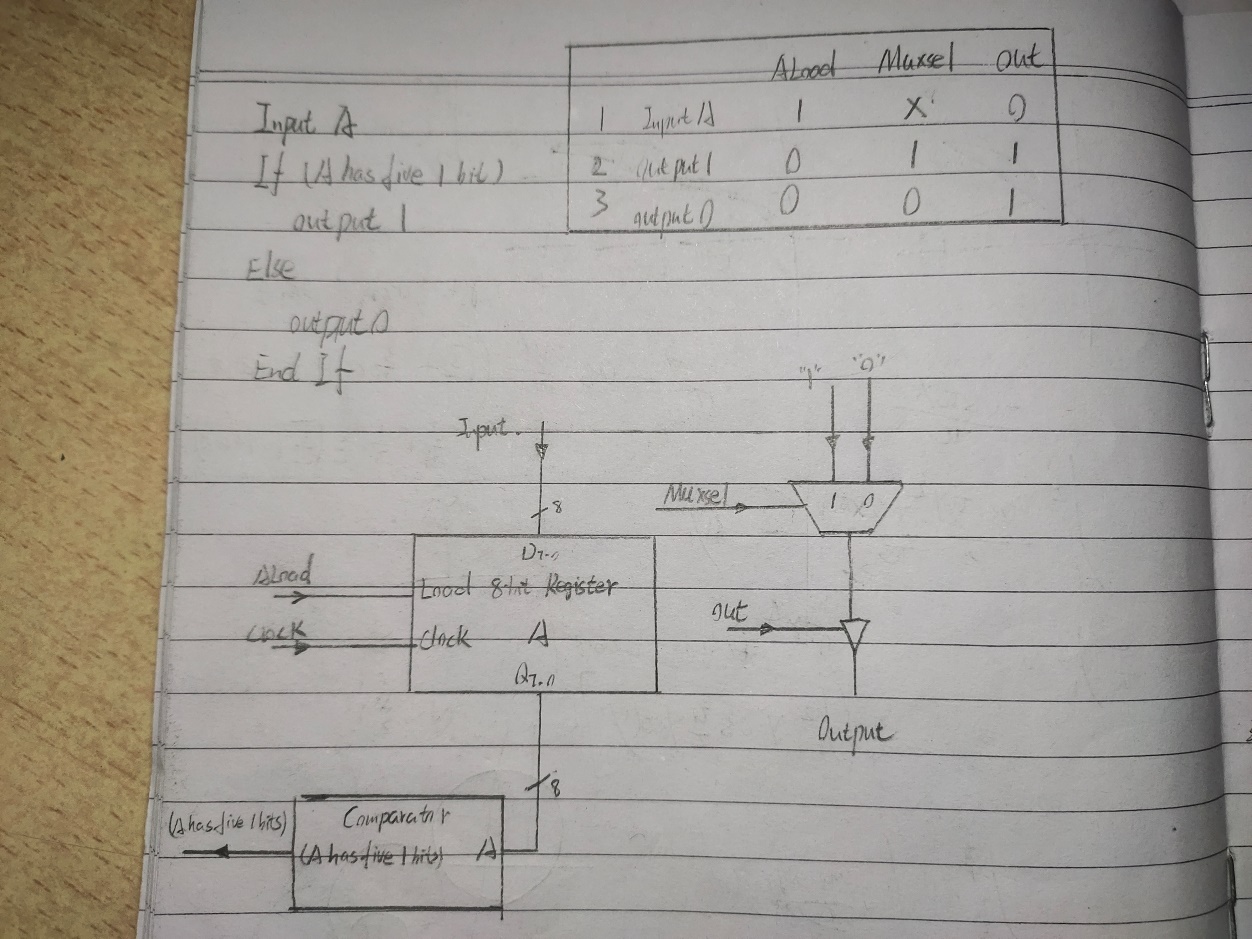


状态图如图所示，使用一个变量cout纪录循环圈数

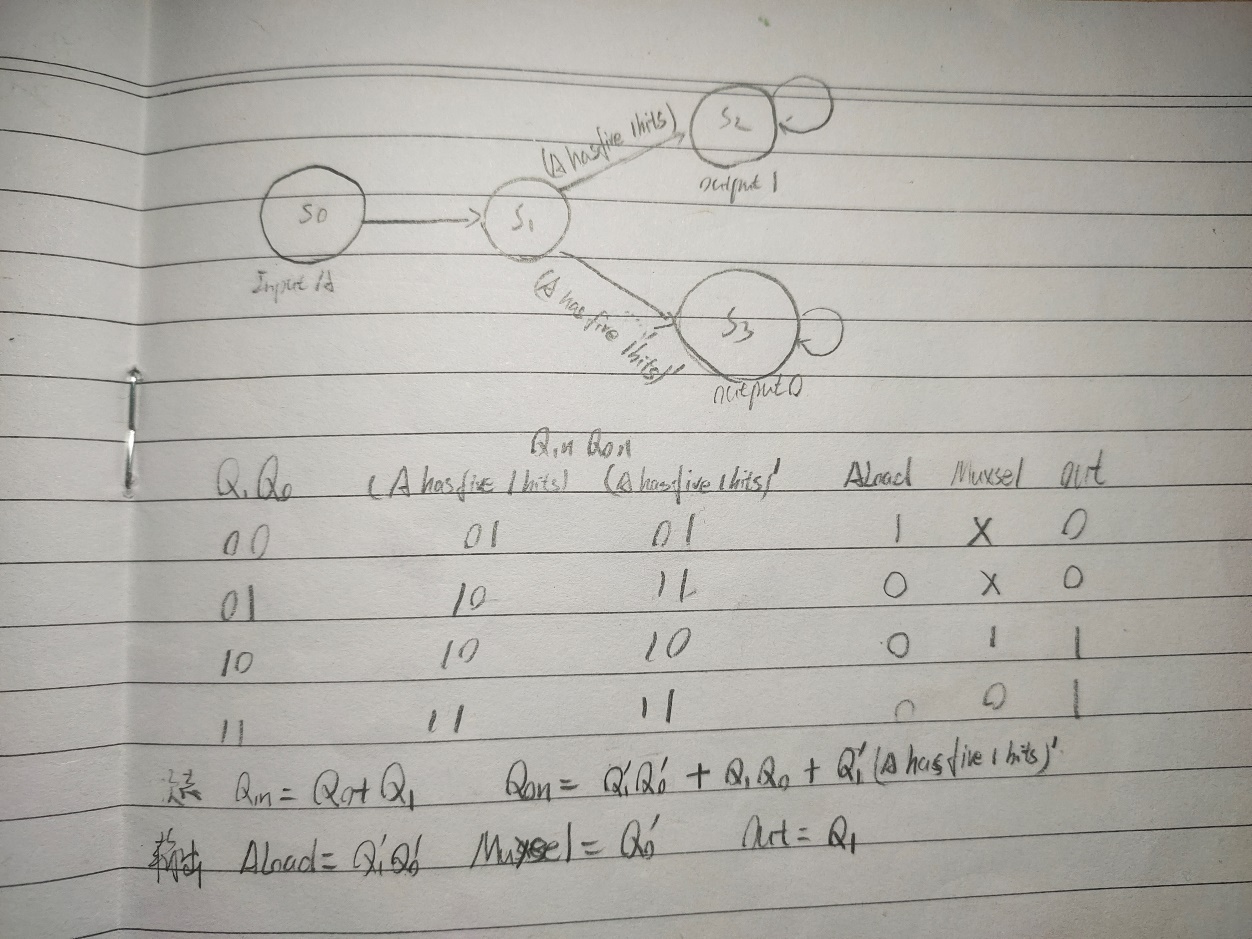


状态机电路

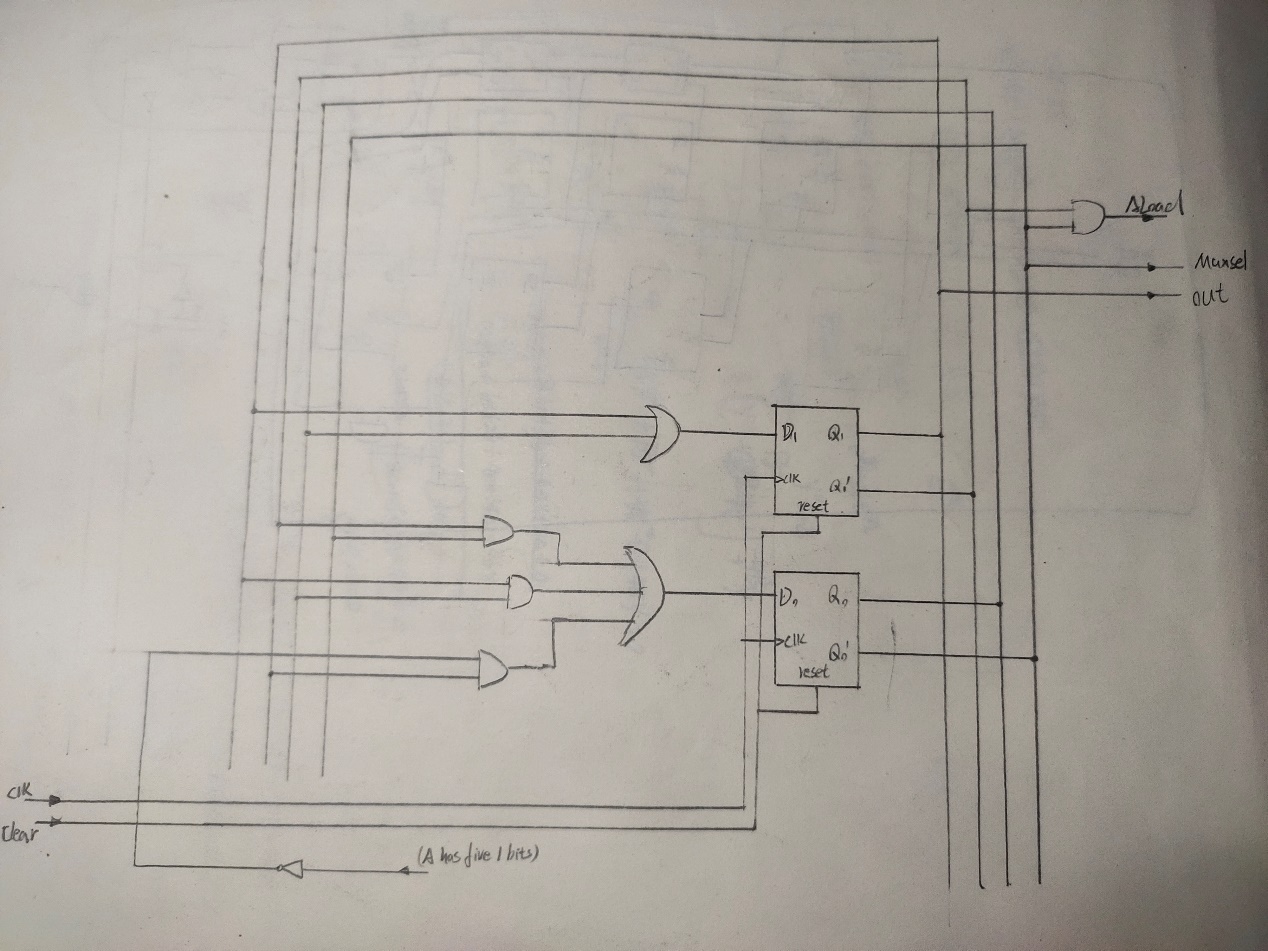
2)Manually design and implement on a FPGA a dedicated microprocessor to enter one 8-bit number. Output a 1 if the number has five 1 bits; otherwise, output a 0.



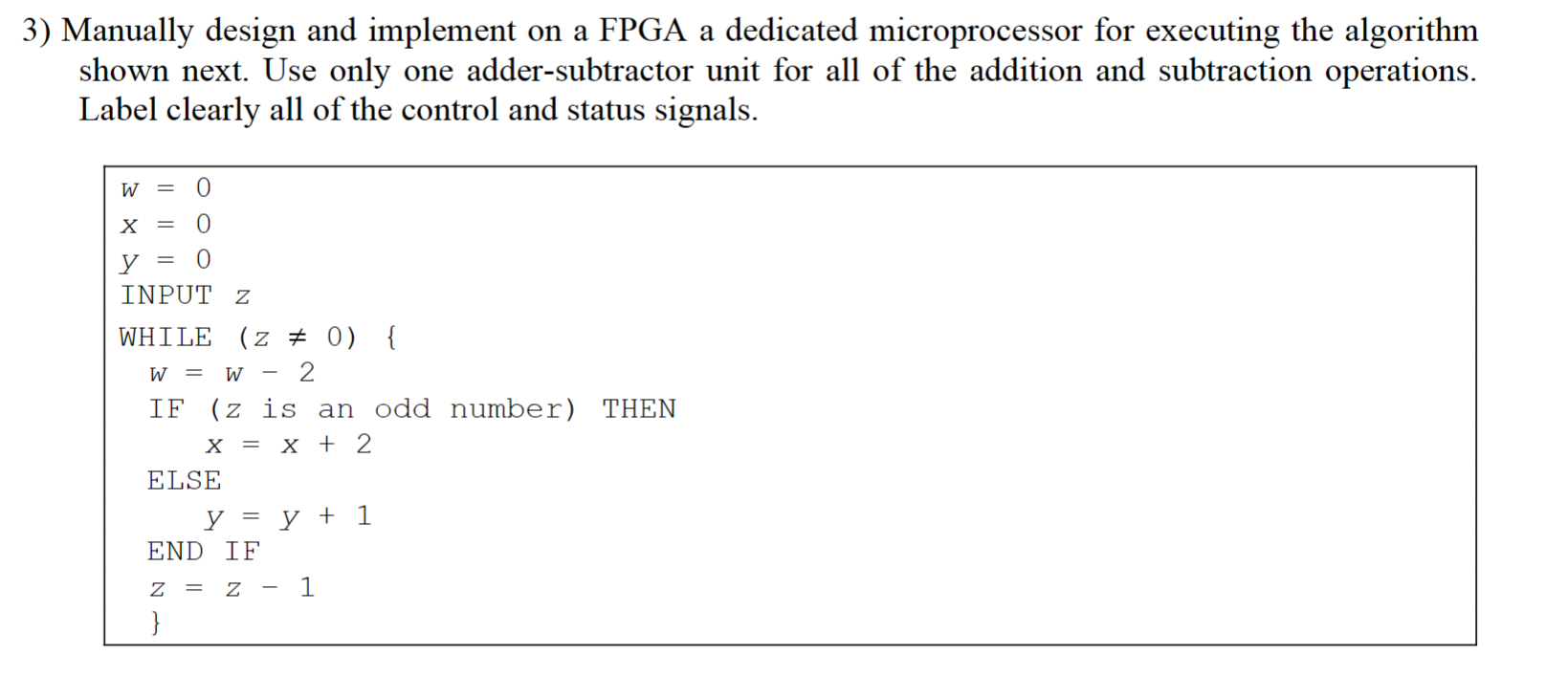
数据通路

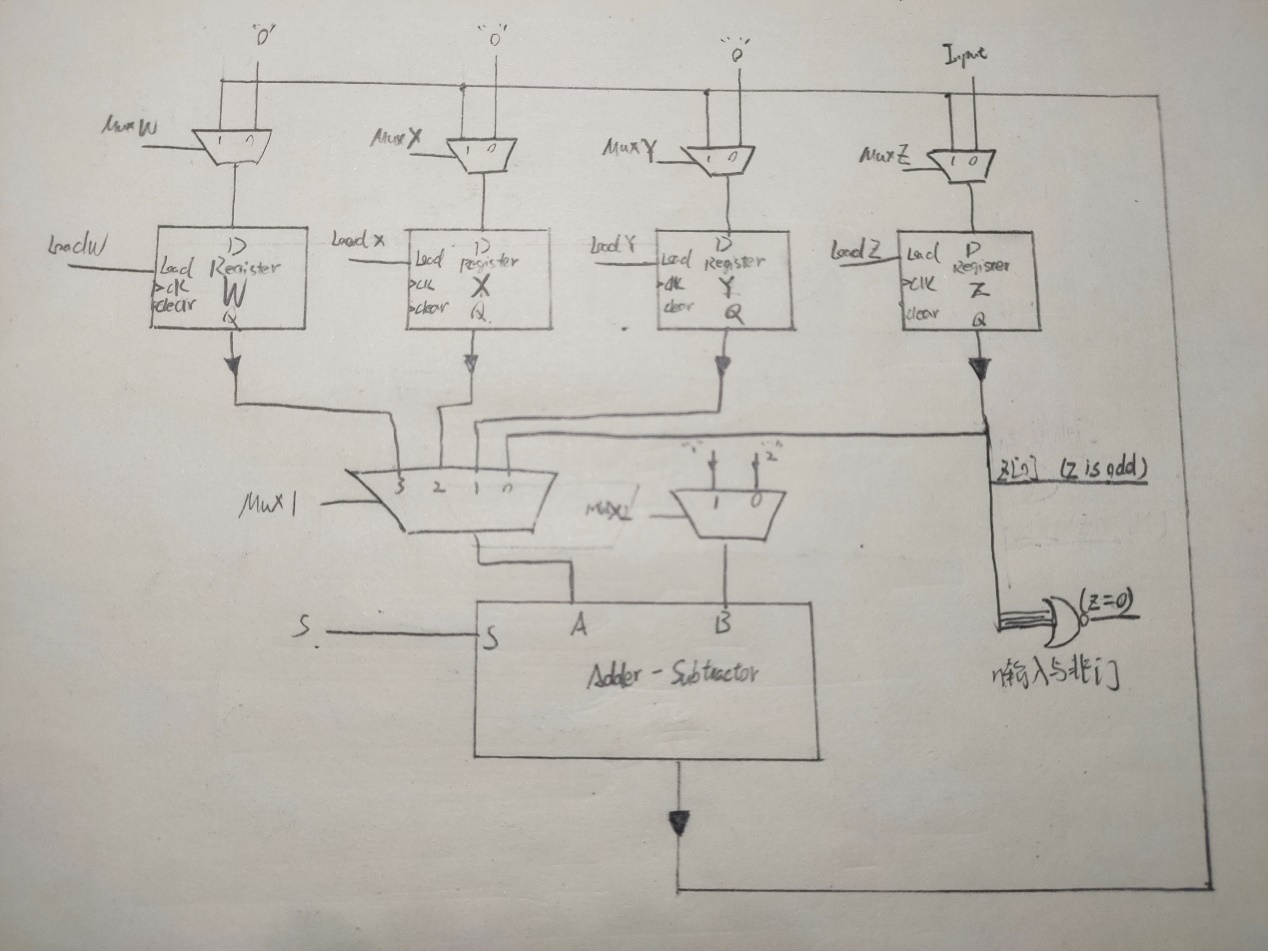


状态图

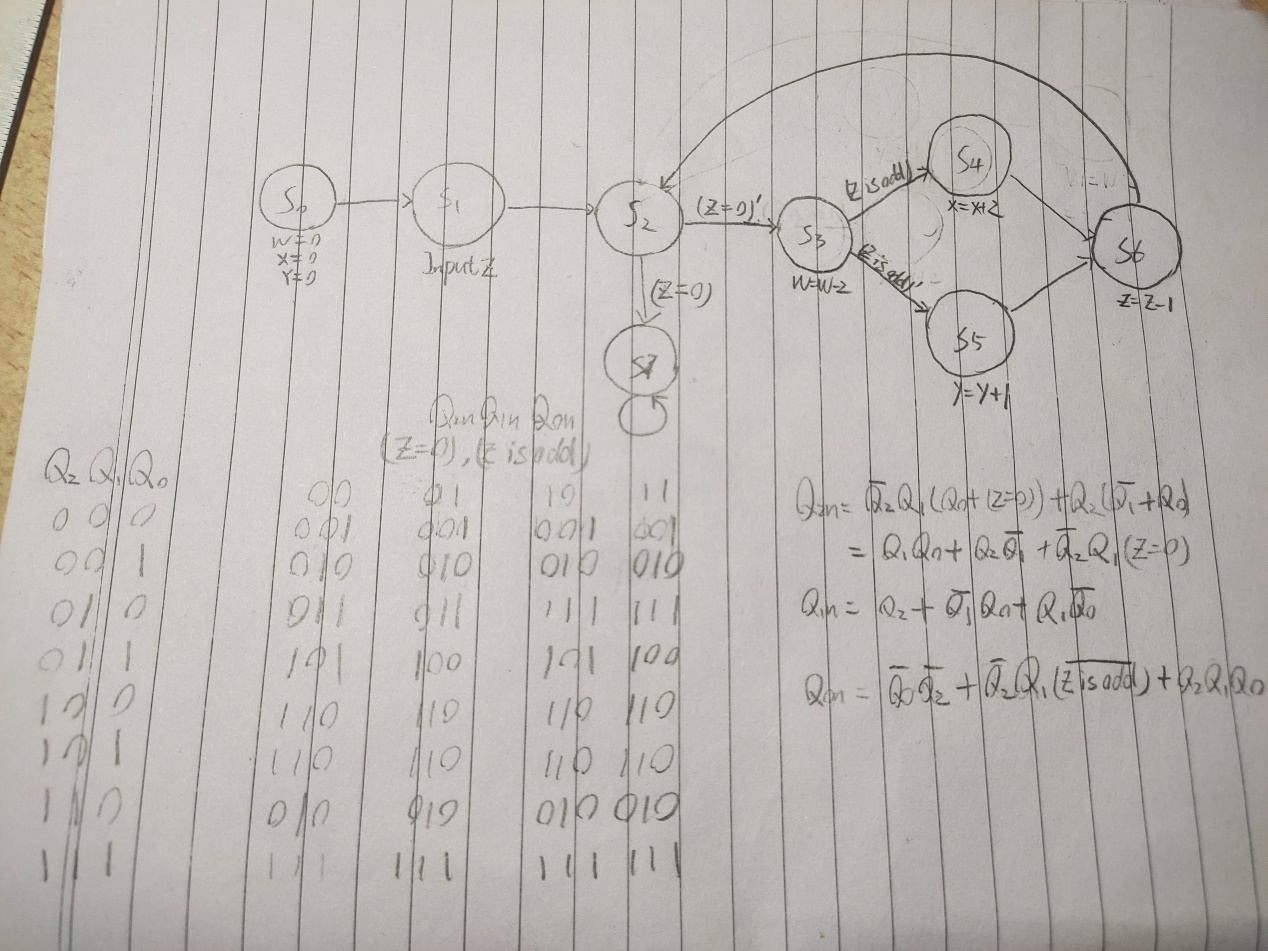


控制单元

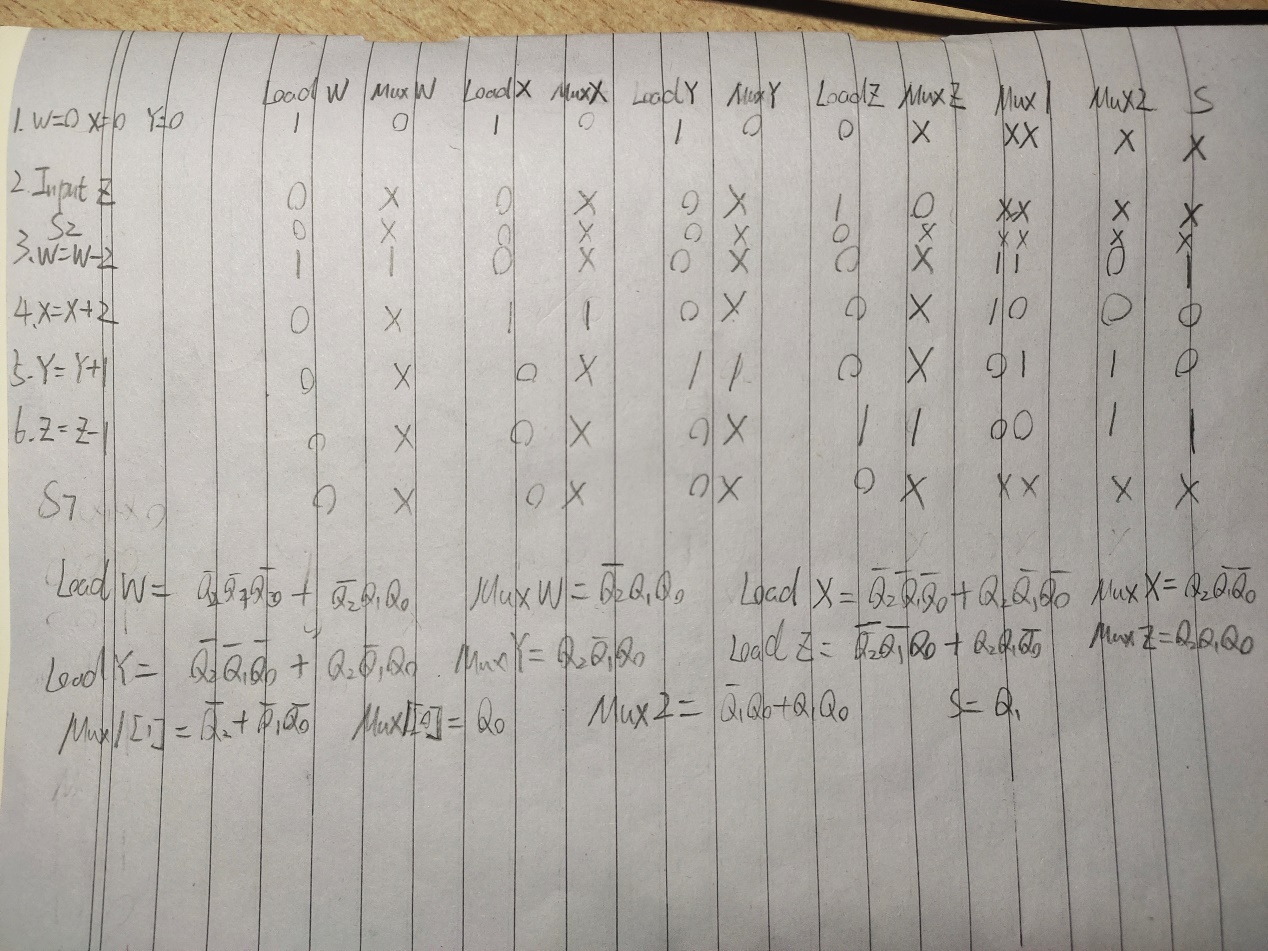


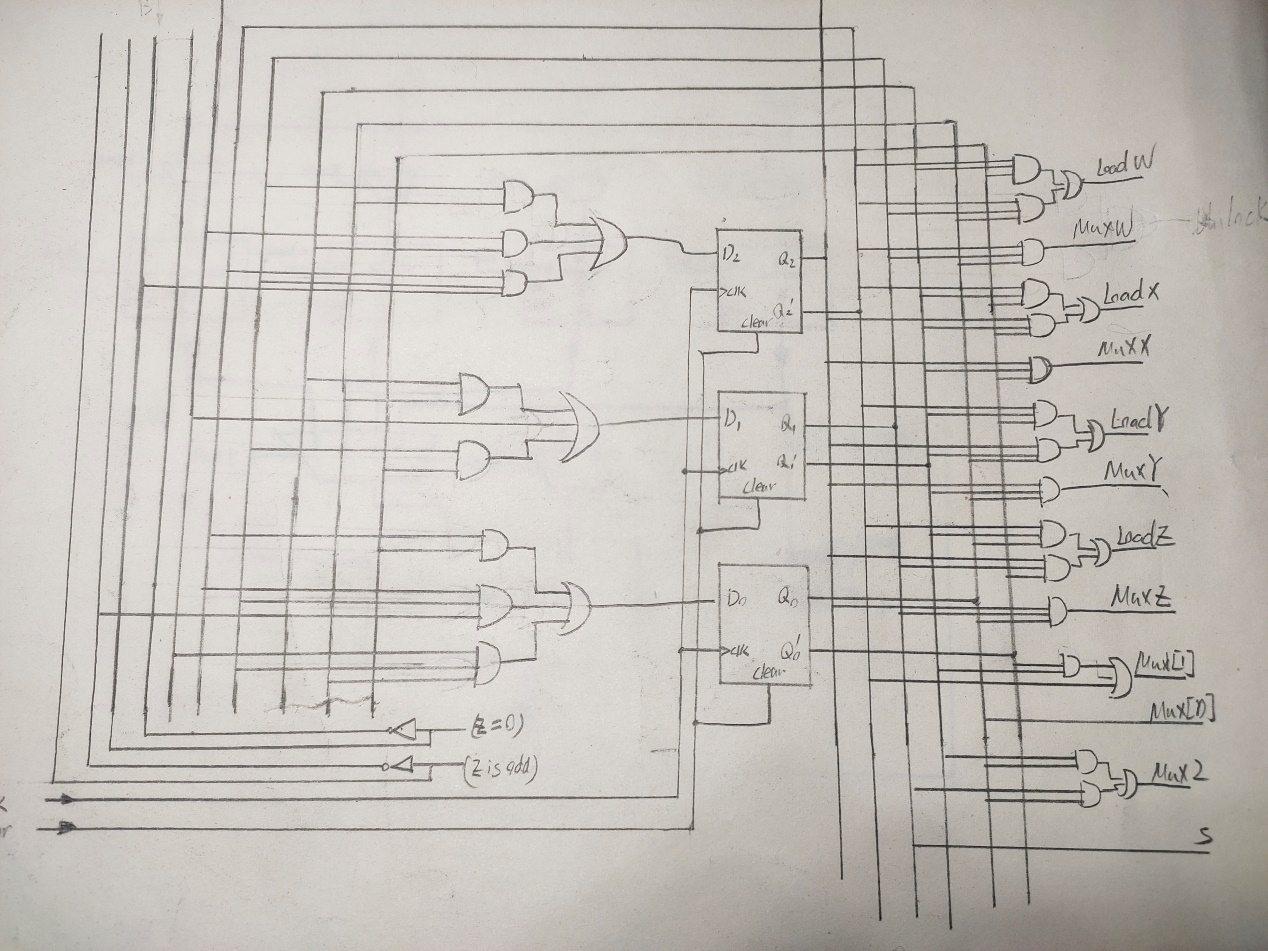


数据通路



状态图



控制字和输出方程

控制单元