

Co-Designing Binarized Transformer and Hardware Accelerator for Efficient End-to-End Edge Deployment

Yuhao Ji^{*,1,2}, Chao Fang^{*,1}, Shaobo Ma¹, Haikuo Shao¹, and Zhongfeng Wang^{1,3}

¹School of Electronic Science and Engineering, Nanjing University, Nanjing, China

²Department of Computer Science and Engineering, Chinese University of Hong Kong, Hong Kong, China

³School of Integrated Circuits, Sun Yat-sen University, Shenzhen, China

arthurxxzh@gmail.com,{fantasysee,201180102,hkshao}@smail.nju.edu.cn,zfwang@nju.edu.cn

ABSTRACT

Transformer models have revolutionized AI tasks, but their large size hinders real-world deployment on resource-constrained and latency-critical edge devices. While binarized Transformers offer a promising solution by significantly reducing model size, existing approaches suffer from algorithm-hardware mismatches with limited co-design exploration, leading to suboptimal performance on edge devices. Hence, we propose a co-design method for efficient end-to-end edge deployment of Transformers from three aspects: algorithm, hardware, and joint optimization. First, we propose BMT, a novel hardware-friendly binarized Transformer with optimized quantization methods and components, and we further enhance its model accuracy by leveraging the weighted ternary weight splitting training technique. Second, we develop a streaming processor mixed binarized Transformer accelerator, namely BAT, which is equipped with specialized units and scheduling pipelines for efficient inference of binarized Transformers. Finally, we co-optimize the algorithm and hardware through a design space exploration approach to achieve a global trade-off between accuracy, latency, and robustness for real-world deployments. Experimental results show our co-design achieves up to 2.14~49.37× throughput gains and 3.72~88.53× better energy efficiency over state-of-the-art Transformer accelerators, enabling efficient end-to-end edge deployment.

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1 INTRODUCTION

Transformer-based neural networks have experienced a remarkable surge in recent years, from BERT [6], to ViT [7, 31], further to the large language models (LLMs) [2, 42], demonstrating exceptional performance across a diverse range of tasks. However, the dramatic increase in model size and computational complexity has imposed

* The first two authors contribute equally to this work.

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significant constraints, particularly in latency-critical and resource-constrained end-to-end edge scenarios.

Quantization [17, 19, 30, 40, 43] emerges as a promising solution to alleviate the challenge of Transformer edge deployment, which reduces model size and computational complexity by lowering the bit width of weights or activations. Among them, *binarized Transformer* [1, 21, 26, 32] stands out, which reduces the bit width of weights to 1-bit and transforms computations to bit-wise operations, minimizing both parameter storage and computational complexity. However, challenges remain on both algorithm and hardware levels for efficient end-to-end edge deployment of binarized Transformers.

On the algorithm level, existing binarized Transformers struggle for efficient edge deployment due to hardware-unaware model architectures, theoretical-practical performance gap, and neglected model robustness. 1) Existing binarized Transformers often lack consideration for hardware implementation, posing challenges to the deployment on edge devices with limited resources. For instance, the use of complex activation functions like GELU in BinaryBERT [1] demands significant hardware resources and sophisticated design [37], increasing implementation costs. 2) Binarized Transformers often prioritize theoretical compression ratios, neglecting the impact on hardware performance. For instance, existing works [1, 21, 32] only evaluate the theoretical reduction in model size and FLOPs of their binarized Transformers without validating the actual speedup performance. Consequently, these models may not translate theoretical compression benefits into real-world performance improvements on edge devices. 3) While accuracy has improved, the robustness of binarized Transformers remains hardly explored, which is crucial for ensuring reliable performance in diverse and challenging environments, especially at the edge where data quality may be various and unpredictable.

On the hardware level, current accelerator designs [9–11, 18, 20, 23, 25, 29, 36, 39] fall short in fully enabling efficient end-to-end edge deployment of binarized Transformers due to limitations in constrained computational support, architectural inefficiencies, and suboptimal hardware configurations. 1) Existing accelerators primarily focus on high-bit quantized models, neglecting the unique requirements of binarized Transformers, resulting in a lack of support for binarized acceleration. Furthermore, the crucial hardware implementation of the quantization process itself remains unexplored, preventing an end-to-end acceleration. 2) Existing accelerator architectures fall into two categories: streaming-like [11, 16, 18, 24, 34, 36] and processor-like [10, 14, 20, 23, 25, 27, 33, 39, 41], but neither offers an ideal solution for edge deployment with binarized Transformers. Streaming-like

Table 1: Comparative Analysis of the Related Works and Ours

Work	Alg Tech.	HW Bit-width	HW Implementation	HW Arch.	End to end	Tune
I-BERT [17]	✓ Quantization (W8A8 ^T)	✓ FIX8	✗ Tesla T4 GPU	N/A	✓ Yes	Alg Tuning
I-ViT [19]	✓ Quantization (W8A8 ^T)	✓ FIX8	✗ RTX 2080 Ti GPU	N/A	✓ Yes	Alg Tuning
BinaryBERT [1]	✓ Binarization (W1A8/4 ^T)	✗ FP32	✗ GPU	N/A	✓ Yes	Alg Tuning
OPTIMUS [25]	✗ N/A	FIX16	✓ ASIC 28nm	Processor	✗ No	✗ N/A
A ³ [11]	✗ N/A	✓ FIX8	✓ ASIC 40nm	Streaming	✗ No	✗ N/A
FTRANS [18]	✓ BCM-based Prune	FIX16	✓ FPGA VCU118	Streaming	✓ Yes	HW Tuning
Lu et al. [23]	✗ N/A	✓ FIX8	✓ FPGA VU13P	Processor	✗ No	✗ N/A
EFA-Trans [39]	✓ Bank-balanced Prune	✓ FIX8	✓ FPGA ZCU102	Processor	✗ No	✓ Alg&HW Co-tuning
FQ-BERT [20]	✓ Quantization (W4A8 ^T)	✓ FIX8/4	✓ FPGA ZCU102	Processor	✓ Yes	✗ N/A
ViA [36]	✗ N/A	✗ FP16	✓ FPGA Alveo U50	Streaming	✓ Yes	HW Tuning
Fan et al. [9]	✓ Butterfly-sparsities Prune	✗ FP16	✓ FPGA Zynq 7045	✓ Mixed	✓ Yes	✓ Alg&HW Co-tuning
Ours	✓ Binarization (W1A8/4/2/1 ^T)	FP16-FIX8/4/2/1 Mixed	✓ FPGA ZCU102	✓ Mixed	✓ Yes	✓ Alg&HW Co-tuning

[†] A network with weights quantized to b_w bits and activations quantized to b_a bits is denoted as Wb_wAb_a .

architectures, optimized for efficiency with large batches, face underutilization issues when dealing with the smaller batch sizes typically encountered at the edge. Conversely, processor-like architectures, designed for versatility, introduce overhead with complex datapaths and scheduling for intricate Transformer operations. 3) Additionally, the hardware configurations of existing accelerators often rely on empirical values rather than a systematic exploration, which contributes to the suboptimal performance observed in practice. Consequently, the resulting accelerators fail to operate at their full potential, hindering efficient edge deployment.

To facilitate efficient end-to-end edge deployment, we propose a co-design approach within binarized Transformers and hardware accelerator that addresses the above challenges from three aspects. From algorithm aspects, we introduce BMT, a novel binarized Transformer model that incorporates hardware-aware quantization methods and computational components, specifically designed for efficient execution on edge devices. Additionally, we develop weighted ternary weight splitting (WTWS) to optimize the training process of BMT. From hardware aspects, to fully exploit the practical acceleration of binarized Transformer, we design BAT, a novel streaming-processor-mixed binarized Transformer accelerator, equipped with highly optimized computational units and scheduling pipelines to enable an efficient end-to-end inference for binarized Transformers. From joint optimization aspects, we further push the performance boundaries by co-optimizing the binarized Transformers and BAT through a design space exploration (DSE) approach, allowing us to find a global trade-off between accuracy, latency, and robustness for real-world deployments.

The contributions of this work are summarized as follows:

- A hardware-friendly binarized Transformer, BMT, which yields a substantial compression ratio compared to the full precision baseline with comparable accuracy, exhibiting significant potential for edge deployment. (Section 3)
- A streaming-processor-mixed binarized Transformer accelerator, BAT, enabling high efficiency and low power end-to-end acceleration of binarized Transformers. (Section 4)
- Dataflow optimizations adaptable for edge scenarios to improve the hardware efficiency, and a DSE approach to jointly optimize both algorithmic and hardware parameters, striking a fine balance between accuracy, robustness, and latency. (Section 5)
- Comprehensive experiments showing our co-design achieves up to 2.14~49.37 \times and 3.72~88.53 \times improvement on throughput and energy efficiency over SOTA Transformer accelerators and

improves energy efficiency by 213.82 \times and 174.01 \times compared to the CPU and GPU implementations. (Section 6)

TABLE 1 summarizes the comparison between the related works and our work, focusing on these critical features for **edge deployment**: algorithm-level technique (Alg Tech.), operating arithmetic precision on hardware (HW Bit-width), type of hardware platform (HW Implementation) and its architecture (HW Arch.), whether the work implements the end-to-end acceleration (End-to-end), whether algorithmic or hardware parameter configuration is tuned (Tune). The comparison reveals that *our work presents significant benefits and potential over prior arts for efficient edge deployment*.

2 BACKGROUND

2.1 Transformer-based Neural Networks

Fig. 1 illustrates the architecture of the encoder-based Transformer network, where each encoder consists of a multi-head attention module (MHA) and a feed-forward network (FFN). Residual addition and layer normalization (LN) are used before and after FFN. Within each MHA, the input (**A**) is projected to query (**Q**), key (**K**) and value (**V**) matrices through three different linear layers (**AW**). The query matrix is then multiplied with \mathbf{K}^T , and the scaled product ($\mathbf{Q}\mathbf{K}^T$) is processed by a softmax module to produce the score matrix (**S**). This matrix **S** is then multiplied with **V** and the product (**SV**) is passed through an additional linear layer (**BW**) to generate the final output of the MHA. In FFN, the input is first projected into an intermediate matrix (**R**) through a linear layer (**CW**), followed by the activation function. The activated result (**R1**) is then subjected to another linear transformation (**R1W**) to obtain the output of FFN. Compared to the vanilla Transformer, the quantized Transformer incorporates quantization processes, which quantizes weights and activations to the designed bit-width, and matrix multiplications are transformed to quantized matrix multiplications (QMMs).

2.2 Binarization and Its Unique Demands

Binarization, which reduces the bit width to 1-bit, has been studied for a long time [1, 15, 21, 22, 26, 28, 32, 38]. A notable work, Binary-Weight-Network (BWN) [15], binarizes full precision weight \mathbf{W}_R with a scaling parameter α according to the following equation:

$$BWN(\mathbf{W}_R) = \alpha \mathbf{W}_B, \quad (1)$$

where $\mathbf{W}_B = \text{Sign}(\mathbf{W}_R)$, $\alpha = \frac{1}{N} \|\mathbf{W}_R\|_1$, N is the total number of elements of \mathbf{W}_R .

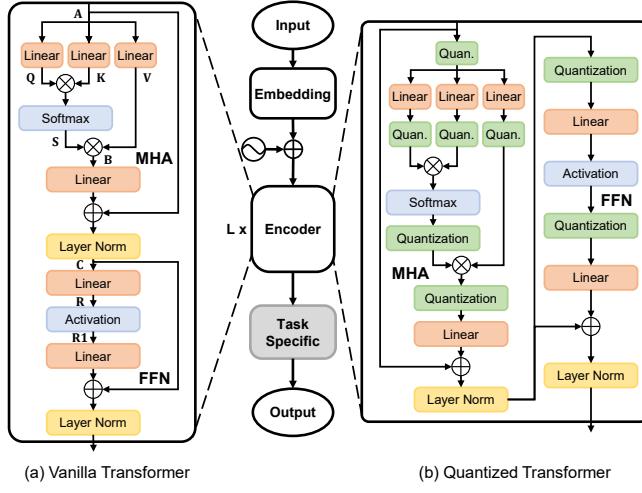


Figure 1: Overview of encoder-based Transformer structure: (a) vanilla Transformer and (b) quantized Transformer.

Binarized Transformers, while offering significant computational efficiency benefits, introduce unique demands that necessitate careful co-design of algorithms and hardware. This partially stems from their reliance on a quantization-dequantization scheme as shown in Fig. 2, which enables efficient hardware acceleration by converting full-precision inputs to lower bit widths but requires dequantization for high-precision tasks. Binarized Transformers further complicate matters by requiring support for two distinct QMM types: *activation* \times *weight* (linear layer) and *activation* \times *activation* (\otimes). For a binarized Transformer in W1AN, two multiplications are involved: N -bit \times 1-bit and N -bit \times N -bit, which is consistent with the aforementioned two QMM types. In addition, the activation quantization may incorporate signed and unsigned quantization.

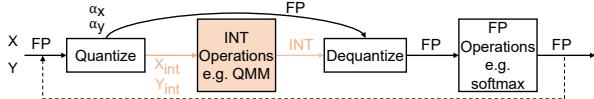


Figure 2: Quantization-dequantization computational flow.

3 ALGORITHM OPTIMIZATION

3.1 Hardware-friendly Model Design

Limited resources in edge devices require hardware-aware design for binarized models. Existing models [1, 21, 26, 32] lack such considerations, hindering efficient deployment. Our binarized Transformer, namely BMT, addresses this with hardware-optimized techniques.

Elastic Activation Quantization. Existing activation quantization methods often incur high hardware resource and latency overhead due to extra scaling factor computations [5] during implementation on dedicated accelerators. To overcome this issue, we incorporate hardware-friendly elastic quantization [21] method for activations when designing our BMT, making it exhibit outstanding performance in the extremely low-bit scenario. The equation can be formulated as follows:

$$X_{INT} = \alpha \lfloor \text{clip}\left(\frac{X_R + \beta}{\alpha}, Q_n, Q_p\right) \rfloor, \quad (2)$$

where $\lfloor \cdot \rfloor$ represents the rounding function. X_R is a full precision tensor and α is the full precision scaling factor. Q_n/Q_p is the min/max value of the quantization range.

BMT benefits from several aspects by using hardware-friendly quantization. First, both coefficients α and bias β of BMT are learnable parameters, but fixed before deployment, reducing computational burden during inference. Second, the pre-computed reciprocal of α and the standardized values of Q_n and Q_p in BMT further streamline online inference by eliminating complex operations and simplifying the clip function implementation.

Non-linear Activation Function. Prioritizing hardware efficiency, BMT employs the simple ReLU activation function instead of the computationally expensive GELU function commonly used in binarized Transformers. ReLU requires minimal hardware resources, as it can be implemented with a single multiplexer, making it ideal for resource-constrained edge devices.

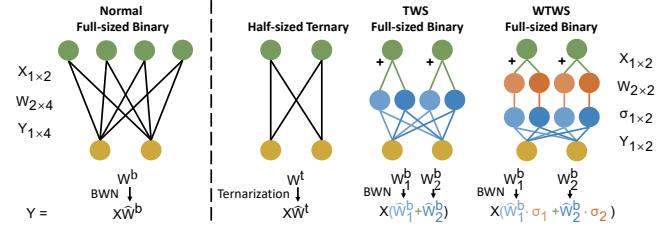


Figure 3: The illustration for WTWS.

3.2 Weighted Ternary Weight Splitting

To compensate for potential accuracy loss from hardware-oriented design choices, BMT introduces a novel technique called weighted ternary weight splitting (WTWS). Unlike prior techniques like TWS in BinaryBERT [1], WTWS leverages trainable coefficients during the splitting process. These coefficients capture the importance of each splitted weight, leading to higher accuracy.

As shown in Fig. 3, TWS starts from training a half-sized ternary Transformer model, and then applies ternary weight splitting operator on its linear layers to obtain the full-sized latent binarized Transformer model, which quantizes weights to $\{-1, 1\}$. The equations are as follows:

$$W_{1,i}^b, W_{2,i}^b = \begin{cases} a \cdot W_i^t, (1-a)W_i^t & \text{if } \hat{W}_i^t \neq 0, \\ b + W_i^t, -b & \text{if } \hat{W}_i^t = 0, W_i^t > 0, \\ b, -b + W_i^t & \text{otherwise,} \end{cases} \quad (3)$$

where a and b are defined as follows:

$$a = \frac{\sum_{i \in \mathcal{I}} |W_i^t| + \sum_{j \in \mathcal{J}} |W_j^t| - \sum_{k \in \mathcal{K}} |W_k^t|}{2 \sum_{i \in \mathcal{I}} |W_i^t|}, b = \frac{\frac{n}{|\mathcal{I}|} \sum_{i \in \mathcal{I}} |W_i^t| - \sum_{i=1}^n |W_i^t|}{2(|\mathcal{J}| + |\mathcal{K}|)}, \quad (4)$$

where $\mathcal{I} = \{i \mid \hat{W}_i^t \neq 0\}$, $\mathcal{J} = \{j \mid \hat{W}_j^t = 0 \text{ and } W_j^t > 0\}$, $\mathcal{K} = \{k \mid \hat{W}_k^t = 0 \text{ and } W_k^t < 0\}$. $|\cdot|$ denotes the cardinality of the set. The equation above ensures the result of the linear layer remains the same, i.e. $\hat{W}^t = \hat{W}_1^b + \hat{W}_2^b$.

However, simply adding the split weights in TWS may discard valuable information. For example, when $\hat{W}_1^b \gg \hat{W}_2^b$, $\hat{W}^t \approx \hat{W}_1^b$ and the information of \hat{W}_2^b may be lost. To alleviate this problem,

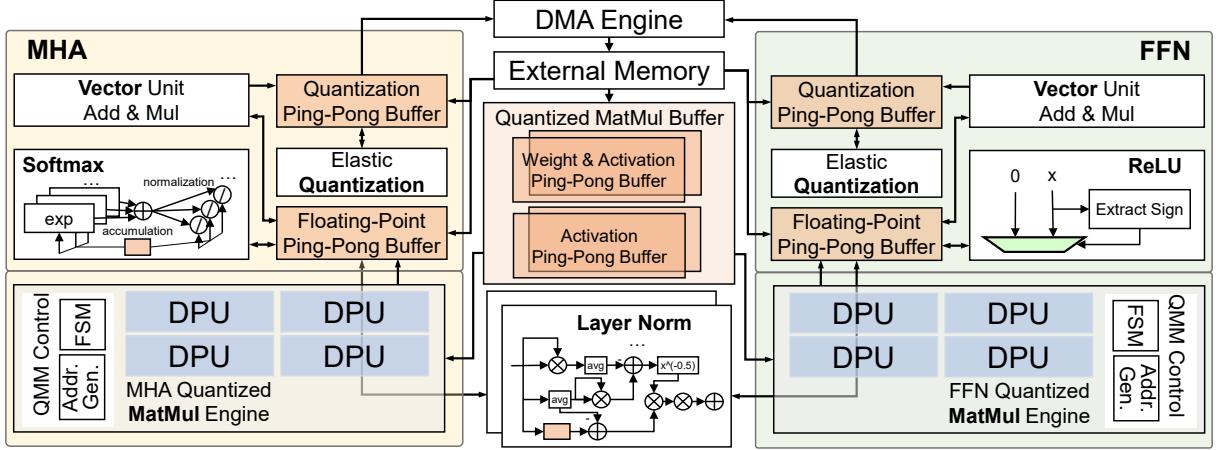


Figure 4: Hardware overview of our proposed BAT.

WTWS introduces trainable coefficients σ_1 and σ_2 to learn the significance of \hat{W}_1^b and \hat{W}_2^b respectively, reformulating the equation to $Y = X(\hat{W}_1^b \cdot \sigma_1 + \hat{W}_2^b \cdot \sigma_2)$. As shown in Fig. 3, WTWS introduces an additional layer highlighted in orange to facilitate this process. Both σ_1 and σ_2 are initialized as all-ones vectors and are column-wise trainable.

4 HARDWARE ACCELERATOR

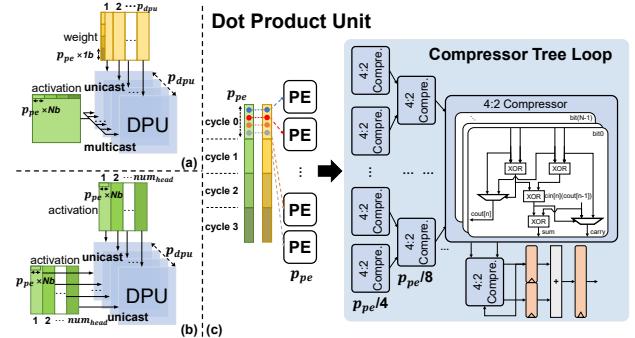
Considering the disadvantages of primitive streaming or processor-like accelerators, our proposed binarized Transformer accelerator, namely BAT, is characterized by a streaming-processor-mixed architecture. On the one hand, the MHA and FFN are executed separately in a pipelined manner following a streaming-like design. On the other hand, the architectures within MHA and FFN modules are designed as a processor-like paradigm.

4.1 Architecture Overview

Fig. 4 shows the architecture of BAT, which is composed of a MHA module, a FFN module, a direct memory access (DMA) engine, an external memory, and several on-chip buffers. Both the MHA and FFN modules are equipped with a QMM engine, a vector unit (VU), a elastic quantization unit (QU) and a layer normalization unit. The MHA module includes a softmax unit while the FFN module features a ReLU activation unit. The individual design of MHA and FFN modules significantly simplifies the control logic and datapath compared to a simple processor-like architecture where the MHA and FFN are processed within a unified architecture [4, 10, 23].

In both MHA and FFN modules, the dominant operations, QMMs, are performed by dot-product-based QMM engine which can flexibly adapt to different matrix multiplication sizes with high efficiency. VU handles operations with low computational density including dequantization and residual addition with vectorized inputs, and QU is designed for elastic quantization. To ease the on-chip memory consumption and avoid the overhead associated with pattern matching between the outputs of QU and the inputs of QMM engine, these intermediate results are temporarily transferred back to the external memory. Despite increasing the bandwidth requirement, it is a strategic trade-off that conserves valuable on-chip resources. Besides, ping-pong buffer technique is also implemented

for all the on-chip buffers to overlap the time between data transfer and computation.

Figure 5: Data access pattern for (a) activation \times weight and (b) activation \times activation QMMs. (c) The structure of DPU.

4.2 Quantized Matrix Multiplication engine

Processor-like architectures hinge on the core computation engine for overall performance, necessitating a QMM engine designed for high throughput and flexibility to support diverse QMMs. Fig. 4 shows the hardware architecture of QMM engine, which consists of p_{dpu} number of dot product units (DPUs) with controllers including a finite state machine (FSM) and an address generator.

As mentioned in Section 2.2, there are two types of QMMs in the quantized Transformer: (a) activation \times weight and (b) activation \times activation. Fig. 5 (a) and (b) illustrates the unified data access pattern of QMM engine for these two QMMs: (a) The weight matrix are partitioned into p_{dpu} tiles along the column direction, with each tile being fed into the corresponding DPU. Concurrently, the activation matrix is multicast to each DPU. (b) QMM follows the multi-head mechanism, both activation matrices are partitioned into num_{head} tiles along the column direction and are then unicast to their respective DPU. When num_{head} and p_{dpu} are not exactly matched, the num_{head} tiles are batched ($num_{head} > p_{dpu}$) or divided along the row dimension ($num_{head} < p_{dpu}$). Notably, the MHA's QMM engine is designed to incorporate both patterns while

the FFN's QMM engine only needs pattern (a), as the FFN contains only the $activation \times weight$ QMMs.

Fig. 5 (c) elaborates on the structure of DPU. Each DPU is composed of p_{pe} -parallel processing element units (PEs), followed by a compressor tree loop. For high throughput, the DPU executes vector dot products in an unfolding factor of p_{pe} , processing p_{pe} elements per vector simultaneously. The compressor tree loop accumulates PE outputs in each iteration. The compressor tree is constructed based on 4:2 compressor, which mitigates the delay of carry chain propagation and thus optimizes the combinational delay.

Table 2: Operands & Operations in Binarized Transformers

x (activation)	y (weight/activation)	Operations
N -bit signed	binarized weight	AW, BW, CW
N -bit signed	N -bit signed activation	QK^T
N -bit unsigned	N -bit signed activation	SV
N -bit unsigned	binarized weight	R1W

4.3 Processing Element Unit

Fig. 6 (a) depicts the detailed architecture of PE for a multiplication $\mathbf{x} \times \mathbf{y}$. TABLE 2 summarizes the operands assigned to PE for different QMMs in binarized Transformer. To improve hardware utilization, PE is implemented with a bit-serial design. Each cycle, PE generates an N -bit \times 1-bit partial product. Consequently, it accomplishes N -bit activation \times binarized weight and N -bit \times N -bit activation multiplications with 1 cycle and N cycles, respectively, maximizing the hardware utilization.

Formally, the decimal value of binary encoded \mathbf{y} can be obtained through $\sum_{i=0}^{N_y-1} y_i 2^i$, where the bit value of y_i is either 1, 0, -1. Based on this, we develop a bit decoder to decode y_i into its real bit value (1: 2'b01, 0: 2'b00, -1: 2'b11) according to its data config, which can be implemented as a 2-bit output look-up table (LUT).

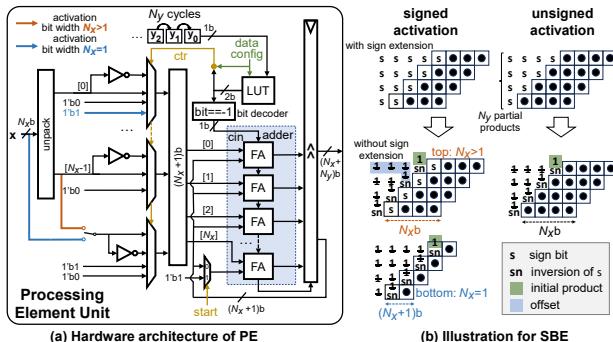


Figure 6: Detailed structure of PE and its SBE approach.

We then introduce a novel Sign Bit Elimination (SBE) approach to preprocess the signed or unsigned N_x -bit activation \mathbf{x} , aiming to save the resource consumption and shorten the critical path of PE. As illustrated in Fig. 6 (b), the multiplication unfolds into a summation of N_y partial products $\mathbf{p} = \mathbf{x} \times \mathbf{y}_i$, represented in two's complement. In the case where \mathbf{x} is signed and $N_x > 1$, referred to as the top case, the traditional extended sign bits of each partial product are reformulated to an addition of the inversion of sign bit (sn) and multiple bit values of 1. Here, most of the bit values of 1 are offset, with only one left, termed initial product, and then

the summation is transformed to a similar structure of unsigned integer addition without sign extension, with the bit width of each partial product increasing to $(N_x + 1)$. Similarly, in the case where \mathbf{x} is unsigned, SBE initiates from the sign bit p_{N_x} and the bit width also increases to $(N_x + 1)$.

When $N_x = 1$ and $\mathbf{p} (-1/0/1)$ requires a binary representation of $N_x + 1 = 2$ bits rather than N_x bits in other cases, SBE initiates from p_1 and the bit width remains $N_x + 1$ after SBE, which is consistent with other cases and shown in the signed bottom case of fig. 6 (b).

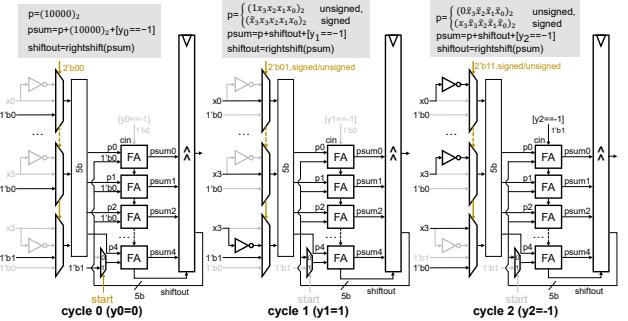


Figure 7: Example of the workflow of the proposed PE ($N_x=4$).

Fig. 7 further showcases the $\mathbf{x} \times \{\dots y_2 y_1 y_0\}$ computation process of PE with SBE when $N_x = 4$. **First cycle:** $y_0 = 0$, the value of partial product $\mathbf{x} \times y_0$ is $(0000)_2$ and sn is 1. Therefore, $\mathbf{p} = (1000)_2$ after SBE, which is fed into the adder together with the initial product 1. The partial sum ($psum$) is then loaded into the right shift register. **Second cycle:** $y_1 = 1$, the value of $\mathbf{x} \times y_1$ is \mathbf{x} . Following the signed top case or the unsigned case, p_i is selected through the multiplexers. **Third cycle:** $y_2 = -1$, the partial product is $-\mathbf{x}$, which can be reformulated to $\tilde{\mathbf{x}} + 1$. Term $\tilde{\mathbf{x}}$ undergoes the SBE transformation and the bit value 1 is directed to the c_{in} port of the adder. Through SBE, PE unifies signed and unsigned QMM operations. Also, since there is no sign extension involved, PE is implemented as a right-shifting sequential multiplier, which requires a smaller adder and prevents long carry propagation compared to a left-shifting design, thereby saving the hardware resource and reducing the path delay [3].

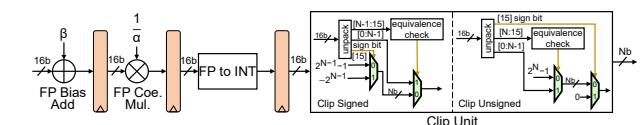


Figure 8: Elastic quantization unit.

4.4 Elastic Quantization Unit

Fig. 8 presents our fully pipelined elastic quantization unit. It consists of a floating-point bias adder, a floating-point coefficient multiplier, a converter from floating-point to integer, and a clip unit. For specific clipping ranges like signed or unsigned numbers, the clip unit logic can be significantly simplified, as shown in Fig. 8, using a combination of bit-wise operations and selection mechanisms. For instance, consider clipping an 16-bit signed activation to a 4-bit signed integer. The first step is to check if the most 13 significant bits are identical. Identical bits indicate that the input falls within the representable range of a 4-bit signed number and

can be directly output. Conversely, non-identical high bits suggest the input is outside this range. In this case, the sign bit is checked and the output is set to $2^{(4-1)} - 1$ if the sign bit is 0, or $-2^{(4-1)}$ if the sign bit is 1. The logic for clipping unsigned integers is similar.

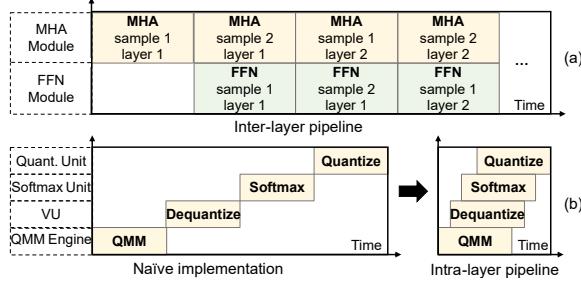


Figure 9: Dataflow optimization: (a) inter-layer pipeline and (b) intra-layer pipeline.

5 SCHEDULING AND CO-OPTIMIZATION

5.1 Dataflow Optimization

We propose two dataflow optimization methods, inter-layer pipeline, and intra-layer pipeline, for the streaming-like and processor-like design in BAT, respectively, enhancing the processing efficiency.

Inter-Layer Pipeline. We propose an inter-layer pipeline to fully utilize the benefits of the streaming-like design with individual computational modules of MHA and FFN. As shown in Fig. 9 (a), in the first stage, the MHA module loads input data and performs computations for sample 1. Once this process is finished, the MHA module proceeds to compute the next sample in the second stage, while the FFN module handles the computations for the output results generated by the MHA module in the first stage. In the third stage, the FFN module sends the output activations to the MHA module for the computations of layer 2 in sample 1. This alternating process enables the MHA and FFN modules to perform computations for multiple layers in both samples without encountering pipeline bubbles. Besides, as we set the batch size to 2 in this case, it is suitable for the mini-batch processing in edge scenarios. The overall latency can be given by:

$$T_{total} = T_{MHA} + (L - 1) \times max(T_{MHA}, T_{FFN}) + T_{FFN}, \quad (5)$$

where L is the number of model layers.

Intra-Layer Pipeline. Given that both processor-like MHA and FFN modules operate with a quantization-dequantization scheme, we introduce an intra-layer pipeline in a row-by-row execution manner to maximize computation overlap. For example, the operations within QMM and softmax units are conducted in integer and floating-point arithmetic, respectively. As shown in Fig. 9(b), once the softmax unit completes the computation of the first row in an input tensor, the results are immediately fed to the quantization unit. By employing our proposed intra-layer pipeline, BAT achieves a noticeable reduction in overall execution latency compared to the non-pipelined implementation with the elimination of waiting time for continuous processing. Additionally, this method allows for buffering data in certain rows instead of the entire intermediate data, leading to efficient utilization of storage resources.

5.2 Algorithm and Hardware Co-Optimization

The overall design space of our end-to-end system is formed by the hyperparameters of binarized Transformers and BAT, consisting of algorithmic parameters and hardware parameters in MHA and FFN modules, as presented in TABLE 3. Since the softmax operation constitutes a relatively small fraction of the total computational process, we set the parallelism of the softmax module to 4 without further exploration.

Table 3: Design Space of Co-Optimization

Algorithmic Parameters*			
Model Type	d_{hid}	d_{inter}	b_{act}
BinaryBERT, BMT, BiT	192, 384, 768	768, 1536, 3072	BinaryBERT: 8, 4 BMT: 4, 2 BiT: 1
Hardware Parameters**			
p_{dpd}	p_{quan}	p_{vu}	p_{ln}
8, 16, 32, 48, 64, 96	32, 64, 128	32, 64, 96, 128, 160	8, 16, 32, 48

* Hidden dimension size (d_{hid}), intermediate dimension size (d_{inter}), activation quantization precision (b_{act}).

** Parallelism of DPUs (p_{dpd}), quantization unit (p_{quan}), vector processing unit (p_{vu}), and LN unit (p_{ln}).

To achieve a globally optimized design, we assess the network deployment performance for each design variable, including accuracy, robustness, latency, and resource consumption. Specifically, the accuracy is determined by training and evaluating the binarized Transformer. In terms of robustness, we introduce perturbation Δx in the embedding layer using Gaussian noise, with a variance set to 0.01 and magnitude set to 10% of the magnitude of its original output, similar to steps in [32] and [13]. After repeating the inference 20 times, we obtain an accuracy array A . We define the robustness as $A_0 / \sqrt{\frac{1}{20} \sum_{i=1}^{20} (A_i - A_0)^2}$, where A_0 represents the reported best accuracy without perturbation. The end-to-end latency is derived from a performance model developed for our BAT, which is cross-validated through RTL simulation results, taking into account memory accesses to external memory. Hardware resource consumption is obtained after synthesis to ensure the accelerator can fit within the target FPGA device. Finally, we employ an exhaustive grid search to explore all the design points under specific constraints, such as the minimal accuracy demand, and identify the Pareto-optimal set.

6 EVALUATION

6.1 Experimental Setup

Benchmarks. We follow the experimental setting of BinaryBERT [1] and BiT [21] and use the pre-trained BERT-base as our full precision baseline. The algorithmic performance is evaluated on the development set of GLUE [35], a widely adopted benchmark across a diverse set of language understanding tasks.

Software Implementation. We train and test our BMT using PyTorch v1.10.1. Following BinaryBERT [1], we obtain the half-sized full precision models from DynaBERT [12]. We adopt LSQ quantization [8] for the half-sized ternary model and elastic quantization for the full-sized binarized model. Nvidia RTX 3090 GPU is used for training. Following BinaryBERT, the hidden dimension size and intermediate dimension size are set to 384 and 1536, respectively for our BMT, termed full-size.

Hardware Implementation. We implement our BAT hardware accelerator using SystemVerilog on Xilinx ZCU102 FPGA board and

Table 4: Results on the GLUE Development Set

Quant	#Bits (E-W-A) [†]	Size (MB)	FLOPs (G) [‡]	MNLI _{m/mm}	QQP	QNLI	SST-2	CoLA	STS-B	MRPC	RTE	Avg.
BERT [6]	32-32-32	418	22.5	84.9/85.5	91.4	92.1	93.2	59.7	90.1	86.3	72.2	83.9
Q-BERT [30]	2-8-8	43.0	6.5	76.6/77.0	-	-	84.6	-	-	68.3	52.7	-
Q2BERT [40]	2-8-8	43.0	6.5	47.2/47.3	67.0	61.3	80.6	0	4.4	68.4	52.7	47.7
TernaryBERT [43]	2-2-8	28.0	6.4	83.3/83.3	90.1	-	-	50.7	-	87.5	68.2	-
BinaryBERT [1]	1-1-8	16.5	3.1	84.2/84.7	91.2	91.5	92.6	53.4	88.6	85.5	72.2	82.7
BinaryBERT [1]	1-1-4	16.5	1.5	83.9/84.2	91.2	90.9	92.3	44.4	87.2	83.3	65.3	79.9
BiT [21]	1-1-4	13.4	1.5	83.6/84.4	87.8	91.3	91.5	42.0	86.3	86.8	66.4	79.5
BMT	1-1-4	16.8	1.5	83.2/83.3	91.0	90.4	92.4	49.7	83.5	87.5	67.1	80.9
BinaryBERT [1]	1-1-2	16.5	0.8	62.7/63.9	79.9	52.6	82.5	14.6	6.5	78.3	52.7	41.0
BiT [21]	1-1-2	13.4	0.8	82.1/82.5	87.1	89.3	90.8	32.1	82.2	78.4	58.1	75.0
BMT	1-1-2	16.8	0.8	81.2/81.5	90.0	88.3	91.5	37.4	71.4	82.1	61.7	76.1
BiT [21]	1-1-1	13.4	0.4	79.5/79.4	85.4	86.4	89.9	32.9	72.0	79.9	62.1	73.5

[†] The E-W-A notation refers to the quantization bit width of embeddings, weights, and activations.

[‡] The FLOPs is calculated followed by the same approach as BinaryBERT [1] and the input sequence length is set to 128.

evaluate it for BinaryBERT [1], BiT [21] and our BMT on the MRPC task in the GLUE benchmark to obtain the end-to-end latency. The running frequency is set to 200 MHz, and Xilinx Vivado 2022.2 is used for synthesis and implementation. Power consumption values are obtained using the Xilinx Power Estimator (XPE) tool. We use 16-bit half-precision floating-point (FP16) numbers to process the full precision operations in the quantization-dequantization computational flow of BMT to ensure model accuracy.

6.2 Algorithmic Performance

We compare our BMT with five existing quantized Transformer models: Q-BERT [30], Q2BERT [40], TernaryBERT [43], BinaryBERT [1], and BiT [21], as well as the full precision pre-trained BERT as the baseline. TABLE 4 presents the main results on the GLUE benchmark. Compared with SOTA binarized Transformers, our proposed BMT improves the average performance by 1.0% and 1.1% in W1A4 and W1A2 quantization configuration, respectively. Notably, compared to the full-precision baseline, our W1A4 BMT retains competitive performance with a significant reduction of model size and computation up to 25× and 15×, respectively, demonstrating significant acceleration potential for edge deployment.

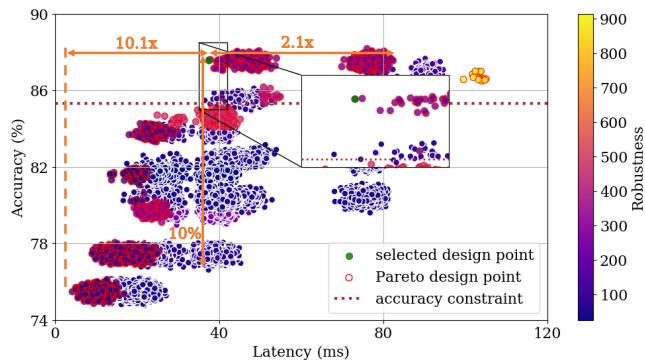


Figure 10: Design points of co-optimization on MRPC dataset.

6.3 Effectiveness of Co-optimization

We then evaluate the effectiveness of our co-design method in finding the Pareto-optimal configurations in both algorithm and hardware aspects. The MRPC dataset is used for demonstration purposes. The design space is presented in Table 3, and we constrain

the total hardware resource consumption to be less than 80% of the available FPGA resources to facilitate implementation.

Fig. 10 illustrates the trade-off between accuracy, robustness, and latency. The red circles indicate the Pareto optimal points. The brown dashed line represents the accuracy constraint, set at a maximum loss of 1% compared to the full-precision BERT-base model. We also set the robustness constraint of exceeding the upper quartile. Among Pareto optimal points satisfying the constraints, we select the one with the lowest latency. The results demonstrate that our co-designed solution achieves up to 10% higher accuracy than other design points within the same latency range and is 2.1× faster than those with similar accuracy, all while maintaining comparable robustness. The resulting optimal configurations for the MRPC dataset are:

- <model type, d_{hid} , d_{inter} , b_{act} > = <BMT, 384, 1536, 4>;
- < p_{dpu} , p_{quan} , p_{vu} , p_{ln} > = <16, 128, 32, 8> for MHA module;
- < p_{dpu} , p_{quan} , p_{vu} , p_{ln} > = <16, 128, 96, 8> for FFN module.

These configurations will be used for the evaluation in the remaining sections unless otherwise specified.

While the selected design point is approximately 10.1× slower than the one with the absolute lowest latency, it adheres to the crucial constraints of accuracy and robustness, which are essential for real-world deployments. This global balance ensures that our system not only performs efficiently but also maintains high standards of reliability and accuracy.

6.4 Hardware Evaluation

6.4.1 Energy Efficiency. To explore the energy efficiency benefits of binarized Transformers, we choose 10 commonly quantized network configurations and deploy their corresponding *activation × weight* QMM on our QMM Engine. The size of QMM is set to (128, 768) × (768, 768). As shown in Fig. 11, the binarized Transformer configuration, where weights are quantized to 1-bit, achieves significantly lower energy consumption compared to other configurations by 2~8× under the same activation precision.

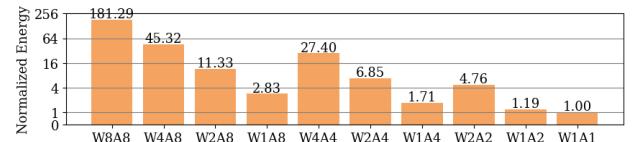


Figure 11: Normalized energy consumption for QMM under different quantization precisions.

Table 5: Comparison of BAT with Prior Arts and Commercial Products

Platform	CPU		GPU	FPGA				
	Intel i9-9900X	AMD EPYC 7302		FTRANS [18]	STA [10]	ViA [36]	FQ-BERT [20]	BAT
Technology	14nm	7nm	8nm	16nm	28nm	16nm	16nm	16nm
Frequency (Hz)	3.5G	3.0G	1.7G	170M	200M	300M	214M	200M
Test Network	BMT	BMT	BMT	BCM-based Compressed RoBERTa	N:M Sparse Shallow Transformer	Swin Transformer	FQBERT	BMT
Throughput (GOPS)	196.73	148.88	413.10	101.80	523.81	309.60	22.74	1122.40
Power (W)	165.00	155.00	350.00	25.06	9.87	39.00	9.80	5.47
Energy Eff. (GOPS/W)	1.19	0.96	1.18	4.06	55.16	7.94	2.32	207.70

6.4.2 Hardware Consumption. TABLE 6 presents the FPGA resource consumption and power breakdown of BAT. Due to its bit-wise operations, the QMM Engine is not efficiently mapped to DSP units and primarily relies on LUT resources. Notably, the QMM Engine consumes a modest 10.90% of the total power consumption, highlighting the effectiveness of our optimization for matrix multiplication. The DSP usage within the Quantization Unit stems from the floating-point bias adders and coefficient multipliers. Other components, mainly consisting of floating-point operations and on-chip buffer, consume 69.19% of the total power consumption, indicating a potential bottleneck for further energy optimization.

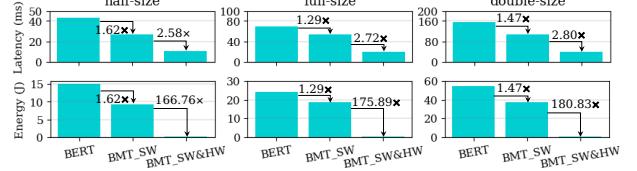
Table 6: FPGA Resource Consumption & Power Breakdown

	LUT	FF	BRAM	DSP	Power (W)
MHA QMM Engine	37338 (25.49%)	13725 (10.02%)	-	-	0.298 (5.45%)
FFN QMM Engine	37330 (25.49%)	13702 (10.00%)	-	-	0.298 (5.45%)
Quantization Unit	13952 (9.53%)	29952 (21.87%)	-	256 (25%)	1.088 (19.01%)
Others	57845 (39.49%)	79594 (58.11%)	114 (100.00%)	768 (75%)	3.781 (69.19%)
Total	146465 (100.00%)	136973 (100.00%)	114 (100.00%)	1024 (100.00%)	5.465 (100.00%)
Available	274080	548160	912	2520	-

6.4.3 Overall System Evaluation. TABLE 5 compares our BAT with SOTA FPGA-based end-to-end Transformer accelerators, as well as commercial CPU and GPU products, in terms of throughput and energy consumption. To adapt to the mini-batch feature at the edge, the batch size on CPU and GPU is set to 2. The quantization-dequantization scheme is adopted on GPU, where the QMM is implemented in high-performance CUDA kernel. Our proposed BAT significantly outperforms other FPGA-based accelerators, achieving 2.14~49.37× improvement in throughput and 3.72~88.53× improvement in energy efficiency. Compared to CPU and GPU implementations, BAT demonstrates up to 7.54× and 2.72× speedup, and 213.82× and 174.01× improvement in energy efficiency, respectively.

6.5 Ablation Study

Fig. 12 evaluates the contributions of our algorithm and hardware design via an ablation study. We first evaluate both BERT-base and

**Figure 12: Speedup and energy reduction of algorithm and hardware optimizations.**

BMT under three configurations, i.e. half-size, full-size, and double-size on the NVIDIA RTX 3090 GPU to validate the performance improvement brought by our algorithm. The results demonstrate a 1.29~1.62× speedup and energy savings. We further evaluate the BMT model on our BAT accelerator under the same configuration. Compared to the optimized GPU implementation, BAT achieves a 2.58~2.80× speedup and a 166.76~180.83× energy reduction. These results demonstrate the effectiveness of our co-design approach.

7 CONCLUSION

The paper proposes the end-to-end acceleration of binarized Transformer via algorithm-hardware co-design enabling efficient edge deployment. From algorithm aspects, we propose BMT, a hardware-friendly binarized Transformer model that achieves a substantial compression ratio while maintaining high accuracy compared to the full precision baseline. From hardware aspects, we propose BAT, a streaming-processor-mixed binarized Transformer accelerator equipped with highly optimized computational units and dataflows, which enables efficient end-to-end inference for binarized Transformers. Moreover, algorithm and hardware design parameters are jointly optimized to push the performance boundaries under real-world constraints from accuracy, latency, and robustness. Experimental results show our co-design yields up to 2.14~49.37× 3.72~88.53× improvement on throughput and energy efficiency, respectively, over the state-of-the-art Transformer accelerators.

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REFERENCES

- [1] Haoli Bai, Wei Zhang, et al. 2021. BinaryBERT: Pushing the Limit of BERT Quantization. In *Proceedings of the 59th Annual Meeting of the Association for Computational Linguistics and the 11th International Joint Conference on Natural Language Processing (ACL/IJCNLP)*. ACL, 4334–4348.
- [2] Tom B. Brown, Benjamin Mann, et al. 2020. Language Models are Few-Shot Learners. In *Advances in neural information processing systems (NeurIPS)*.
- [3] Vincent Camus, Linyan Mei, et al. 2019. Review and Benchmarking of Precision-Scalable Multiply-Accumulate Unit Architectures for Embedded Neural-Network Processing. *IEEE J. Emerg. Sel. Topics Circuits Syst.* 9, 4 (2019), 697–711.
- [4] Jialin Cao, Xuanda Lin, et al. 2023. PP-Transformer: Enable Efficient Deployment of Transformers Through Pattern Pruning. In *IEEE/ACM International Conference on Computer Aided Design (ICCAD)*. IEEE, 1–9.
- [5] Tim Dettmers, Mike Lewis, et al. 2022. LLM.int8(0): 8-bit Matrix Multiplication for Transformers at Scale. *CoRR* abs/2208.07339 (2022).
- [6] Jacob Devlin, Ming-Wei Chang, et al. 2019. BERT: Pre-training of Deep Bidirectional Transformers for Language Understanding. In *Proceedings of the North American Chapter of the Association for Computational Linguistics: Human Language Technologies (NAACL-HLT)* (1). Association for Computational Linguistics, 4171–4186.
- [7] Alexey Dosovitskiy, Lucas Beyer, et al. 2021. An Image is Worth 16x16 Words: Transformers for Image Recognition at Scale. In *International Conference on Learning Representations (ICLR)*.
- [8] Steven K. Effer, Jeffrey L. McKinstry, et al. 2020. Learned Step Size quantization. In *International Conference on Learning Representations (ICLR)*. OpenReview.net.
- [9] Hongxiang Fan, Thomas Chau, et al. 2022. Adaptable Butterfly Accelerator for Attention-based NNs via Hardware and Algorithm Co-design. In *IEEE/ACM International Symposium on Microarchitecture (MICRO)*. IEEE, 599–615.
- [10] Chao Fang, Aojun Zhou, et al. 2022. An Algorithm-Hardware Co-Optimized Framework for Accelerating N:M Sparse Transformers. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems (TVLSI)* 30, 11 (2022), 1573–1586.
- [11] Tae Jun Ham, Sungjun Jung, et al. 2020. A³: Accelerating Attention Mechanisms in Neural Networks with Approximation. In *IEEE International Symposium on High Performance Computer Architecture (HPCA)*. IEEE, 328–341.
- [12] Lu Hou, Zhiqi Huang, et al. 2020. DynaBERT: Dynamic BERT with Adaptive Width and Depth. In *Advances in Neural Information Processing Systems (NeurIPS)*.
- [13] Hang Hua, Xingjian Li, et al. 2021. Noise Stability Regularization for Improving BERT Fine-tuning. In *Proceedings of the North American Chapter of the Association for Computational Linguistics: Human Language Technologies (NAACL-HLT)*.
- [14] Longwei Huang, Chao Fang, et al. 2024. A Precision-Scalable RISC-V DNN Processor with On-Device Learning Capability at the Extreme Edge. In *Asia and South Pacific Design Automation Conference (ASP-DAC)*. IEEE, 927–932.
- [15] Itay Hubara, Matthieu Courbariaux, et al. 2016. Binarized Neural Networks. In *Advances in neural information processing systems (NeurIPS)*, Vol. 29. Curran Associates, Inc.
- [16] Minsik Kim, Kyoungseok Oh, et al. 2024. A Low-Latency FPGA Accelerator for YOLOv3-Tiny With Flexible Layerwise Mapping and Dataflow. *IEEE Transactions on Circuits and Systems I: Regular Papers (TCAS-I)* 71, 3 (2024), 1158–1171.
- [17] Schoon Kim, Amit Gholami, et al. 2021. I-BERT: Integer-only BERT Quantization. In *Proceedings of International Conference on Machine Learning (ICML)* (*Proceedings of Machine Learning Research*), Vol. 139. PMLR, 5506–5518.
- [18] Bingbing Li, Santosh Pandey, et al. 2020. FTRANS: energy-efficient acceleration of Transformers using FPGA. In *Proceedings of the ACM/IEEE International Symposium on Low Power Electronics and Design (ISLPED)*. ACM, 175–180.
- [19] Zhihai Li and Qingyi Gu. 2023. I-ViT: Integer-only Quantization for Efficient Vision Transformer Inference. In *IEEE/CVF International Conference on Computer Vision (ICCV)*. IEEE, 17019–17029.
- [20] Zejian Liu, Gang Li, et al. 2021. Hardware Acceleration of Fully Quantized BERT for Efficient Natural Language Processing. In *Design, Automation & Test in Europe Conference (DATE)*. IEEE, 513–516.
- [21] Zechun Liu, Barlas Ooguz, et al. 2022. BiT: Robustly Binarized Multi-distilled Transformer. In *Advances in neural information processing systems (NeurIPS)*, Vol. 35. 14303–14316.
- [22] Zechun Liu, Baoyuan Wu, et al. 2018. Bi-Real Net: Enhancing the Performance of 1-Bit CNNs with Improved Representational Capability and Advanced Training Algorithm. In *European Conference on Computer Vision (ECCV)* (15), Vol. 11219. Springer, 747–763.
- [23] Siyuan Lu, Meiqi Wang, et al. 2020. Hardware Accelerator for Multi-Head Attention and Position-Wise Feed-Forward in the Transformer. In *IEEE International System-on-Chip Conference (SOCC)*. IEEE, 84–89.
- [24] Duy Thanh Nguyen, Hyun Kim, et al. 2021. Layer-Specific Optimization for Mixed Data Flow With Mixed Precision in FPGA Design for CNN-Based Object Detectors. *IEEE Transactions on Circuits and Systems for Video Technology (TCSVT)*. 31, 6 (2021), 2450–2464.
- [25] Junki Park, Hyunsung Yoon, et al. 2020. OPTIMUS: OPTImized matrix MULTIpliCATION Structure for Transformer neural network accelerator. In *Proceedings of Machine Learning and Systems (MLSys)*. mlsys.org.
- [26] Haotong Qin, Yifu Ding, et al. 2022. BiBERT: Accurate Fully Binarized BERT. In *International Conference on Learning Representations (ICLR)*.
- [27] Jiantao Qiu, Jie Wang, et al. 2016. Going Deeper with Embedded FPGA Platform for Convolutional Neural Network. In *International Symposium on Field-Programmable Gate Arrays (ISFPGA)*. ACM, 26–35.
- [28] Mohammad Rastegari, Vicente Ordóñez, et al. 2016. XNOR-Net: ImageNet Classification Using Binary Convolutional Neural Networks. In *European Conference on Computer Vision (ECCV)* (4), Vol. 9908. Springer, 525–542.
- [29] Haikuo Shao, Huihong Shi, et al. 2024. An FPGA-Based Reconfigurable Accelerator for Convolution-Transformer Hybrid EfficientViT. *CoRR* abs/2403.20230 (2024).
- [30] Sheng Shen, Zhen Dong, et al. 2020. Q-BERT: Hessian Based Ultra Low Precision Quantization of BERT. In *Proceedings of AAAI Conference on Artificial Intelligence (AAAI)*. AAAI Press, 8815–8821.
- [31] HongRui Song, Ya Wang, et al. 2022. UCViT: Hardware-Friendly Vision Transformer via Unified Compression. In *IEEE International Symposium on Circuits and Systems (ISCAS)*. IEEE, 2022–2026.
- [32] Jiayi Tian, Chao Fang, et al. 2023. BEBERT: Efficient and robust binary ensemble BERT. In *IEEE International Conference on Acoustics, Speech and Signal Processing (ICASSP)*. IEEE, 1–5.
- [33] Fengbin Tu, Weiwei Wu, et al. 2020. Evolver: A deep learning processor with on-device quantization–voltage–frequency tuning. *IEEE Journal of Solid-State Circuits (JSSC)* 56, 2 (2020), 658–673.
- [34] Quang Hieu Vo, Linh Ngoc Le, et al. 2022. A Deep Learning Accelerator Based on a Streaming Architecture for Binary Neural Networks. *IEEE Access* 10 (2022), 21141–21159.
- [35] Alex Wang, Amanpreet Singh, et al. 2019. GLUE: A Multi-Task Benchmark and Analysis Platform for Natural Language Understanding. In *International Conference on Learning Representations (ICLR)*.
- [36] Teng Wang, Lei Gong, et al. 2022. ViA: A Novel Vision-Transformer Accelerator Based on FPGA. *IEEE Trans. Comput. Aided Des. Integr. Circuits Syst. (TCAD)* 41, 11 (2022), 4088–4099.
- [37] Xiao Wu, Shuang Liang, et al. 2023. ReAFM: A Reconfigurable Nonlinear Activation Function Module for Neural Networks. *IEEE Transactions on Circuits and Systems II: Express Briefs* 70, 7 (2023), 2660–2664.
- [38] Yuzhuang Xu, Xu Han, et al. 2024. OneBit: Towards Extremely Low-bit Large Language Models. *CoRR* abs/2402.11295 (2024).
- [39] Xin Yang and Tao Su. 2022. EFA-Trans: An Efficient and Flexible Acceleration Architecture for Transformers. *Electronics* 11, 21 (2022).
- [40] Ofir Zafir, Guy Boudoukh, et al. 2019. Q8bert: Quantized 8bit bert. In *Fifth Workshop on Energy Efficient Machine Learning and Cognitive Computing-NeurIPS Edition (EMC2-NIPS)*. IEEE, 36–39.
- [41] Min Zhang, Linpeng Li, et al. 2019. Optimized Compression for Implementing Convolutional Neural Networks on FPGA. *Electronics* 8, 3 (2019).
- [42] Susan Zhang, Stephen Roller, et al. 2022. OPT: Open Pre-trained Transformer Language Models. *CoRR* abs/2205.01068 (2022).
- [43] Wei Zhang, Lu Hou, et al. 2020. TernaryBERT: Distillation-aware Ultra-low Bit BERT. In *Proceedings of the 2020 Conference on Empirical Methods in Natural Language Processing (EMNLP)*. ACL, 509–521.