Slides for lecture 6

CE/CZ 3001:
Advanced Computer Architecture

(Module 3: Data-path and Control Design)

Single-cycle datapath design of I , CB and B type instructions

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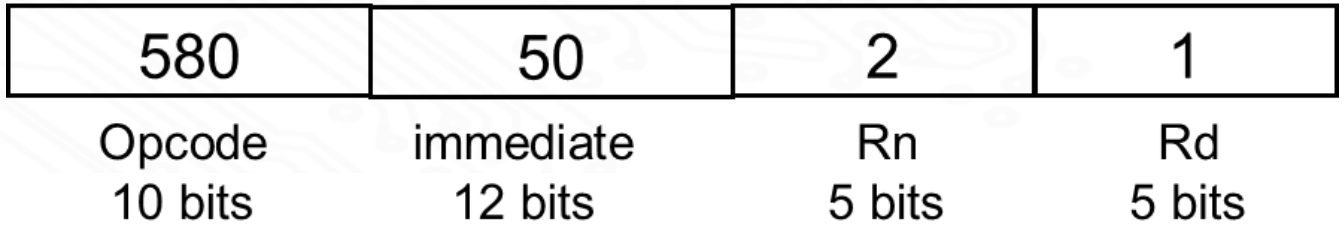
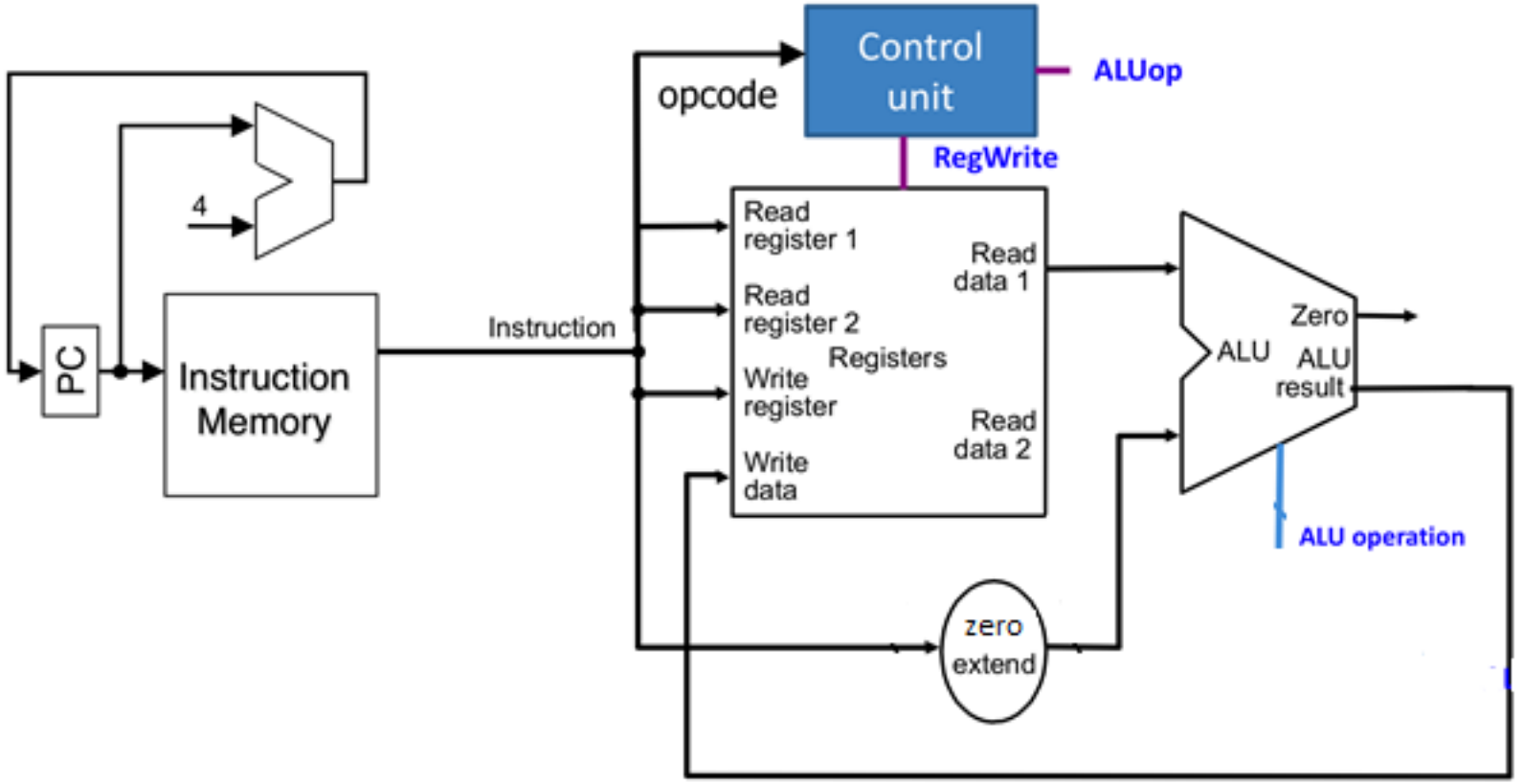
Outline

- Single-cycle datapath design
  - R-type
  - D-type
  - Combined R and D type
  - I-type
  - CB- type
  - Combined R, D, I and CB type
  - B type
  - Combined R, D, I , CB and B type

Datapath for I type – Immediate addressing



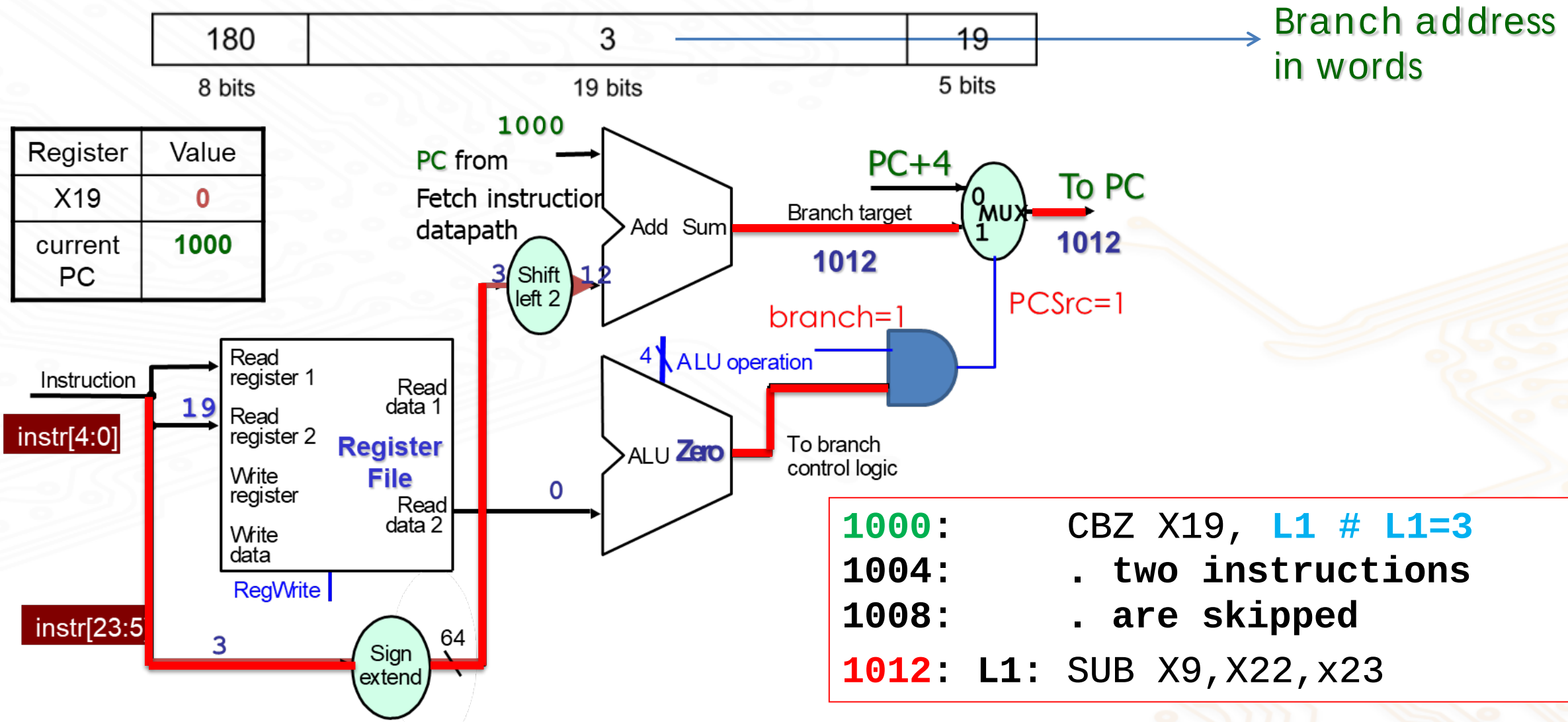
Register	Value
X2	30



ADDI X1, X2, #50
meaning([X1] ← [X2]+ 50])

Adapted from *Computer organization and design: the hardware/software interface*, by D. A. Patterson, J. L. Hennessy & P. Alexander, 2015, Amsterdam: Morgan Kaufmann.

Datapath for CB type – Branch instruction




```
1000:      CBZ X19, L1 # L1=3
1004:      . two instructions
1008:      . are skipped
1012: L1:  SUB X9,X22,x23
```

Adapted from *Computer organization and design: the hardware/software interface* , ARM edition, by D. A. Patterson, J. L. Hennessy & P. Alexander, 2015, Amsterdam: Morgan Kaufmann

Datapath for R , D, I and CB type Instructions

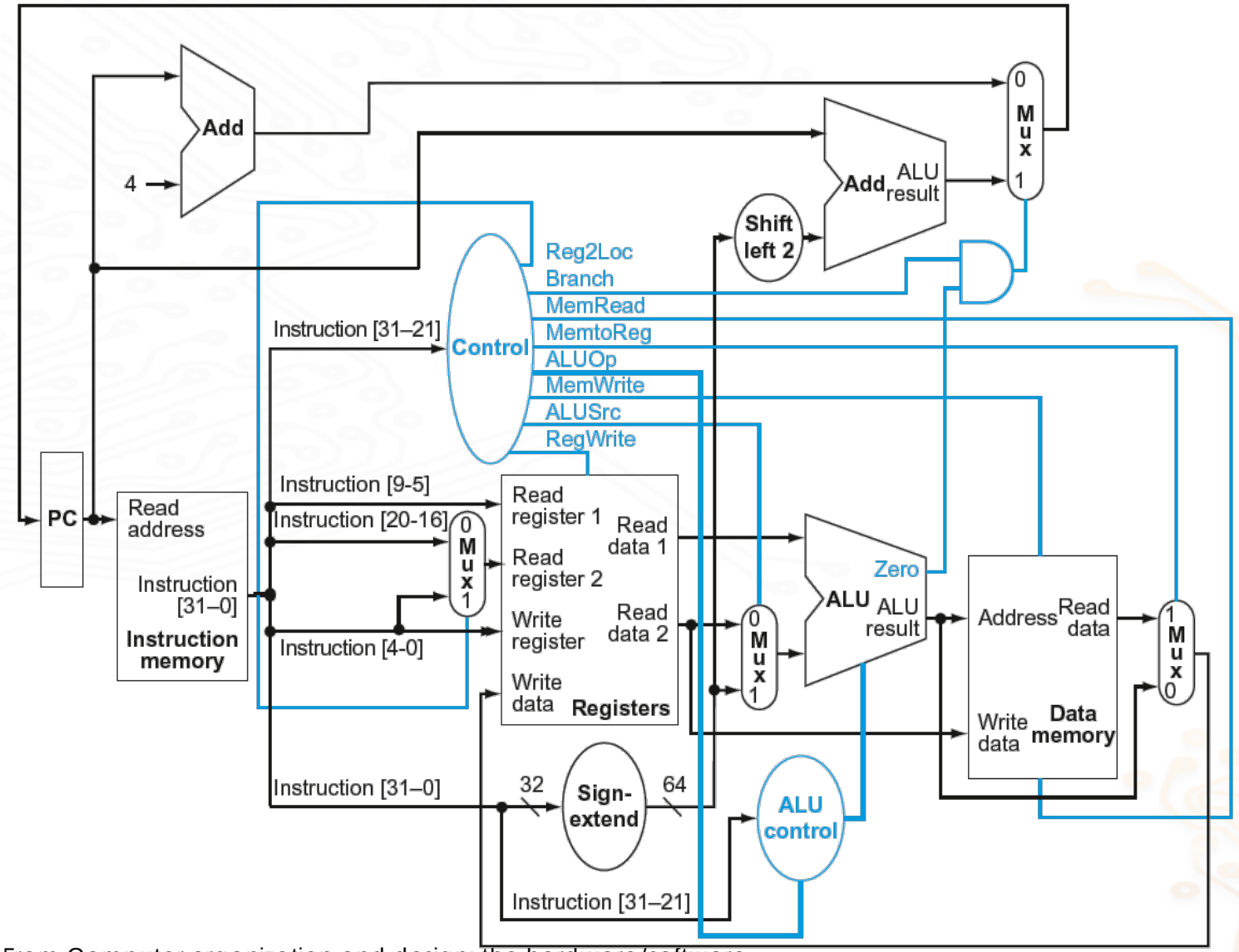
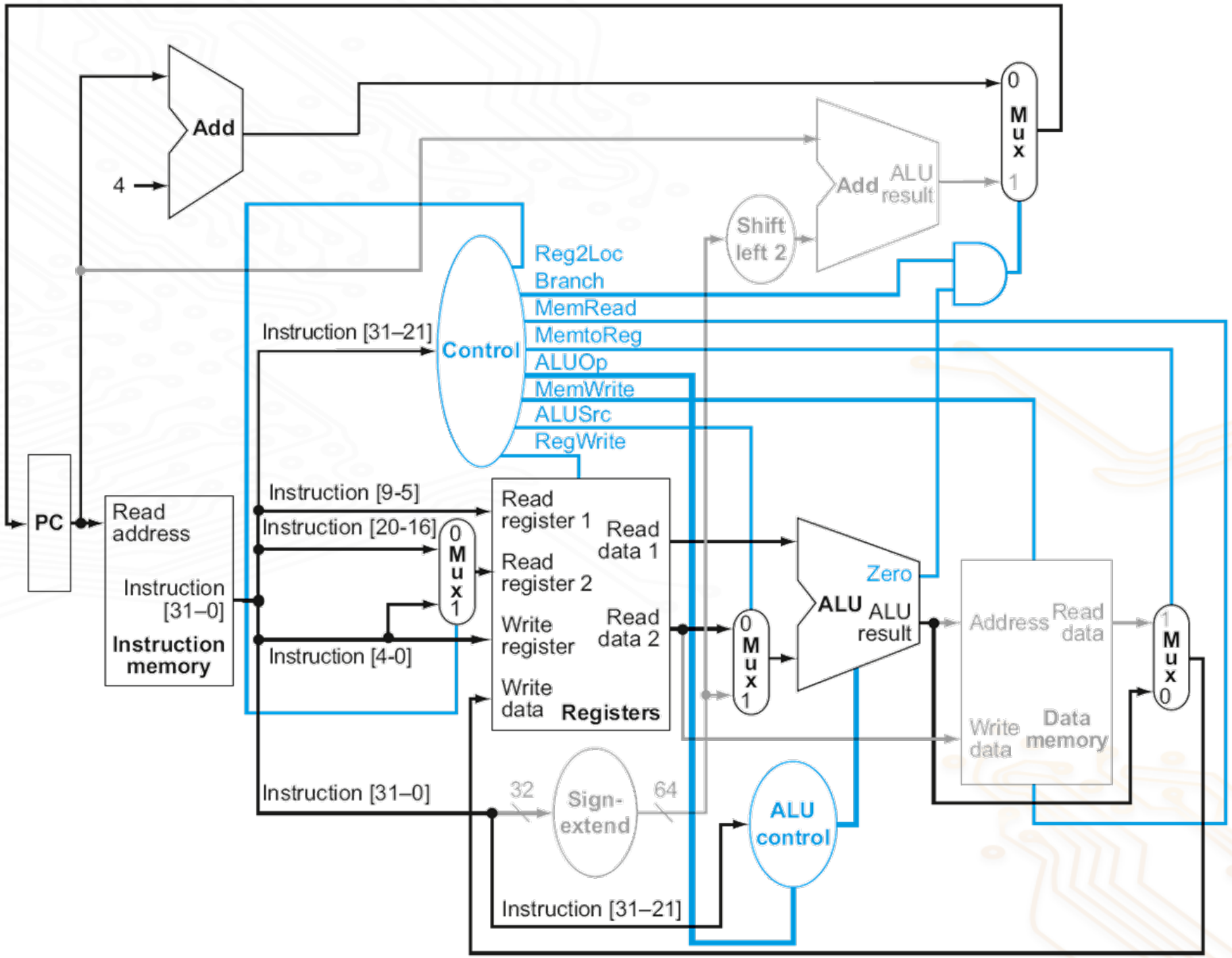
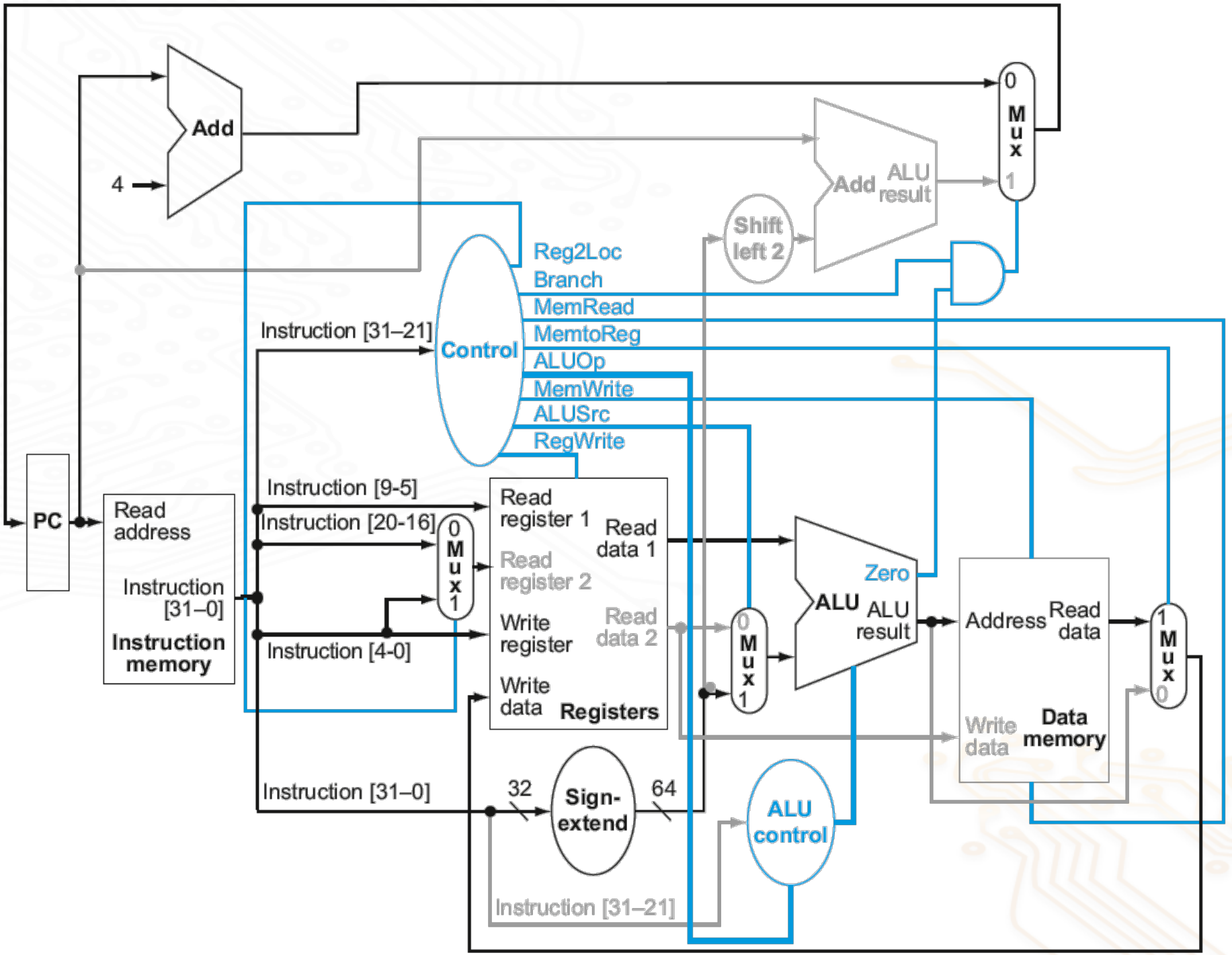


Figure 4.15, page 359 From Computer organization and design: the hardware/software interface ARM edition, by D. A. Patterson, J. L. Hennessy & P. Alexander, 2017 Amsterdam: Morgan Kaufmann.

R-type datapath



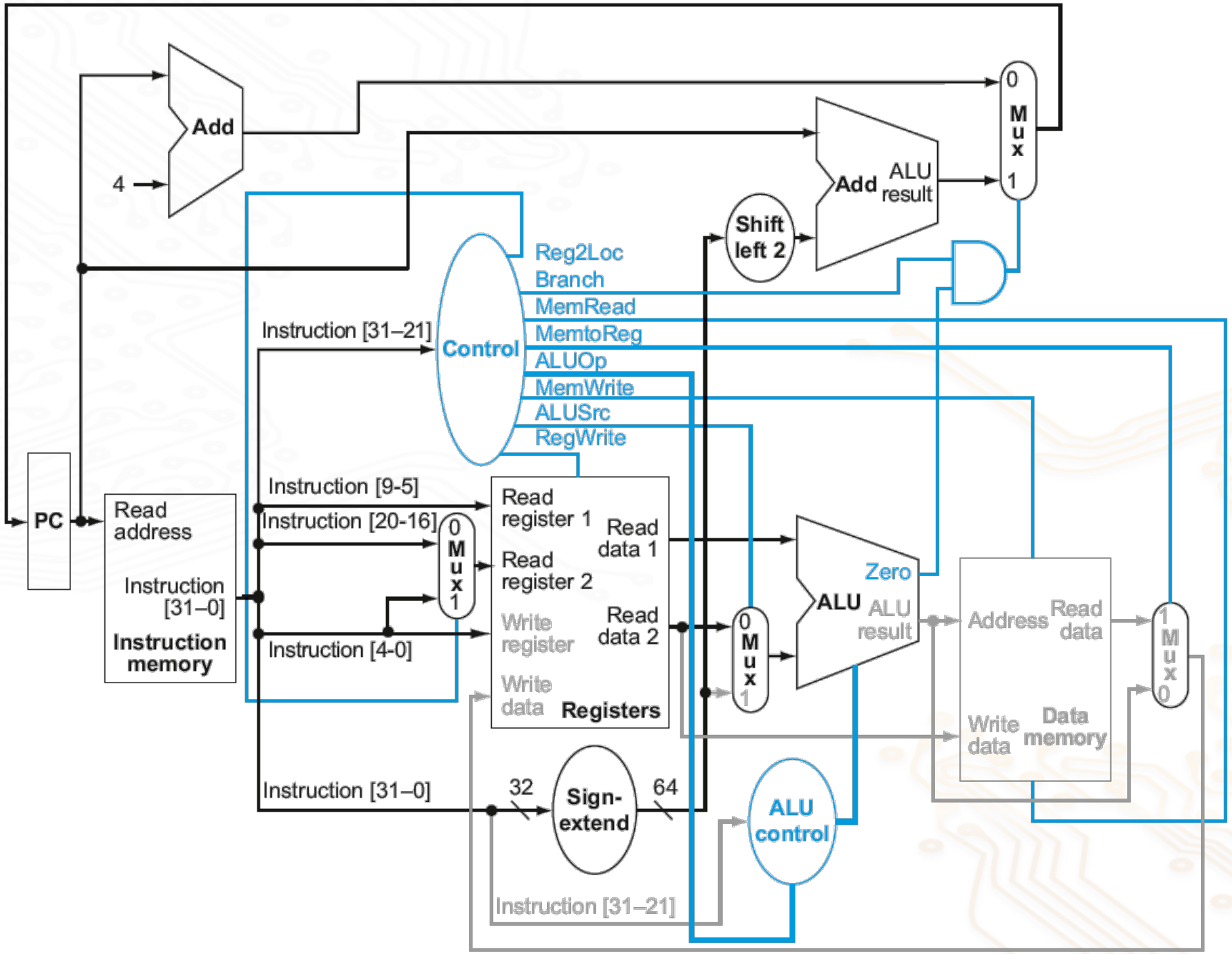
Load (D-type) datapath



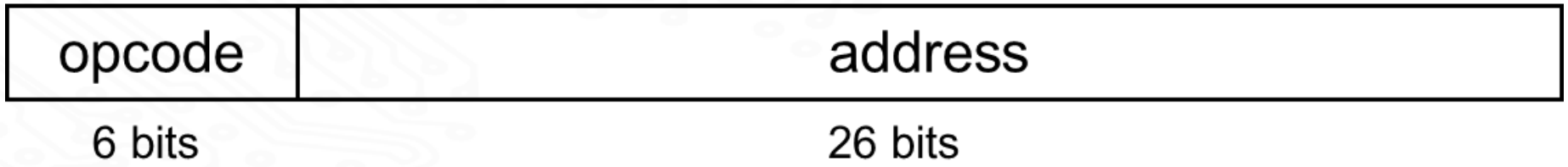
CBZ

(CB-type)

datapath

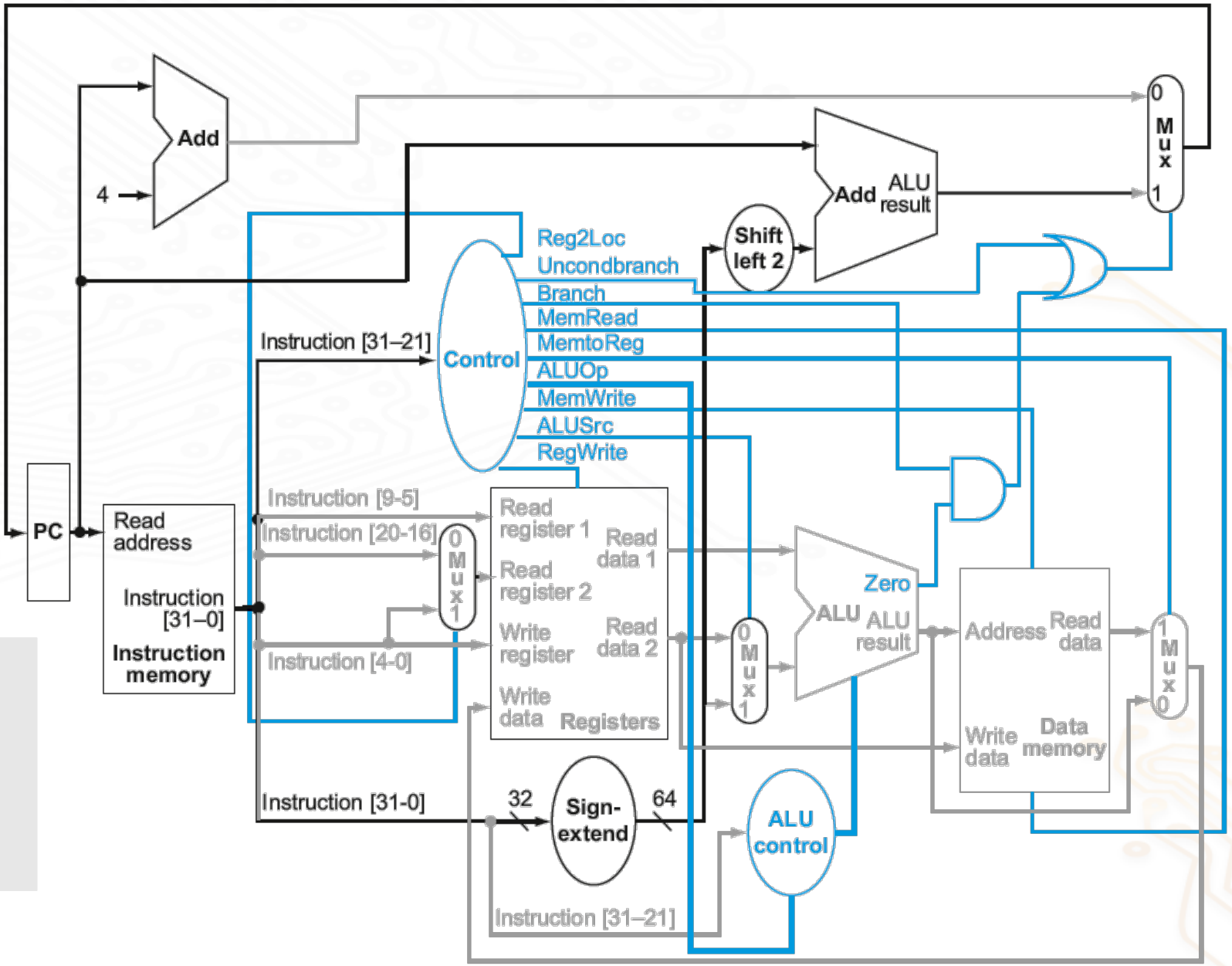


Implementing Un-Conditional Branch Instructions



- Branch uses word address
  - 26-bit unconditional Branch address
  - Left shift by 2 (or add “00” to LSB)
  - Add with PC
- Need an extra control signal decoded from opcode

Complete Datapath including B Instructions



B

(B-type)

datapath

Summary of creating an architecture

- Combine all into a single architecture
  - Using mux with control signals
- Five steps finishes in a single clock cycle
  - Step 1: Instruction Fetch
  - Step 2: Instruction Decode and Register Fetch
  - Step 3: Execution, Memory Address Computation, or Branch Completion
  - Step 4: Memory Access or R-type instruction completion
  - Step 5: Write-back step

- No functional unit can be used twice in one clock cycle
- The clock period is decided by the slowest instruction

Performance issue of single cycle architecture

- Longest delay determines clock period
  - Critical path: load instruction
  - Instruction memory → register file → ALU → data memory → register file
- Not feasible to vary period for different instructions
- Violates design principle
  - Making the common case fast
- **improve performance by pipelining**