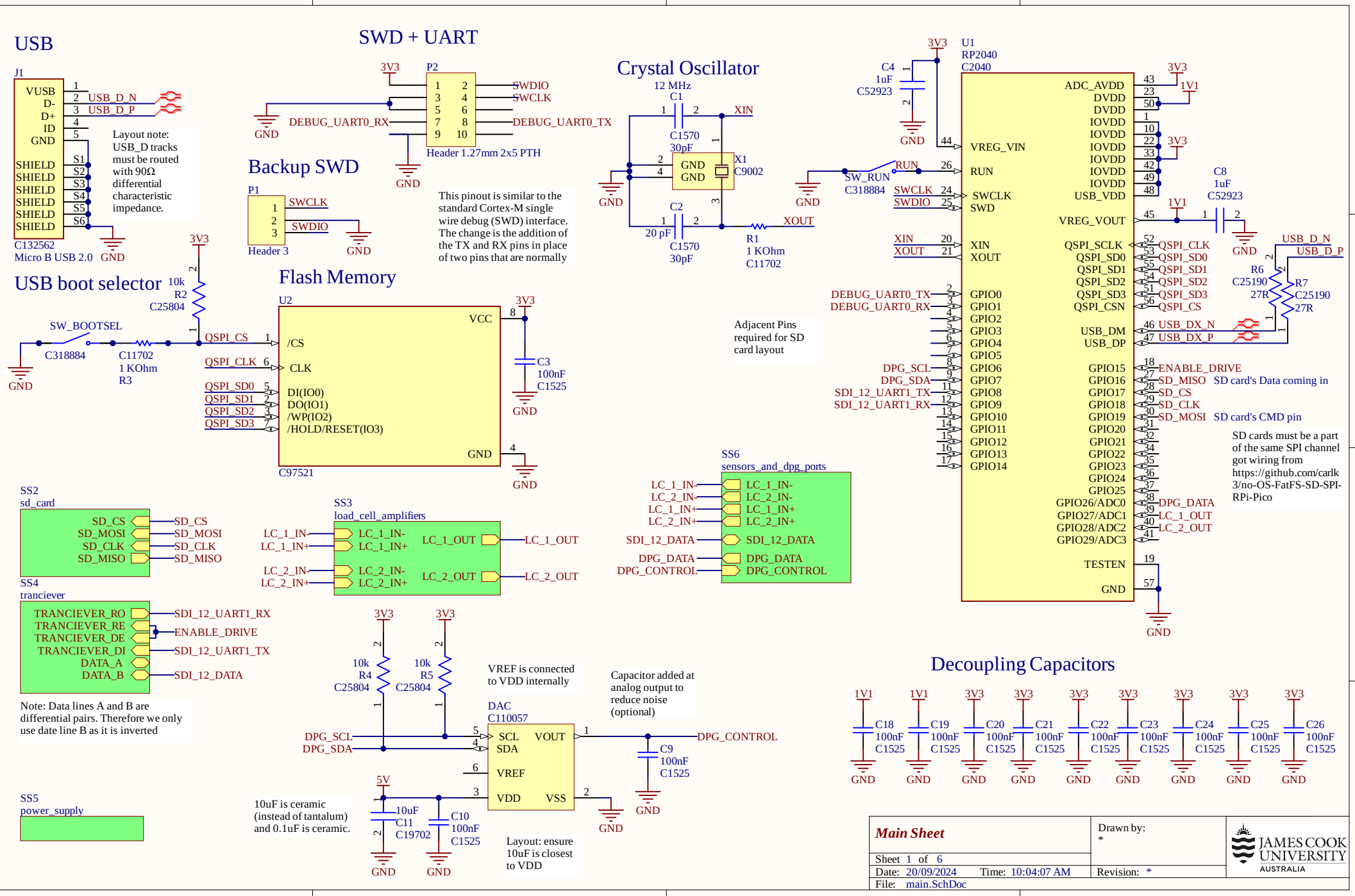
USB
J1
VUSB
D-
D+
ID
GND
SHIELD
USB_D_N
USB_D_P
Layout note: USB_D tracks must be routed with 90Ω differential characteristic impedance.
C132562
Micro B USB 2.0
SWD + UART
P2
SWDIO
SWCLK
DEBUG_UART0_RX
DEBUG_UART0_TX
Header 1.27mm 2x5 PTH
Backup SWD
P1
Header 3
This pinout is similar to the standard Cortex-M single wire debug (SWD) interface. The change is the addition of the TX and RX pins in place of two pins that are normally
Crystal Oscillator
12 MHz
C1570 30pF
X1 C9002
C2 20 pF
R1 1 KOhm C11702
XIN
XOUT
U1 RP2040 C2040
C4 1uF C52923
VREG_VIN
RUN
SW_RUN C318884
SWCLK
SWD
VREG_VOUT
C8 1uF C52923
QSPI_SCLK
QSPI_SD0
QSPI_SD1
QSPI_SD2
QSPI_SD3
QSPI_CSN
USB_DM
USB_DP
R6 C25190 27R
R7 C25190 27R
USB_VDD
ADC_AVDD
DVDD
IOVDD
GPIO0
GPIO1
GPIO2
GPIO3
GPIO4
GPIO5
GPIO6
GPIO7
GPIO8
GPIO9
GPIO10
GPIO11
GPIO12
GPIO13
GPIO14
GPIO15
GPIO16
GPIO17
GPIO18
GPIO19
GPIO20
GPIO21
GPIO22
GPIO23
GPIO24
GPIO25
GPIO26/ADC0
GPIO27/ADC1
GPIO28/ADC2
GPIO29/ADC3
TESTEN
USB boot selector
10k R2 C25804
SW_BOOTSEL
C318884
C11702 1 KOhm R3
Flash Memory
U2
/CS
CLK
DI(IO0)
DO(IO1)
/WP(IO2)
/HOLD/RESET(IO3)
VCC
C3 100nF C1525
C97521
Adjacent Pins required for SD card layout
SD cards must be a part of the same SPI channel got wiring from https://github.com/carlk3/no-OS-FatFS-SD-SPI-RPi-Pico
SS2
sd_card
SD_CS
SD_MOSI
SD_CLK
SD_MISO
SS3
load_cell_amplifiers
LC_1_IN-
LC_1_IN+
LC_1_OUT
LC_2_IN-
LC_2_IN+
LC_2_OUT
SS6
sensors_and_dpg_ports
SDI_12_DATA
DPG_DATA
DPG_CONTROL
SS4
tranciever
TRANCIEVER_RO
TRANCIEVER_RE
TRANCIEVER_DE
TRANCIEVER_DI
DATA_A
DATA_B
SDI_12_UART1_RX
ENABLE_DRIVE
SDI_12_UART1_TX
SDI_12_DATA
Note: Data lines A and B are differential pairs. Therefore we only use date line B as it is inverted
10k R4 C25804
10k R5 C25804
DAC C110057
SCL
SDA
VOUT
VREF
VDD
VSS
VREF is connected to VDD internally
Capacitor added at analog output to reduce noise (optional)
C9 100nF C1525
10uF C11 C19702
C10 100nF C1525
10uF is ceramic (instead of tantalum) and 0.1uF is ceramic.
Layout: ensure 10uF is closest to VDD
SS5
power_supply
Decoupling Capacitors
C18 100nF C1525
C19 100nF C1525
C20 100nF C1525
C21 100nF C1525
C22 100nF C1525
C23 100nF C1525
C24 100nF C1525
C25 100nF C1525
C26 100nF C1525
Main Sheet
Sheet 1 of 6
Date: 20/09/2024 Time: 10:04:07 AM
File: main.SchDoc
Drawn by: *
Revision: *
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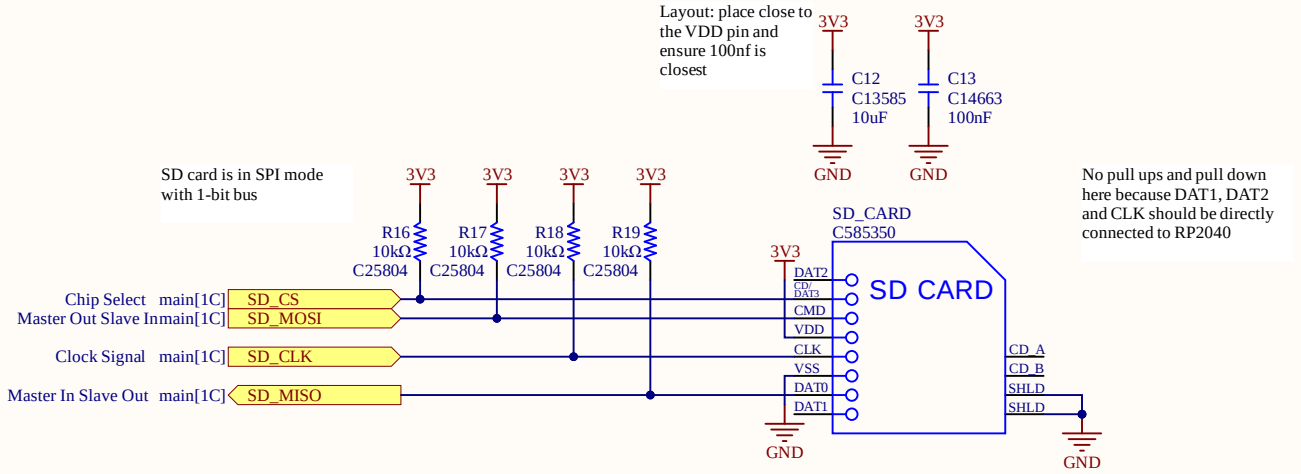
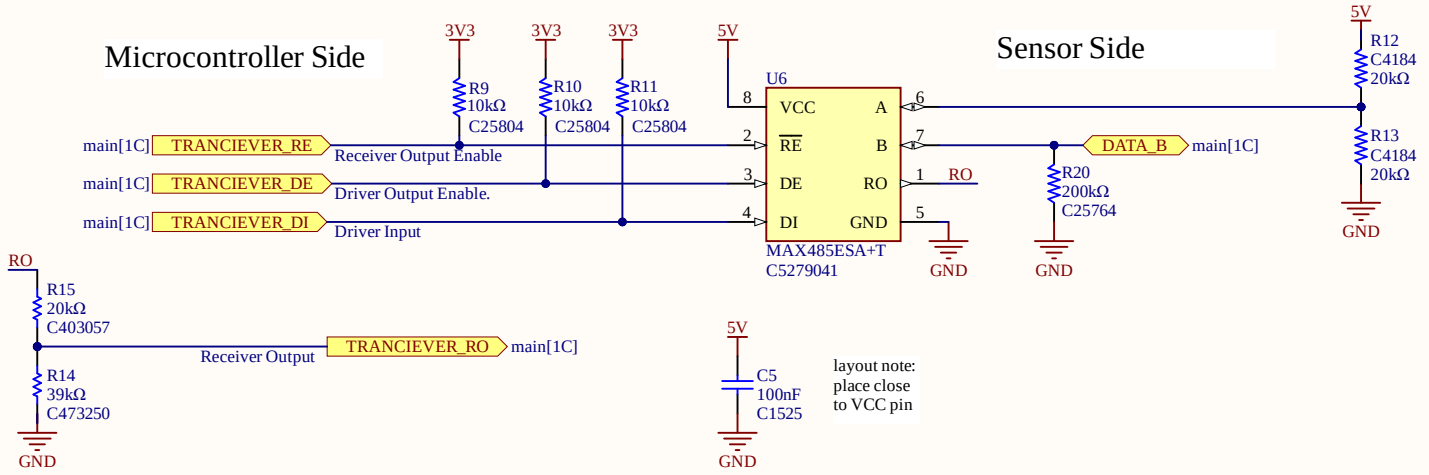


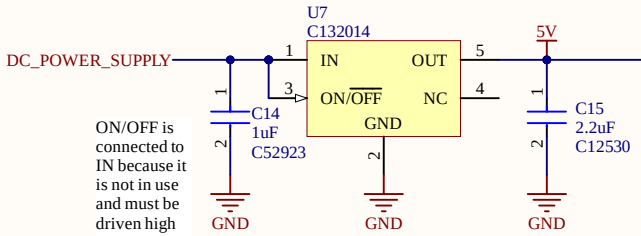
SD Card Reader Header	Drawn by: Hunter Kruger-Ilingworth	JAMES COOK UNIVERSITY AUSTRALIA
Sheet 2 of 6		
Date: 20/09/2024 Time: 10:04:07 AM	Revision: *	
File: sd_card.SchDoc		

Note: We are using the footprint of MAX485ESA+T which is identical to MAX485ESA (available on JLCPCB with JLCPCB Part no. C5279041). "T" suffix signifies that the component is supplied in tape and reel packaging.



Tranciever Circuit	Drawn by: Thomas Mehes	JAMES COOK UNIVERSITY AUSTRALIA
Sheet 3 of 6		
Date: 20/09/2024 Time: 10:04:07 AM	Revision: *	
File: tranciever.SchDoc		

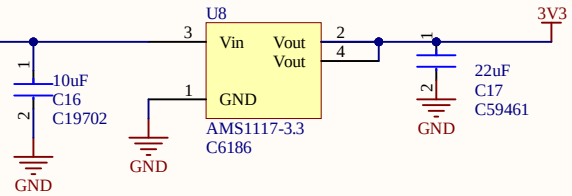
5V Regulator



ON/OFF is connected to IN because it is not in use and must be driven high

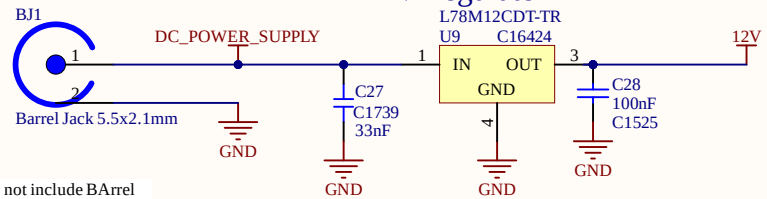
3.3V Regulator

We do not want the USB powering the board, the board needs to be able to operate without USB connection



Layout note: place these capacitors near the regulator

12V Regulator



Do not include BArrel Jack in BOM, will be using one from lab

TODO: PUT A BULK CAP

Power Circuitry	Drawn by: Quentin Bouet	JAMES COOK UNIVERSITY AUSTRALIA
Sheet 4 of 6		
Date: 20/09/2024 Time: 10:04:07 AM	Revision: *	
File: power_supply.SchDoc		

Dew Point Generator

BNC
282836-4

This terminal block will connect to bulk BNC connectors

DPG_CONTROL main[3C]
GND
GND
R21
20kΩ
C403057
DPG_DATA main[3C]
R22
39kΩ
C473250
GND

NOTE: Do not include in BOM as these will be odered through MOUSER and will be soldered on ourselves. MFR Part no. are shown here (not JLCPCB Part no.)

Sensors

H1
TB002-500-10BE

12V
12V GND SDI_12_DATA
12V GND SDI_12_DATA
main[3C], load_cell_amplifiers[2B] LC_1_IN-
main[3C], load_cell_amplifiers[2B] LC_1_IN+
GND

H2
TB002-500-10BE

12V
12V GND SDI_12_DATA
12V GND SDI_12_DATA
main[3C], load_cell_amplifiers[2C] LC_2_IN-
main[3C], load_cell_amplifiers[2C] LC_2_IN+
GND

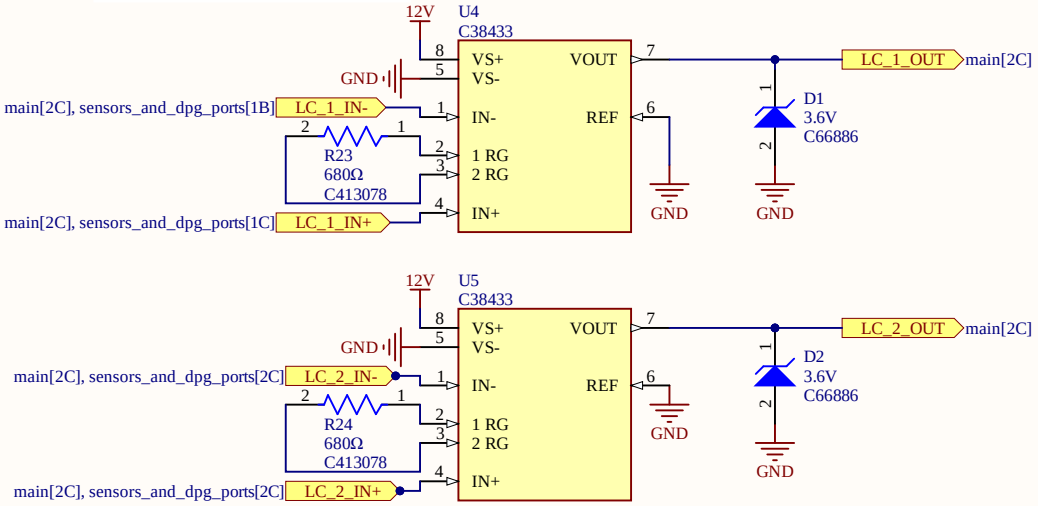
main[3C] SDI_12_DATA SDI_12_DATA

Sensor Interfacing Components	Drawn by: Quentin Boet	JAMES COOK UNIVERSITY AUSTRALIA
Sheet 5 of 6		
Date: 20/09/2024 Time: 10:04:07 AM	Revision: *	
File: sensors_and_dpg_ports.SchDoc		

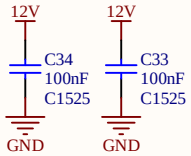
the datasheet at https://www.ti.com/lit/ds/symlink/ina826.pdf says the gain is 1 + (49400/R_G)

by my tests, the required gain to get the output to 3.3V (minus a fair bit for safety) is 150.

I am assuming that we will give alex the option of having up to 2 load cells connected. This is why I have two indstrumentation amplifiers, as one is requred for each of the load cells



Decoupling Capacitors



Load Cell Amplifier Circuitry		Drawn by: Hunter Kruger-Ilingworth
Sheet 6 of 6		
Date: 20/09/2024 Time: 10:04:07 AM		Revision: *
File: load_cell_amplifiers.SchDoc		

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