TRUE/FALSE. Write 'T' if the statement is true and 'F' if the statement is false.

1) All multivibrators require feedback. 1) _____

2) All multivibrators are level triggered. 2) _____

3) The symbol for an edge-triggered flip-flop has a triangle on its clock input. 3) _____

4) A D flip-flop is constructed by connecting an inverter between the Set and Clock terminals of a S-R flip-flop. 4) _____

5) The J-K flip-flop toggles when both inputs are high during the transition of the clock signal. 5) _____

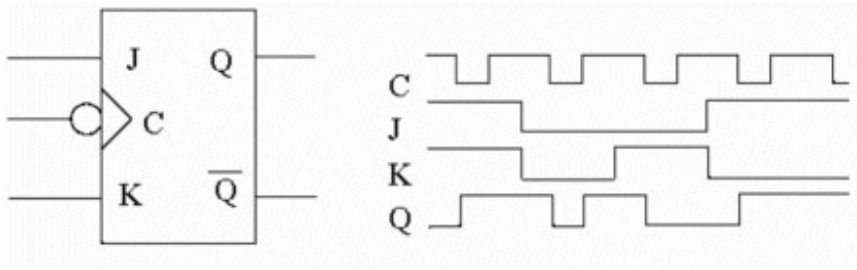
6) Preset and Clear inputs are normally synchronous. 6) _____

7) A pulse-triggered flip-flop is identified by a bubble on its Q output terminal. 7) _____

8) A one-shot is a multivibrator that must be triggered to produce each output pulse. 8) _____

9) The 555 timer has three basic operating modes: monostable, bistable, and astable. 9) _____

10) The waveforms for this J-K flip-flop indicate the circuit is operating properly. 10) _____



11) The ON time of a 555 monostable multivibrator is determined by t_W = 1.1RC. 11) _____

12) A diode can be added to the discharge path for a 555 astable multivibrator to obtain duty cycles that are less than 50%. 12) _____

MULTIPLE CHOICE. Choose the one alternative that best completes the statement or answers the question.

13) An active-HIGH input S-R latch has a 1 on the S input and a 0 on the R input. What state is the latch in? 13) _____

A) $Q = 1, \overline{Q} = 0$ B) $Q = 0, \overline{Q} = 0$ C) $Q = 1, \overline{Q} = 1$ D) $Q = 0, \overline{Q} = 1$

14) What advantage does a J-K flip-flop have over an R-S flip-flop? 14) _____

A) It does not require a clock input.
B) It has no invalid input states.
C) It has only one output.
D) It has fewer gates.

TRUE/FALSE. Write 'T' if the statement is true and 'F' if the statement is false.

15) A J-K flip-flop can be used as a divide-by-two frequency divider with an output duty cycle of 50%. 15) _____

MULTIPLE CHOICE. Choose the one alternative that best completes the statement or answers the question.

16) What is one disadvantage of an R-S flip-flop? 16) _____

A) It has no CLOCK input.
B) It has only a single output.
C) It has no Enable input.
D) It has an invalid input state.

17) How is the invalid input state problem associated with the S-R flip-flop overcome? 17) _____
A) The R terminal is eliminated. B) The R input is fed through an inverter.
C) A single input terminal is used (D). D) Both B and C are correct.

18) Which of the following is correct for a gated D latch? 18) _____
A) Only one of the inputs can be high at a time.
B) Q output follows the input D when the ENABLE is high.
C) The output complement follows the input when enabled.
D) The output toggles if one of the inputs is held high.

19) What symbol is used to identify edge-triggered flip-flops? 19) _____
A) An inverted "L" on the output B) A bubble on the Clock input
C) A triangle on the Clock input D) The letter E on the Enable input

20) An edge-triggered flip-flop must have _____. 20) _____
A) a pulse transition detector
B) active-low inputs and complemented outputs
C) at least two inputs to handle rising and falling edges
D) a very fast response time

21) Which of the following describes the operation of a positive edge-triggered D flip-flop? 21) _____
A) If both inputs are high, the output will toggle.
B) When both inputs are low, an invalid state will exist.
C) The input is toggled into the flip-flop on the leading edge of the clock and is passed to the output on the trailing edge of the clock.
D) The output will follow the input on the leading edge of the clock.

22) What primary advantage does the J-K flip-flop have over the S-R flip-flop? 22) _____
A) The J-K flip-flop does not have propagation delay problems.
B) The J-K flip-flop only needs one output.
C) The J-K flip-flop does not have an invalid input state.
D) The J-K flip-flop is much faster.

23) If both inputs of an S-R flip-flop are low, what happens when the clock goes high? 23) _____
A) An invalid state is produced. B) The output resets.
C) The output toggles. D) No change occurs in the output.

24) Asynchronous inputs are best described as _____. 24) _____
A) having full control over the FF, regardless of the input or clock states
B) being tied to the inputs, but independent of the clock
C) having little or no control over the FF, except during the active clock input
D) being tied to the clock, but not to the inputs

25) The asynchronous inputs to a flip-flop are normally labeled _____ and _____, and are normally active _____ inputs. 25) _____
A) SET, RESET, high B) PRE, CLR, low
C) START, STOP, low D) ON, OFF, high

26) Which of the following best describes the action of pulse-triggered flip-flops? 26) _____
A) A pulse on the clock transfers data from input to output.
B) The synchronous inputs must be pulsed.

C) The clock and R-S inputs must be pulse shaped.
D) The data is entered on the leading edge of the clock, and transferred out on the trailing edge of the clock.

27) When both inputs of a J-K pulse-triggered FF are high, and the clock cycles, the output will _____. 27) _____
A) remain unchanged B) not change
C) toggle D) be invalid

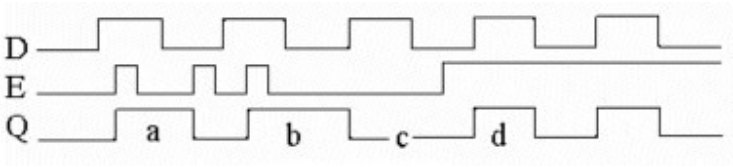
28) The L in 74L71 stands for _____. 28) _____
A) low frequency B) lock-out flip-flop
C) low power D) the type of package

29) Which of the following is a primary characteristic of the data lock-out flip-flop? 29) _____
A) Data cannot be entered into the FF unless the EN line is high.
B) Data can only be entered when the clock is high.
C) Data is only clocked into the FF on the clock transition.
D) The master section is a pulse triggered type FF.

30) Which of the following ratings is NOT associated with flip-flops? 30) _____
A) Propagation delay time B) Interval time
C) Set-up time D) Hold time

31) Set-up time specifies _____. 31) _____
A) how long the operator has in order to get the flip-flop running before the maximum power level is exceeded
B) how long it takes the output to change states after the clock has transitioned
C) the minimum time required for the control levels to be maintained at the inputs of a flip-flop prior to the triggering edge of the clock in order for data to be reliably clocked into the component
D) the maximum time interval required for the control levels to remain on the inputs before the triggering edge of the clock in order for the data to be reliably clocked out of the FF

32) These waveforms are applied to a gated D latch, which is initially RESET. Which of the areas identified on the Q waveform is incorrect? 32) _____



A) Area a B) Area b C) Area c D) Area d

33) Flip-flops are normally used for all of the following applications, except _____. 33) _____
A) data storage B) frequency division
C) counting D) logic gates

34) A J-K flip-flop is being used as a divide-by-2 circuit when _____. 34) _____
A) the J and K inputs are tied to ground B) the reset is tied to the clock
C) the J and K inputs are tied to Vcc D) all the inputs are connected to the preset

35) A one-shot is classified as a(n) _____. 35) _____
A) astable multivibrator B) one-pulse multivibrator

C) monostable multivibrator D) bistable multivibrator

36) A retriggerable one-shot has a pulse width of 10 ms. Three milliseconds (3 ms) after being triggered, another trigger pulse is applied. The duration of the resulting output pulse will be _____ ms. 36) _____

A) 13 B) 7 C) 3 D) 10

37) An astable multivibrator is a circuit that _____. 37) _____

A) has two stable states B) has one stable state

C) produces a continuous output signal D) Both B and C are correct.

38) A push-button switch is used to input data to a register. The output of the register is erratic. Which of the following could be the cause of the problem? 38) _____

A) The register IC is intermittent and failure is imminent.

B) The socket contacts on the register IC are corroded.

C) The switch contacts are bouncing.

D) The power supply is probably noisy.

39) A positive edge-triggered J-K flip-flop is used to produce a two-phase clock. However, when the circuit is operated it produces erratic results. Close examination with an oscilloscope reveals the presence of glitches. What might be the source of these glitches? 39) _____

A) A race condition exists between the Q and $\overline{Q}$ outputs to the AND gate.

B) A race condition exists between the J and K inputs.

C) A race condition exists between the CLOCK and the outputs of the flip-flop feeding the AND gate.

D) The PRESET and CLEAR terminals may have been left floating.