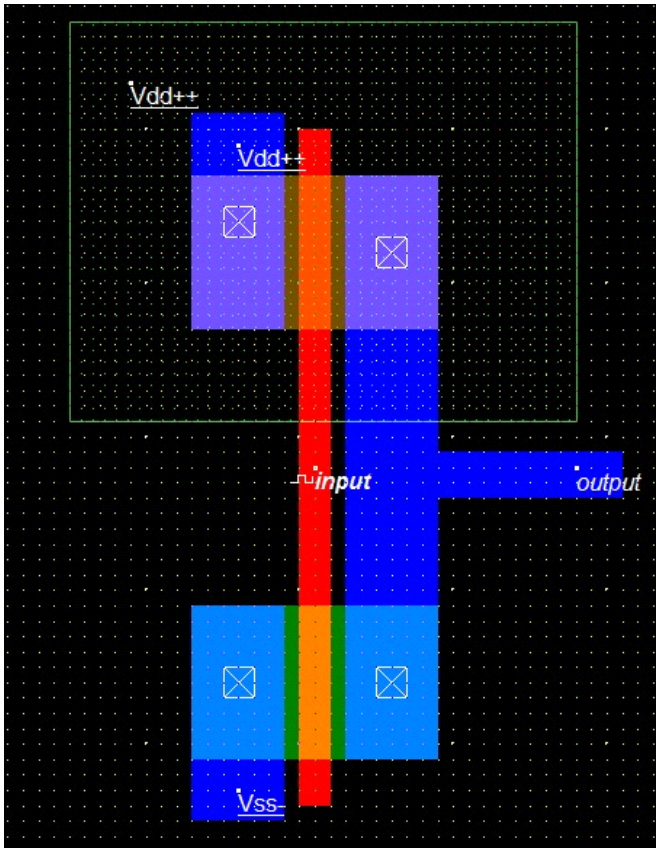
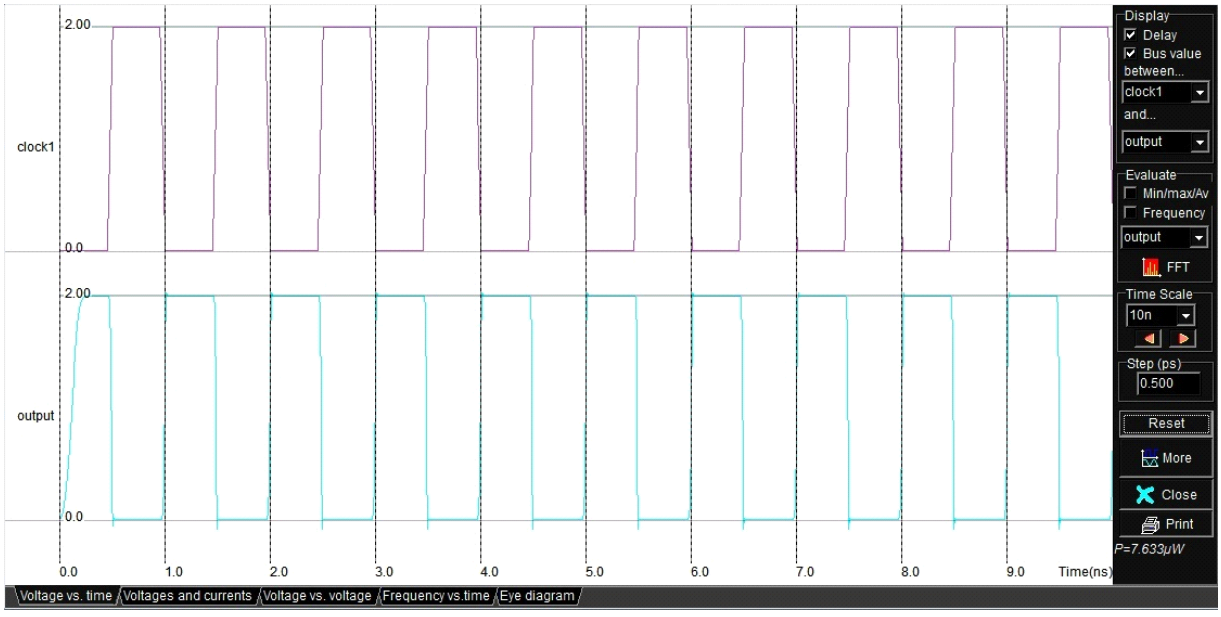
Part A: Wp=Wn=1 µm , Ln=Lp=0.2 µm

Design Layout & Timing Diagram of CMOS Inverter

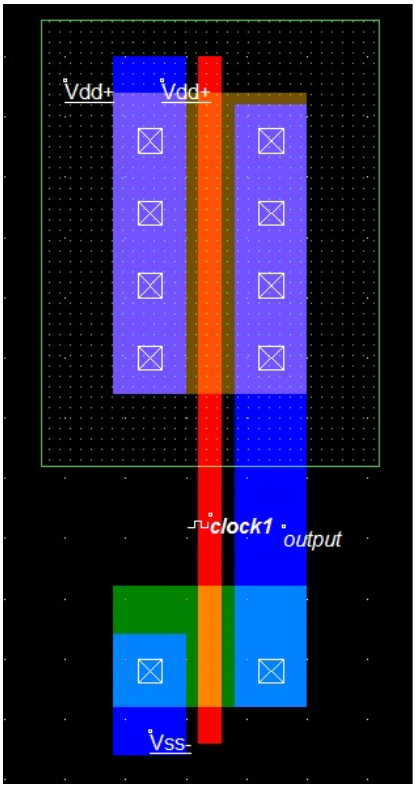


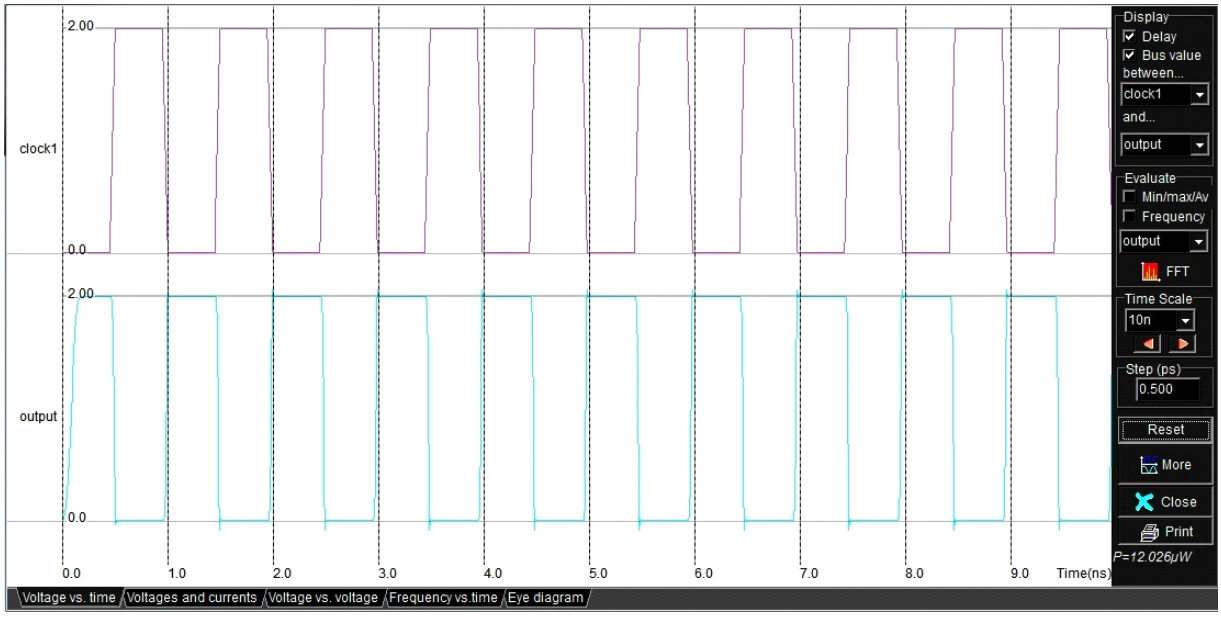


NAME OF THE STUDENT:
CLASSS:
ROLL NUMBER:

Part B: Wp=2.5Wn (Wn=1 µm) , Ln=Lp=0.2 µm

Design Layout & Timing Diagram of CMOS Inverter

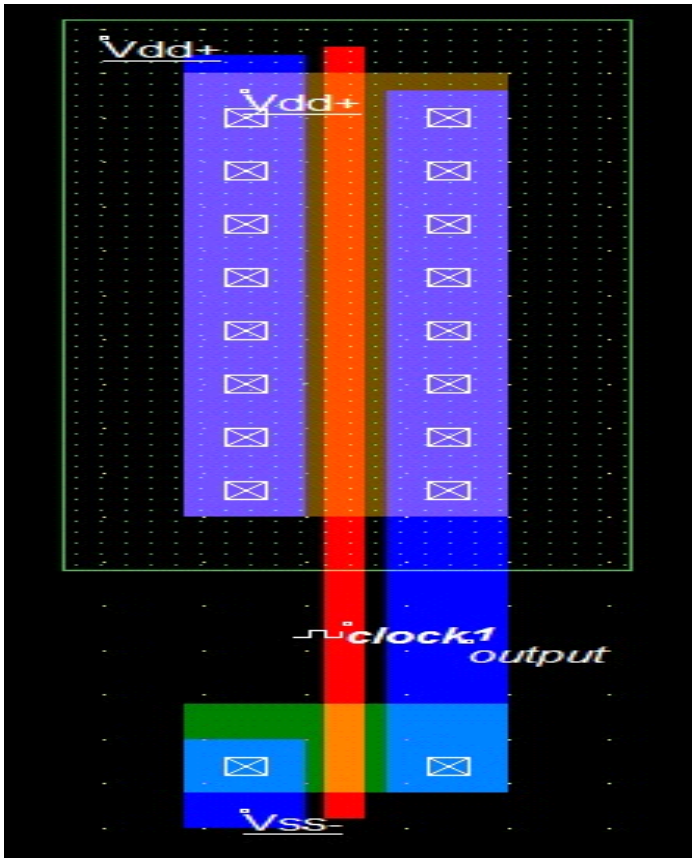


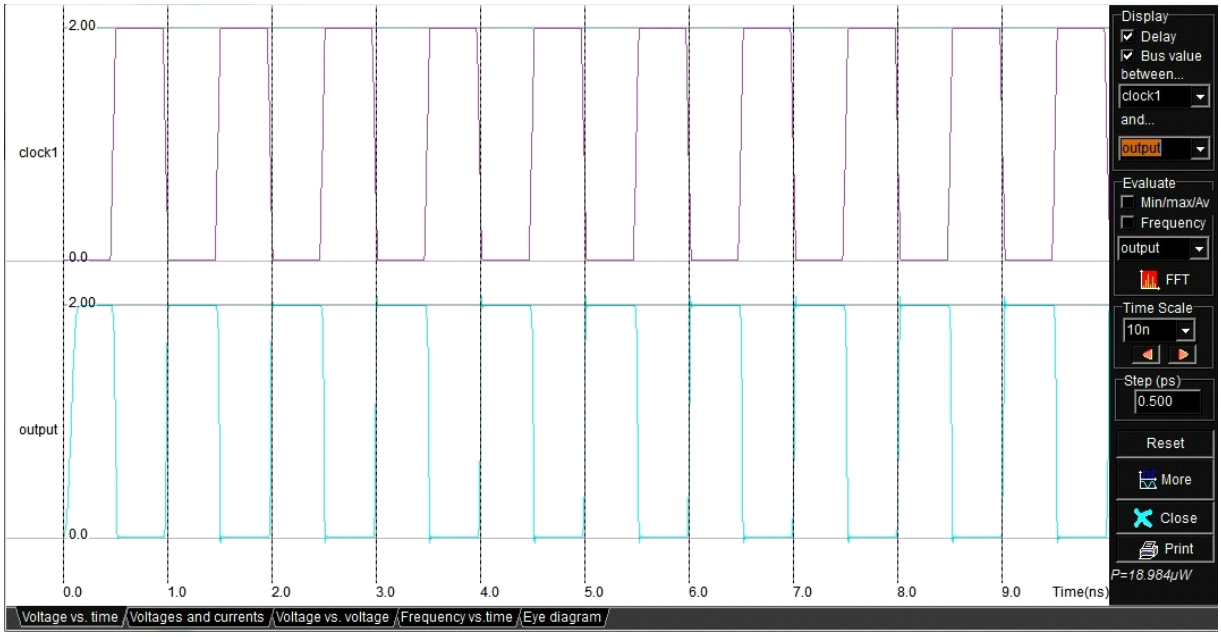


NAME OF THE STUDENT:
CLASSS:
ROLL NUMBER:

Part C: Wp=5Wn (Wn=1 µm) , Ln=Lp=0.2 µm

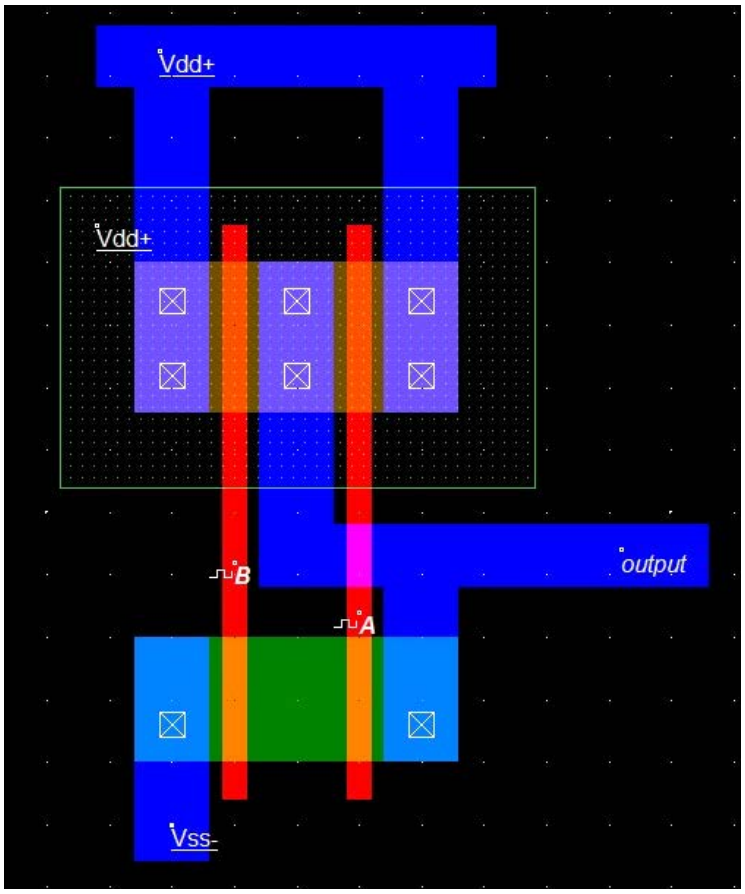
Design Layout & Timing Diagram of CMOS Inverter

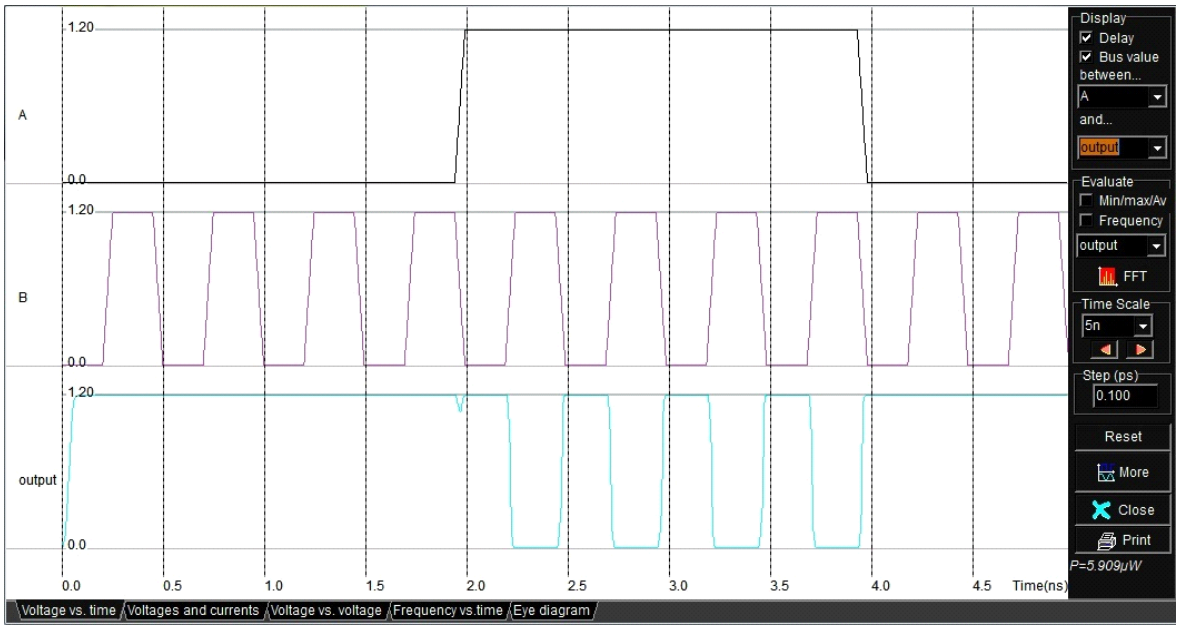




NAME OF THE STUDENT:
CLASSS:
ROLL NUMBER:

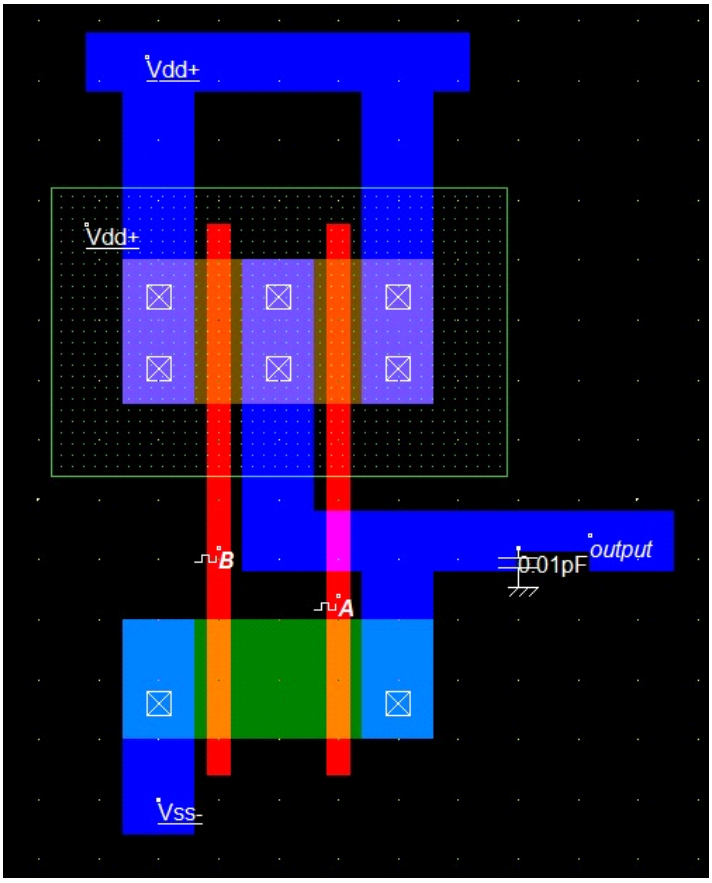
Part A: Design Layout & Timing Diagram of CMOS NAND Gate without capacitor

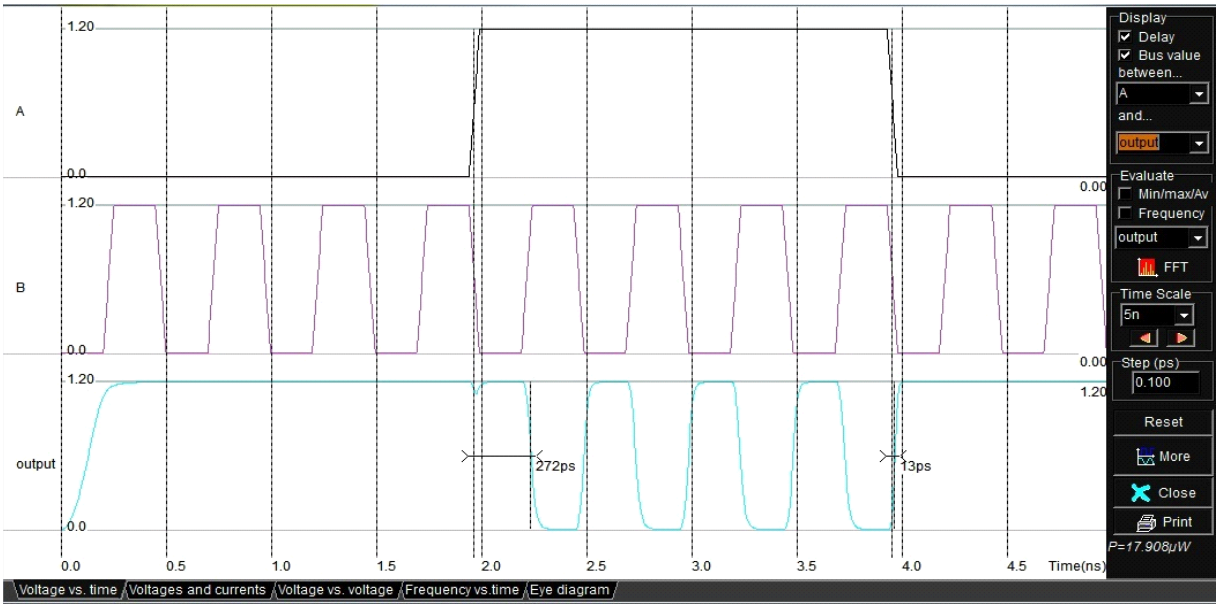




NAME OF THE STUDENT:
CLASSS:
ROLL NUMBER:

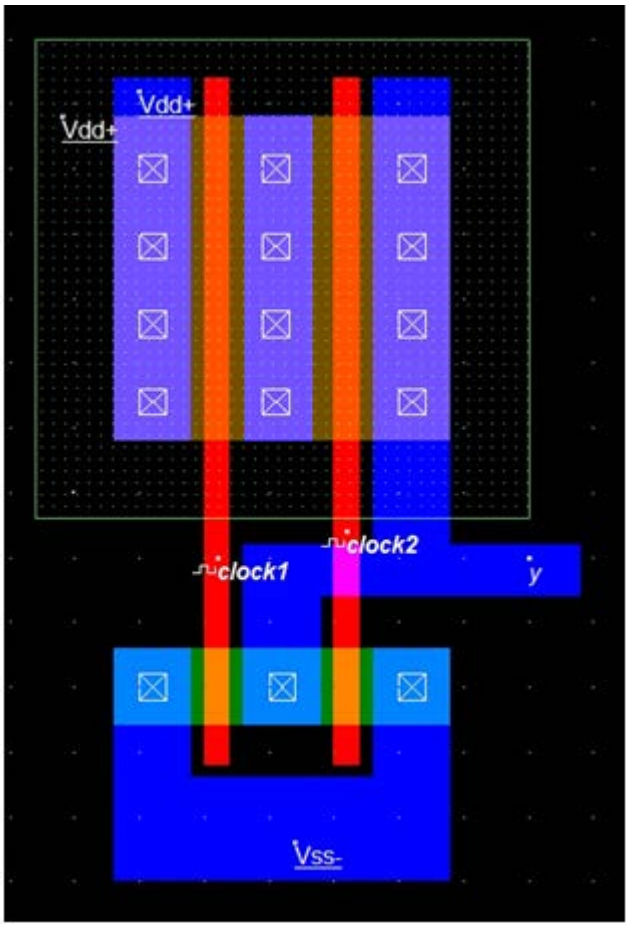
Part B: Design Layout & Timing Diagram of CMOS NAND Gate with capacitor

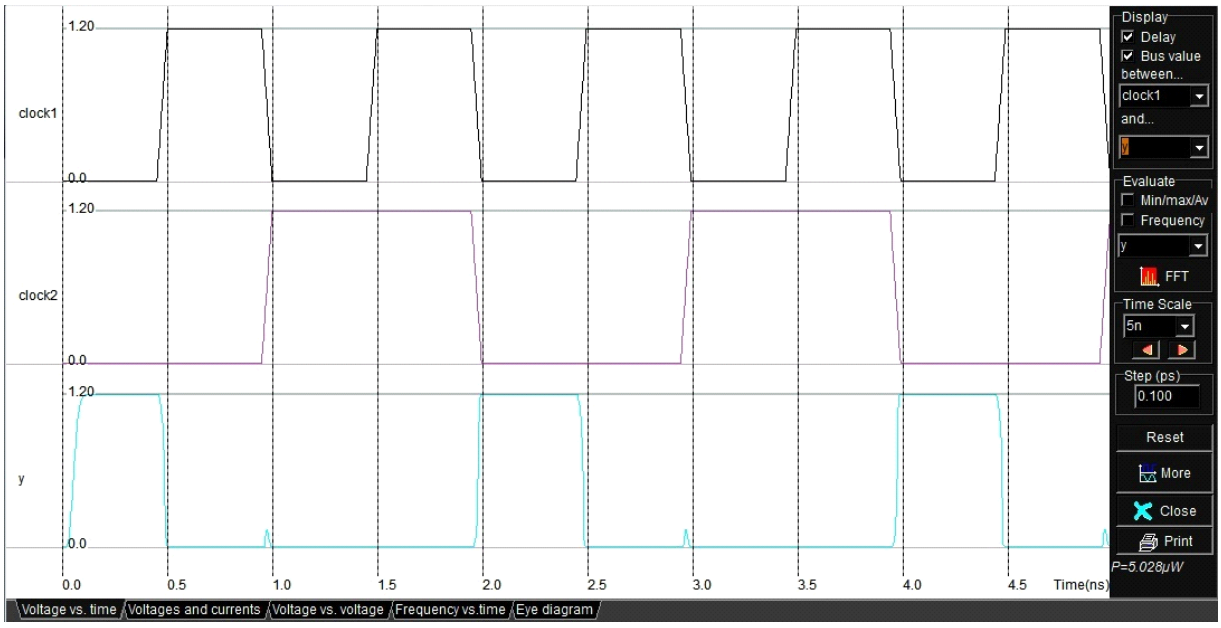




NAME OF THE STUDENT:
CLASSS:
ROLL NUMBER:

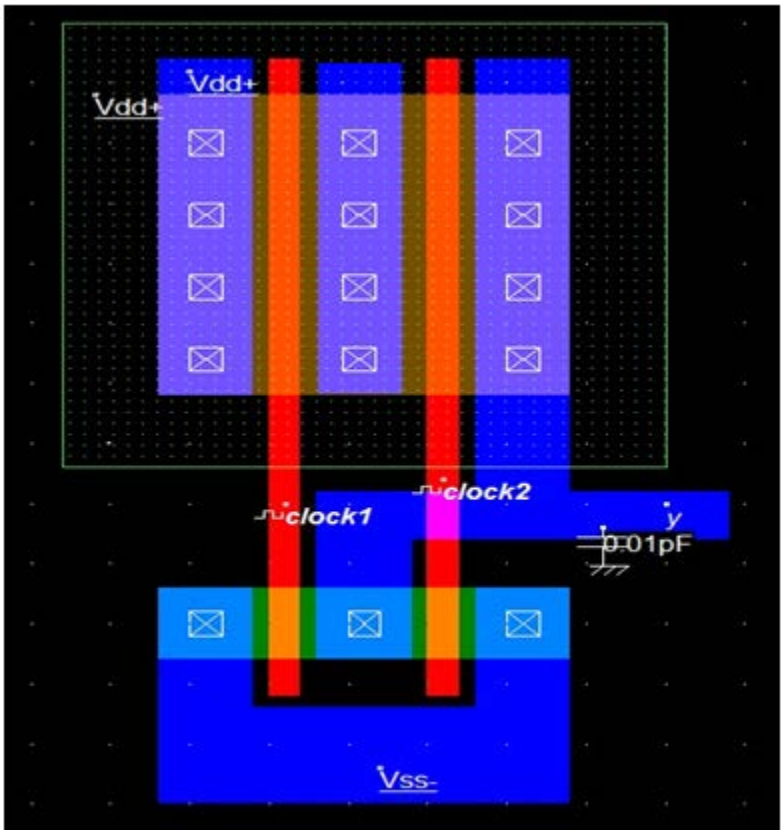
Part A: Design Layout & Timing Diagram of CMOS NOR Gate without capacitor

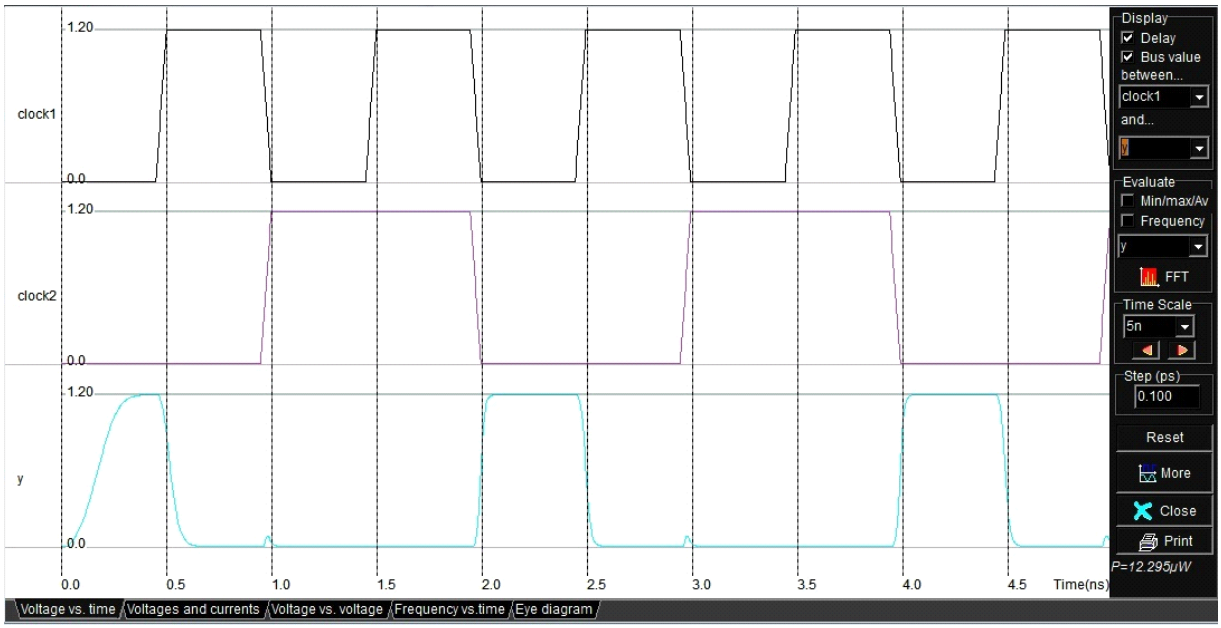




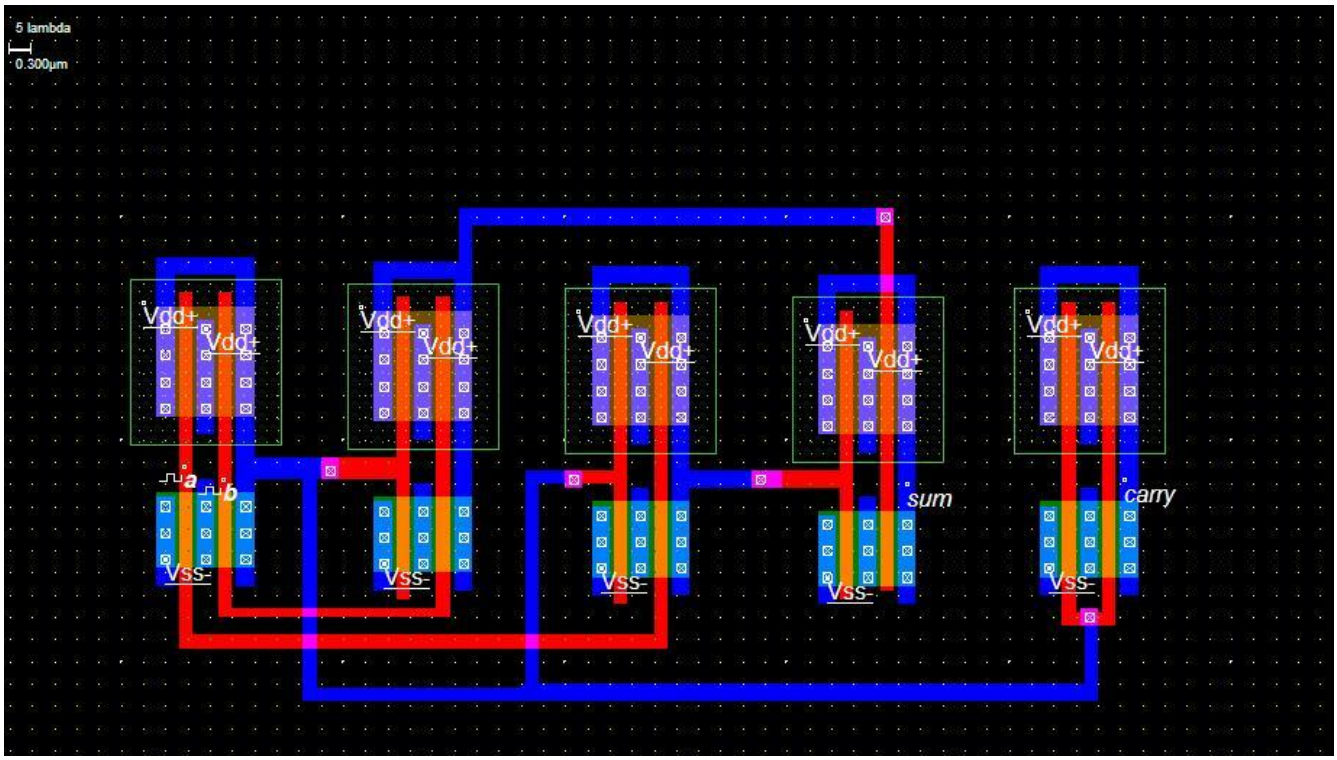
NAME OF THE STUDENT:
CLASSS:
ROLL NUMBER:

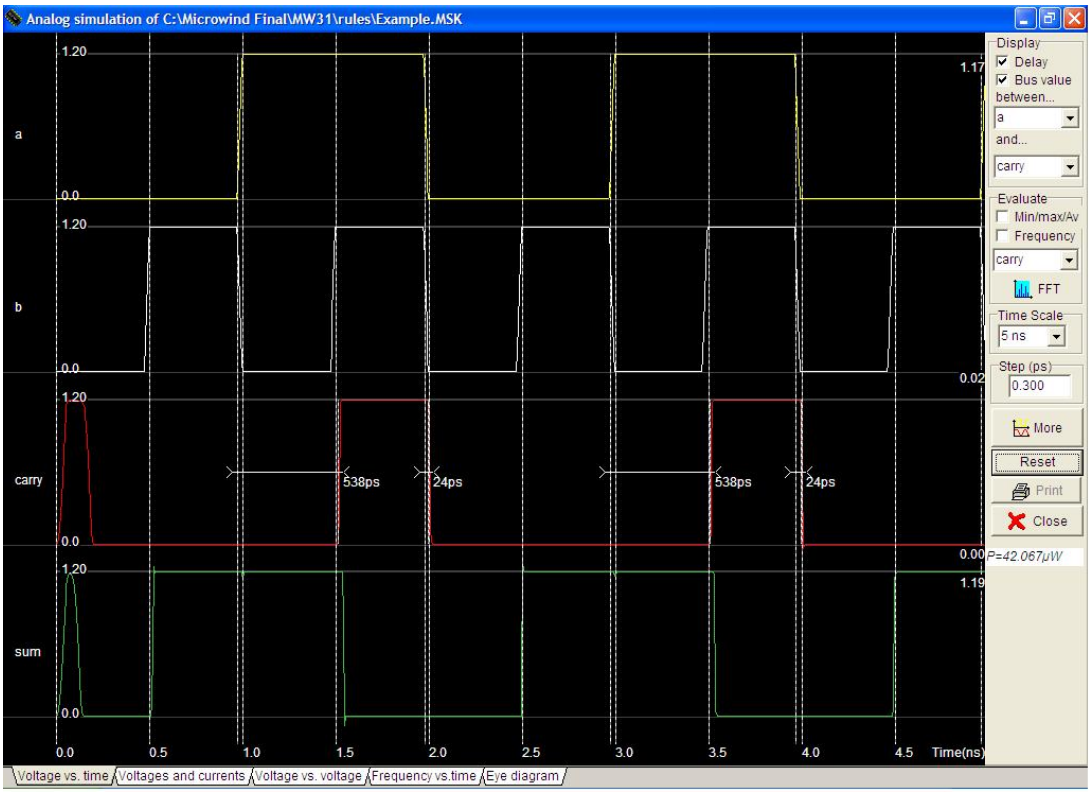
Part B: Design Layout & Timing Diagram of CMOS NOR Gate with capacitor



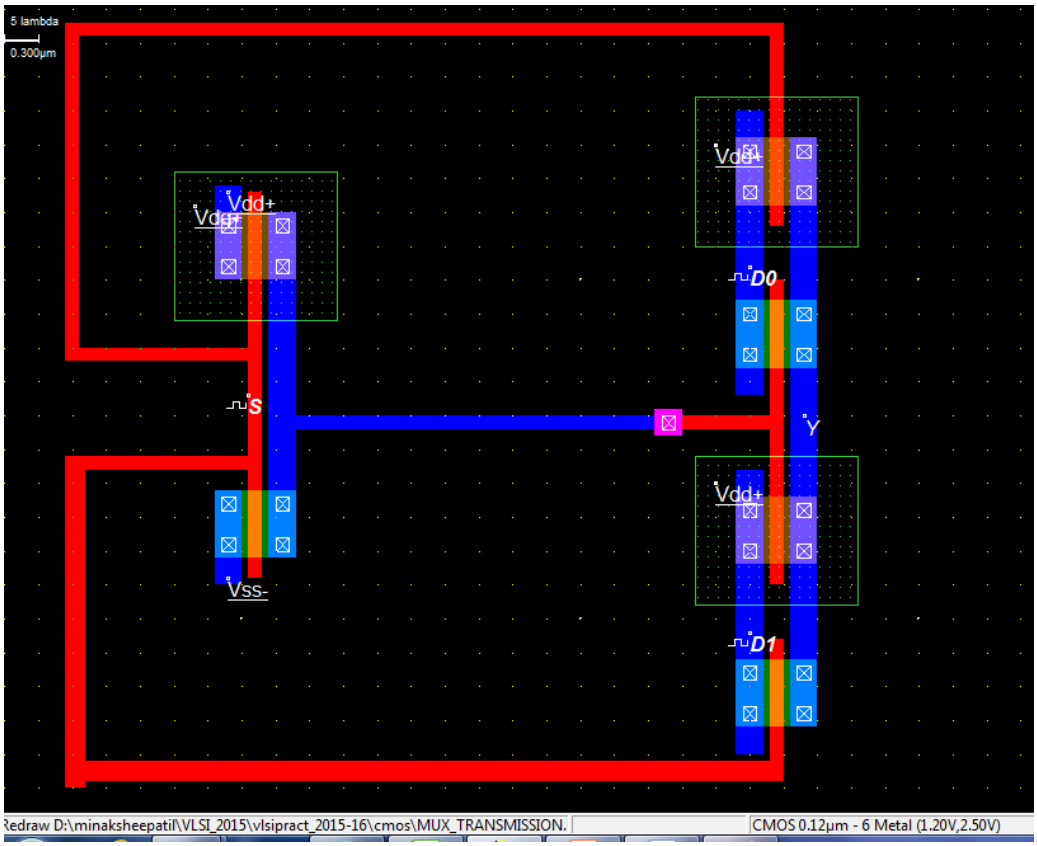


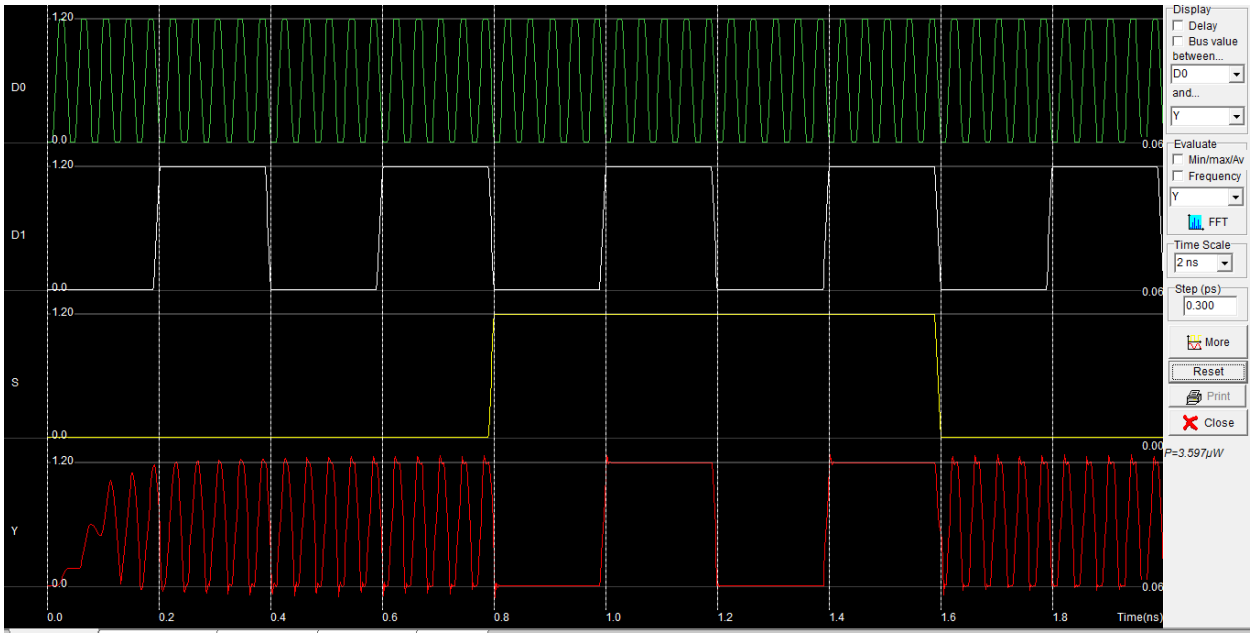
NAME OF THE STUDENT:
CLASSS:
ROLL NUMBER:





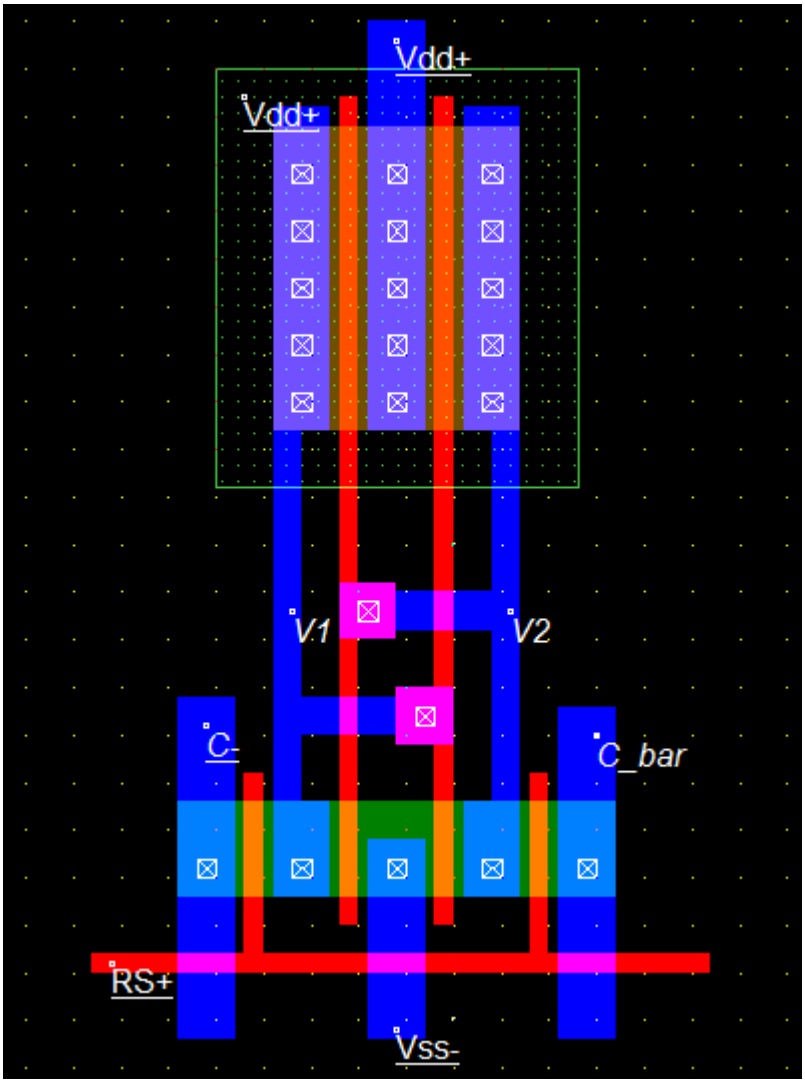
NAME OF THE STUDENT:
CLASSS:
ROLL NUMBER:



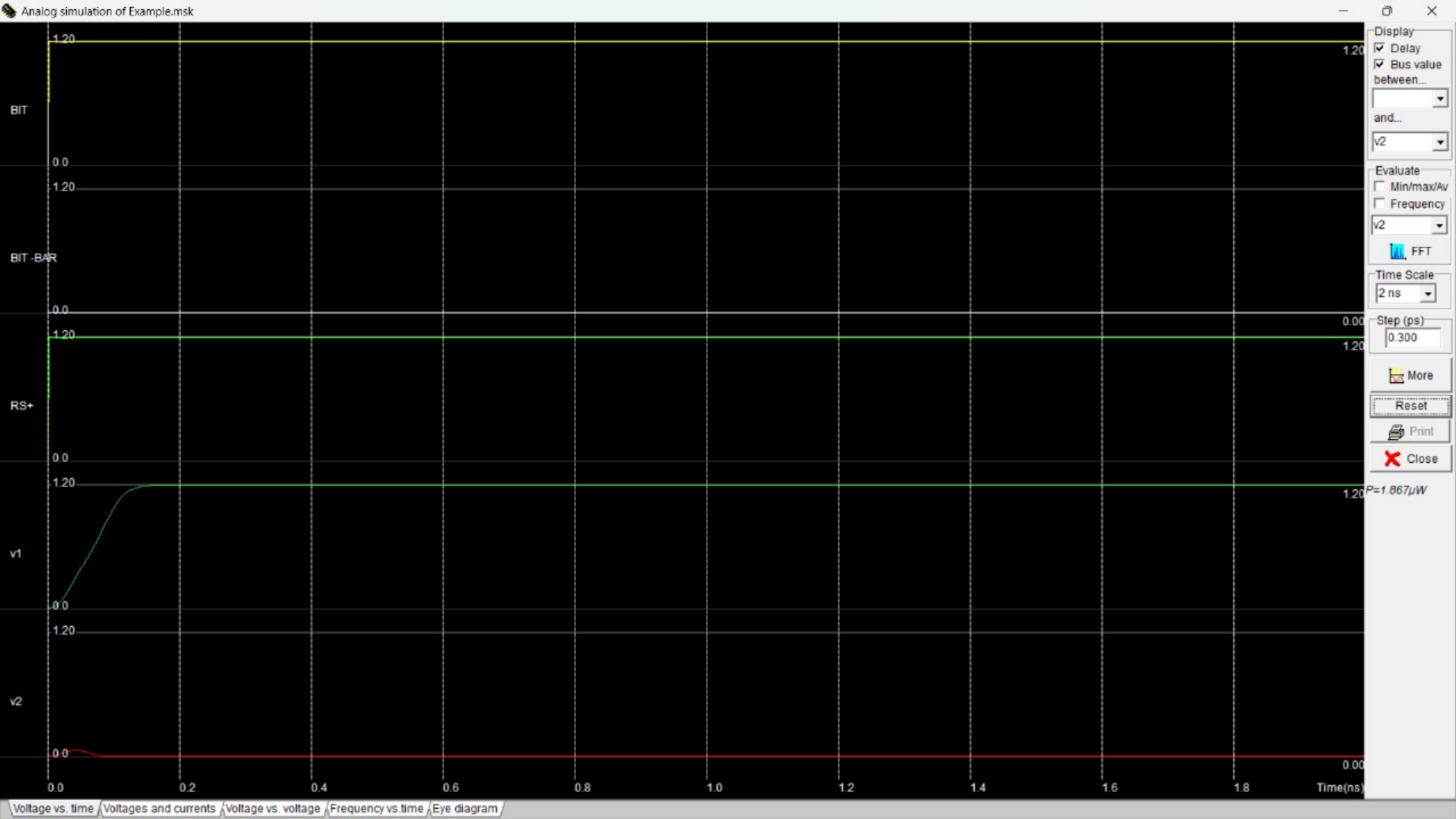


NAME OF THE STUDENT:
CLASSS:
ROLL NUMBER:

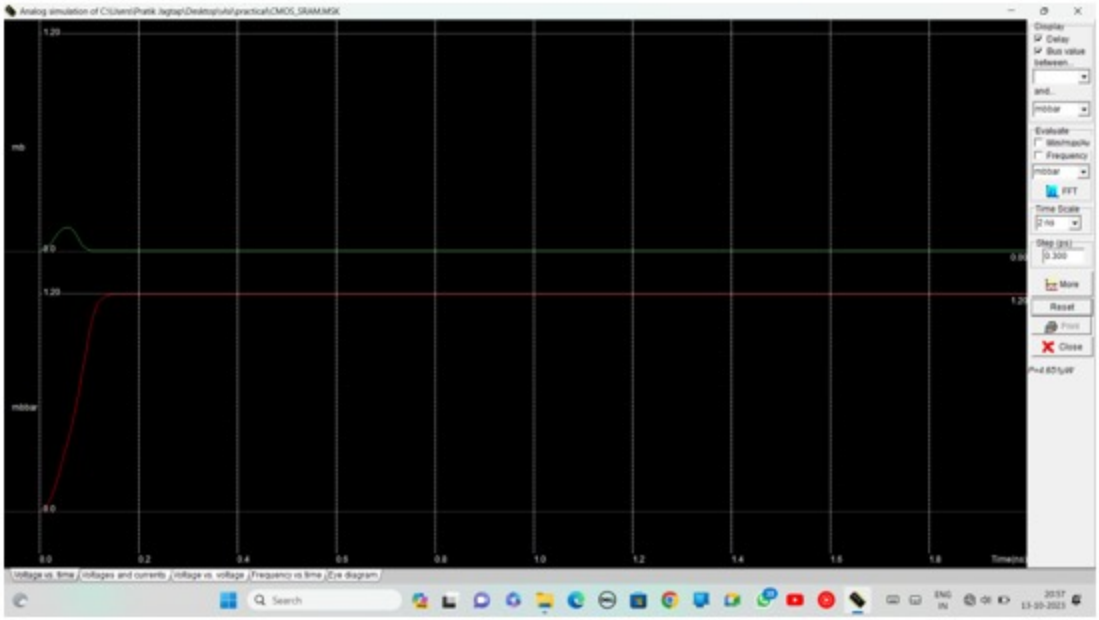
Layout Diagram:

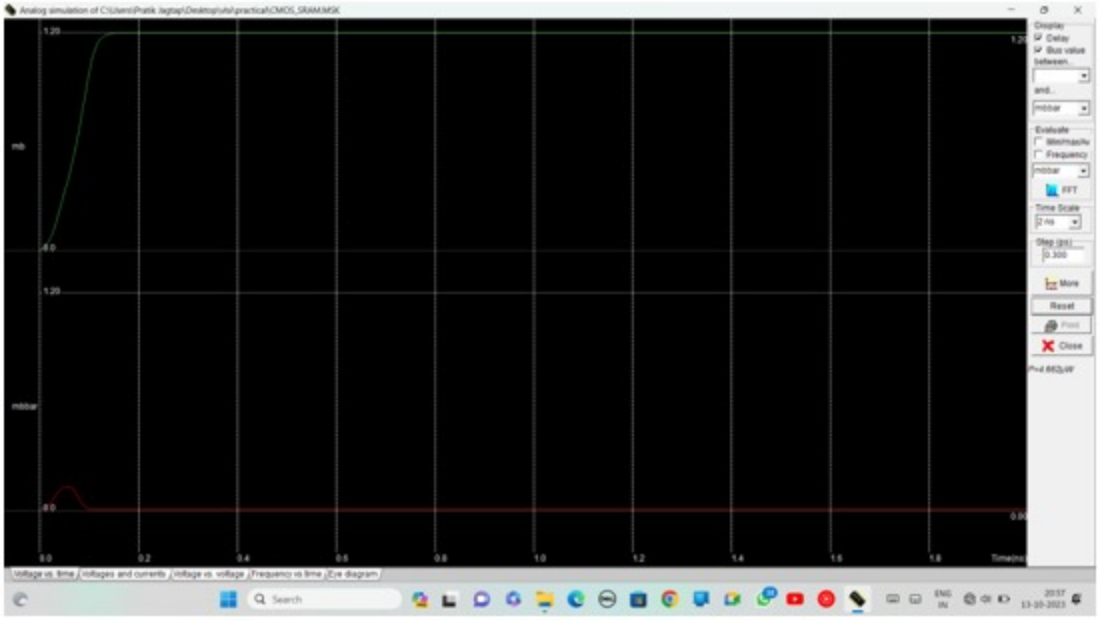


NAME OF THE STUDENT:
CLASSS:
ROLL NUMBER:


Analog simulation of Example.msk
BIT
BIT -BAR
RS+
v1
v2
1.20
0.0
0.00
Time(ns)
0.2
0.4
0.6
0.8
1.0
1.2
1.4
1.6
1.8
Display
Delay
Bus value
between...
and...
v2
Evaluate
Min/max/Av
Frequency
FFT
Time Scale
2 ns
Step (ps)
0.300
More
Reset
Print
Close
P=1.867µW
Voltage vs. time
Voltages and currents
Voltage vs. voltage
Frequency vs.time
Eye diagram

Simulation Results:





Conclusion:

NAME OF THE STUDENT:
CLASSS:
ROLL NUMBER: