# Lab exam
# Sequential Circuits

The scoring of this lab exam is 1,3 points

## Important information

After finishing the lab exam, the student must submit to Moodle the file `A_surname_name.circ` including the requested circuit.

Don't use switches for constant signals, instead use Logisim constants 0 and 1 (in *Wiring*).

Use binary inputs. Don't use bit-vectors as inputs.

Remember that all circuits must be ready for simulation, otherwise the score of the circuit will be zero points.

## Lab exercise

A particular sequence of 7 values have been assigned to each student according his/her ID number. You can find it in the .pdf file uploaded to Moodle.

First of all, type in the upper part of the main panel:

- Your ID number.

- Your assigned sequence (according to your ID).

Design an integrated digital circuit in the *main* panel that includes the followings requirements:

- The circuit must generate the assigned sequence cyclically using FFs and gates. Take the number and type of FF freely. (60%). You can include this circuit in the *main* or in a subcircuit.
- Visualize, in the *main* panel, the value of the sequence using a Hex Digit Display. Note that for values greater than 9 the display will show letters A, B, C, D, E or F. Remember that this display must be included in the *main* circuit. (20%)
- Visualize, in the *main* panel, the order of the corresponding value of the sequence as it is generated by using a second Hex Digit Display. Remember that this numbering starts with number 1 instead of 0. The table below, illustrates the values shown in the first and second displays when the sequence is, for example, 2, 3, 6, 9, 10 (A), 13 (D), 14 (E). This second display must be included in the main circuit, but you can design the circuit that solve this problem in the main panel or in a subcircuit. (20%)

| Cycle | Display 1 | Display 2 |
|---|---|---|
| 0 (Initial state) | 2 | 1 |
| 1 | 3 | 2 |
| 2 | 6 | 3 |
| 3 | 9 | 4 |
| 4 | A | 5 |
| 5 | D | 6 |
| 6 | E | 7 |

**IMPORTANT**: The use of Logisim modules in the circuit that generates the assigned sequence will reduce the score from 60% to 40%.