Computer Technology (Course: 2022/2023)

(A) Examination laboratory

Surname: **Name:** **ID #:**

Instructions: Answer in this document and make the requested circuits with Logisim. The delivery of the exercise will consist of the answers on paper in this sheet of answers and **a single CIRC** file with the requested Logisim circuits that will be uploaded to Moodle. It is not necessary to draw the circuits on paper if the corresponding Logisim circuit is delivered in Moodle, but it must be explained concisely how the result has been reached.

Combinational System

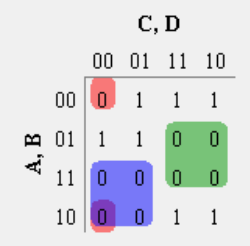
Given the logical function of 4 variables *f(A,B,C,D) = A'B'D+B'C+A'BC'*. It is requested:

A	B	C	D	f
0	0	0	0	0
0	0	0	1	1
0	0	1	0	1
0	0	1	1	1
0	1	0	0	1
0	1	0	1	1
0	1	1	0	0
0	1	1	1	0
1	0	0	0	0
1	0	0	1	0
1	0	1	0	1
1	0	1	1	1
1	1	0	0	0
1	1	0	1	0
1	1	1	0	0
1	1	1	1	0

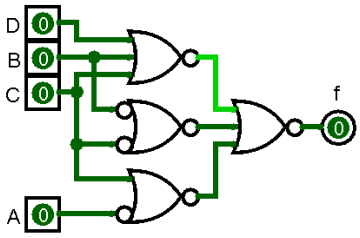
1. **[0,5 pts.]** Truth table of the function *f(A,B,C,D)*.

2. **[0,5 pts.]** Canonical forms of *f(A,B,C,D)*.
   - 1st. canonical form of minterms (SOP): $f = \sum m(1,2,3,4,5,10,11)$
   - 2nd. canonical form of maxterms (POS): $f = \prod M(0,6,7,8,9,12,13,14,15)$

3. **[1 pts.]** Simplified POS (Product of Sums) form of *f(A,B,C,D)* using Karnaugh maps: $f = (B + C + D)(B' + C')(A' + C)$

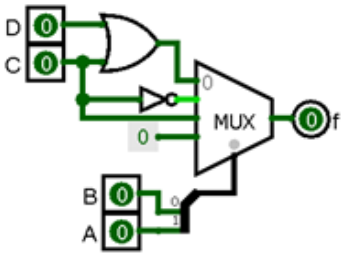


4. **[1 pt.]** Subcircuit-1 (**Logisim**) corresponding to *the implementation of f(A,B,C,D)*, using only NOR gates. Using the simplified POS form, double negation and De Morgan's laws are applied to express the POS form with NOR gates: $f = ((B + C + D)' + (B' + C')' + (A' + C)')'$



5. **[2 pts.]** Subcircuit-2 (**Logisim**) corresponding to the implementation of *f(A,B,C,D)* using a MUX 4x1 and the necessary logic gates.

A	B	C	D	f	
0	0	0	0	0	
0	0	0	1	1	Si A=B=0 ⇒ f=C+D
0	0	1	0	1	
0	0	1	1	1	
0	1	0	0	1	
0	1	0	1	1	Si A=0,B=1 ⇒ f=C'
0	1	1	0	0	
0	1	1	1	0	
1	0	0	0	0	
1	0	0	1	0	Si A=1,B=0 ⇒ f=C
1	0	1	0	1	
1	0	1	1	1	
1	1	0	0	0	
1	1	0	1	0	Si A=B=1 ⇒ f=0
1	1	1	0	0	
1	1	1	1	0	



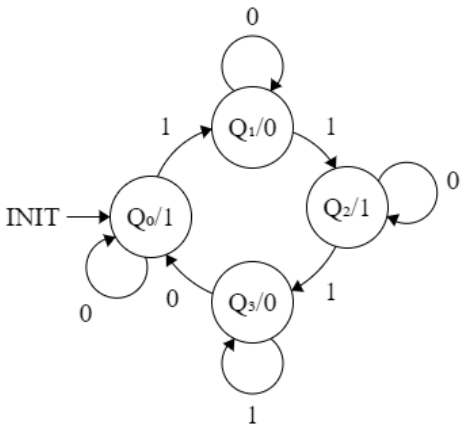
Sequential System

Given the DTE of the attached figure, it is requested to respond to the following paragraphs:

1. **[2 pts.]** Elaborate the corresponding state transition table and the output table, consider implementation only with **T flip-flops**:

Q_t			Q_{t+1}			
q_1	q_0	X	q_1	q_0	T_1	T_0
0	0	0	0	0	0	0
0	0	1	0	1	0	1
0	1	0	0	1	0	0
0	1	1	1	0	1	1
1	0	0	1	0	0	0
1	0	1	1	1	0	1
1	1	0	0	0	1	1
1	1	1	1	1	0	0

q_1	q_0	y
0	0	1
0	1	0
1	0	1
1	1	0



2. **[1 pt.]** Calculate the excitation functions of the flip-flops and the output function, in both their canonical and simplified forms:

- Canonical forms (T_1): $T_1 = \sum m(3,6) = \prod M(0,1,2,4,5,7)$
- Simplified forms (T_1): $T_1 = q_1{}'q_0X + q_1q_0X' = q_0(q_1 \oplus X) = (q_1 + X)q_0(q_1{}' + X')$
- Canonical forms (T_0): $T_0 = \sum m(1,3,5,6) = \prod M(0,2,4,7)$
- Simplified forms (T_0): $T_0 = q_1{}'X + q_0{}'X + q_1q_0X' = (q_1 + X)(q_0 + X)(q_1{}' + q_0{}' + X')$
- Canonical forms (y): $y = \sum m(0,2) = \prod M(1,3)$
- Simplified forms (y): $y = q_0{}'$

3. **[2 pts.]** Implement the resulting circuit with **Logisim**, use at least **one DEC 3x8** for some of the flip-flop excitation functions.