COMPUTER TECHNOLOGY PRACTICAL SESSION P6 (LOGISIM) REGISTERS AND COUNTERS

The objective of this practical session is to design and simulate the main sequential modules: registers and counters.

PART 1.

Design the universal shift register circuit shown in Figure 1. Verify the performance of the circuit by following the chronogram below. Select the "Tick Once" mode in order to see the changes in the circuit as a new clock cycle comes out. Use variables for the control inputs m_1 and m_2 , buttons for asynchronous inputs Clear and Preset. Use also two displays to show input E, the content of the register and a LED for the serial output.

Universal Shift Register S1A B C D m1 m1 MUX 50 SO Preset Output CK Clear Valu Name: D CK Preset M₁M₀ 00 shift right D 01 Load 0 0 ΗO 1 1 3 11 shift left Η7 ■ E[0..2] Output D H0Content 0 3 0 6

PART 2.

Design a circuit that shows the sequence of numbers 0, 2, 4, 2, 0, 2, 4, 2, 0 You can do it using two different solutions. In the first one, design a 2-bit counter using T FFs and then, a suitable decoder circuit, which will be connected to the display (*Hex Digit Display*). In the second solution four FF are taken and the LSB FFs are directly connected to the display.