COMPUTER TECHNOLOGY
PRACTICAL SESSION P5 (LOGISIM)
DESIGN OF SEQUENTIAL CIRCUITS

Given the state diagram of Figure 1:

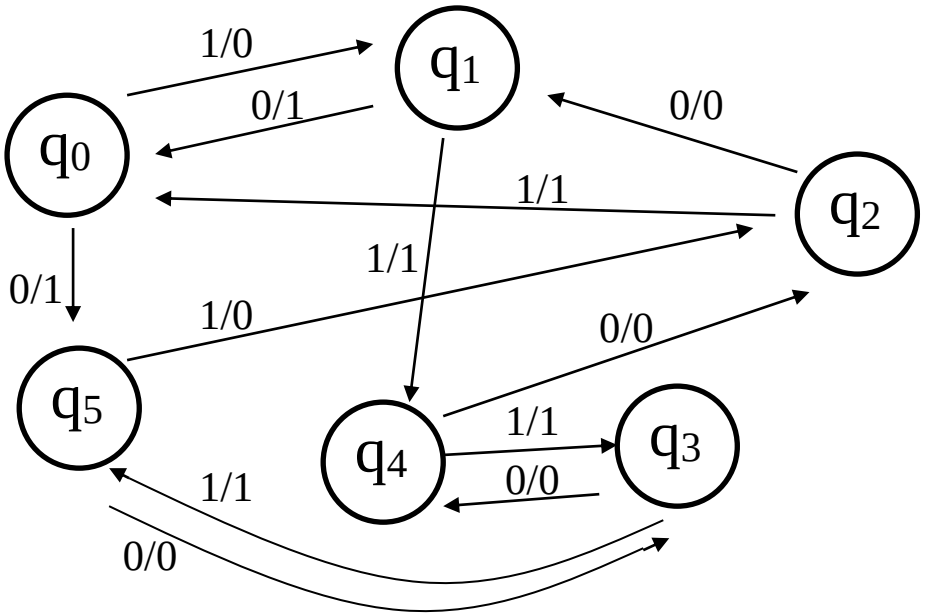

Figure 1

Design the sequential circuit using the following flip flops:

- T FF for the most significant flip-flop (T_2).
- D FF for the middle flip-flop (D_1).
- JK FF for the least significant flip-flop (J_0K_0).

Implement T_2 using logic gates, D_1 at the discretion of the student, and J_0K_0 using an active-high output DEC 4x16. The output S must be implemented using a MUX 4x1. Design and simulate the circuit with Logisim.

Check that if x=0 the state sequence is:

q0 → q5 → q3 → q4 → q2 → q1 → q0

Check that if x=1 the state sequence is:

q0 → q1 → q4 → q3 → q5 → q2 → q0

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REMARK 1: The state encoding is shown in Table 1.

	Q_2	Q_1	Q_0
q_0	0	0	0
q_1	0	0	1
q_2	0	1	0
q_3	0	1	1
q_4	1	0	0
q_5	1	0	1

Table 1

REMARK 2: The state of the circuit must be visualized using 3 orange LEDs and a display (take *Hex Digit Display*), corresponding to the outputs of the three flip-flops. These LEDs must be placed horizontally, in the following order: $Q_2Q_1Q_0$. The output S must be visualized using a green LED.

FILL OUT THE TABLE BELOW:

E	$Q_2(t)$	$Q_1(t)$	$Q_0(t)$	$Q_2(t+1)$	$Q_1(t+1)$	$Q_0(t+1)$	T_2	D_1	J_0	K_0	S
0	0	0	0								
0	0	0	1								
0	0	1	0								
0	0	1	1								
0	1	0	0								
0	1	0	1								
0	1	1	0								
0	1	1	1								
1	0	0	0								
1	0	0	1								
1	0	1	0								
1	0	1	1								
1	1	0	0								
1	1	0	1								
1	1	1	0								
1	1	1	1								