COMPUTER TECHNOLOGY
PRACTICAL SESSION P3
COMBINATIONAL CIRCUITS: SUB-CIRCUITS INTEGRATION

INTRODUCTION

The objective of this practical session is to design a digital circuit composed of three sub-circuits (see figure below). The input of the circuit is a 8-bit vector V={V_7,…V_0}, that is extracted according the DNI of the student as follows. If the i-th digit of the DNI is even then V_i=0, otherwise V_i=1. For example if DNI=08.453.392, then V=**00011110**

Design the following subcircuits:

- Subcircuit 1 visualizes de number of the highest active-high bit in V (highest priority). Call this number as n_h . For example if DNI=08.453.392, then V=**00011110 and** n_h=4.
- Subcircuit 2 implements function F, which takes value 1 if n_h is even, with the exception of number 0, in which F is 0. Otherwise, F=0.
- Subcircuit 3 implements function G, which takes value 1 if the number of 1's of the binary code of n_h is odd. Otherwise, V=0.

Figure 1 shows the main circuit and one example in which the 8-bit input is V=00011110. According to this input, the number of the highest active-high bit is 4. The display then visualizes 4. Since 4 is an even number, F=1. Finally, the binary code of 4 is 100, which contain one 1, which is an odd number, and, consequently, G=1.

The student must implement Subcircuits 1, 2 and 3 and, finally, implement the main circuit as follows:

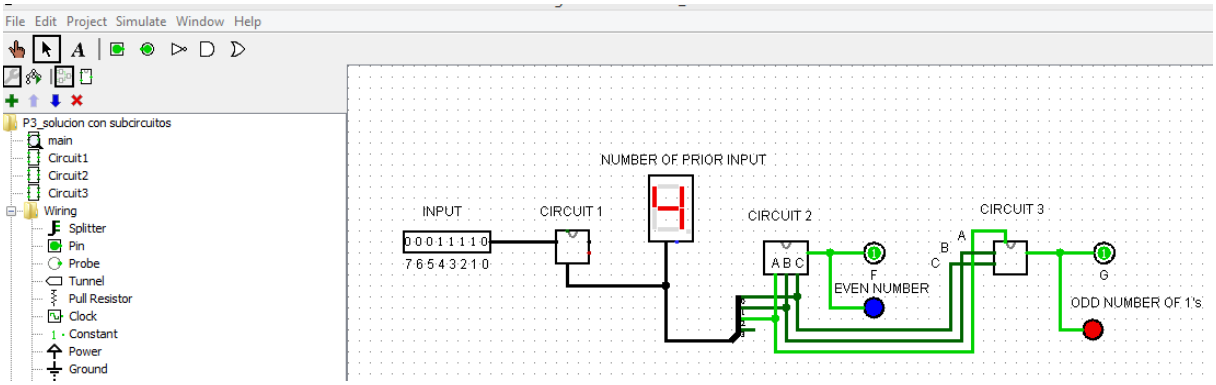

Figure 2

PART 1. Subcircuit 1

Design and implement subcircuit 1 using the following modules of Logisim:

- Priority Encoder (in *Plexers*)
- Hex Digit Display, which visualizes a BCD number in a display.

Suggestions:

- Move the mouse pointer over the small dots of the modules (see figure below) in order to see and understand the meaning of the inputs and outputs.
- Use the Splitter (in the *Wiring* panel) to convert separate data to a databus (bit-vector) and vice versa.

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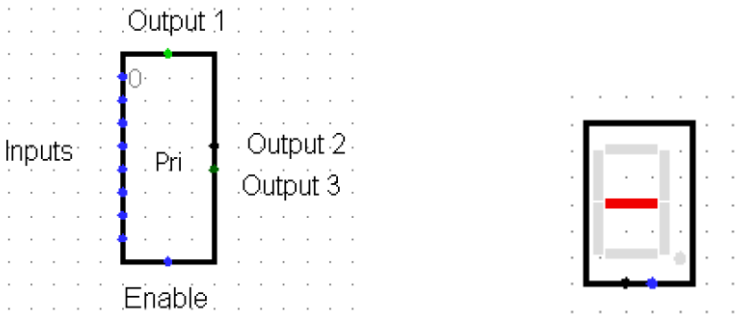

Figure 2. Priority Encoder and Hex Digit Display. The small dots represent different inputs and outputs

PART 2. Subcircuit 2

Design and implement subcircuit 2 using a MUX 4x1 and the necessary logic gates

PART 3. Subcircuit 3

Design and implement subcircuit 3 using a multiplexer MUX 4x1 network and the necessary logic gates

PART 4. Main circuit. Integration

Implement the main circuit using Subcircuits 1, 2 and 3.