11.2 Overflow for signed numbers only occurs when adding numbers with the same sign (positive or negative). The numbers overflow (V) if the sign of the result Y does not match the sign of the inputs A and B:

$$V = A_{N-1}B_{N-1}\overline{Y}_{N-1} + \overline{A}_{N-1}\overline{B}_{N-1}Y_{N-1}$$

11.6 8 stages for 32-bit, 11 stages for 64-bit addition.

11.10

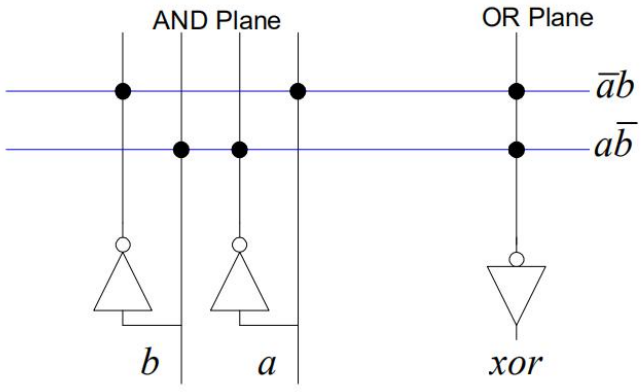
$$\begin{aligned} C_{out} &= \overline{(A \oplus B)\overline{C} + \overline{(A \oplus B)}\overline{A}} \\ &= \overline{A\overline{B}\,\overline{C} + \overline{A}B\overline{C} + \overline{A}\,\overline{B}} \\ &= MAJ(A, B, C) \end{aligned}$$

11.22 The following equations are a slight modification of EQ 10.50. Use the base case $X_{1:1} = 1$, $W_{1:1} = 0$.

$$\begin{aligned} X_{i:i} &= \overline{A_i \overline{A}_{i-1}} && \text{bitwise precomputation} \\ W_{i:i} &= A_i \overline{A}_{i-1} \\ X_{i:j} &= X_{i:k} \bullet X_{k-1:j} \\ W_{i:j} &= W_{i:k} \bullet X_{k-1:j} + X_{i:k} \bullet W_{k-1:j} && \text{group logic} \\ Y_i &= W_{i:i} \bullet W_{i-1:1} && \text{output logic} \end{aligned}$$

12.2 The dimensions are (128 columns * 1.3 μm/col* 1.1) x (128 rows * 1.44 μm/row* 1.1) = 183 μm x 203 μm.

12.10



12.12 NAND ROMs use series rather than parallel transistors and one-cold rather than one-hot wordlines. They tend to be smaller than NOR ROMs because they do not require contacts between the series transistors, but they are also slower because of the series transistors.