集成电路自动化设计方法
(Design Automation of VLSI)
2015-秋季学期

电子科学与技术系：陈 松

2015年9月10日

Course Webpage:

http://staff.ustc.edu.cn/~songch/da-ug.htm

Terminologies

- EDA (Electronic Design Automation)
  - 电子设计自动化
  - Synopsys, Cadence, Mentor Graphics, Agilent, etc.
- VLSI CAD (Very Large Scale Integration Computer-aided Design)
  - 超大规模集成电路计算机辅助设计
- IC CAD (Integrated Circuit Computer-aided Design)
  - 集成电路计算机辅助设计

Outline

- Course Overview
  - Contents
  - Evaluation
  - Course information
- History of Integrated Circuits

Course Info

- Name: Design Automation of VLSI (集成电路自动化设计方法)
- Teacher： 陈松 songch@ustc.edu.cn， 3A303, Thursday 3,4
  - Tel: 63602675 Mobile: 13155167790
- Text books
  - **Lecture Notes**
  - Wang, Chang, and Cheng (Ed.), ***Electronic Design Automation: Synthesis, Verification, and Test***, Morgan Kaufmann, 2009.
  - Meil H. E. Weste and David Money Narris, ***CMOS VLSI Design: A circuits and Systems Perspective***, fourth edition, Addison-Wesley, 2011.
  - David A. Patterson and John L. Hennessy, **Computer Organization and Design: The hardware/software interface**, 4th edition, Appendix C, Chapter 3, Chapter 4.

Available on the following webpage:

- **http://staff.ustc.edu.cn/~songch/da-ug.htm**

What

- Design methodology
  - Standard Cell / IP (Intellectual Property), FPGA, PLA
- Design Metrics
  - Power, Performance, Area, etc.
- Logic Design (Logic Synthesis)
  - Front-end design: From RTL to Logic Gates
- Physical Design (Physical Synthesis, Layout)
  - Back-end design: From Gates to GDSII
- Labs (Begin at the third week)
  - Verilog Hardware Description Language Basics
  - Synopsys Tool Suits: vcs, design compiler/power compiler/primetime, ICC compiler

Why

- EDA Tool Designers
  - Basic requirements
- Theoretical guide for problem solving in using VLSI design tools
- VLSI System Architecture Designers
  - Coupling the front-end design and back-end design to shorten the design cycle and improve the chip performance
    - **Complex multiplexer structures often cause congestion problem**

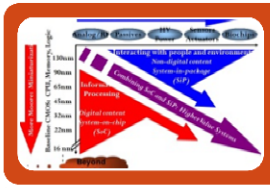
Grading Policy

- Lecture Attendance: 10%
- Lab attendance: 50%
- Homework: 40%

提纲

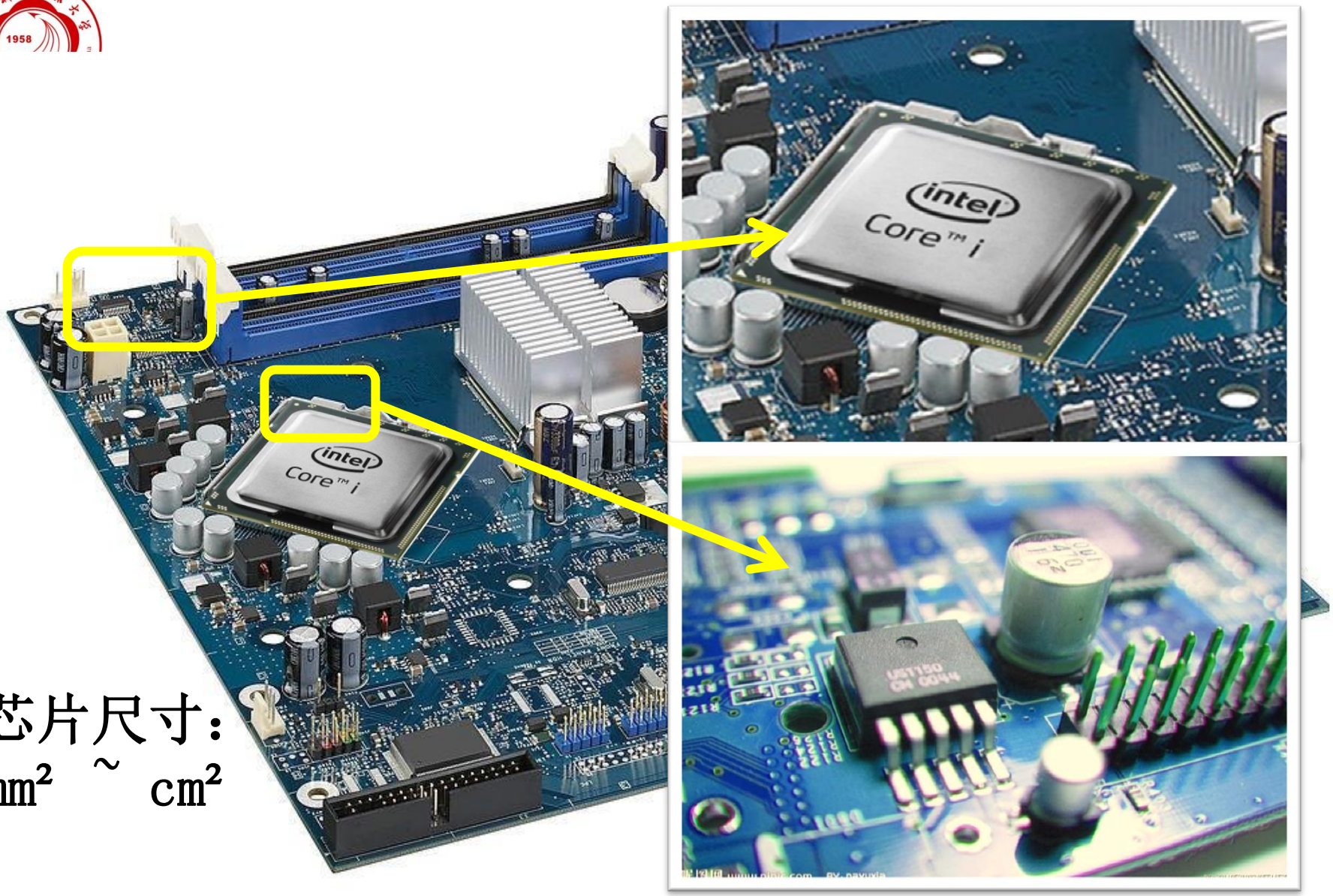
集成电路

Golden Moore & Von Neumann



纳米电子时代的挑战

集成电路设计



芯片尺寸：

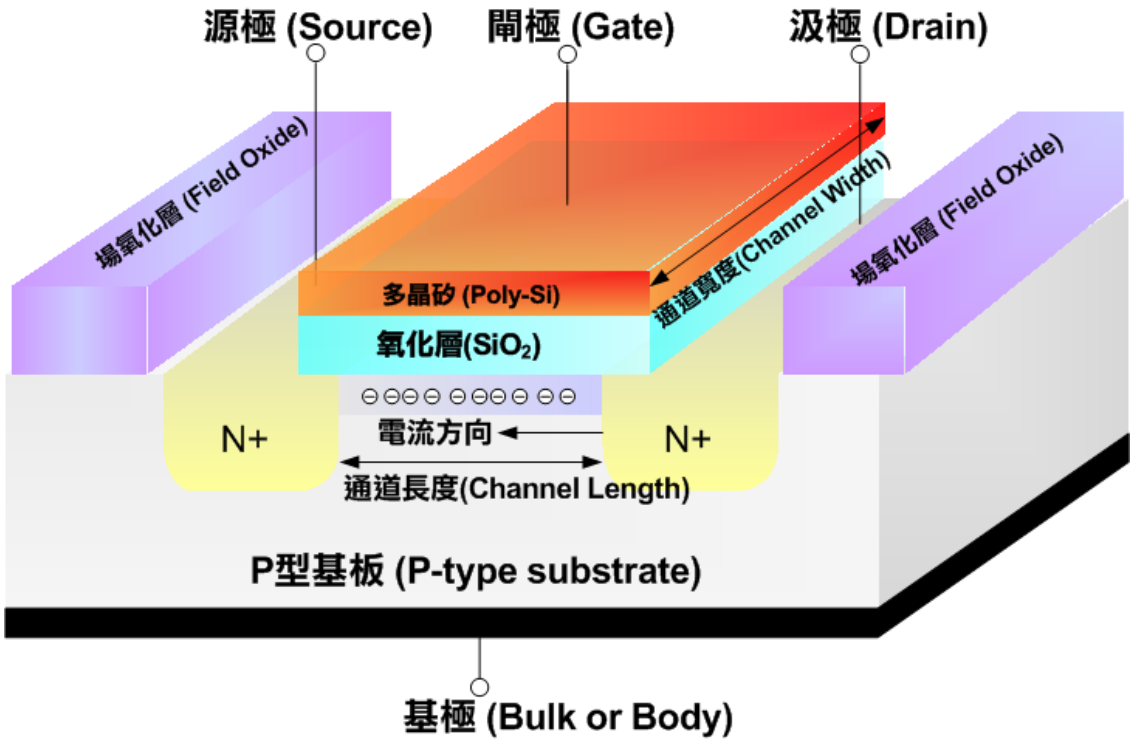
mm^2 ~ cm^2

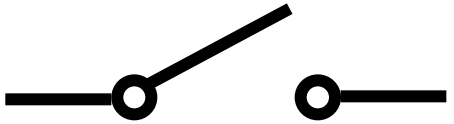
晶体管

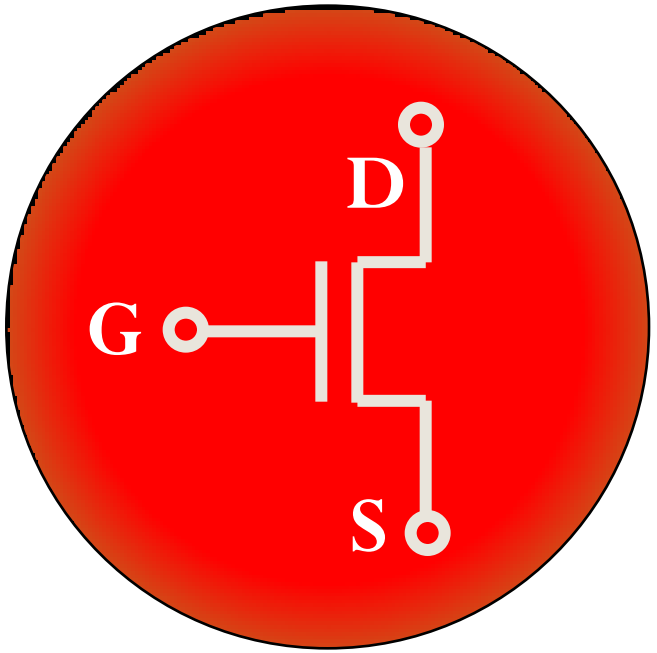
W. Shockley, J. Bardeen and W. Brattain

1947年，第一支晶体管在美国贝尔实验室诞生，**肖克利、巴丁**和**布拉顿**获得**1956年诺贝尔物理学奖**

半导体晶体管

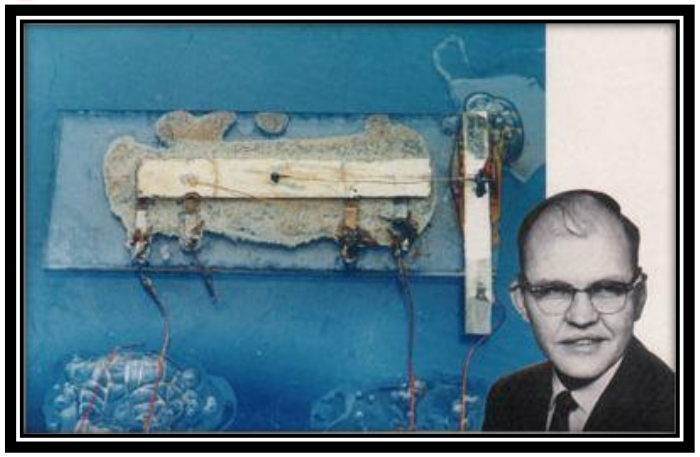






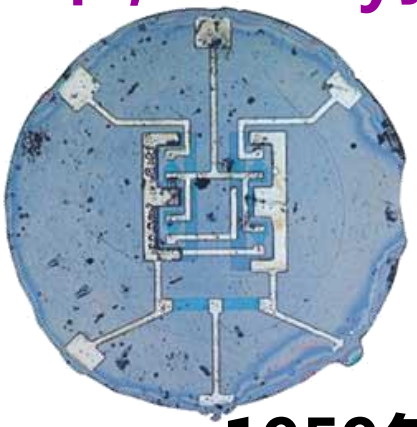
金属氧化物半导体晶体管
（MOS晶体管）结构图

集成电路

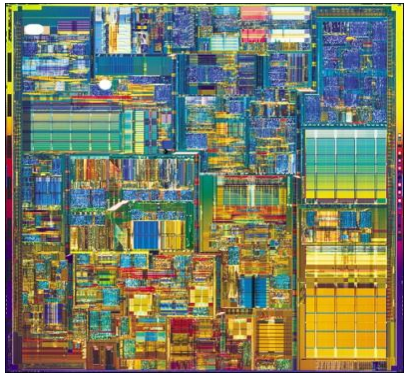


1958年， Jack S. Kilby
发明了集成电路的雏型

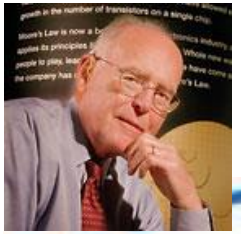
2000年，J. Kilby获得诺贝尔物理学奖

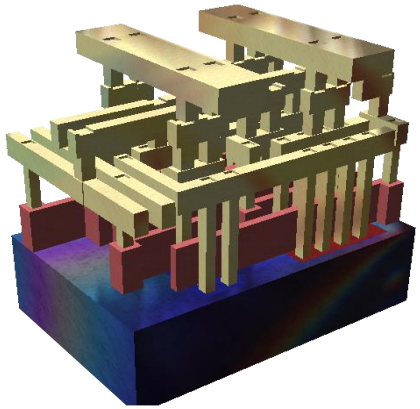


1959年，R. Noyce
发明了今天的集成电路

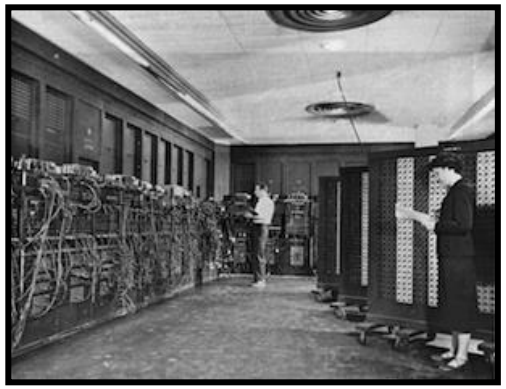


Pentium IV





计算机的演变



ENIAC：1945年第一台电子计算机诞生，它使用18000只电子管，70000只电阻，500万个焊点，耗电160千瓦，占地170平方米，重30吨，运算速度5000次/秒

P4004：1971年世界上第一个微处理器在英特尔公司诞生

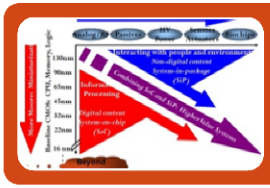
TRADIC：1954年第一台晶体管计算机在贝尔实验室诞生，它使用800只晶体管

IBM360:1964年第一台集成电路计算机在IBM公司诞生，共6个型号，兼顾了科学计算和事务处理两方面的应用，各种机器全都相互兼容。它的研制开发经费高达50亿美元，是研制第一颗原子弹的曼哈顿计划的2.5倍。

提纲

集成电路

Golden Moore & Von Neumann



纳米电子时代的挑战

集成电路设计

戈登·摩尔 和 约翰·冯·诺依曼

Golden Moore

Von Neumann

按比例缩小

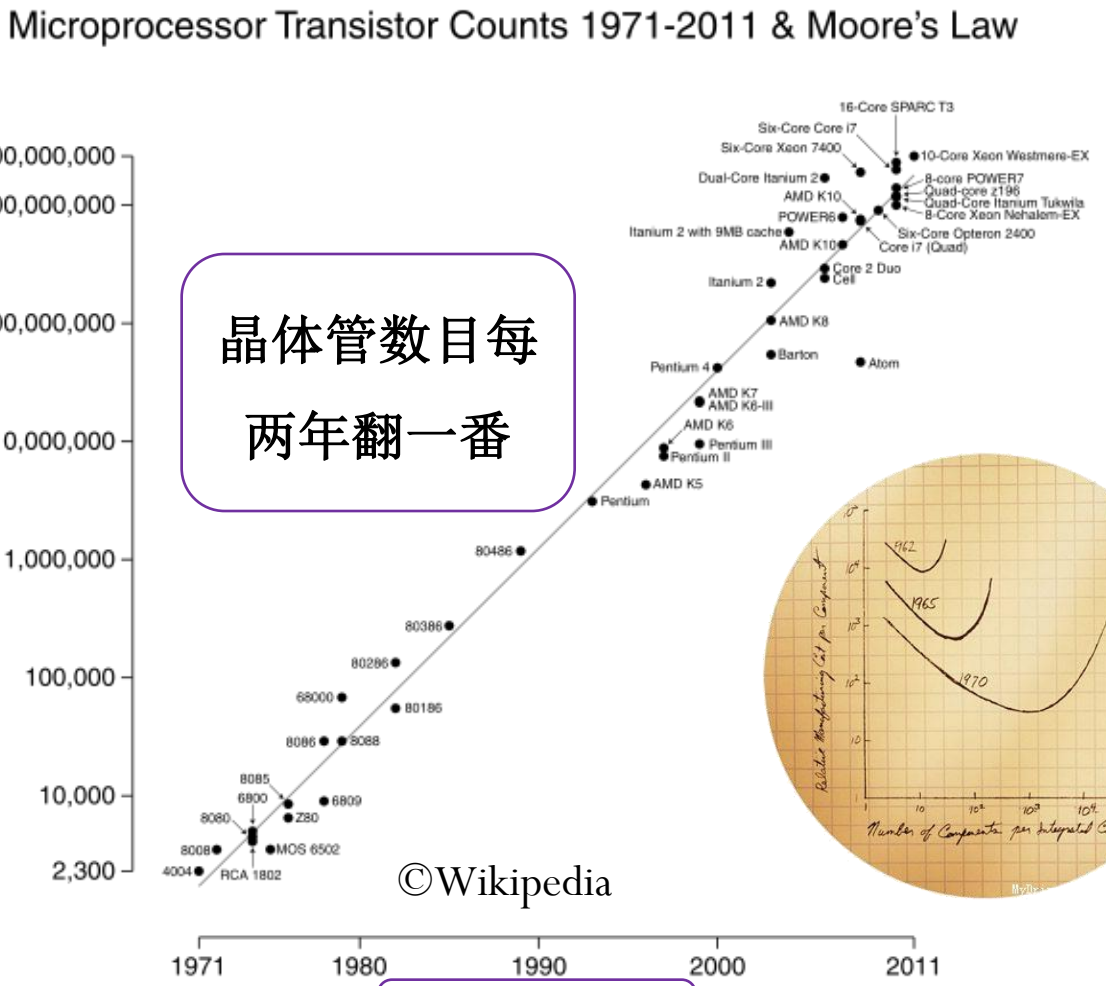
P4004：1971年世界上第一个微处理器在英特尔公司诞生

冯·诺依曼体系结构

半导体

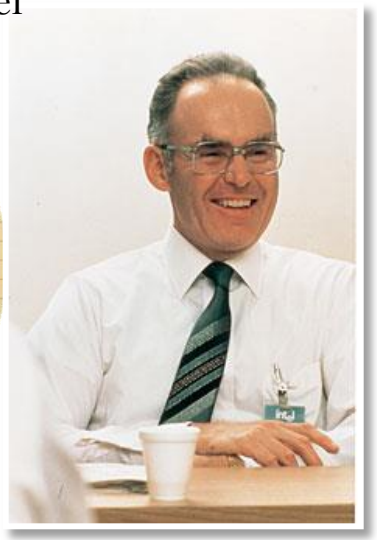
计算机

摩尔定律



©Wikipedia

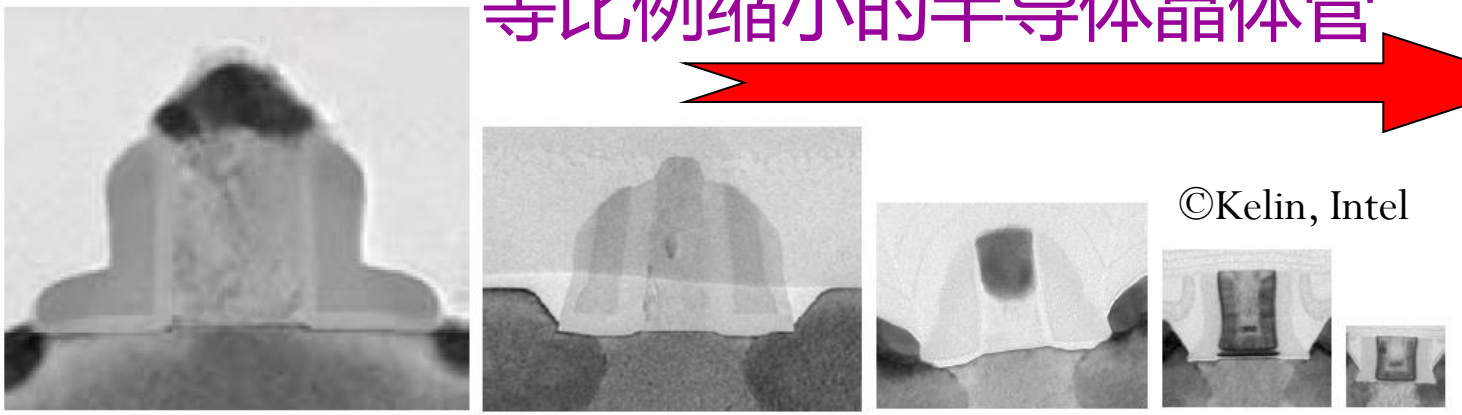
©Intel



等比例缩小（Scaling Down）

原因之一：按比例缩小（Scaling Down）

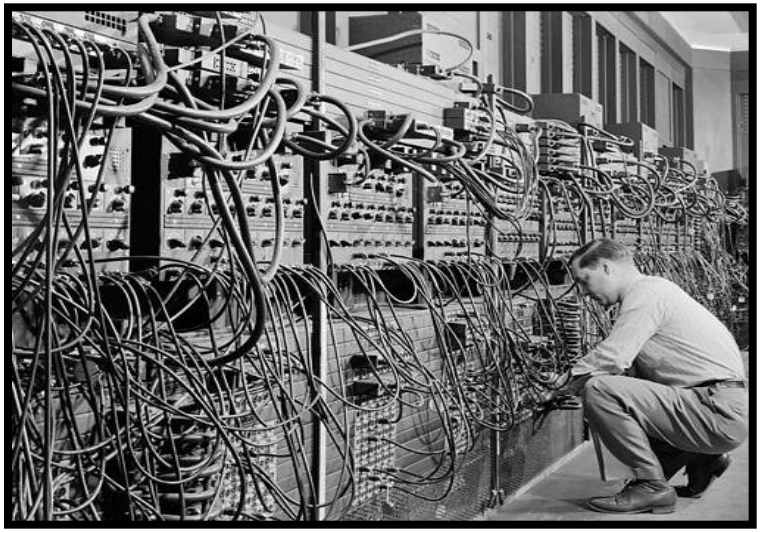
等比例缩小的半导体晶体管



- 等比例缩小是地将一组硅器件的技术参数(通常多余20个)同步缩小
- 摩尔定律讲的是技术密度
- 摩尔定律是对集成电路产业的预测
- 等比列缩小是实现摩尔定律的方法

ENIAC：专用计算机

原因之二：计算（Computation）

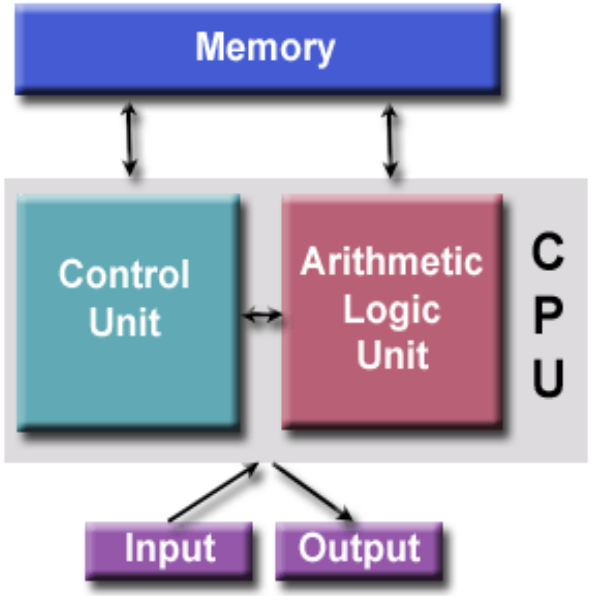


ENIAC是一台专为美国军方计算火炮弹道轨迹设计的专用计算机。虽然具备一定的编程能力，但程序是事先预置好的。改变程序就要求工作人员改变硬件的连线结构。严格意义上讲，ENIAC不是一台通用计算机。

ENIAC运行时，安排了一批年轻的女性工作人员按照计算要求插拔众多的接头，以实现不同的运算。工作十分繁琐，出错概率很大，效率很低。硬件的准备时间大大超过实际的计算所需的时间。

冯·诺依曼体系结构

原因之二：计算（Computation）



数字计算机的数制采用二进制；

计算机应该按照程序顺序执行

计算机：**控制器、运算器、存储器、输入设备、输出设备**；

从ENIAC到当前最先进的计算机都采用的是冯诺依曼体系结构。

各种不同的体系结构

原因之二：计算（Computation）

流水线

哈佛

多核

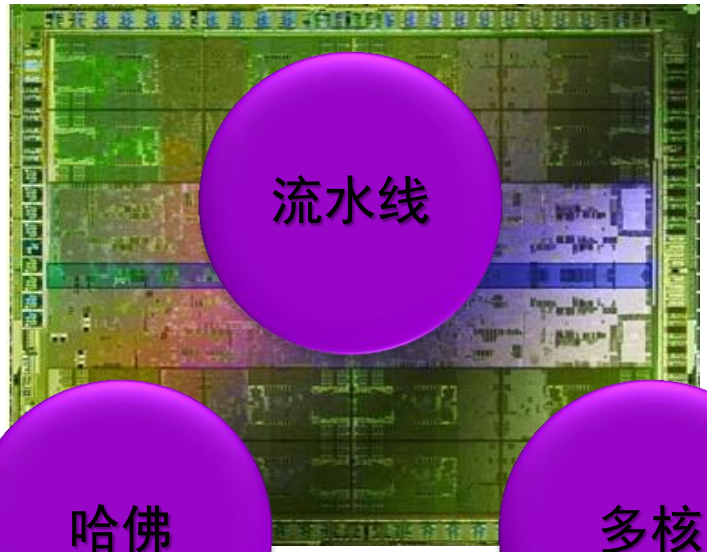
双核

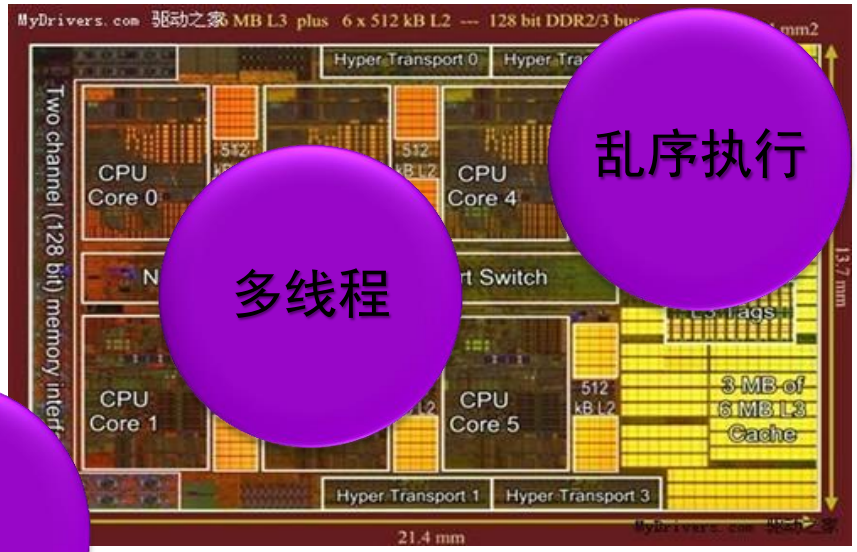
乱序执行

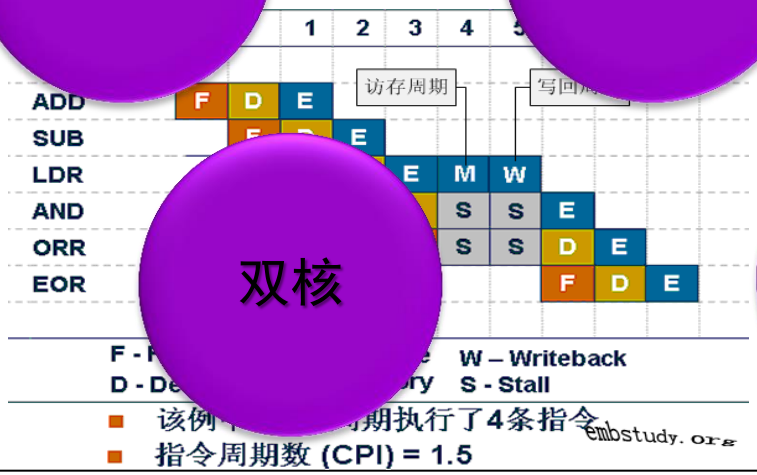
多线程

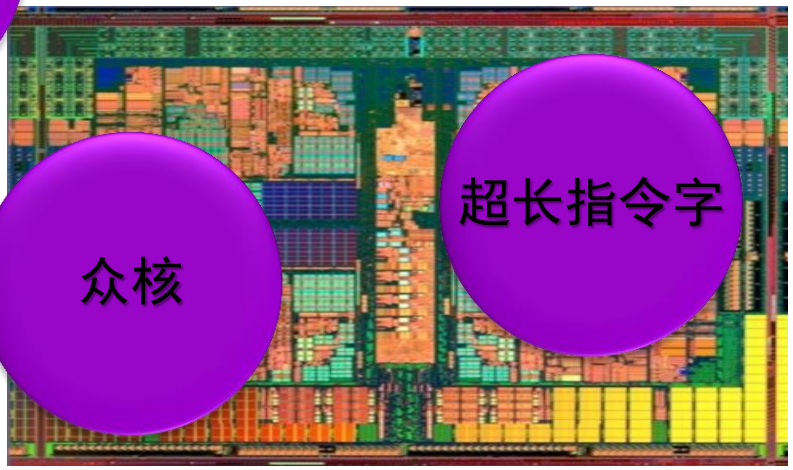
超长指令字

众核





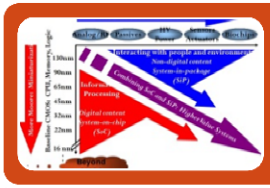




提纲

集成电路

Golden Moore & Von Neumann



纳米电子时代的挑战

集成电路设计

传统半导体行业

晶体管按比例缩小

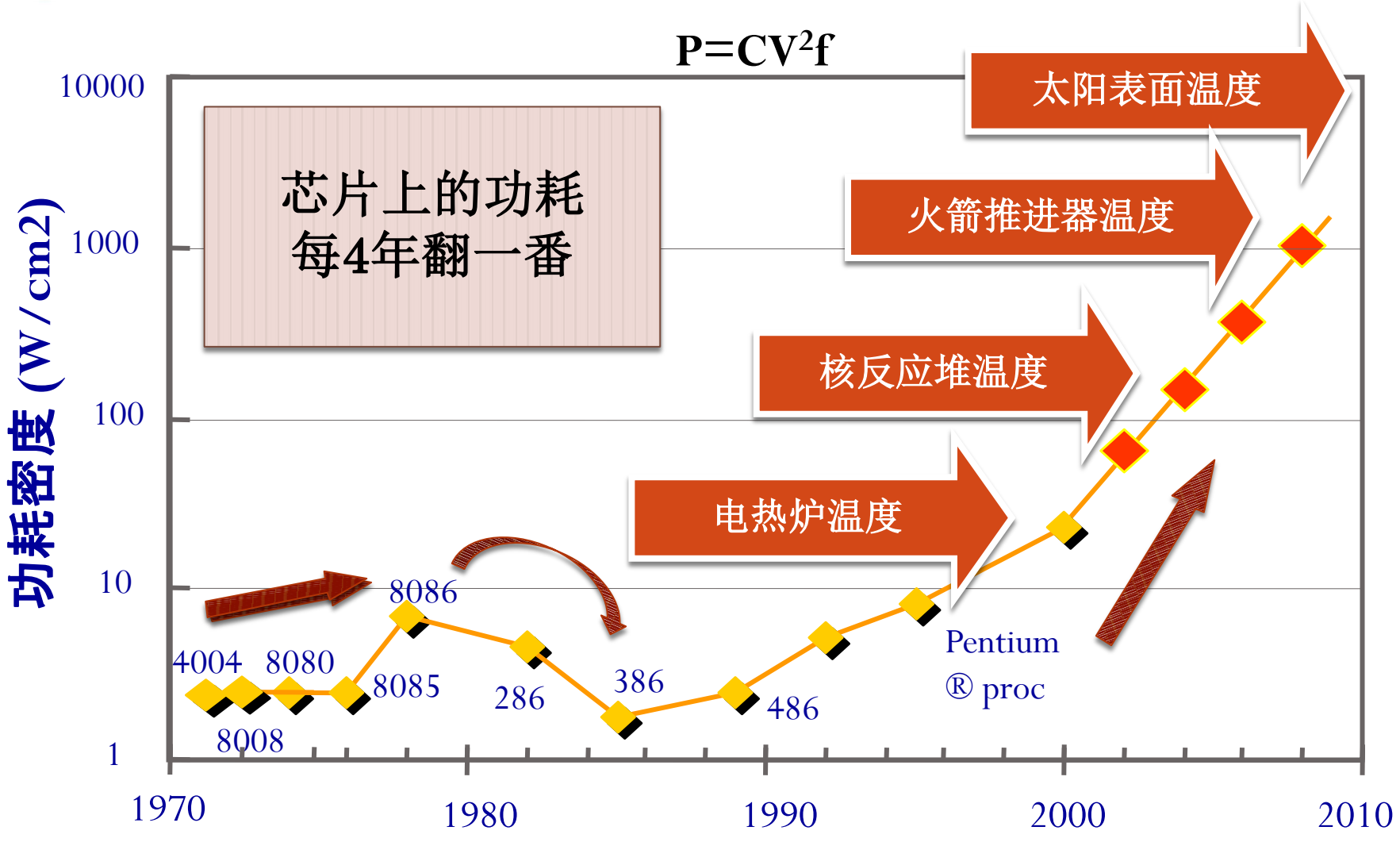
摩尔定律

性能更高
成本更低

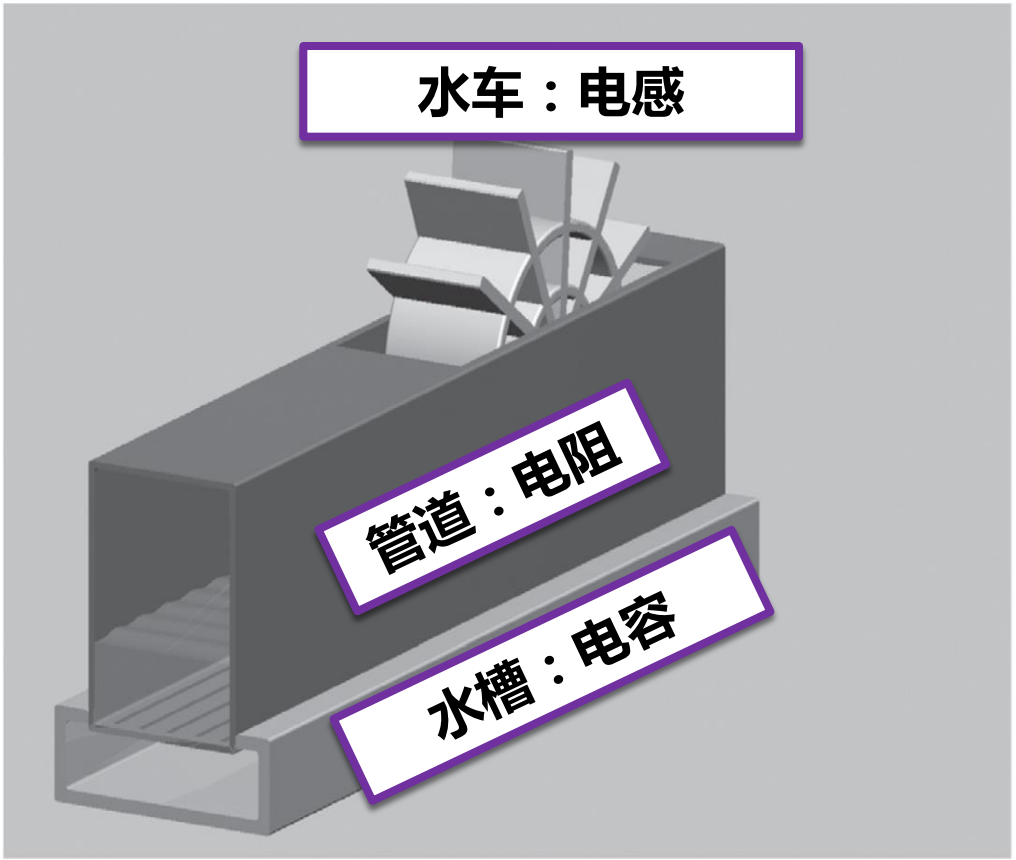
市场增长

投资

功耗是最关键问题


P=CV²f
芯片上的功耗
每4年翻一番
太阳表面温度
火箭推进器温度
核反应堆温度
电热炉温度
功耗密度 (W/cm2)
10000
1000
100
10
1
1970
1980
1990
2000
2010
4004
8008
8080
8085
8086
286
386
486
Pentium
® proc

导线延时 （Wire Delay）



金属线变细：

电阻 R ↗

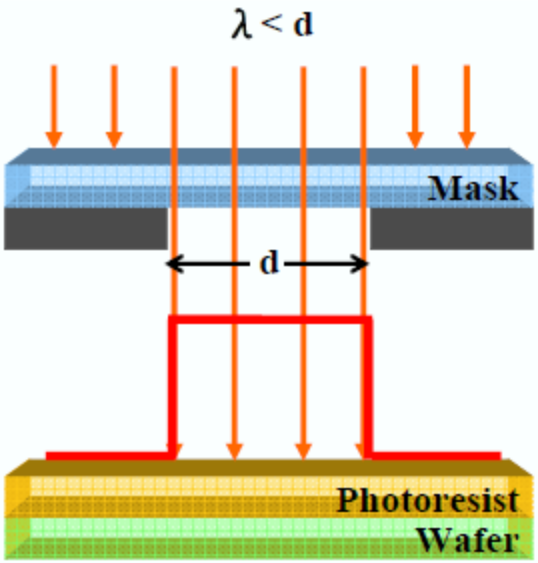
电容 C ↘

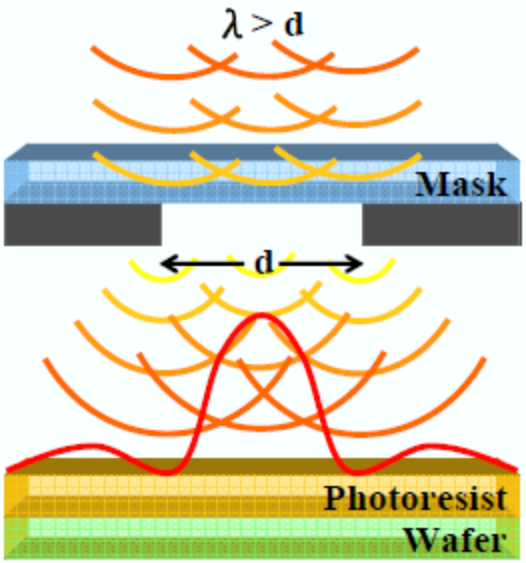
延时 D = R × C

↗ ↗ ↘

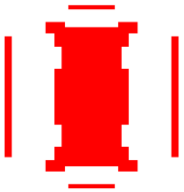
电阻增大速度远大于电容减少速度！

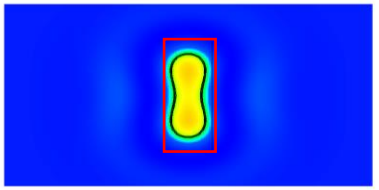
可制造性问题

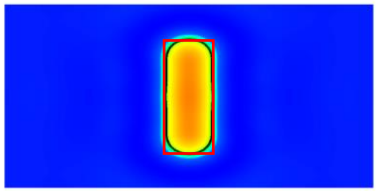




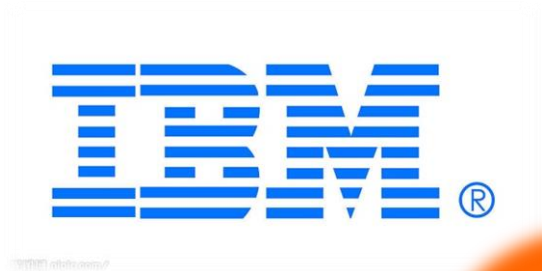
- 良片率
- 193nm vs. 40nm, 28nm, 16nm
  - OPC（光学邻近校正技术），Multiple Patterning Lithography
- 极紫外光刻 （10+nm）







大公司的游戏



16nm
12-15B $

22nm
8-10B $

32nm
5-7B $

45nm
3.5-5B $

现代半导体行业

技术、器件和电路
创新，系统集成

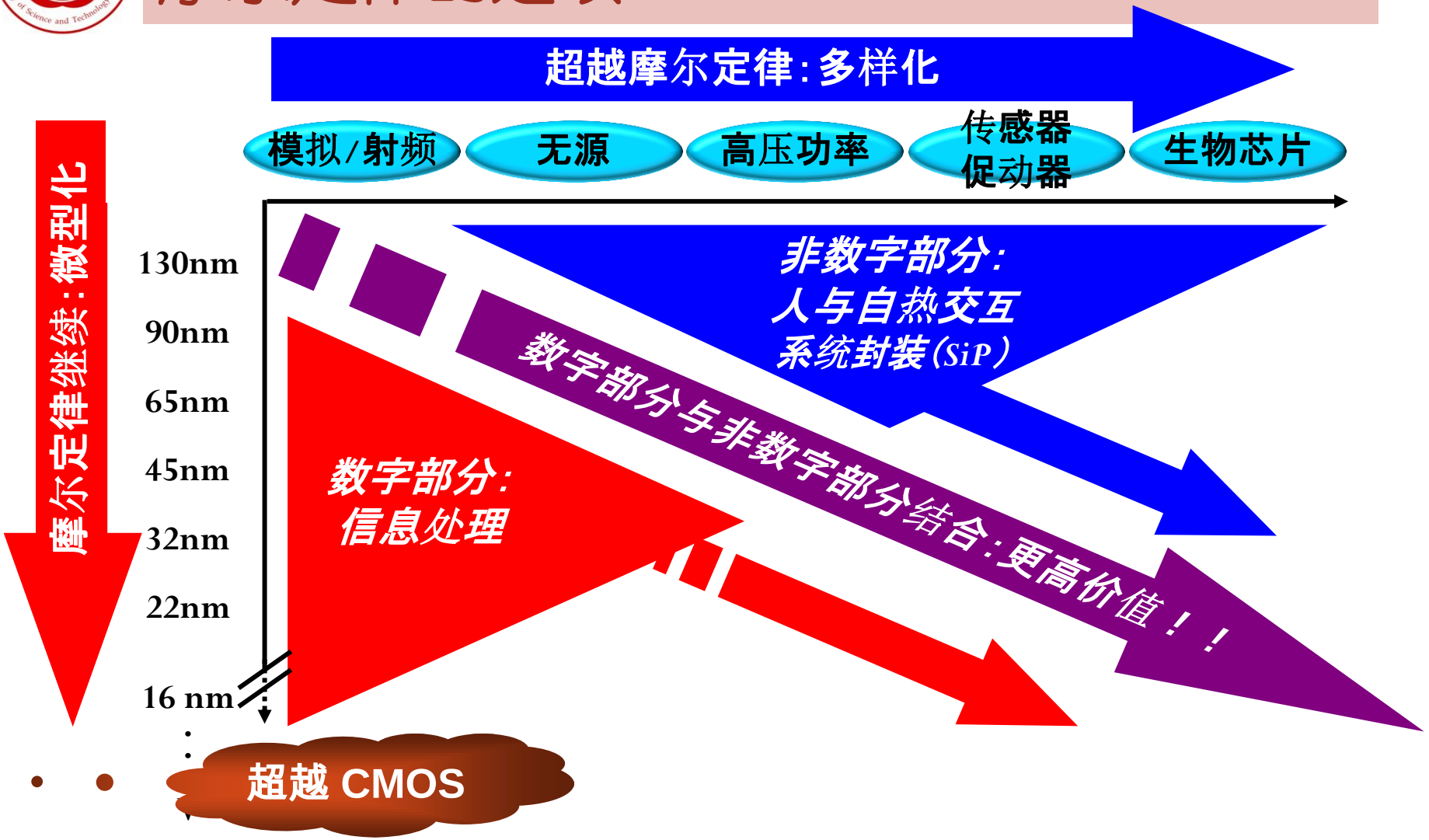
功能增强
和/或
成本更低

市场增长

投资

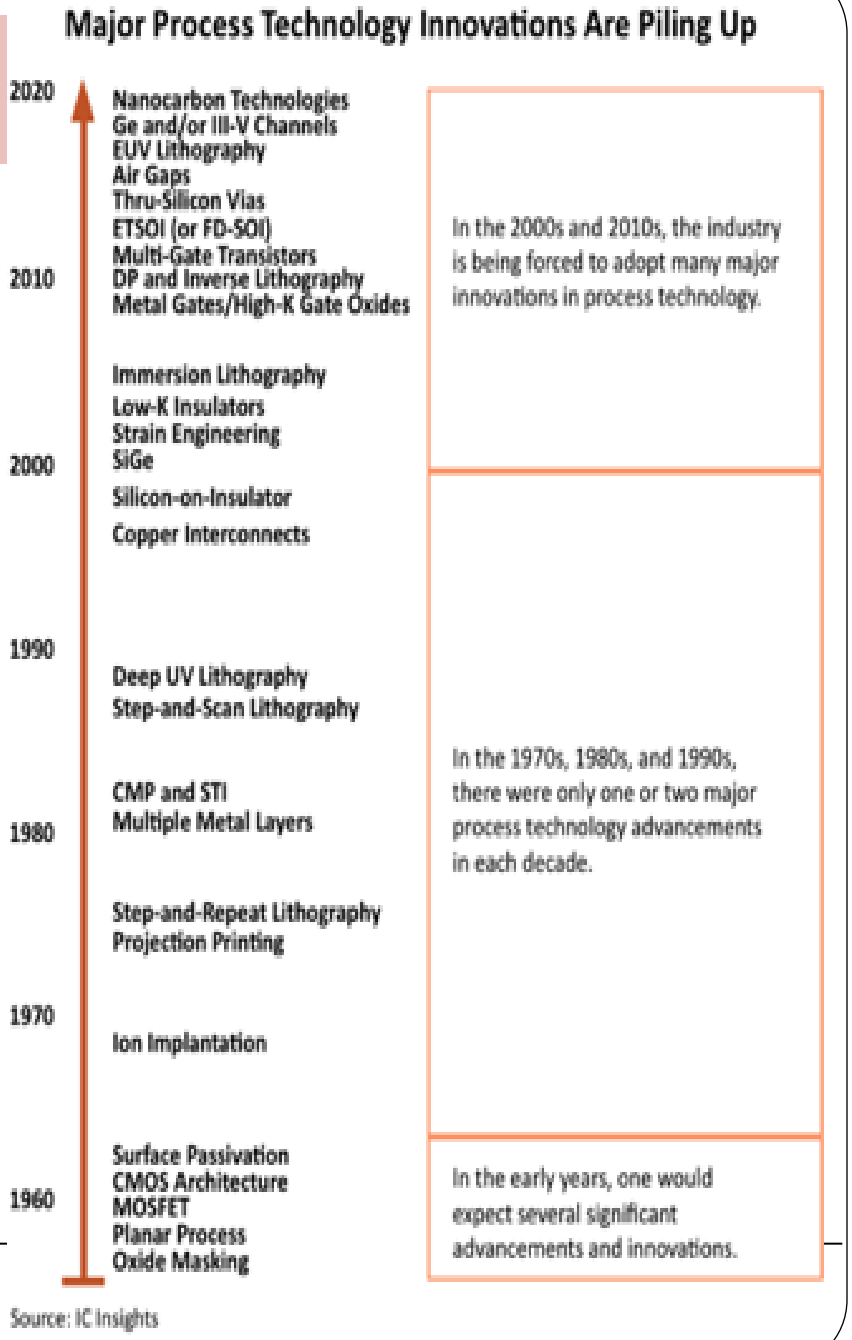
超越摩尔定律

摩尔定律的延续


超越摩尔定律：多样化
模拟/射频
无源
高压功率
传感器
促动器
生物芯片
摩尔定律继续：微型化
130nm
90nm
65nm
45nm
32nm
22nm
16 nm
非数字部分：
人与自热交互
系统封装（SiP）
数字部分与非数字部分结合：更高价值！！
数字部分：
信息处理
超越 CMOS

Technology Trends

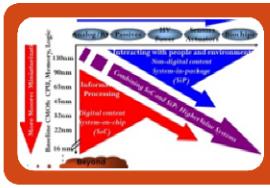
- Advanced lithography methods needed to continue shrinking chip geometries
- New interconnect schemes
- Strain engineering for improved performance and lower power consumption
- 3D integration
- Novel transistor structures
- Migration to larger wafers



提纲

集成电路

Golden Moore & Von Neumann



纳米电子时代的挑战

集成电路设计

Integrated Circuits Industry

Design(设计)

Tools & IP: Synopsys, Cadence, Mentor Graphics, etc.	Fabless: Qualcomm, MediaTek, Huawei (华为), Xilinx, Altera, Spreadtrum (展讯), etc.

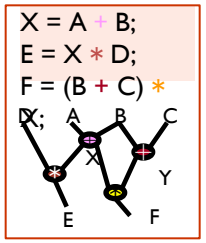
Wafer Manufacturing (晶圆制造)

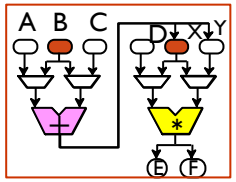
Lithography Instruments: ASML, NEC, etc.	**Foundries**: TSMC, UMC, GF, Intel, Samsung, SMIC (中芯国际)

Packaging & Testing （封装与测试）

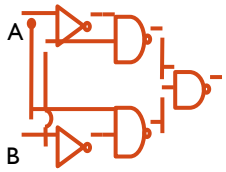
Testing Instruments : Agilent (安捷伦), Rohde&Schwarz	ASE Global, Amkor, etc.

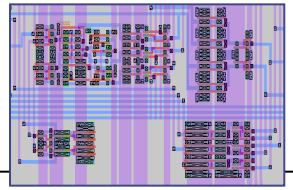
ASIC (专用集成电路)





Adder 1 Multiplier 1
Register 8 Multiplexer 4





System / Behavioral Descriptions

Register Transfer Level Descriptions

Gate Level Netlist

Layout mask

Design Automation

High-level Synthesis
高层次综合
- Scheduling;
- Binding;
- Allocation.

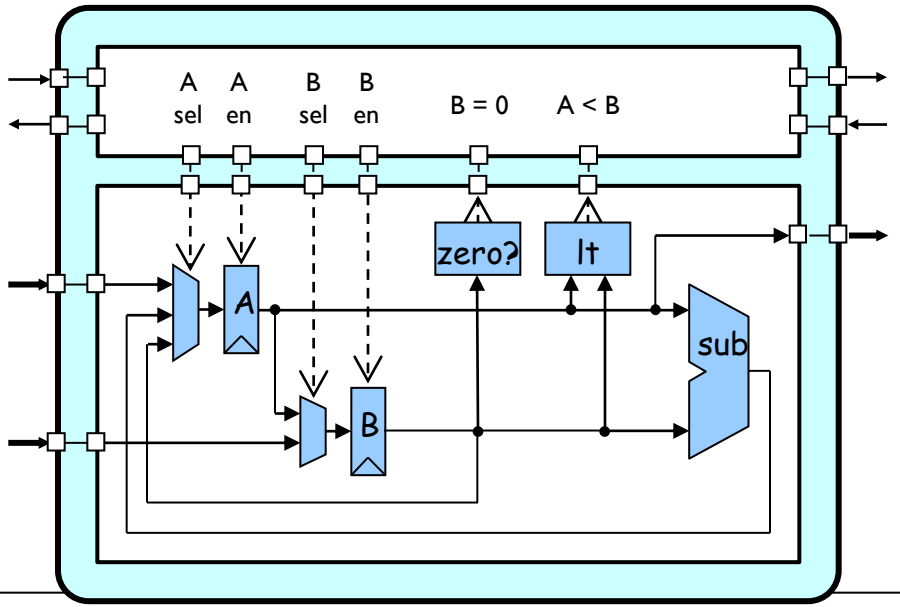
Logic Synthesis
逻辑综合
- Logic Optimization;
- Technology Mapping.

Physical Synthesis
物理综合/芯片布图
- Floorplanning;
- Placement;
- Routing;
- etc.

High-level Synthesis (高层次综合)

- **Transformation from a behavioral specification of a system to its RTL structure specification**
  - E.g., from C/C++ to RTL, Bluespec, Xilinx AutoESL
  - Promote the productivity
  - Essential tasks: scheduling, binding, allocation

```
begin
    done = 0; A = inA; B = inB;
    while ( !done )
    begin
      if ( A < B )
        swap = A;
        A = B; B = swap;
      else if ( B != 0 )
        A = A - B;
      else
        done = 1;
    end
```



Logic Synthesis (逻辑综合)

- Transformation from a Register-Transfer-Level (RTL) description to a gate-level netlists
  - Hardware Description Language
    - Verilog HDL, VHDL
  - Logic Optimization
  - Technology Mapping

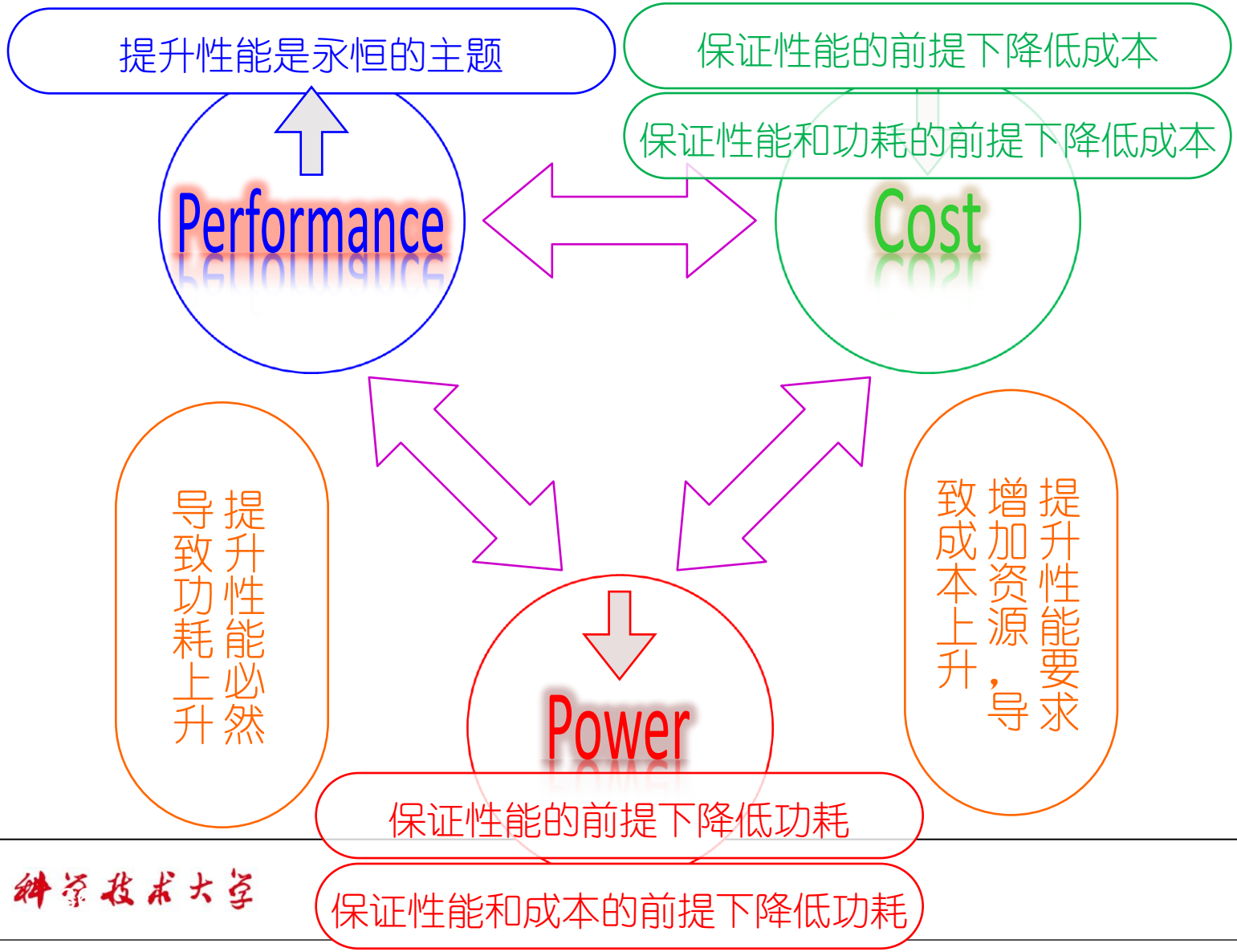
Physical synthesis(物理综合)

- **Transformation from a gate-level netlists to its physical layouts (masks)**
  - Partitioning (划分)
  - Floorplanning （布图规划）
  - Power/Ground Network Synthesis （电源线/地线网络合成）
  - Placement （布局）
  - Routing （布线）： Clock Tree, Signal, Power/Ground
  - Post-routing （后布线优化）
    - Redundant Via Insertion (Design for Yield)

Large Scale Discrete Optimization Problems: Computation-Consuming.

How to find good solutions in acceptable time?

Performance, Power, Cost



Modern Chip (VLSI) Design

- Managing Design Complexity (设计复杂性)
  - System-on-Chip: IP reuse, Platform-based Design Methodology
  - Electronic System Level Synthesis (High-level synthesis)
    - Raising the design abstraction
- Power (功耗)
  - Low Power Technologies: LeakagePower, Dynamic Power
  - New Device: FinFET
- Interconnect （互连）
  - Delay, System-level design & Physical Design
  - Network-on-Chip
  - 3D ICs
  - Optical-/wireless-/CNT-/RF Interconnect
- Reliability （可靠性）
- Design For Manufacturability: EUV, OPC, PSM, …