数字集成电路设计实验

——第五次实验

信息科学技术学院

姓名：胡睿　PB17061124

实　验　报　告

评分：

信 院 系 17 级　姓名　胡　睿　日期 2021-01-13　NO.

【实验题目】乘法器设计与实现

【设计要求】

设计一个 32 位乘法器，端口定义如下：

输入信号　clk　时钟，上升沿触发

输入信号　rst　同步复位，高有效

输入信号　a　宽度 32，乘数

输入信号　b　宽度 32，乘数

输出信号　c　宽度 64，乘积

乘数输入 a,b 和乘积输出 c 都是寄存器暂存的。在每个时钟周期的上升沿，输入信号 a，b 被采样存入寄存器，利用随后的一个时钟周期完成运算，在下一个上升沿，乘积存入寄存器 c 中，并输出。

复位信号有效时，输出为 0。

【目录结构】

/bks2/Chenglin_Stu2019/PB17061124/vlsi/multiplier_design_database_45nm

captable	寄生参数模型
constraints	设计约束，SDC 文件
Equivalence_checking	等价性检查运行目录
gate_level_simulation	门级仿真运行目录
lef	物理模型，LEF 文件
lib	时序模型，LIB 文件
physical_design	物理设计运行目录
QRC_Tech	QRC 工艺文件
rtl	RTL 级代码，Verilog 文件
simulation	代码仿真运行目录
STA	静态时序分析运行目录

实　验　报　告

评分：

信 院 系 17 级　姓名 胡 睿　日期 2021-01-13　NO.

synthesis　　逻辑综合运行目录

【实验代码】

```
1.  `timescale 1ns/10ps
2.
3.  module multiplier(clk,rst,a,b,c);
4.      input clk;
5.      input rst;
6.      input [31:0] a;
7.      input [31:0] b;
8.      reg  [31:0] a_reg;
9.      reg  [31:0] b_reg;
10.     output reg [63:0] c;
11.
12. always@(posedge clk)
13.     begin
14.         if(rst)
15.             c=0;
16.         else
17.         begin
18.             a_reg<=a;
19.             b_reg<=b;
20.             c=a_reg*b_reg;
21.         end
22.     end
23.
24. endmodule
```

【代码仿真】

一、图形模式运行仿真

$ setdt incisive

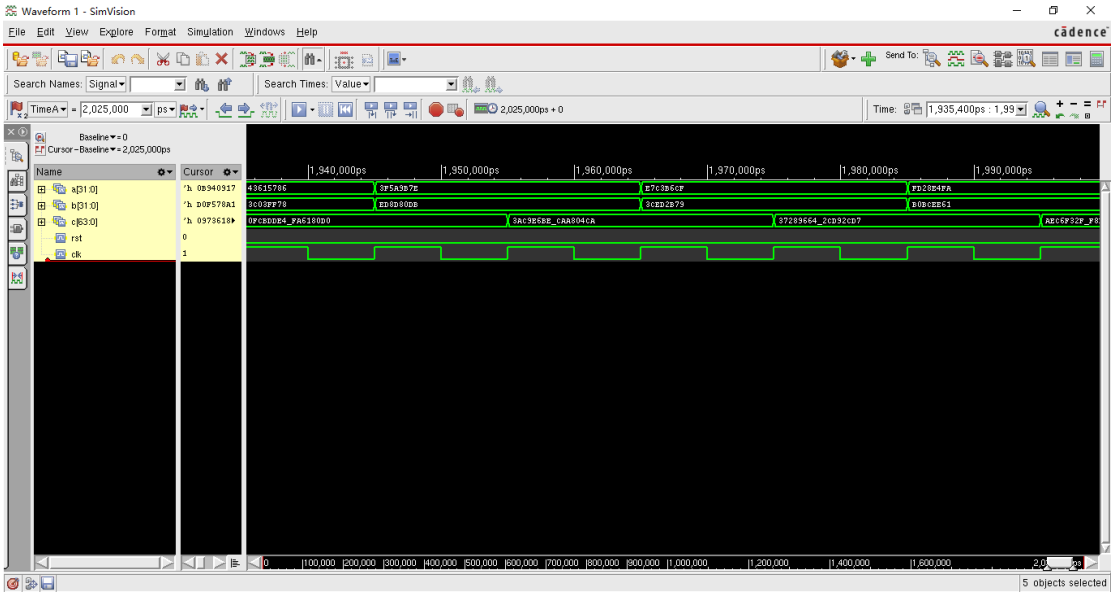
$ cd multiplier_design_database_45nm/simulation

$ irun multiplier.v multiplier.v -access +rwc – gui

实　验　报　告

评分：

信 院 系 17 级　姓名 胡 睿　日期 2021-01-13　NO.



使用计算器对波形结果进行验证：

二、批处理模式运行仿真

```
$ irun -clean

$ rm  – rf irun.* waves.shm

$ irun counter.v counter_test.v -access +rwc
```

实　验　报　告

评分：

信 院 系 17 级　姓名 胡 睿　日期 2021-01-13　NO.

```
PASS: a=f3e301, b=6d7cd0d, c=684e90501540d
PASS: a=3b23f176, b=1e8dcd3d, c=70ef881b1ea071e
PASS: a=76d457ed, b=462df78c, c=209366461f9ec09c
PASS: a=7cfde9f9, b=e33724c6, c=6ef012f970c8fa96
PASS: a=e2f784c5, b=d513d2aa, c=bce9849c86e6c4d2
PASS: a=72aff7e5, b=bbd27277, c=5424d1b54d0a3573
PASS: a=8932d612, b=47ecdb8f, c=268c09e7771efa0e
PASS: a=793069f2, b=e77696ce, c=6d92d34e16950cbc
PASS: a=f4007ae8, b=e2ca4ec5, c=d8293ff5b4e14488
PASS: a=2e58495c, b=de8e28bd, c=284a4bf67bac88ec
PASS: a=96ab582d, b=b2a72665, c=692583aeb00b77c1
PASS: a=b1ef6263, b=573870a, c=3c9f95151b50cde
PASS: a=c03b2280, b=10642120, c=c4ee22120d6d000
PASS: a=557845aa, b=cecccc9d, c=450b283691be3142
PASS: a=cb203e96, b=8983b813, c=6d1cc50c8d227522
PASS: a=86bc380d, b=a9a7d653, c=594a96962b5c0a37
PASS: a=359fdd6b, b=eaa62ad5, c=3126ef0639b8c807
PASS: a=81174a02, b=d7563eae, c=6c960c95ec6cc95c
PASS: a=effe91d, b=e7c572cf, c=d947d01a50d6873
PASS: a=11844923, b=509650a, c=5839fe2140aa5e
PASS: a=e5730aca, b=9e314c3c, c=8dc93001aad47f58
PASS: a=7968bdf2, b=452e618a, c=20cf3a467deb1674
PASS: a=20c4b341, b=ec4b34d8, c=1e3ef5a40a6b72d8
PASS: a=3c20f378, b=c48a1289, c=2e29a8859d70bb38
PASS: a=75c50deb, b=5b0265b6, c=29de26471d6b9c12
PASS: a=634bf9c6, b=571513ae, c=21c6febfe86b7694
PASS: a=de7502bc, b=150fdd2a, c=124d62441792bed8
PASS: a=85d79a0b, b=b897be71, c=60824c74dcfc28db
PASS: a=42f24185, b=27f2554f, c=a72474c4b3d610b
PASS: a=9dcc603b, b=1d06333a, c=11e3f94467db8e5e
PASS: a=bf23327e, b=aaa4b15, c=7f68567715a0e56
PASS: a=78d99bf1, b=6c9c4bd9, c=33459632e400ca49
PASS: a=31230762, b=2635fb4c, c=7558f9501ed4718
PASS: a=4fa1559f, b=47b9a18f, c=164f7c96eaded2d1
PASS: a=7c6da9f8, b=dbcd60b7, c=6ad5a33a55b98048
PASS: a=cfc4569f, b=ae7d945c, c=8d9d5e268a460d24
PASS: a=adcbc05b, b=44de3789, c=2ec0fb7cc3477db3
PASS: a=a4ae3249, b=e8233ed0, c=955489cb05b18950
PASS: a=ebfec0d7, b=a8c7fc51, c=9b978a2e708fa807
PASS: a=4b212f96, b=61d7f0c, c=1cb6f28e427a508
PASS: a=e12ccec2, b=6457edc8, c=5842d82472592190
PASS: a=bb825a77, b=1ef2ed3d, c=16ab3597d24db95b
PASS: a=90cdb12, b=bf05007e, c=6c0c4b729add2dc
PASS: a=36e5816d, b=1cd9e739, c=62fd447f2482c45
PASS: a=fd28f1f, b=e9ebf6d3, c=e7539cdf888c08d
PASS: a=42d92f85, b=bc148878, c=311cdb801970ee58
PASS: a=2dda595b, b=248b4b49, c=68ba79b5bda23f3
PASS: a=9ff2ae3f, b=150caf2a, c=d26d51c78e1a756
PASS: a=2c156358, b=c33f3886, c=219f2dab3b954010
PASS: a=c71a0c8e, b=ce2ff29c, c=a05c409285cfe288
PASS: a=7d3599fa, b=937dbc26, c=4823469cb01a731c
PASS: a=39961773, b=d18bb4a3, c=2f22f645d17eca39
PASS: a=9799a82f, b=d9d292b3, c=80fdf27b6fe966dd
PASS: a=afd8565f, b=22290d44, c=1776ee3b2510c43c
PASS: a=7bf8fdf7, b=e59b36cb, c=6f30e5788b907cdd
PASS: a=f3091ae6, b=2d28db5a, c=2adf6364dd2636dc
PASS: a=14cfc129, b=f682e2ed, c=140a479029ae04f5
PASS: a=ed536cda, b=b29fb665, c=a598119720b2ee02
PASS: a=da8ae2b5, b=efbe94df, c=ccaa5bd1e7621fab
PASS: a=3cf11979, b=2231ff44, c=823ec4c4a934b24
PASS: a=e8740cd0, b=15090b2a, c=1319bb44a2e70a20
PASS: a=55f6adab, b=76fcf0e, c=27f4a3c240fc45a
PASS: a=6e5daddc, b=cd5ebc9a, c=5889dbee32d02658
PASS: a=fedf72fd, b=e1f102c3, c=e0f2572b804790b7
PASS: a=2b0eed56, b=2779e94e, c=6a3c773fc359634
PASS: a=b3d97667, b=8531340a, c=5d928bb25f428c06
PASS: a=5b6fb9b6, b=9c0e8a38, c=37bd46a54a80bbd0
PASS: a=3cd18779, b=dc2bc4b8, c=344e7659dfa502f8
PASS: a=4a74bf94, b=49c65d93, c=1574fc248b1ac5fc
PASS: a=823f2c04, b=acb7ca59, c=57dff3ae478d7564
PASS: a=6dcb69db, b=a6fcde4d, c=479e5a37a18ec0df
PASS: a=6cb0b7d9, b=b6a4266d, c=4d8b543a8f8c7d65
PASS: a=bb45e276, b=653b49ca, c=4a0df16e71ea571c
PASS: a=5b172db6, b=4a937195, c=1a8929f01b2cf0ee
PASS: a=a3071a46, b=2749b04, c=19050244cbccb18
PASS: a=7bd261f7, b=34980769, c=19704465e09fef4f
PASS: a=da6ebab4, b=44018d88, c=3a06bcc9925c53a0
PASS: a=147cd928, b=9690042d, c=c0cadcd23d6cc08
PASS: a=e3c530c7, b=975c9c2e, c=86abb597ffac07c2
PASS: a=8477e408, b=e41451c, c=76054ac239b18e0
PASS: a=fea7a6fd, b=149e0729, c=14824ba43290a985
PASS: a=8e37901c, b=43356786, c=255635baf5dcb2a8
PASS: a=ed3408da, b=9eb7c63d, c=93106557a414b7f2
PASS: a=334ea766, b=b855c470, c=24f1b8cd8f7154a0
PASS: a=b9f50473, b=5d7199ba, c=43e0876f4970f68e
PASS: a=2f3ab35e, b=7d4779fa, c=171cd95d832c97cc
PASS: a=6a8e05d5, b=8d24f61a, c=3abf9b9e6efb45a2
PASS: a=dcf000b9, b=1b876137, c=17c2268a4c6540bf
PASS: a=4b273796, b=603921c0, c=1c3f7a7c0bfa0680
PASS: a=13259f26, b=db461ab6, c=10666d6e754d0104
PASS: a=3e99837d, b=6e5f0fdc, c=1afd35584c04526c
PASS: a=43615786, b=3c03ff78, c=fcbdde4fa6180d0
PASS: a=3f5a9b7e, b=ed8d80db, c=3ac9e6becaa804ca
PASS: a=e7c3b6cf, b=3ced2b79, c=372896642cd92cd7
PASS: a=fd28e4fa, b=b0bcee61, c=aec6f32ff8f72eba
PASS: a=b940917, b=d0f578a1, c=97361840f5f7f77
Simulation complete via $finish(1) at time 2025 NS + 0
./multiplier_test.v:43      $finish;
ncsim> exit
[PB17061124@mgt simulation]$ ls
INCA_libs  cleanup_dirs  irun.history  irun.log  multiplier.v  multiplier_test.v
[PB17061124@mgt simulation]$
```

三、逻辑综合

$ cd counter_design_database_45nm/synthesis

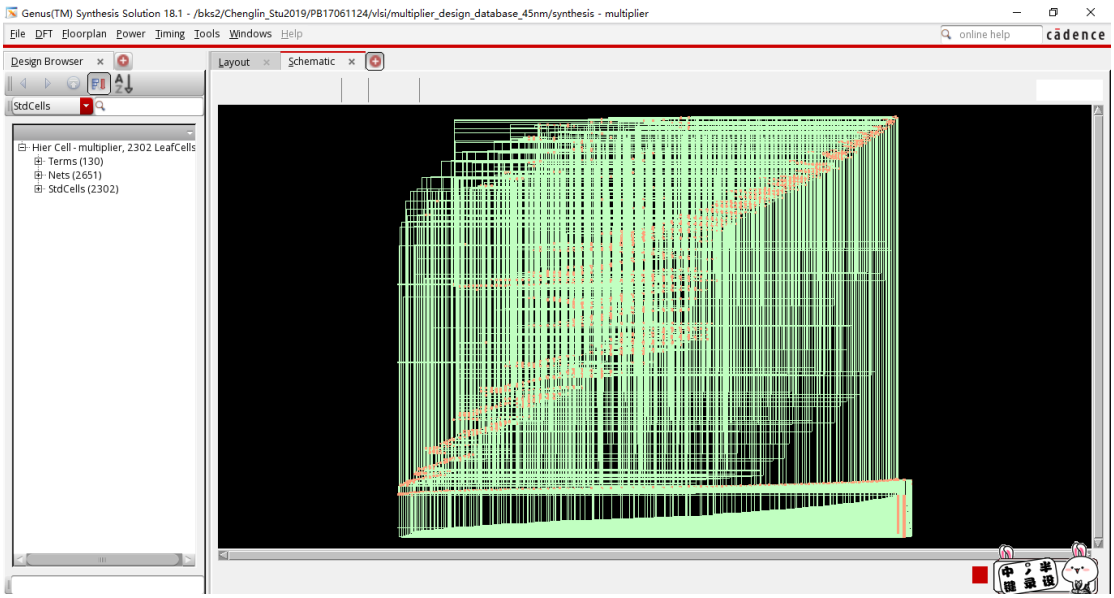
$ setdt genus

@genus> gui_show

实　验　报　告

评分：

信 院 系 17 级　姓名 胡 睿　日期 2021-01-13　NO.




```
@genus:root: 13> report_timing
Warning : Possible timing problems have been detected in this design. [TIM-11]
        : The design is 'multiplier'.
        : Use 'report timing -lint' for more information.
============================================================
  Generated by:           Genus(TM) Synthesis Solution 18.10-p003_1
  Generated on:           Jan 13 2021  11:25:02 pm
  Module:                 multiplier
  Operating conditions:   PVT_0P9V_125C (balanced_tree)
  Wireload mode:          enclosed
  Area mode:              timing library
============================================================


Path 1: MET (2 ps) Setup Check with Pin c_reg[63]/CK->D
          Group: clk
     Startpoint: (R) b_reg_reg[8]/CK
          Clock: (R) clk
       Endpoint: (R) c_reg[63]/D
          Clock: (R) clk

                    Capture       Launch
       Clock Edge:+   10000            0
      Src Latency:+       0            0
      Net Latency:+       0 (I)        0 (I)
          Arrival:=   10000            0

              Setup:-      96
        Uncertainty:-      10
     Required Time:=    9894
      Launch Clock:-       0
         Data Path:-    9891
             Slack:=       2

#-------------------------------------------------------------------------------------------------
-------
#      Timing Point        Flags    Arc   Edge   Cell     Fanout Load Trans Delay Arrival In
stance
#                                                           (fF)  (ps)  (ps)   (ps)  Lo
cation
#-------------------------------------------------------------------------------------------------
-------
  b_reg_reg[8]/CK          -       -     R     (arrival)    128    -   100     -       0
 (-,-)
  b_reg_reg[8]/Q           -       CK->Q R     SDFFQX1       36  7.8   172   308     308
 (-,-)
  mul_20_11_g23285/Y       -       A->Y  F     INVX1         41  9.2   266   237     544
 (-,-)
  g23547/Y                 -       A1->Y F     OA22X1         2  0.9    46   277     822
 (-,-)
  mul_20_11_g22725/Y       -       A->Y  R     NOR2X2        30 10.6   259   186    1008
 (-,-)
  mul_20_11_g22705/Y       -       A->Y  F     INVX1          5  2.0   105   192    1200
 (-,-)
  mul_20_11_g22464/Y       -       A1->Y R     OAI22X1        1  0.2    84   106    1306
 (-,-)
  g23533/Y                 -       B0->Y F     AOI2BB1XL      1  0.4    52    87    1393
```

实　验　报　告

评分：

信 院 系 17 级　姓名 胡 睿　日期 2021-01-13　NO.

report_timing 命令运行结果中的部分数据

Critical Path	Value
Group	clk
Start Point	b_reg_reg[8]/CK
End Point	c_reg[63]/D
Clock Edge (ps)	capture+10000 launch0
Require Time (ps)	9894
Data Path Delay (ps)	9891
Slack (ps)	2

```
@genus:root: 14> report_power
============================================================
  Generated by:           Genus(TM) Synthesis Solution 18.10-p003_1
  Generated on:           Jan 13 2021  11:36:25 pm
  Module:                 multiplier
  Operating conditions:   PVT_0P9V_125C (balanced_tree)
  Wireload mode:          enclosed
  Area mode:              timing library
============================================================

                  Leakage    Dynamic     Total
 Instance   Cells Power(nW)  Power(nW)  Power(nW)
------------------------------------------------------------
multiplier   2302   122.063 559212.846 559334.909

@genus:root: 15>
```

report_power 命令运行结果中的部分数据

Item	Value
Instance	multiplier
Cells	2302
Leakage Power (nW)	122.063
Dynamic Power (nW)	559212.846
Total Power (nW)	559334.909

实　验　报　告

评分：

信 院 系 17 级　姓名 胡 睿　日期 2021-01-13　NO.

```
@genus:root: 15> report_qor
============================================================
  Generated by:           Genus(TM) Synthesis Solution 18.10-p003_1
  Generated on:           Jan 13 2021  11:39:53 pm
  Module:                 multiplier
  Operating conditions:   PVT_0P9V_125C (balanced_tree)
  Wireload mode:          enclosed
  Area mode:              timing library
============================================================

Timing
--------

Clock  Period
-------------
clk   10000.0


  Cost    Critical         Violating
 Group   Path Slack  TNS     Paths
-------------------------------------
clk            2.4   0.0         0
default    No paths   0.0
-------------------------------------
Total                0.0         0

Instance Count
--------------
Leaf Instance Count             2302
Physical Instance count            0
Sequential Instance Count        128
Combinational Instance Count    2174
Hierarchical Instance Count        0

Area
----
Cell Area                          6119.064
Physical Cell Area                 0.000
Total Cell Area (Cell+Physical)    6119.064
Net Area                           0.000
Total Area (Cell+Physical+Net)     6119.064

Max Fanout                         128 (clk)
Min Fanout                         1 (c[0])
Average Fanout                     2.7
Terms to net ratio                 3.6658
Terms to instance ratio            4.2215
Runtime                            75.572517 seconds
Elapsed Runtime                    1208 seconds
Genus peak memory usage            795.84
Innovus peak memory usage          no_value
Hostname                           c01n09
@genus:root: 16>
```

report_qor 命令运行结果中的部分数据

Item	Value
Clock Period (ps)	10000.0
Critical Path Slack (ps)	2.4
Total Negative Slack (TNS) (ps)	0.0

实　验　报　告

评分：

信 院 系 17 级　姓名 胡 睿　日期 2021-01-13　NO.

Sequential Instance Count	128
Combinational Instance Count	2174
Total Area (um^2)	6119.064
Max Fanout	128(clk)
Min Fanout	1(c[0])
Average Fanout	2.7

逻辑综合脚本：

```
set_db init_lib_search_path ../lib/
set_db init_hdl_search_path ../rtl/
read_libs slow_vdd1v0_basicCells.lib

read_hdl counter.v
elaborate
read_sdc ../constraints/constraints_top.sdc

set_db syn_generic_effort medium
set_db syn_map_effort medium
set_db syn_opt_effort medium

syn_generic
syn_map
syn_opt

write_hdl > multiplier_netlist.v
write_sdc > multiplier_sdc.sdc
write_sdf -timescale ns -nonegchecks -recrem split -edges check_edge  -
setuphold split > delays.sdf
```

扫描插入脚本：

```
set_db init_lib_search_path ../lib/
set_db init_hdl_search_path ../rtl/
read_libs slow_vdd1v0_basicCells.lib
read_hdl multiplier.v
elaborate
read_sdc ../constraints/constraints_top.sdc

```

```
set_db dft_scan_style muxed_scan
set_db dft_prefix dft_
define_shift_enable -name SE -active high -create_port SE
check_dft_rules

set_db syn_generic_effort medium
syn_generic
set_db syn_map_effort medium
syn_map
set_db syn_opt_effort medium
syn_opt

check_dft_rules
set_db design:multiplier .dft_min_number_of_scan_chains 1
define_scan_chain -name top_chain -sdi scan_in -sdo scan_out -
create_ports

connect_scan_chains -auto_create_chains
syn_opt -incr

report_scan_chains
write_dft_atpg -library ../lib/slow_vdd1v0_basiccells.v
write_hdl > multiplier_netlist_dft.v
write_sdc > multiplier_sdc_dft.sdc
write_sdf -nonegchecks -edges check_edge -timescale ns -recrem split  -
setuphold split > dft_delays.sdf
write_scandef > multiplier_scanDEF.scandef
```

四、等价性检查

等价性检查脚本:

```
set log file counter_lec.log -replace
read library ../lib/slow_vdd1v0_basiccells.v -verilog -both
read design ../rtl/counter.v -verilog -golden
read design ../synthesis/counter_netlist_dft.v -verilog -revised
add pin constraints 0 SE  -revised
add ignored inputs scan_in -revised
add ignored outputs scan_out -revised
set system mode lec
add compare point -all
```

实　验　报　告

评分：

信 院 系 17 级　姓名　胡　睿　日期 2021-01-13　NO.

```
10. compare
```

set system mode lec 命令运行结果

Mapped points: SYSTEM class				
Mapped points	**PI**	**PO**	**DFF**	**Total**
Golden	**66**	**64**	**128**	**258**
Revised	**66**	**64**	**128**	**258**

compare 命令运行结果

Compared points	**PO**	**DFF**	**Total**
Equivalent	**64**	**76**	**140**
Abort	**0**	**52**	**52**

report verification 命令运行结果

Verification Report	
Category	**Count**
1. Non-standard modeling options used:	**0**
2. Incomplete verification:	**1**
3. User modification to design:	**0**
4. Conformal Constraint Designer clock domain crossing checks recommended:	**0**
5. Design ambiguity:	**0**
6. Compare Results:	**ABORT**

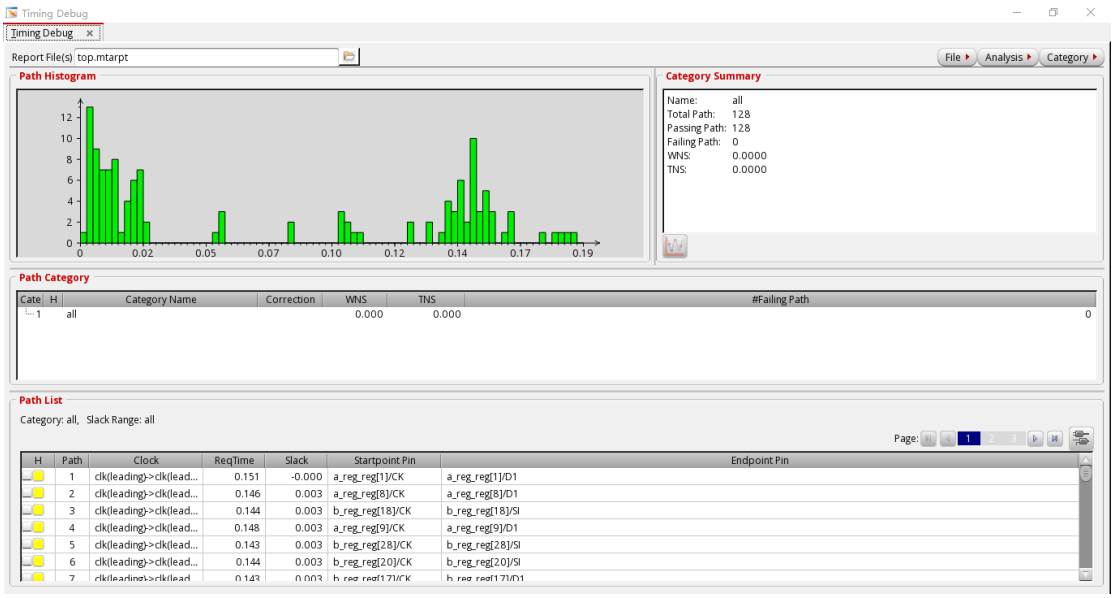
五、物理设计与时序调试

Timing Debug:

实　验　报　告

评分：

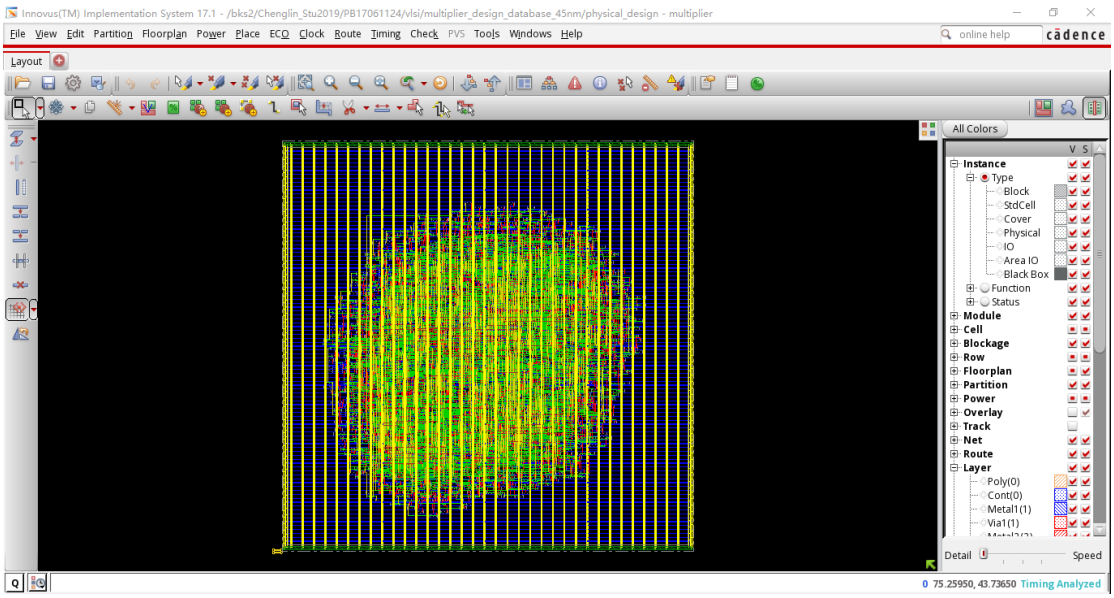
信 院 系 17 级　姓名 胡 睿　日期 2021-01-13　NO.



面积信息：

```
Area
----
Cell Area                          6337.260
Physical Cell Area                 0.000
Total Cell Area (Cell+Physical)    6337.260
Net Area                           0.000
Total Area (Cell+Physical+Net)     6337.260
```

新的版图：



电路图：

实　验　报　告

评分：

信 院 系 17 级　姓名 胡 睿　日期 2021-01-13　NO.