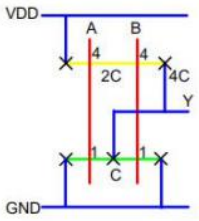
3.2 中 Hf02 的相对介电常数在不同的排列下不一样，所以只要式子对即可

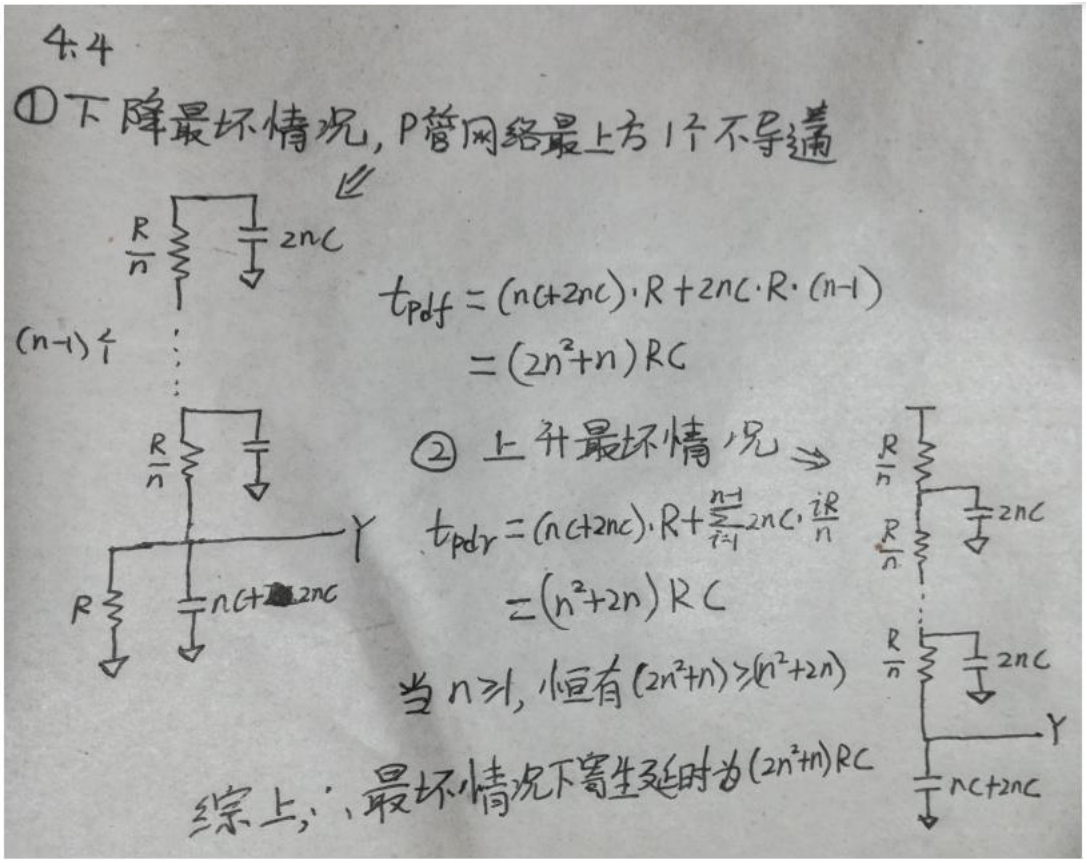
3.2 The answer to this question is based on the difference in dielectric constant between SiO_2 (k=3.9) and HfO_2 (k=20). The oxide thickness would be 2 nm*(20/3.9) = 10.26 nm.

3.6 Metal1 has a 2x2 contact with an overlap of 1 on each side, requiring a 4-λ width. The metal spacing is 3 λ, so the pitch is 7 λ if contacts can meet head to head.

A denser wiring strategy is to offset contacts. The pitch is reduced by half the distance that the contact extends beyond minimum metal width, thus giving a 6.5 λ pitch.

4.2 The rising delay is (R/2)*2C + R*(5C+5hC) = (6+5h)RC and the falling delay is R*2C+R*(5C+5hC) = (7+5h)RC.





4.10 (a) should be faster than (b) because the NAND has the same parasitic delay but lower logical effort than the NOR. In each design, $H = 6$, $B = 1$, $P = 1 + 2 = 3$. For (a), $G = (4/3) * 1 = (4/3)$. $F = GBH = 8$. $f = 8^{1/2} = 2.8$. $D = 2f + P = 8.6\ \tau$. $x = 6C * 1 / f = 2.14C$. For (b), $G = 1 * (5/3)$. $F = GBH = 10$. $f = 10^{1/2} = 3.2$. $D = 2f + P = 9.3\ \tau$. $x = 6C * (5/3) / f = 3.16C$.

4.20 NAND: $g = (\mu + k) / (\mu + 1)$; NOR: $g = (\mu k + 1) / (\mu + 1)$. As μ increases, NOR gates get worse compared to NAND gates because the series pMOS devices become more expensive.