Exercise

1. Setup the environment for the simulation

   Please refer to the tutorial **http://222.195.93.219/notes-2013/Servers.Login.Tutorial.pdf for how to** login the EDA server.

   Add the following lines to the file **.cshrc** in your home directory:

   alias setdt 'set toolsList = (\!*); source /soft1/eda/bin/setdt.csh'

   alias rm 'rm -i'

   alias vcs 'vcs -full64'

   % source .cshrc

   % setdt vcs // setup the vcs

2. Simulating a full adder

a) Copy the file **/js1/songch/DA_VLSI/DA_VLSI_Lab1.tgz** to your home directory.

b) Extract the files % **tar zxvf DA_VLSI_Lab1.tgz**

c) Build a simulator for the adder and do the simulation. (**step a to c** in the following tutorial)

d) Add a ***carry in*** (进位) to the adder defined in file and do the simulation

e) Add stimulus for the ***carry in*** port you added to the test bench.

3. Simulating a 4-to-1 multiplexer

a) Copy the file **/js1/songch/DA_VLSI/Multiplexor.tgz** to your home directory.

b) Extract the files % **tar zxvf Multiplexor.tgz,** and enter this directory.

c) Build a simulator for the 4-to-1 multiplexer and do the simulation. (**Step a to c** in the following tutorial)

4. Simulating a 16-to-1 multiplexer

a) Create the new verilog source file **mux16to1.v** and put your exercise 2: **Use 4-to-1 multiplexer module to build a 16-to-1 multiplexer module** source code into the file.

b) Create the new test bench file **mux16to1_test.v** for your 16-to-1 multiplexer module by reference to the origin test bench file **mux4to1_test.v**.

#tips: when using **vcs** to compile your 16-to-1 multiplexer module, you should include both **mux16to1.v** and **mux4to1.v**.

c) Build a simulator for the 16-to-1 multiplexer and do the simulation. (**Step a to c** in the following tutorial)

Please refer to **http://staff.ustc.edu.cn/~songch/da-ug.htm** for the following resources

1. Verilog-basics-1 for the Verilog HDL.

2. the Linux tutorial and simple vi manual, respectively, for the simple Linux command and use of **vi/ emacs/gedit(recommended)** editor.

Please read the **error** information carefully if any.

Tutorial on Simulation Full Adder

a) Type the compile command of vcs tool

```
% vcs -PP +lint=all +v2k -debug -line full_adder.v full_adder_test.v
```

//-PP compile the modules

//+lint=all link the modules

//+v2k: supporting Verilog IEE 1364-2001 syntax

//-debug add debug information, otherwise you cannot execute `./simv -gui`

//-line enable line callback

(You can use command `vcs -doc` for more information about tool vcs.)

The above command will build a simulator with a default name '**simv**' for your circuit.

b) Type the simulate command of vcs tool

```
% ./simv
```

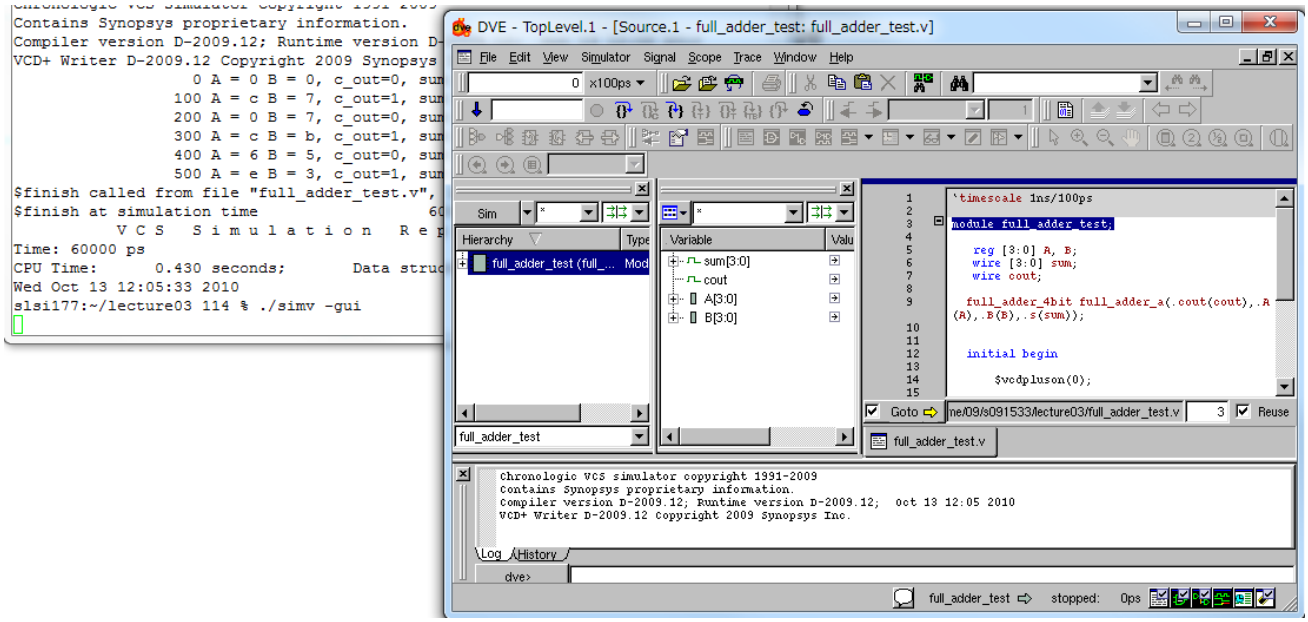
//get the simulation results and generate Database file

```
slsi177:~/lecture03 113 % ./simv
Chronologic VCS simulator copyright 1991-2009
Contains Synopsys proprietary information.
Compiler version D-2009.12; Runtime version D-2009.12;  Oct 13 01:41 2010
VCD+ Writer D-2009.12 Copyright 2009 Synopsys Inc.
                   0 A = 0 B = 0, c_out=0, sum = 0
                 100 A = c B = 7, c_out=1, sum = 3
                 200 A = 0 B = 7, c_out=0, sum = 7
                 300 A = c B = b, c_out=1, sum = 7
                 400 A = 6 B = 5, c_out=0, sum = b
                 500 A = e B = 3, c_out=1, sum = 1
$finish called from file "full_adder_test.v", line 25.
$finish at simulation time                  600
           V C S   S i m u l a t i o n   R e p o r t
Time: 60000 ps
CPU Time:      0.430 seconds;       Data structure size:   0.0Mb
Wed Oct 13 01:41:02 2010
slsi177:~/lecture03 114 %
```

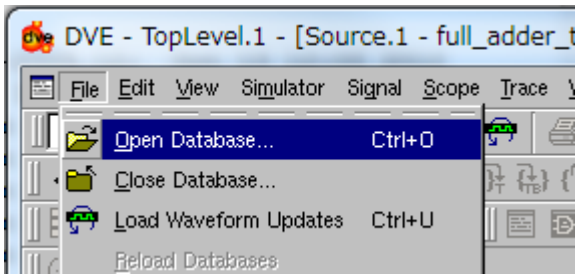
c) Check the waveform result

```
% ./simv -gui
```

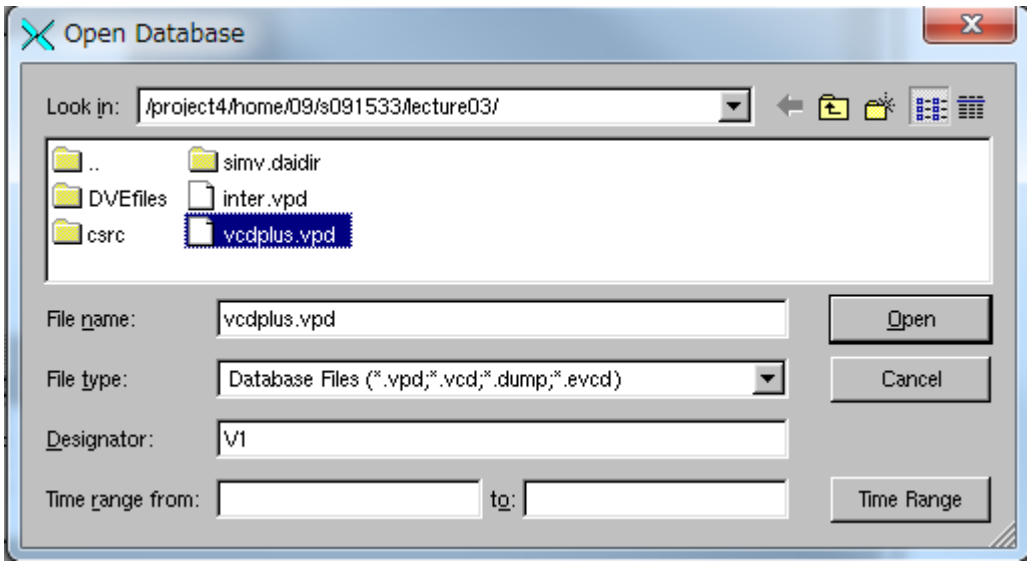
//effective only when you compile the sources using **-debug** option



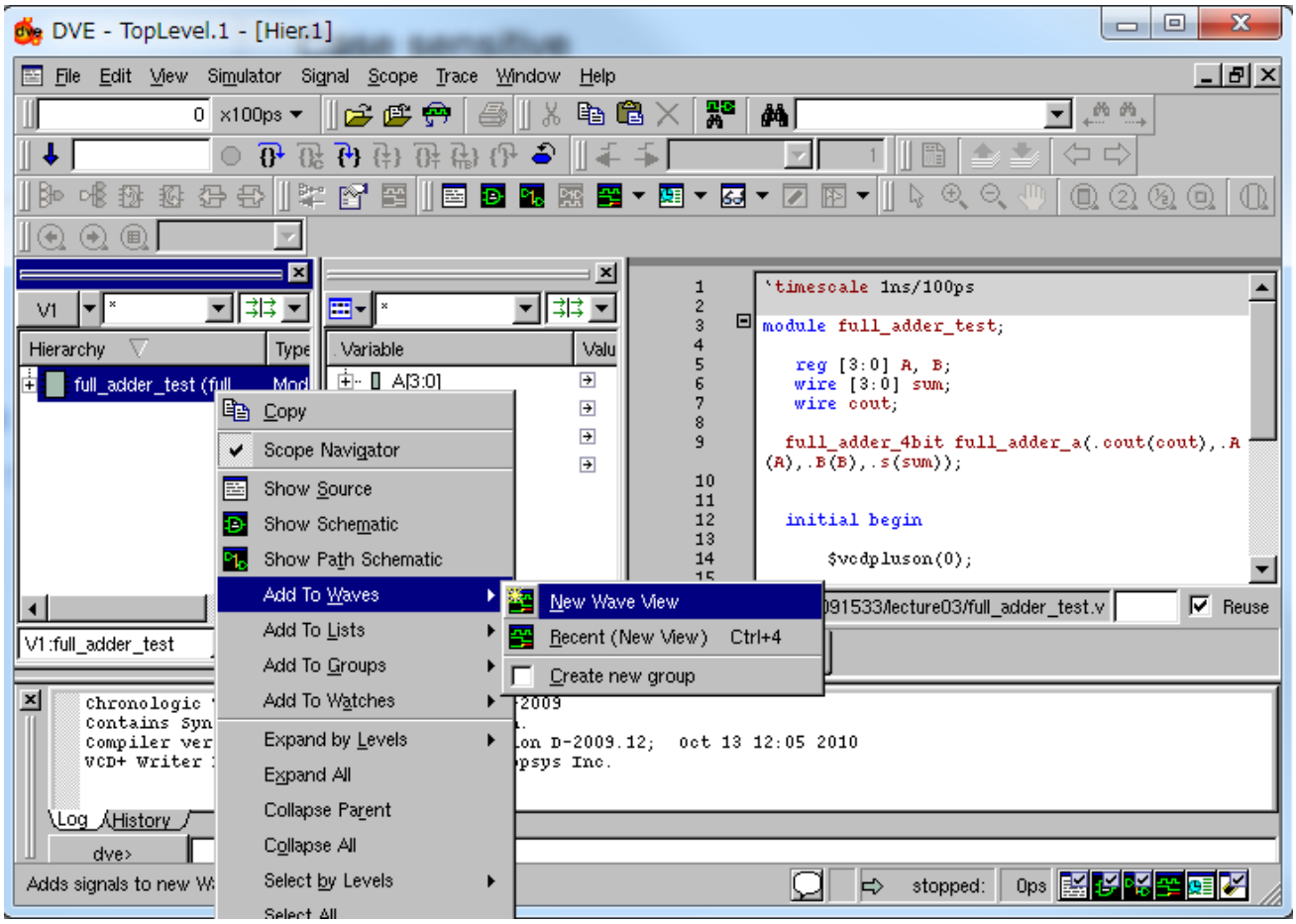
File→ Open Database



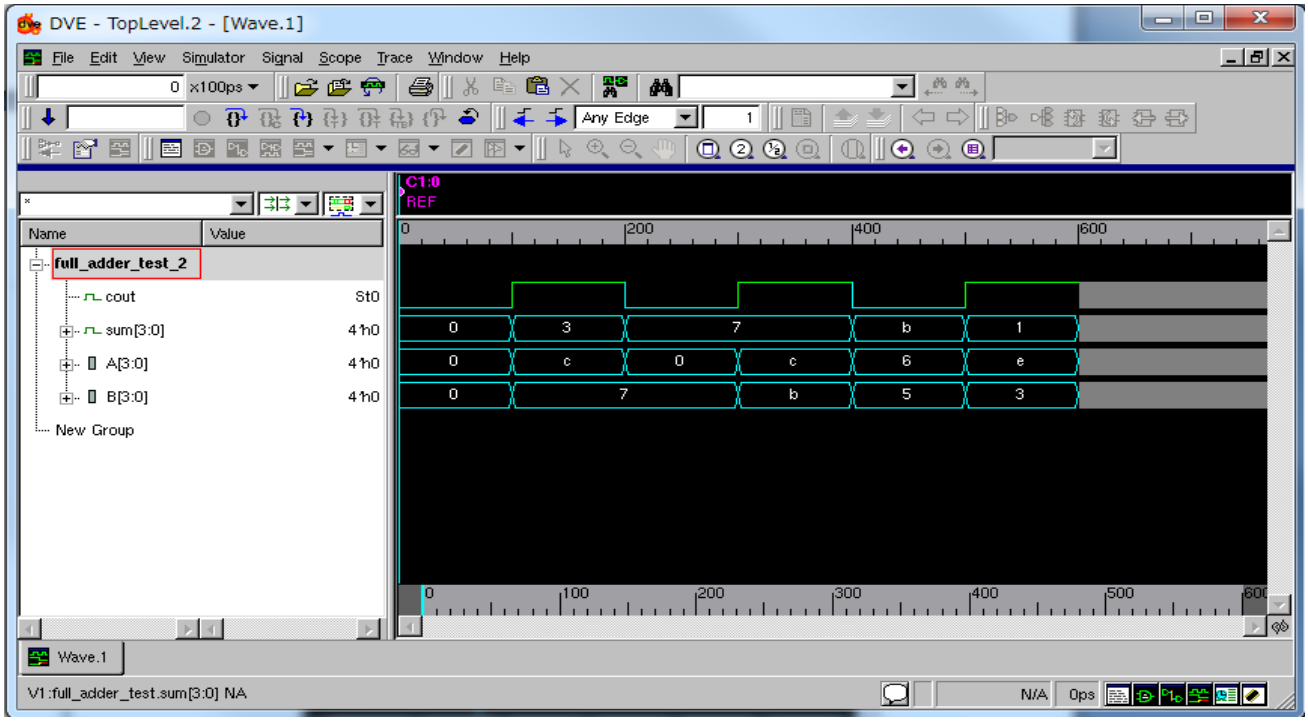
Choose **vcdplus.vpd**, click **open**



Add a wave view

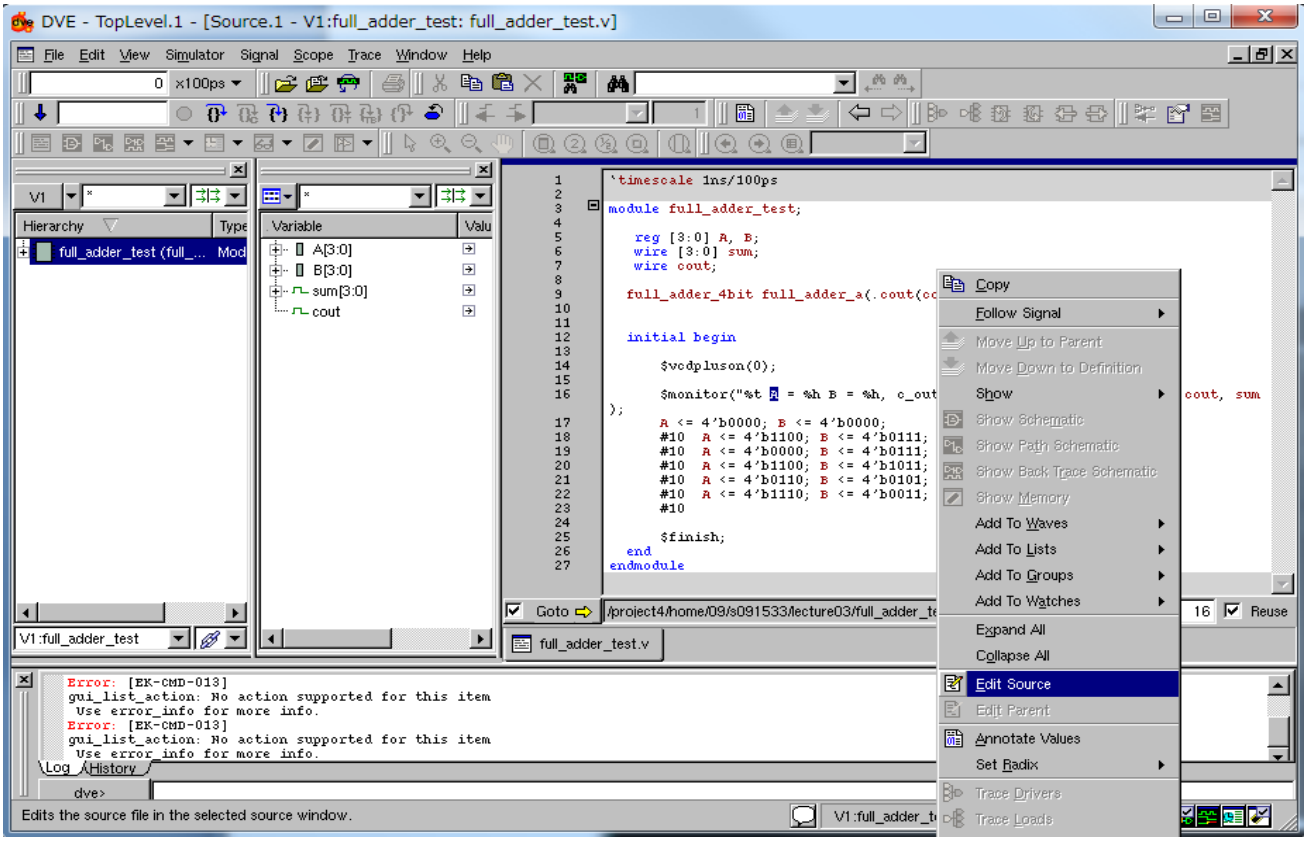


Then the following window will prompt out. You can push the button ② and ½ to zoom.

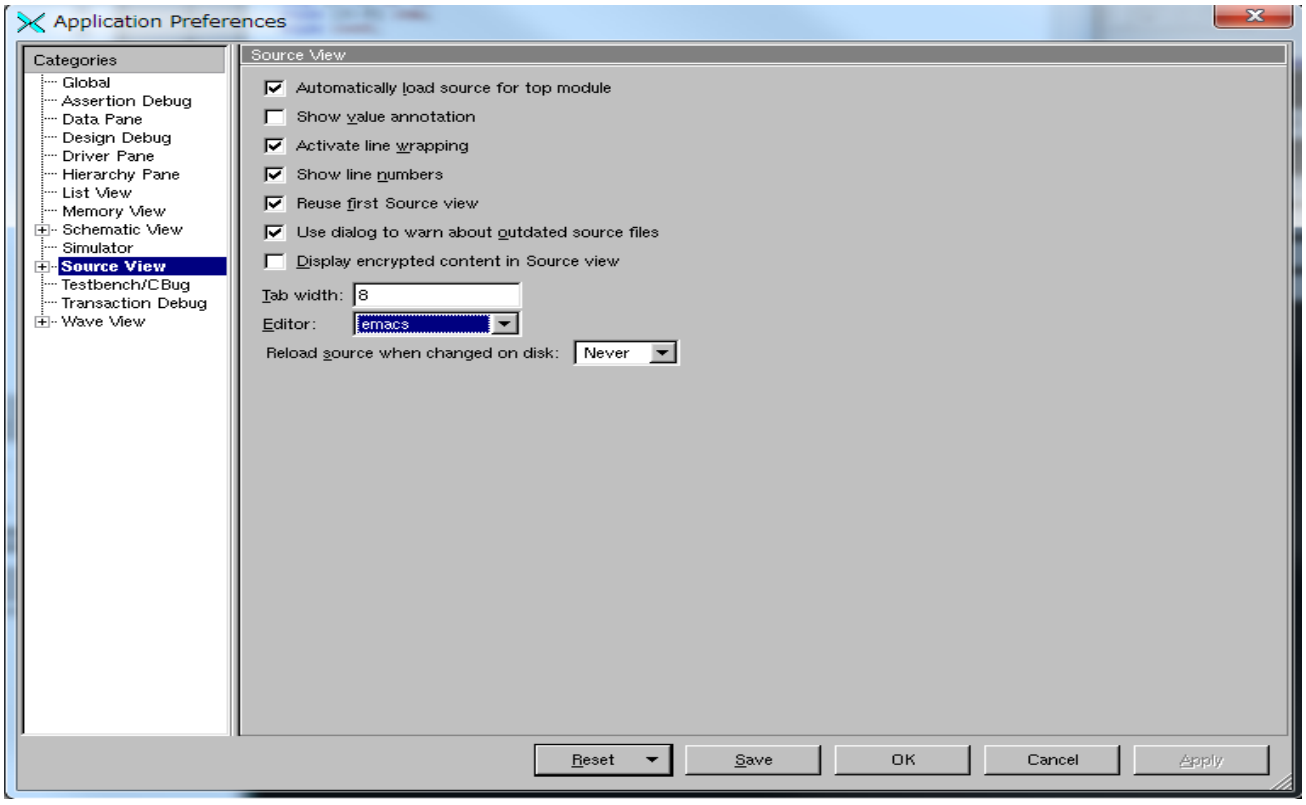


d) Debug----only used when you see a wrong waveform

Right-click the source text area and then choose **Edit Source**



The default editor is **vi.** You can change it by the menu **Edit→Preferences→Source view→Editor**



Tutorial on Simulation Multiplexer

a) Type the compile command of vcs tool

```
% vcs -PP +lint=all +v2k -debug -line mux4to1.v mux4to1_test.v
```

//-PP compile the modules

//+lint=all link the modules

//+v2k: supporting Verilog IEE 1364-2001 syntax

//-debug add debug information, otherwise you cannot execute ./simv -gui

//-line enable line callback

(You can use command vcs -doc for more information about tool vcs.)

The above command will build a simulator with a default name '**simv**' for your circuit.

b) Type the simulate command of vcs tool

```
% ./simv
```

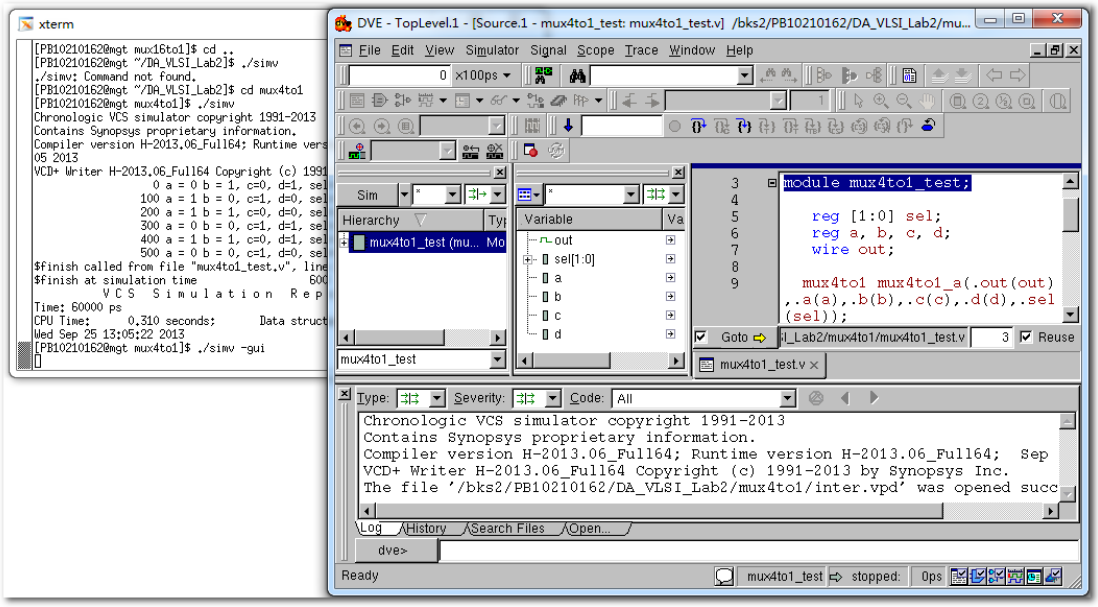
//get the simulation results and generate Database file

```
[PB10210162@mgt mux4to1]$ ./simv
Chronologic VCS simulator copyright 1991-2013
Contains Synopsys proprietary information.
Compiler version H-2013.06_Full64; Runtime version H-2013.06_Full64;  Sep 25 13:
05 2013
VCD+ Writer H-2013.06_Full64 Copyright (c) 1991-2013 by Synopsys Inc.
                   0 a = 0 b = 1, c=0, d=1, sel=0, out=0
                 100 a = 1 b = 0, c=1, d=0, sel=3, out=0
                 200 a = 1 b = 1, c=0, d=0, sel=2, out=0
                 300 a = 0 b = 0, c=1, d=1, sel=2, out=1
                 400 a = 1 b = 1, c=0, d=1, sel=1, out=1
                 500 a = 0 b = 0, c=1, d=0, sel=0, out=0
$finish called from file "mux4to1_test.v", line 25.
$finish at simulation time                  600
          V C S   S i m u l a t i o n   R e p o r t
Time: 60000 ps
CPU Time:      0.310 seconds;       Data structure size:   0.0Mb
Wed Sep 25 13:05:22 2013
```

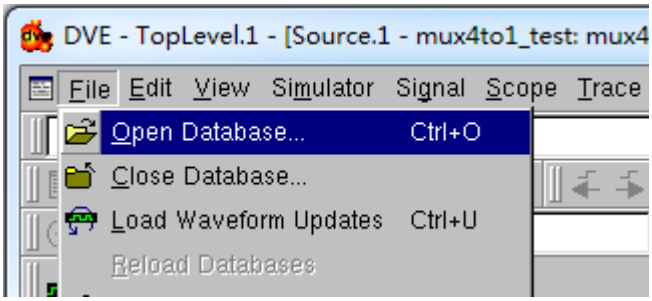
c) Check the waveform result

```
% ./simv -gui
```

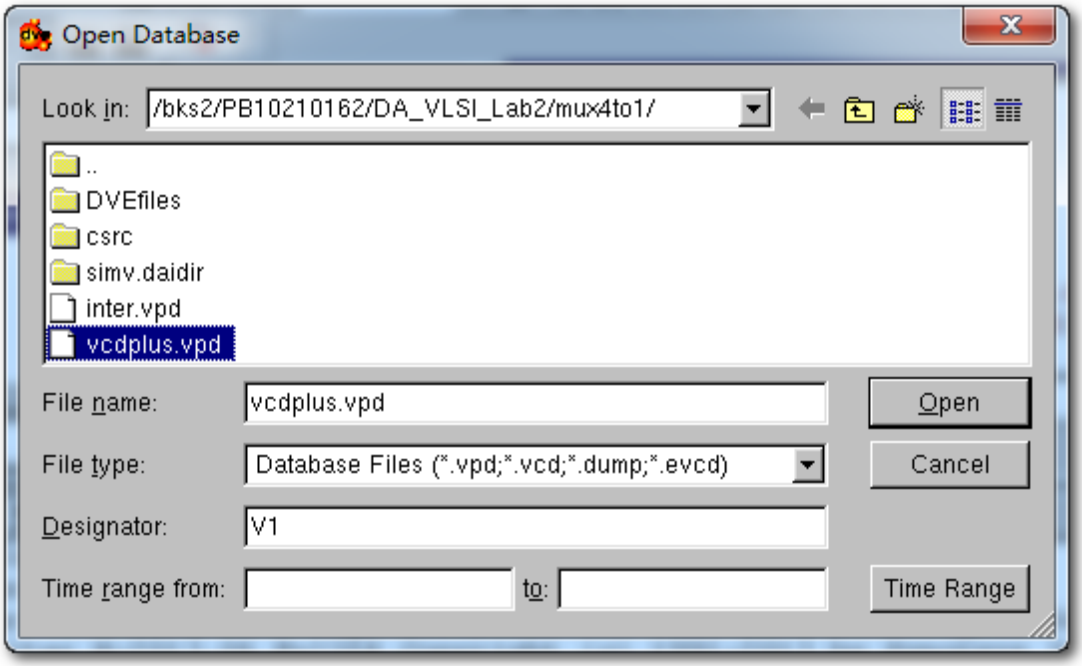
//effective only when you compile the sources using **-debug** option



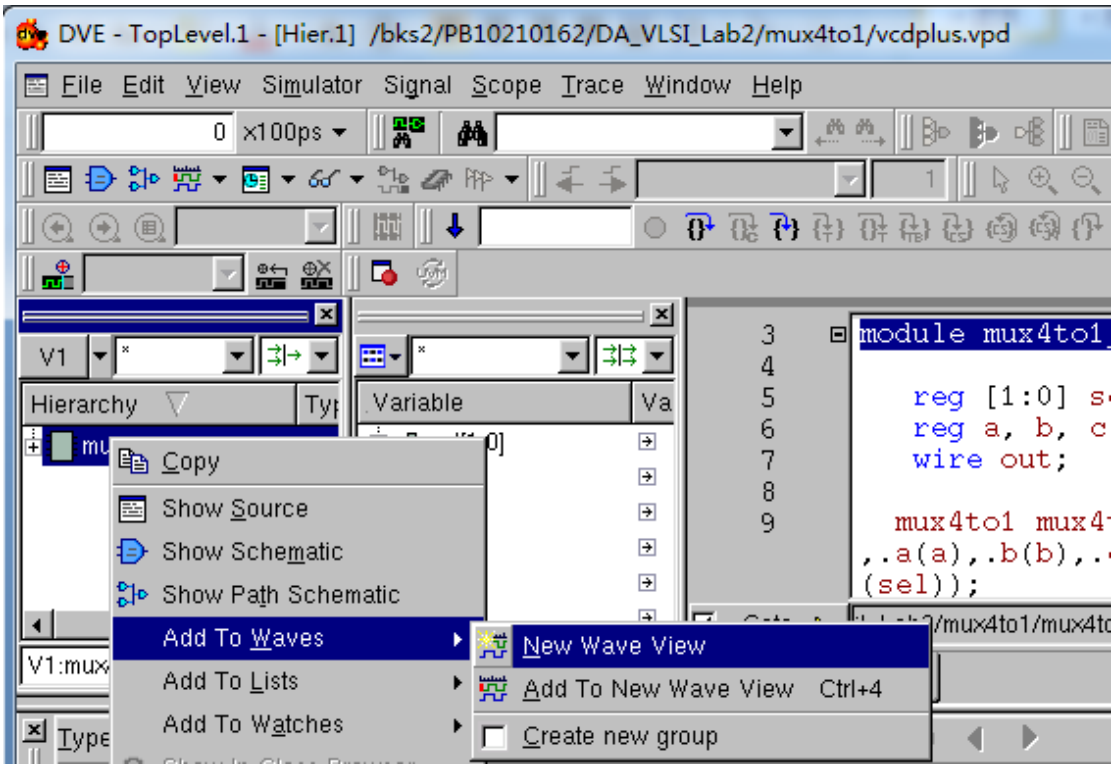
File☐ Open Database



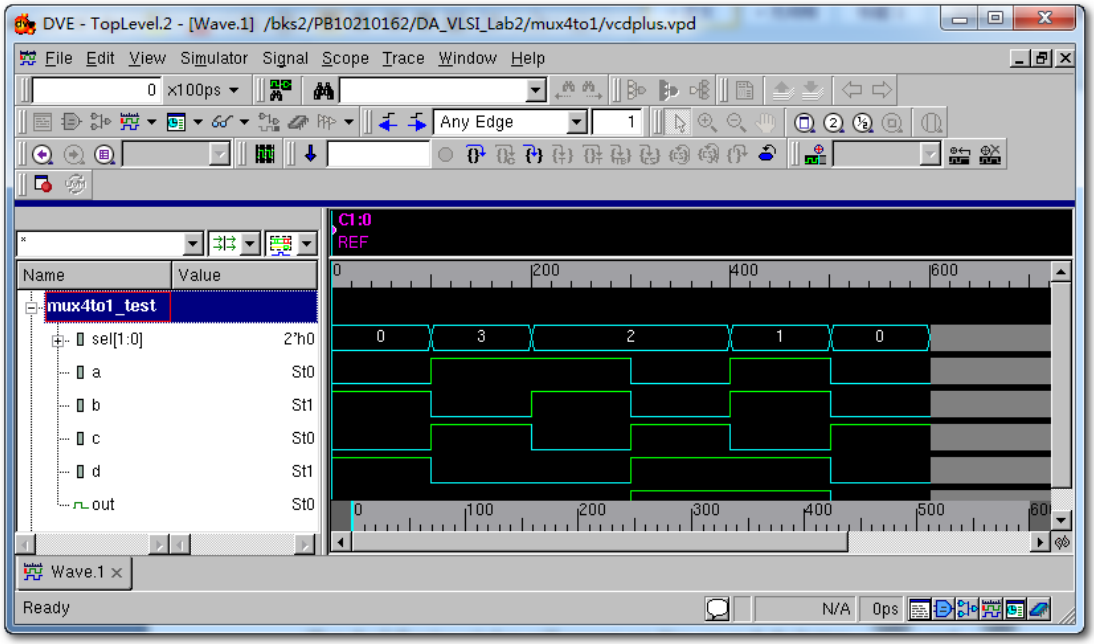
Choose **vcdplus.vpd**, click **open**



Add a wave view

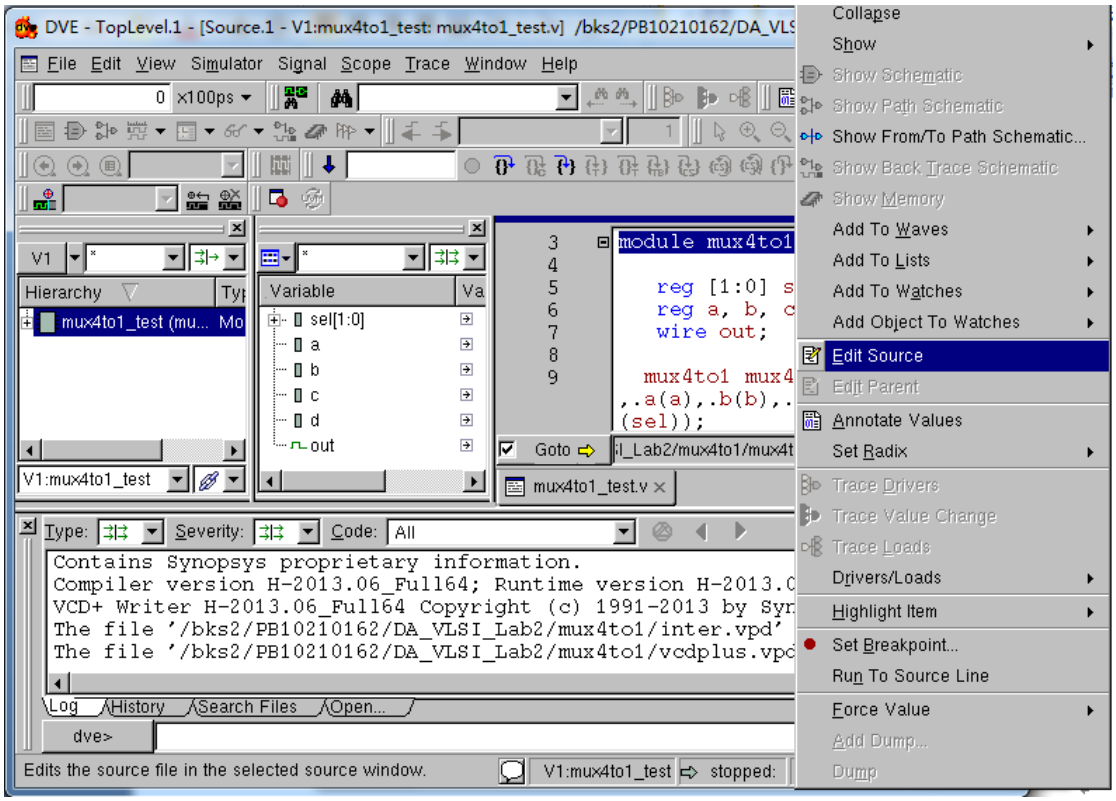


Then the following window will prompt out. You can push the button  and  to zoom.



d) Debug----only used when you see a wrong waveform

Right-click the source text area and then choose **Edit Source**


DVE - TopLevel.1 - [Source.1 - V1:mux4to1_test: mux4to1_test.v] /bks2/PB10210162/DA_VLS
File Edit View Simulator Signal Scope Trace Window Help
Hierarchy
mux4to1_test (mu... Mo
Variable
sel[1:0]
a
b
c
d
out
module mux4to1
reg [1:0] s
reg a, b, c
wire out;
mux4to1 mux4
,.a(a),.b(b),.
(sel));
Goto
mux4to1_test.v
Type: Severity: Code: All
Contains Synopsys proprietary information.
Compiler version H-2013.06_Full64; Runtime version H-2013.0
VCD+ Writer H-2013.06_Full64 Copyright (c) 1991-2013 by Syn
The file '/bks2/PB10210162/DA_VLSI_Lab2/mux4to1/inter.vpd'
The file '/bks2/PB10210162/DA_VLSI_Lab2/mux4to1/vcdplus.vpd
Log History Search Files Open...
dve>
Edits the source file in the selected source window.
V1:mux4to1_test
stopped:
Collapse
Show
Show Schematic
Show Path Schematic
Show From/To Path Schematic...
Show Back Trace Schematic
Show Memory
Add To Waves
Add To Lists
Add To Watches
Add Object To Watches
Edit Source
Edit Parent
Annotate Values
Set Radix
Trace Drivers
Trace Value Change
Trace Loads
Drivers/Loads
Highlight Item
Set Breakpoint...
Run To Source Line
Force Value
Add Dump...
Dump