Static Timing Analysis

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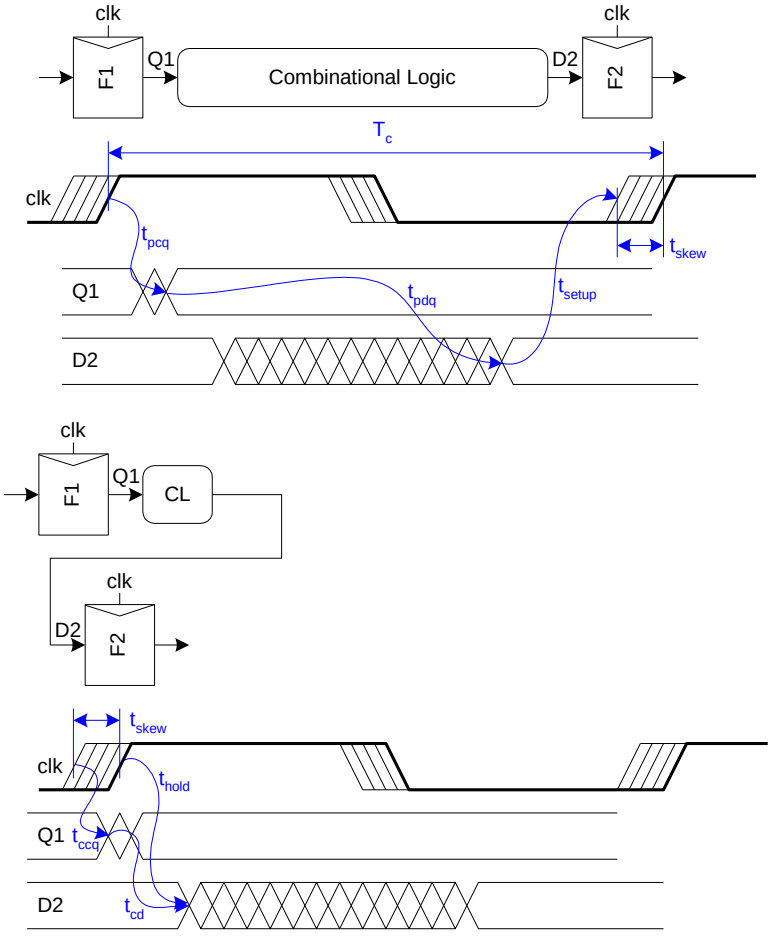
Skew: Flip-Flops

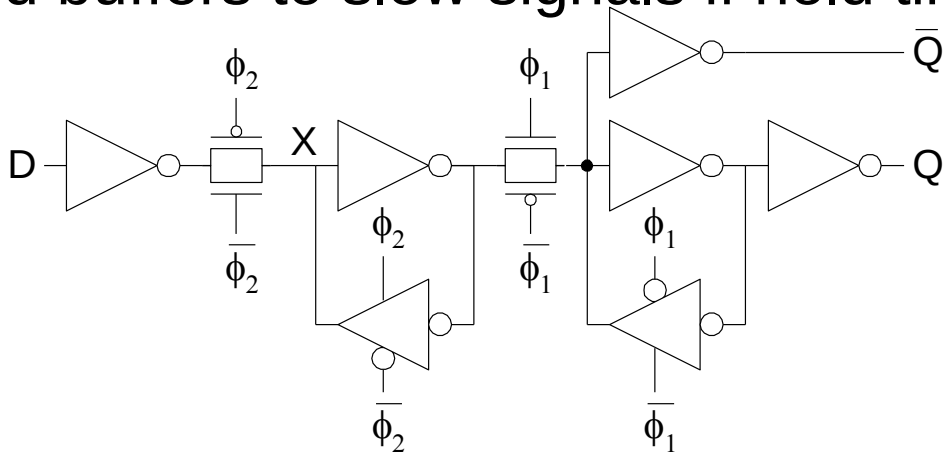
$$t_{pd} \leq T_c - \underbrace{\left(t_{pcq} + t_{\text{setup}} + t_{\text{skew}}\right)}_{\text{sequencing overhead}}$$

$$t_{cd} \geq t_{\text{hold}} - t_{ccq} + t_{\text{skew}}$$



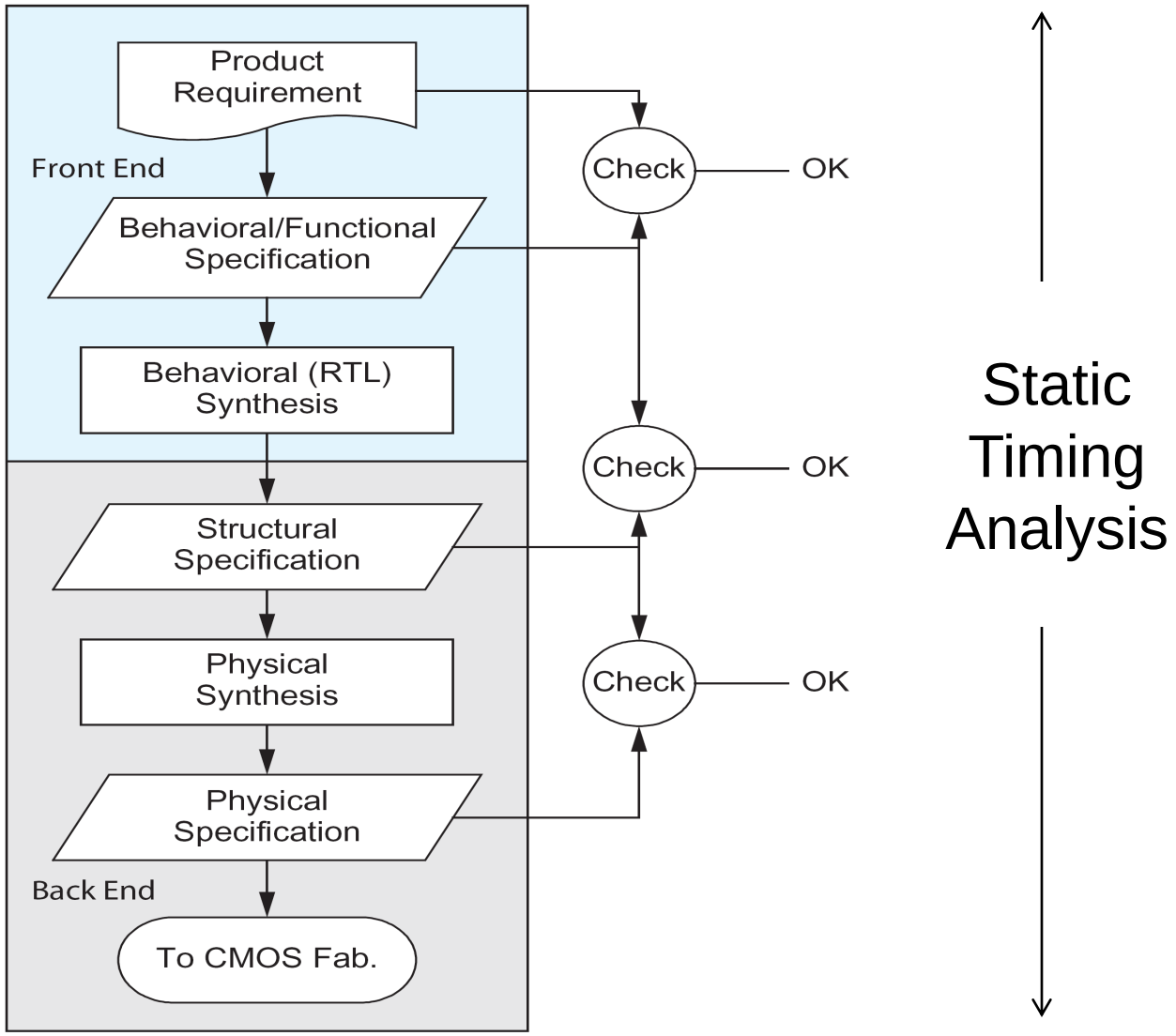
Safe Flip-Flop

- In industry, use a better timing analyzer
  - Add buffers to slow signals if hold time is at risk



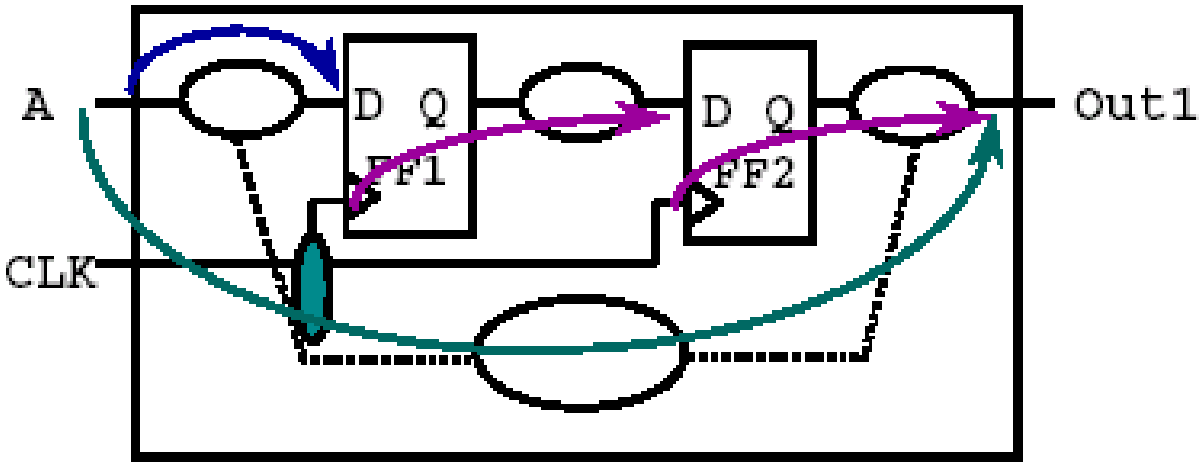
Pls. refer to [1].Chapter 10.3 for the circuit design of flip-flops and latches.

STA in ASIC Design Flow



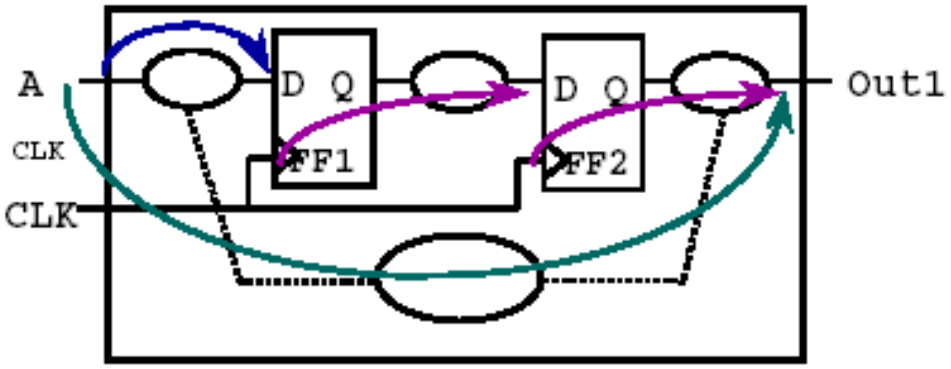
Three Steps in Static Timing Analysis

- Circuit is broken down into sets of timing paths
- Delay of each path is calculated
- Path delays are checked to see if timing constraints have been met



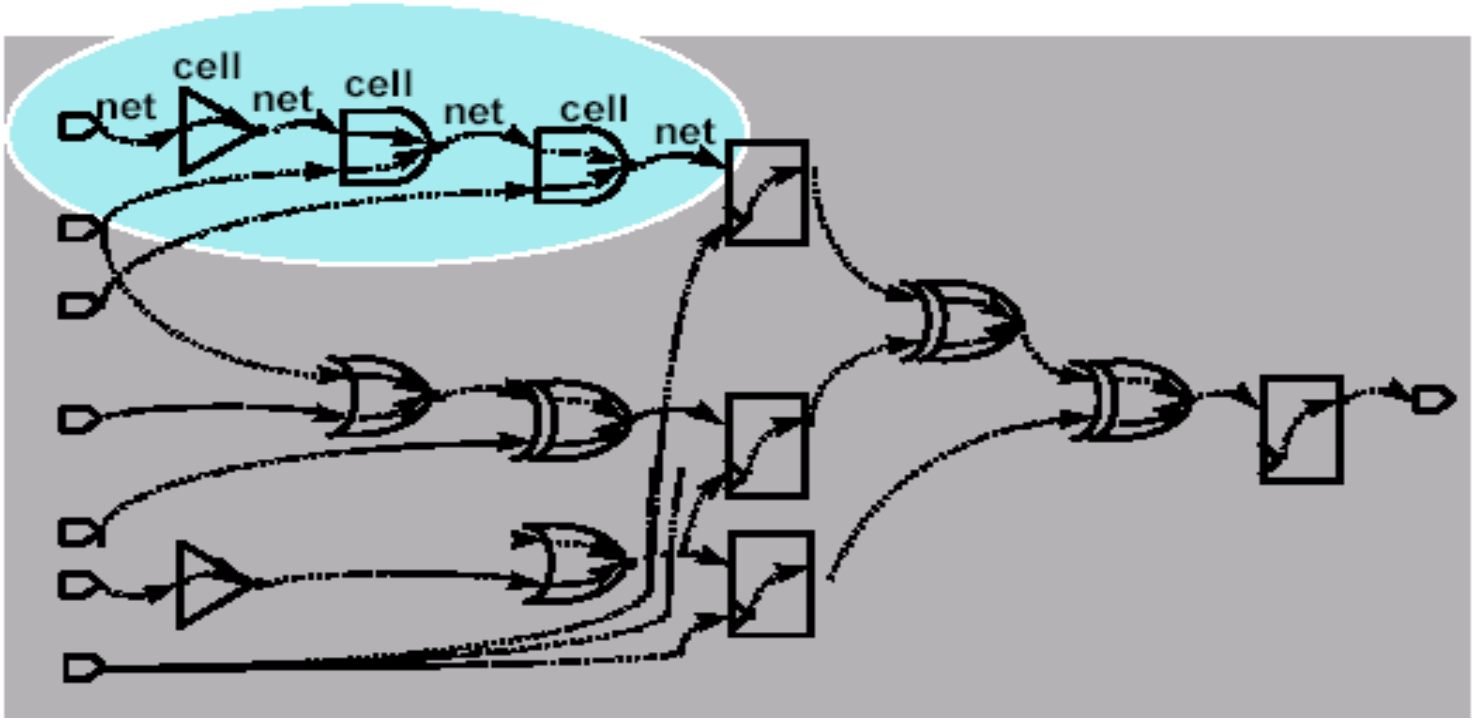
Timing Path

- A Timing Path is a point-to-point path in a design which can propagate data from one flip-flop to another
  - Each path has a start point and an endpoint
  - Start point: Input ports, Clock pins of flip-flops
  - End points: Output ports, Data input pins of flip-flops



Net and Cell Timing Arcs

- The actual path delay is the sum of net and cell delays along the timing path



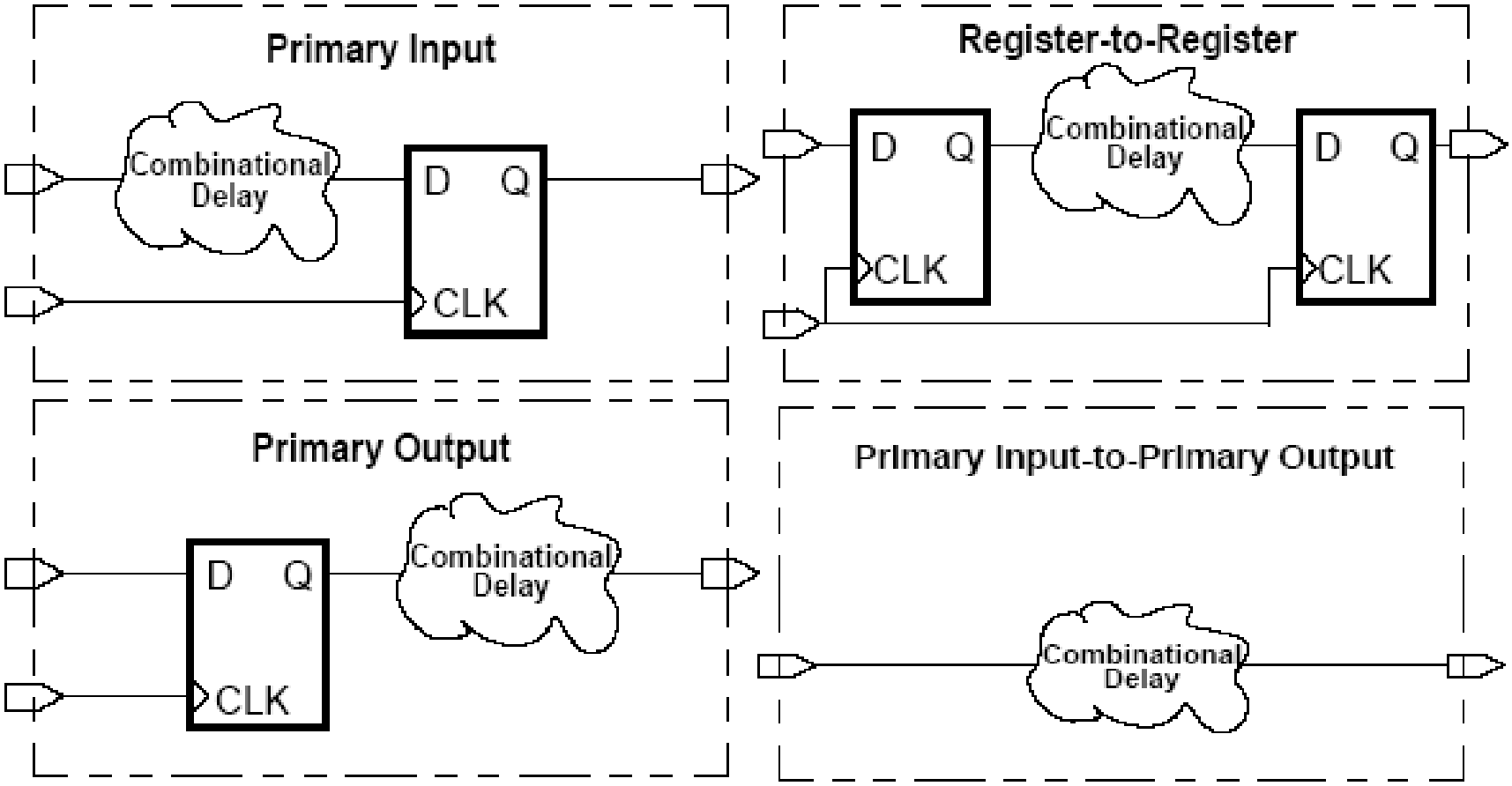
Net and Cell Delay

- "Net Delay" refers to the total time needed to charge or discharge all of the parasitics of a given net
  - Total net parasitics are affected by
    - net length
    - net fanout
  - Net delay and parasitics are typically
    - Back-Annotated (Post-Layout) from data obtained from an extraction tool
    - Estimated (Pre-Layout), wireload model
      - E.g., dc_shell in -*topograchical* mode

Slack and Critical Path

- Slack
  - It is the difference between the required (constraint) time and the arrival time (inputs and delays).
  - Negative slack indicates that constraints have not been met, while positive slack indicates that constraints have been met.
  - Slack analysis is used to identify timing critical paths in a design by the static timing analysis tool
- Critical path
  - Any logical path in the design that violates the timing constraints
  - Path with a negative slack

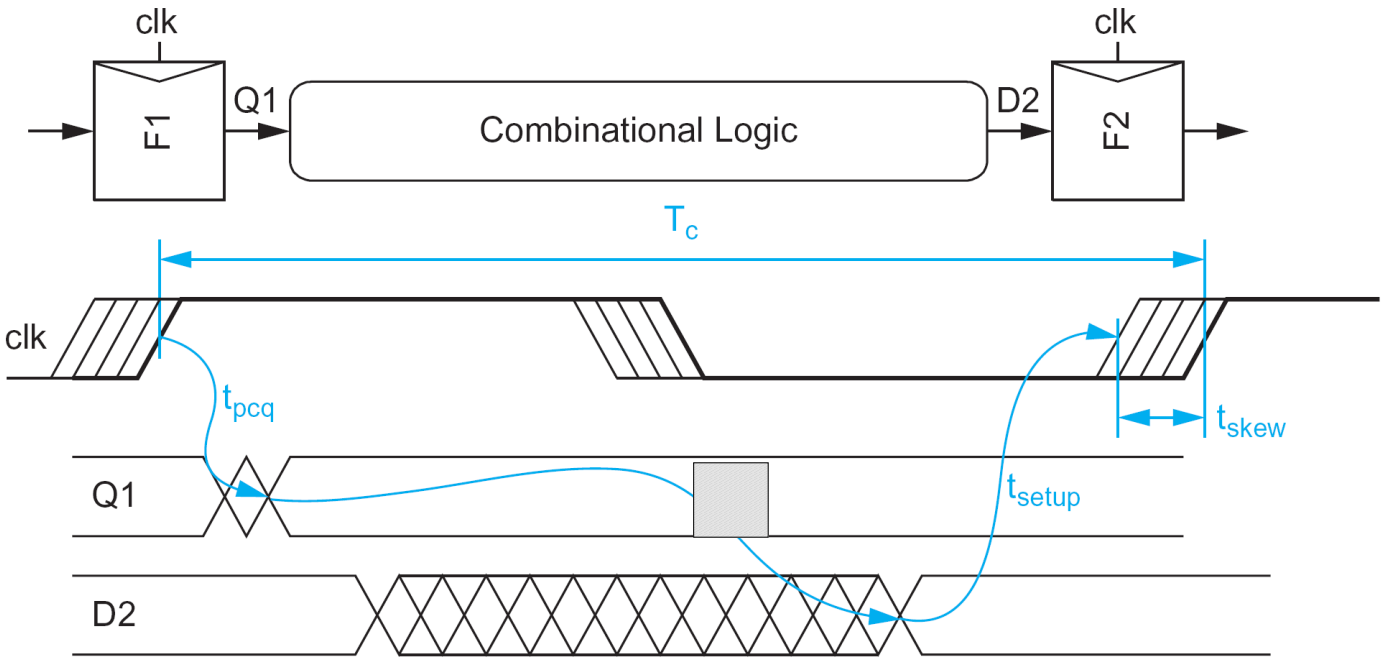
Slack Analysis – Data Path Types



Slack Analysis – Data Path types

- Primary input-to-register paths
  - Delays off-chip + Combinational logic delays up to the first sequential device.
- Register-to-primary output paths
  - Start at a sequential device
  - CLK-to-Q transition delay + the combinational logic delay + external delay requirements
- Register-to-register paths
  - Delay and timing constraint (Setup and Hold) times between sequential devices for synchronous clocks
- Primary input-to-primary output paths
  - Delays off-chip + combinational logic delays + external delay requirements.

Setup Slack Calculation



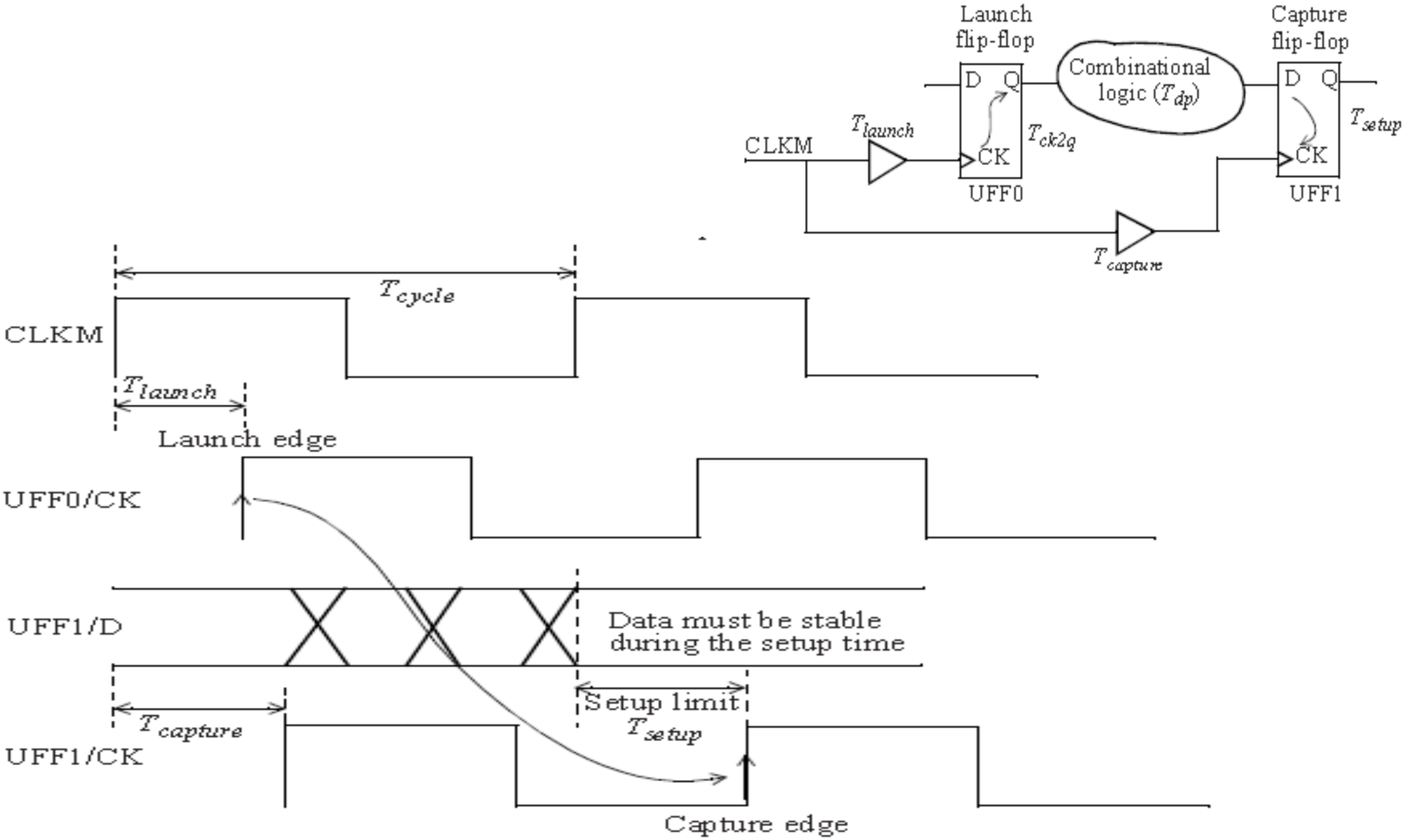
$$t_{pd} \leq T_c - \left(t_{pcq} + t_{\text{setup}} + t_{\text{skew}} \right)$$

Required time $RAT = T_c - (t_{setup} + t_{skew})$

Arrival time $AAT = t_{pcq} + t_{pd}$

Slack $RAT - AAT$

Setup Slack Calculation



$$T_{launch} + T_{ck2q} + T_{dp} < T_{capture} + T_{cycle} - T_{setup}$$

Arrival time

Required time

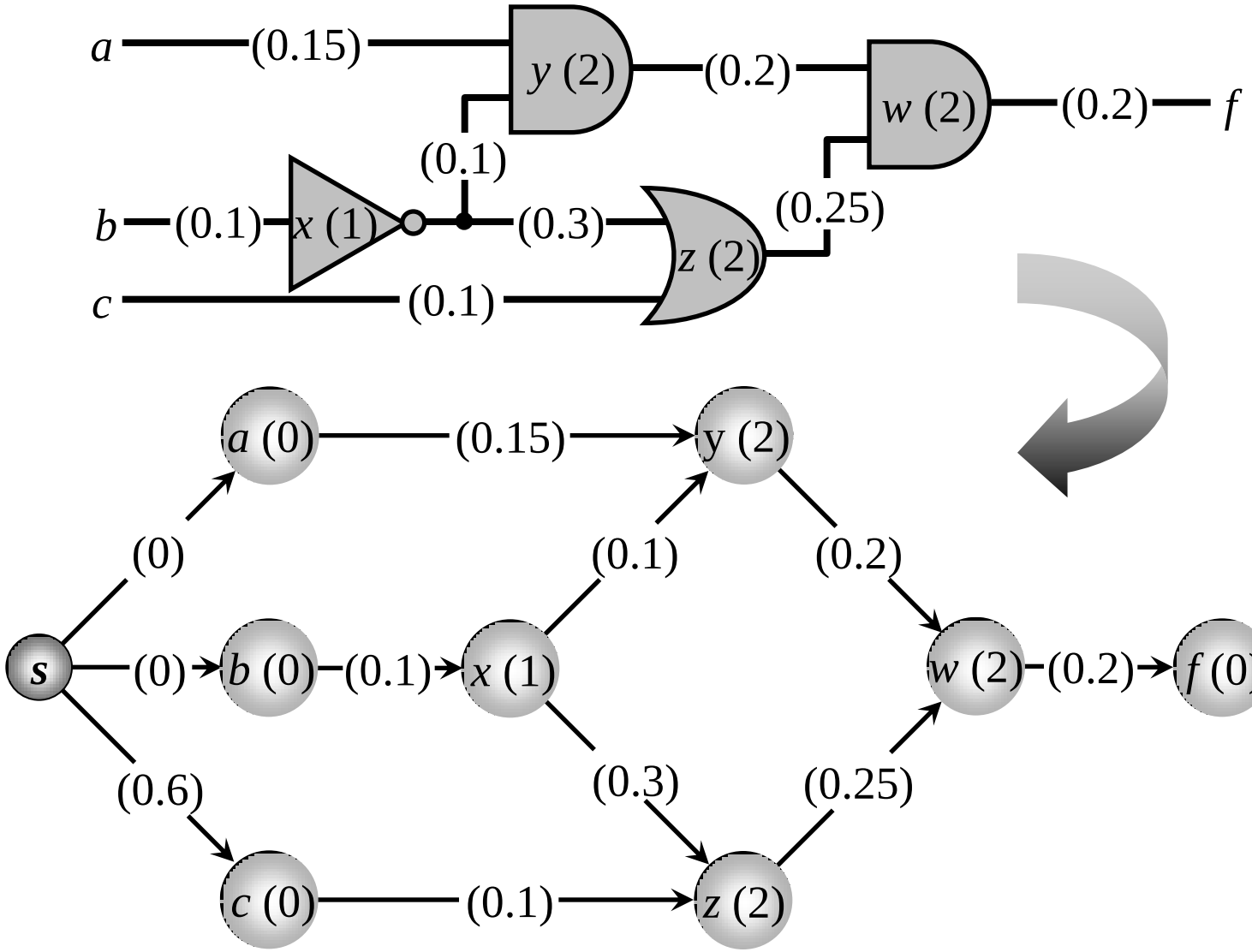
Example of Setup Check

Startpoint: UFF0 (**rising edge-triggered flip-flop clocked by CLKM**)
Endpoint: UFF1 (**rising edge-triggered flip-flop clocked by CLKM**)
Path Group: CLKM
Path Type: max

Point	Incr	Path
clock CLKM (rise edge)	**0.00**	0.00
clock network delay (ideal)	0.00	0.00
UFF0/CK (DFF)	0.00	0.00 r
UFF0/Q (DFF) <-	0.16	0.16 f
UNOR0/ZN (NR2)	0.04	0.20 r
UBUF4/Z (BUFF)	0.05	0.26 r
UFF1/D (DFF)	0.00	0.26 r
data arrival time		0.26
clock CLKM (rise edge)	**10.00**	10.00
clock network delay (ideal)	0.00	10.00
clock uncertainty	-0.30	9.70
UFF1/CK (DFF)		9.70 r
library setup time	-0.04	9.66
data required time		9.66
data required time		9.66
data arrival time		-0.26
slack (MET)		9.41

Computation of path delay

Combinational circuit as DAG



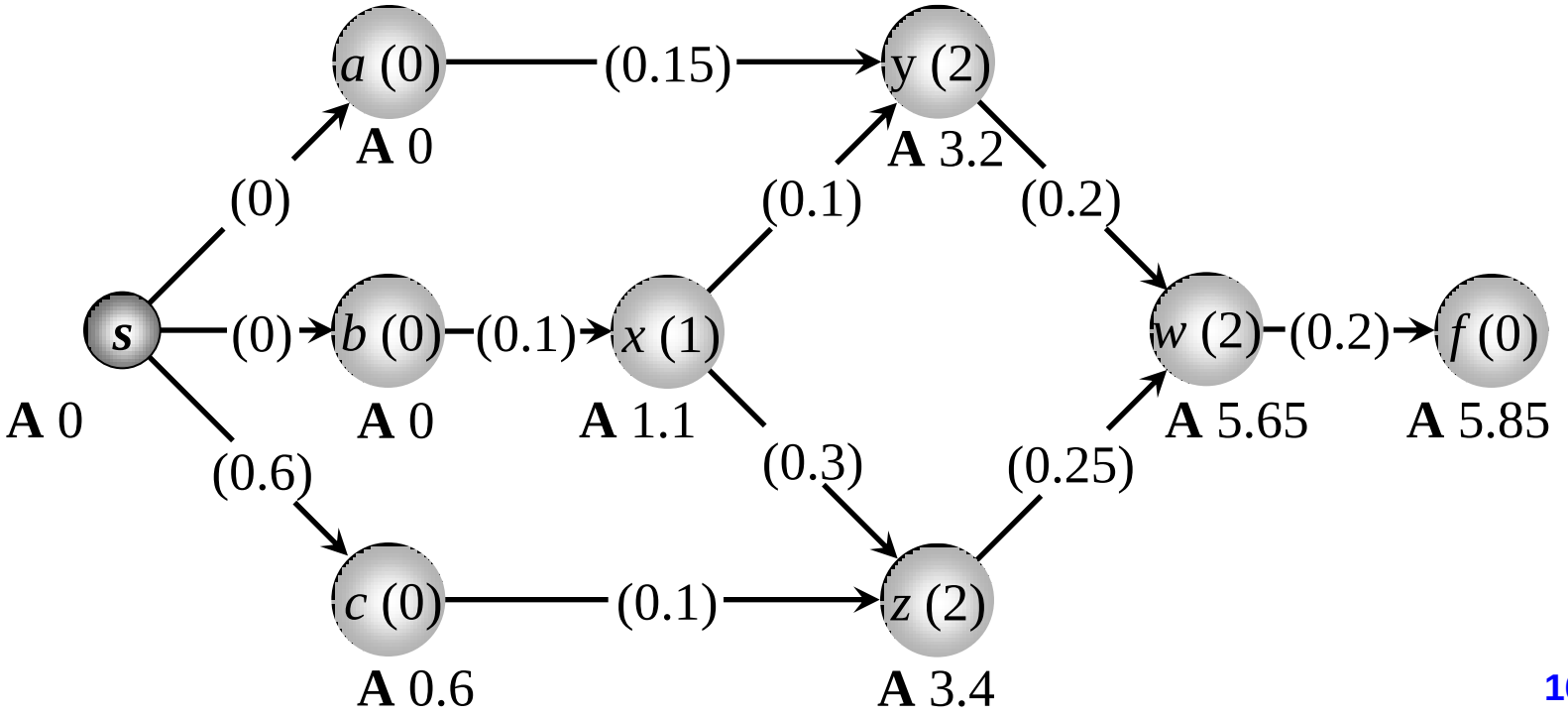
Computation of path delay

Compute AATs at each node:

$$AAT(v) = \max_{u \in FI(v)} \left(AAT(u) + t(u,v) \right)$$

where $FI(v)$ is the fanin nodes, and $t(u,v)$ is the delay between u and v

(AATs of inputs are given)



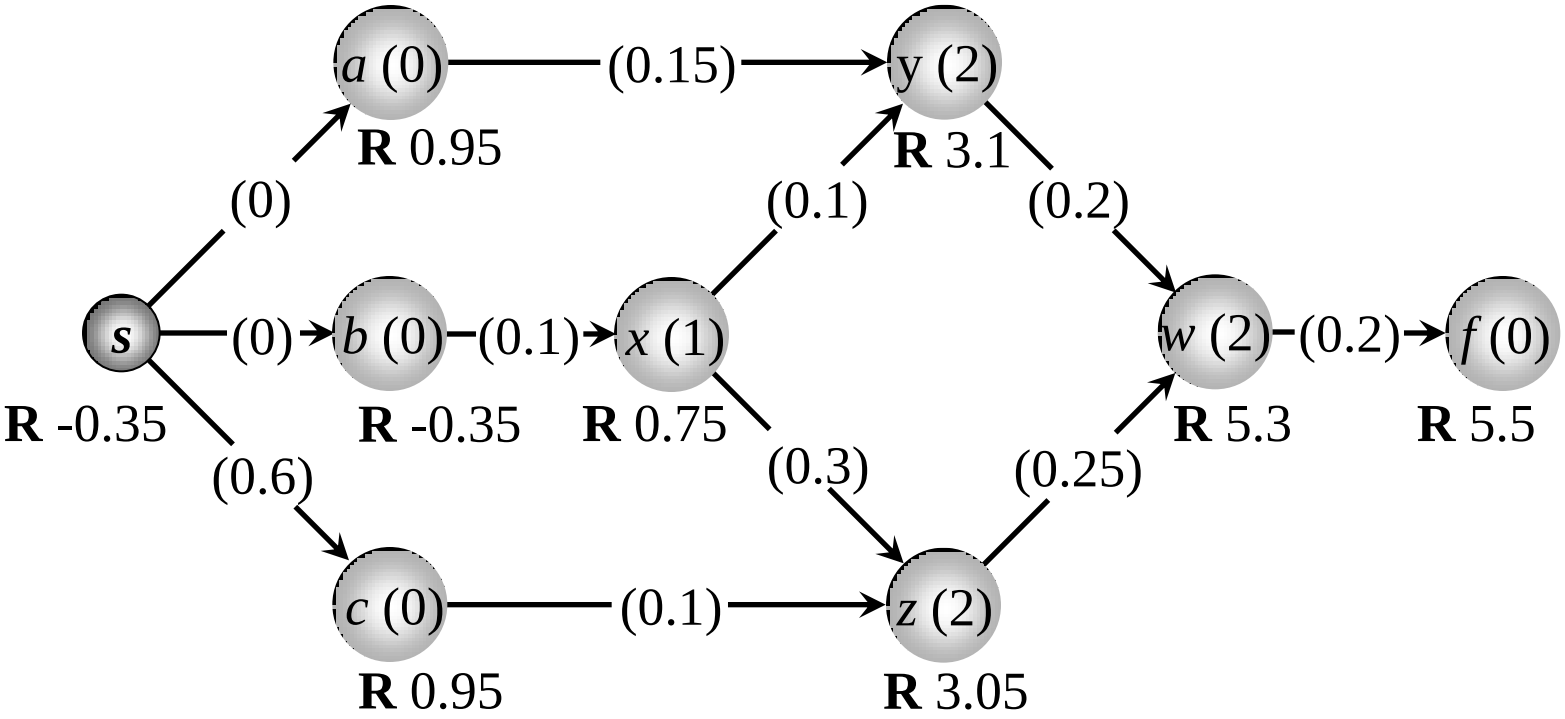
Computation of path delay

Compute RATs at each node:

$$RAT(v) = \min_{u \in FO(v)} \left(RAT(u) - t(u,v) \right)$$

where $FO(v)$ are the fanout nodes, and $t(u,v)$ is the delay between u and v

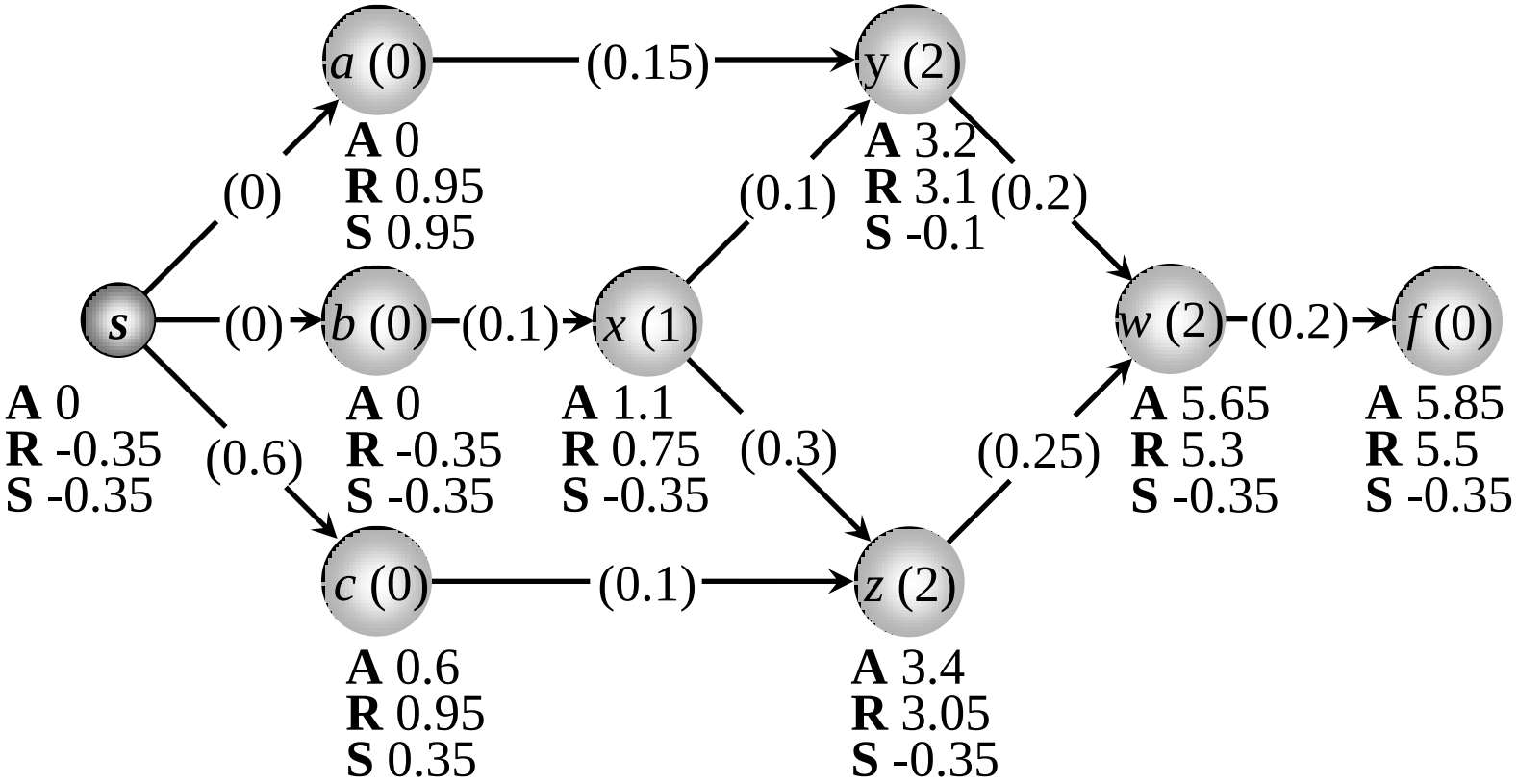
(RATs of outputs are given)



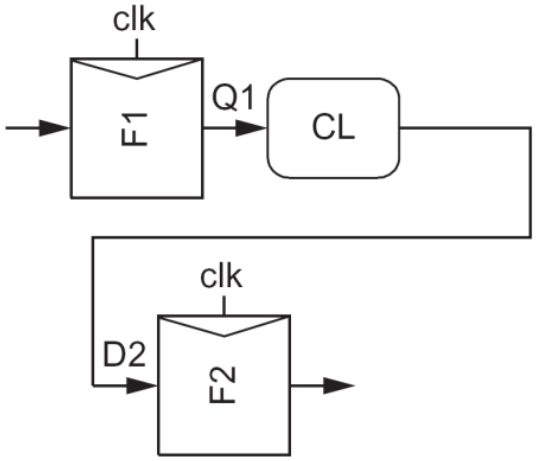
Computation of path delay

Compute slacks at each node:

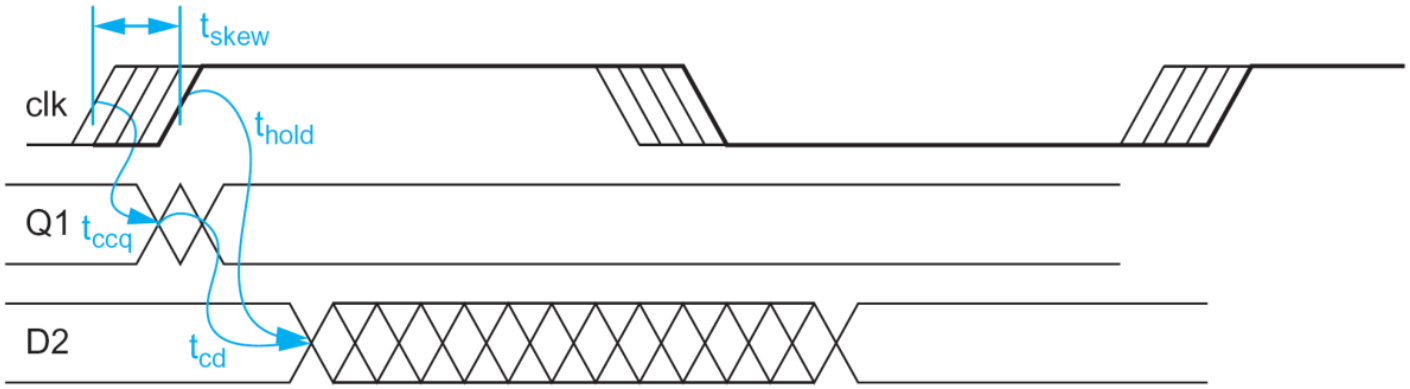
$$slack(v) = RAT(v) - AAT(v)$$



Hold Time Check

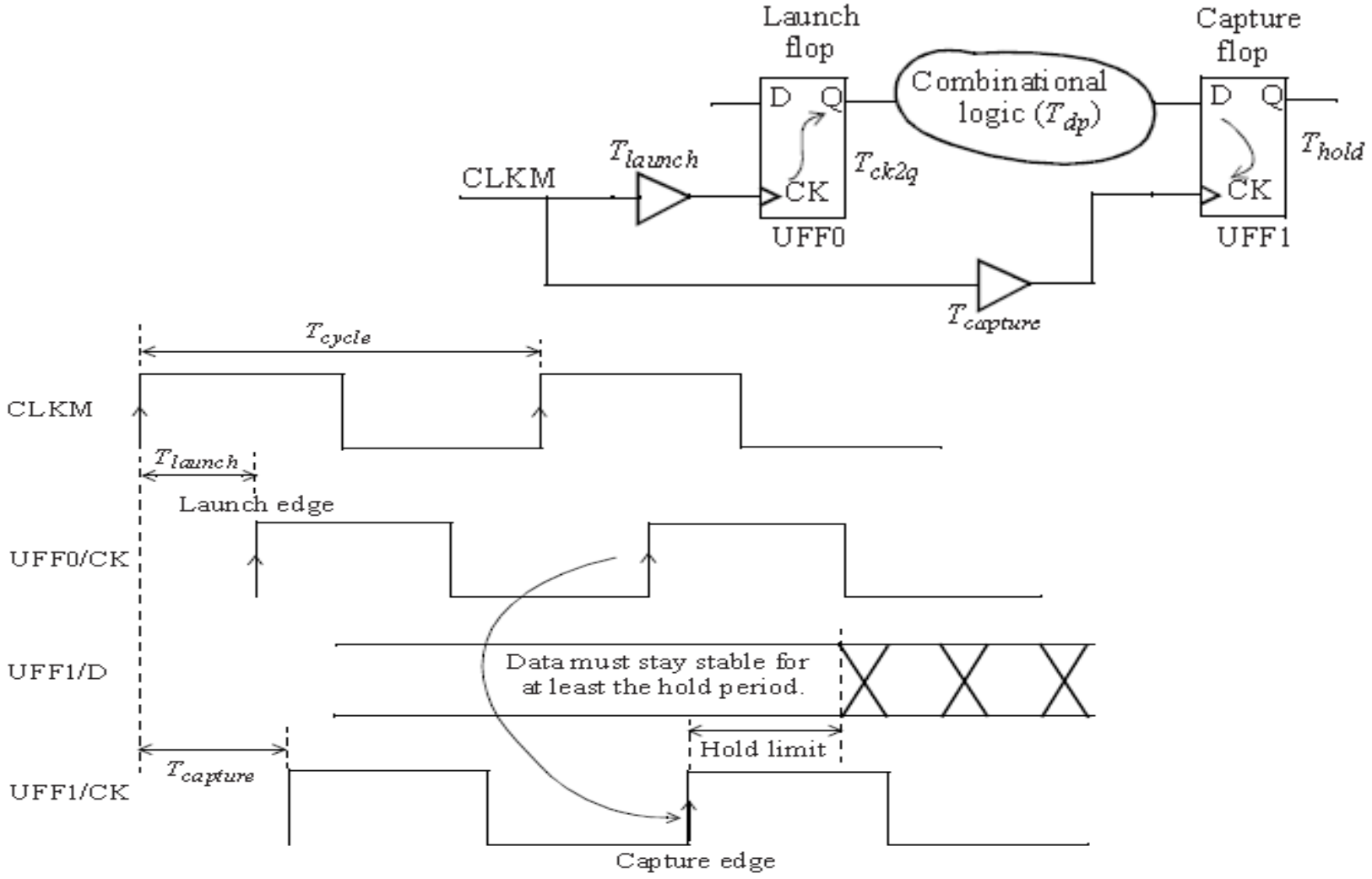


$$t_{cd} \geq t_{\text{hold}} - t_{ccq} + t_{\text{skew}}$$



$$Slack = (t_{cd} + t_{ccq}) - (t_{skew} + t_{hold})$$

Hold Timing Check



$$T_{launch} + T_{ck2q} + T_{dp} > T_{capture} + T_{hold}$$

Arrival time

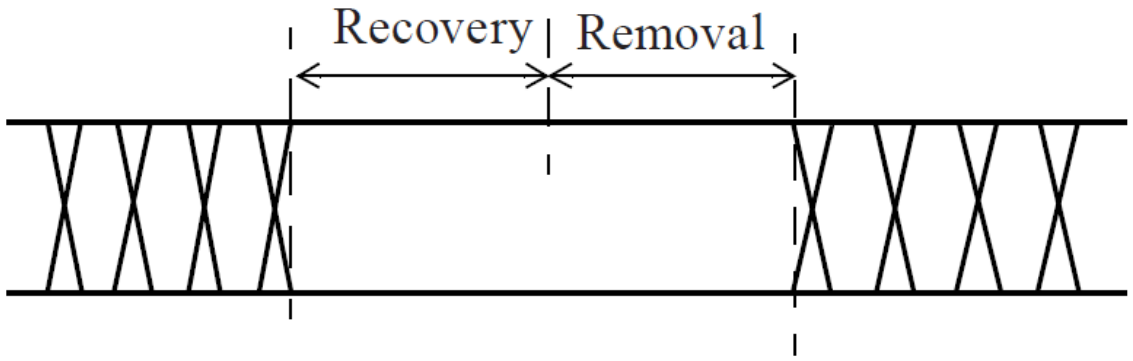
Required time

Hold Check Example

```
Startpoint: UFF0 (rising edge-triggered flip-flop clocked by CLKM)
  Endpoint: UFF1 (rising edge-triggered flip-flop clocked by CLKM)
  Path Group: CLKM
  Path Type: min

  Point                                              Incr       Path
  -----------------------------------------------------------------
  clock CLKM (rise edge)                             0.00       0.00
  clock source latency                               0.00       0.00
  CLKM (in)                                          0.00       0.00 r
  UCKBUF0/C (CKB  )                                  0.06       0.06 r
  UCKBUF1/C (CKB  )                                  0.06       0.11 r
  UFF0/CK (DFF )                                     0.00       0.11 r
  UFF0/Q (DFF ) <-                                   0.14       0.26 r
  UNOR0/ZN (NR2  )                                   0.02       0.28 f
  UBUF4/Z (BUFF  )                                   0.06       0.33 f
  UFF1/D (DFF )                                      0.00       0.33 f
  data arrival time                                             0.33

  clock CLKM (rise edge)                             0.00       0.00
  clock source latency                               0.00       0.00

  CLKM (in)                                          0.00       0.00 r
  UCKBUF0/C (CKB  )                                  0.06       0.06 r
  UCKBUF2/C (CKB  )                                  0.07       0.12 r
  UFF1/CK (DFF )                                     0.00       0.12 r
  clock uncertainty                                  0.05       0.17
  library hold time                                  0.01       0.19
  data required time                                            0.19
  -----------------------------------------------------------------
  data required time                                            0.19
  data arrival time                                            -0.33
  -----------------------------------------------------------------
  slack (MET)                                                   0.14
```

Recovery and Removal Time

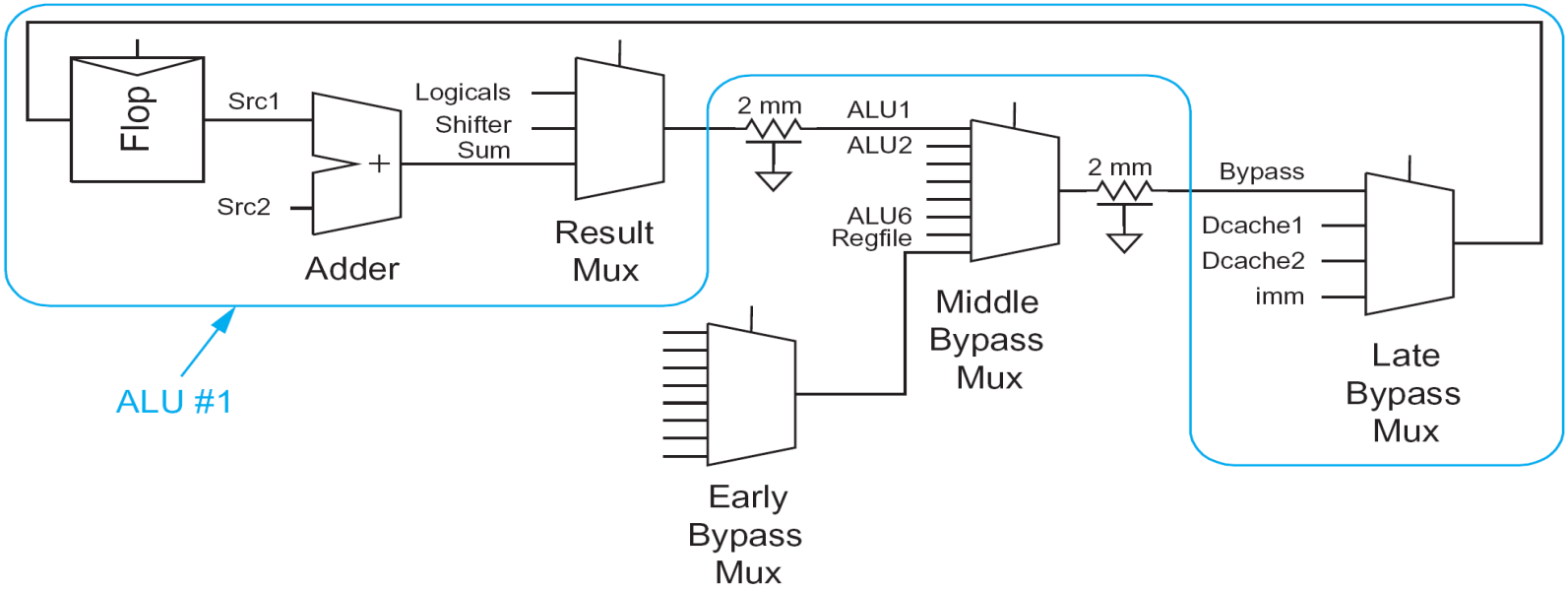
- Recovery Time
  - Like setup time for asynchronous port (set, reset)
  - It is the time available between the asynchronous signal going active and the active clock edge
- Removal Time
  - Like hold time for asynchronous Port (set, reset)
  - It is the time between active clock edge and asynchronous signal going inactive



Reference

- Please see the website.
  - http://staff.ustc.edu.cn/~songch/vlsi-cad.htm

Timing Analysis Exercise



- The Integer Execution Unit of the Itanium 2 contains self-bypass paths for six separate ALUs (Arithmetic Logic Unit). The path for one of the ALUs begins at registers (flip-flops) containing the inputs to an adder, as shown in the above figure.

(1) What is the **minimum cycle time** of the system?
(2) How much **clock skew** can the system have before **hold-time** failures occurs?
Pls. see next slide for the timing parameters & delay values.

Timing Parameters & Delays

- The propagation delays and contamination delays of the data path components are given in the following Table. Suppose the **registers** are built from flip-flops with a **setup time of 50 ps**, **hold time of –7 ps**, **propagation delay of 70 ps**, and **contamination delay of 60 ps**, and the **55 ps clock skew** between flip-flops in the various ALUs.

Element	Propagation Delay	Contamination Delay
Adder	590 ps	100 ps
Result Mux	60 ps	35 ps
Early Bypass Mux	110 ps	95 ps
Middle Bypass Mux	80ps	55 ps
Late Bypass Mux	60ps	45 ps
2-mm Wire	100 ps	70ps