Chapter 9

运算放大器

Operational Amplifiers

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教材：模拟CMOS集成电路设计

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第9章内容

9.1 概述

9.2 一级运放

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9.9 转换速率

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9.1 概述 General considerations

9.1.1 运放性能参数
Performance Parameters:

- Gain
- Small-signal bandwidth
- Large-signal bandwidth（转换速率）
- Output Swing
- Linearity
- Noise and offset(失调)
- 输入/输出阻抗(s)
- 输入/输出范围
- Supply Rejection
- 稳定性（相位裕量）
- 功耗

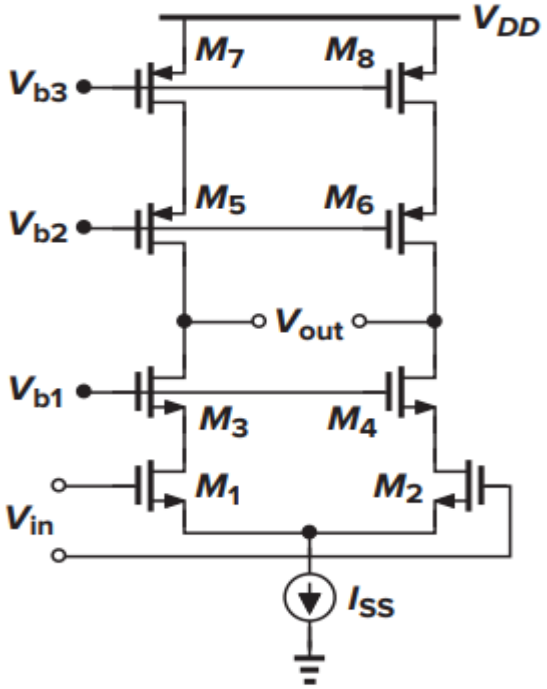


Figure 9.1 Cascode op amp.

运放：很高电压增益的差动放大器。输出阻抗很大（后级电路一般要有更大的输入阻抗），或多级放大电路级联组成。

例9.1 确定放大器最小开环增益一种方法

The circuit is designed for a nominal gain of 10, i.e., 1 + R1/R2 = 10. Determine the minimum value of A1 for a gain error of 1%。

$$\frac{V_{out}}{V_{in}} = \frac{A_1}{1 + \frac{R_2}{R_1 + R_2} A_1}$$

$$= \frac{R_1 + R_2}{R_2} \frac{A_1}{\frac{R_1 + R_2}{R_2} + A_1}$$

$$\approx \left(1 + \frac{R_1}{R_2}\right)\left(1 - \frac{R_1 + R_2}{R_2}\frac{1}{A_1}\right)$$

开环A1实际为$A_1(s)$，与频率有关；因V-V反馈闭环输出阻抗小，故一般情况下（环路增益远大于1）电路中RL负载影响不大

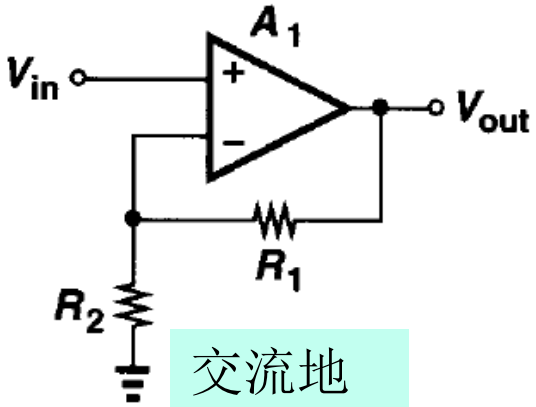


Figure 9.2

由gain error of 1% ⟶

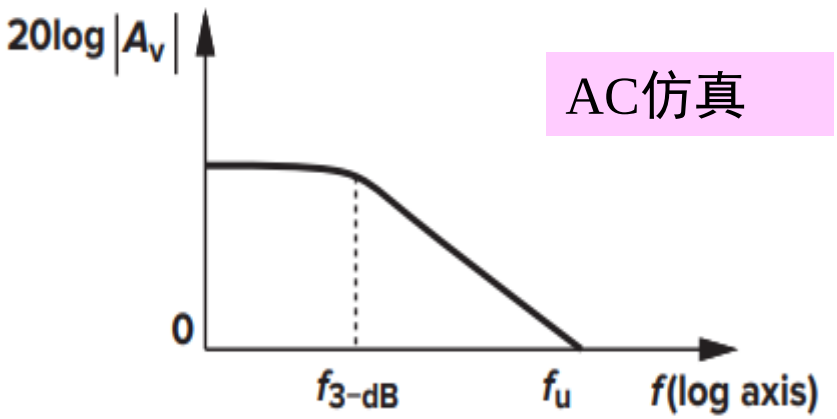
A1 > 1000

这里是按低频闭环增益精度确定开环增益

AC仿真时需加负载电容

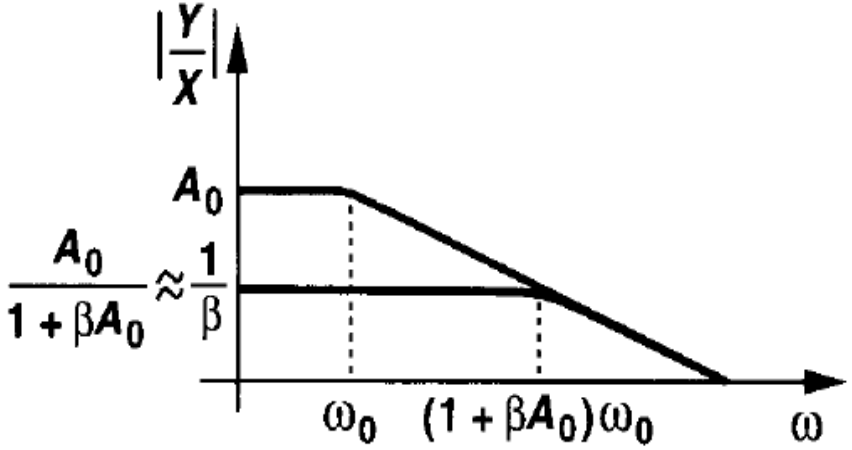
若开环增益$A_1(s)$高频时降为100，则闭环电压增益$A_{vf}(s)$约为9。

小信号带宽Small-signal bandwidth



AC仿真

Figure 9.4，一阶系统



一阶（或近似）系统电路：

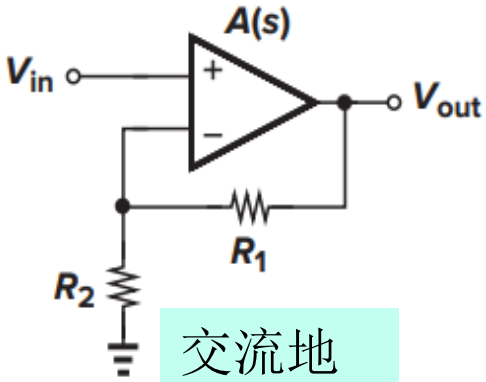
增益 × 带宽积

= 常数（开环=闭环）= $A_0 \frac{\omega_0}{2\pi}$

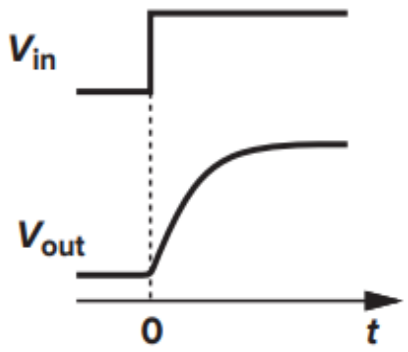
=单位增益带宽 $\frac{\omega_u}{2\pi}$

（如电压跟随器）

例9.2 确定放大器的单位增益带宽



交流地



设1+R1/R2=10,
上升至终值1%时的稳定时间<5ns。
求运放的单位增益带宽?

Tran仿真

$$\left(V_{in} - V_{out}\frac{R_2}{R_1+R_2}\right)A(s) = V_{out}$$

$$\frac{V_{out}}{V_{in}}(s) = \frac{A(s)}{1+\frac{R_2}{R_1+R_2}A(s)}$$

设$A(s) = \dfrac{A_0}{1+\dfrac{s}{\omega_0}}$一阶传输函数，$\omega_0$为3 dB带宽，$A_0\omega_0$为单位增益带宽。

例9.2 (续) 确定运放的单位增益带宽

$$\frac{V_{out}}{V_{in}}(s) = \frac{A_0}{1 + \frac{R_2}{R_1 + R_2}A_0 + \frac{s}{\omega_0}} = \frac{\frac{A_0}{1 + \frac{R_2}{R_1 + R_2}A_0}}{1 + \frac{s}{\left(1 + \frac{R_2}{R_1 + R_2}A_0\right)\omega_0}}$$

一般有A0 R2 / (R1 + R2) >> 1

闭环时间常数：s的系数

$$\tau = \frac{1}{\left(1 + \frac{R_2}{R_1 + R_2}A_0\right)\omega_0} \approx \left(1 + \frac{R_1}{R_2}\right)\frac{1}{A_0\omega_0}$$

设阶跃输入　Vin = a*u(t)
则输出为：

$$V_{out}(t) \approx a\left(1 + \frac{R_1}{R_2}\right)\left(1 - \exp\frac{-t}{\tau}\right)u(t)$$

the final value：
VoutFinal ≈ a (1 + R1/R2)

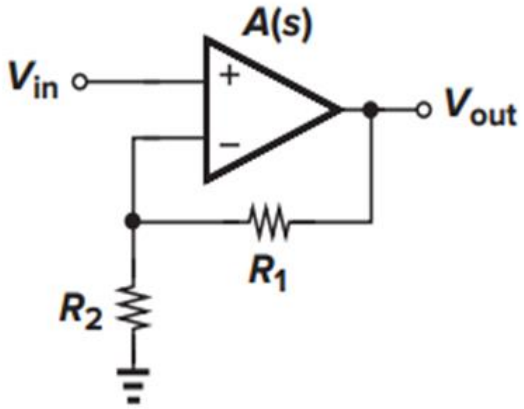
例9.2 (续2) 确定运放的单位增益带宽

For 1% settling, Vout = 0.99VoutFinal ,

$$1 - \exp\frac{-t_{1\%}}{\tau} = 0.99$$

$$t_{1\%} = \tau \ln 100 \approx 4.6\tau \quad = 5\text{ns}$$

$$\tau = 1.08574 \times 10^{-9} s$$



闭环运放的增益带宽积 =运放的单位增益带宽

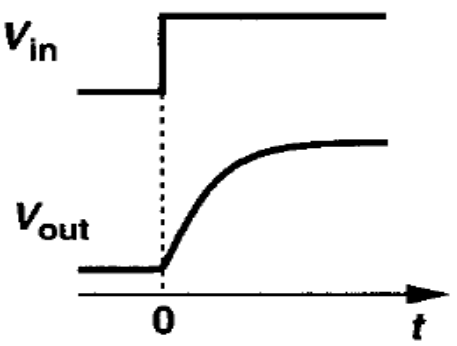
$$=A_0 \frac{\omega_0}{2\pi} = (1 + \frac{R_1}{R_2}) \frac{1}{2\pi\tau} = 10 \times \frac{1}{2\pi \times 1.08574 \times 10^{-9}}$$

$$= \frac{9.21}{2\pi} \times 10^9 \quad Hz = 1.47 \ G \ Hz$$

Performance Parameters (cont.)

- Large-signal bandwidth

  - 幅度变化大，进入非线性，不适合AC仿真;
  - 采用转换速率（slew rate）分析，大的阶跃输入tran仿真。



tran仿真

- Output Swing

  差动电路是单端电路的2倍。

- Linearity（幅度变化很大时）

  非线性问题通过两种方法解决:

  1.采用全差动抑制偶次谐波;

  2.足够高的开环增益(实际上是减小净输入信号)以使反馈系统达到所要求的线性。

Performance Parameters (cont.)

- 噪声和失调(offset)

  噪声限制能处理的最小信号电平，分析关键器件噪声(例如输入管)。

  失调由差动对失配（包括直流偏置和器件参数）引起。

- 稳定性（相位裕量）

  仅针对构建的多零极点负反馈系统。

- 功耗

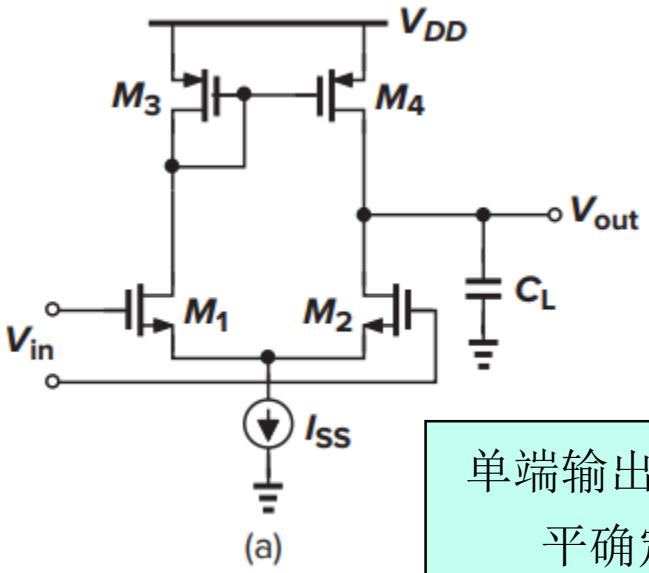
  1. 若是微弱信号（通常在几十uV以下)放大器输入级由信噪比确定，输入跨导与电流有关，输入管gm大则电路的参考输入噪声小；

  2. 若输出是大信号或重负载（低电阻值）时，输出级相关的尾电流源需要大电流。

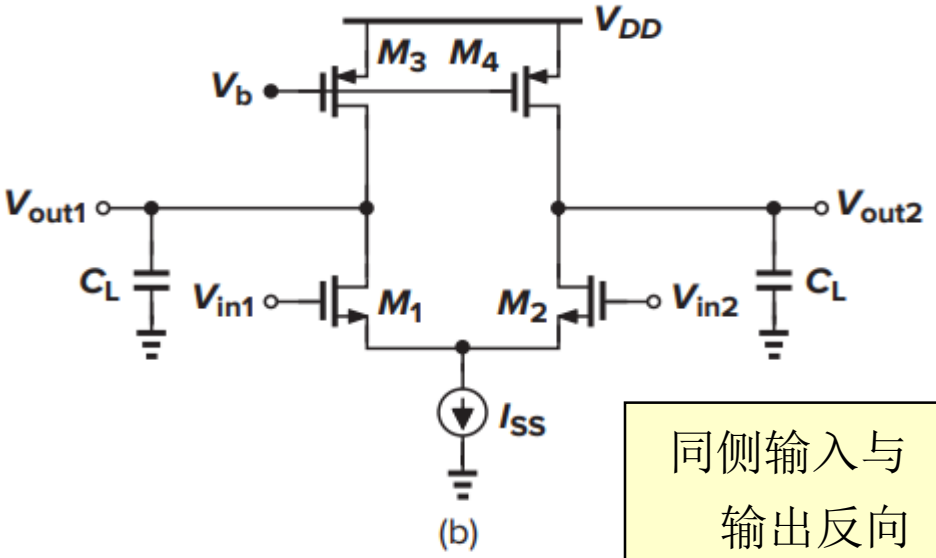
- 输入、输出阻抗和电压范围：

  合适的级联接口。

9.2 一级运放 One-Stage OP Amplifiers



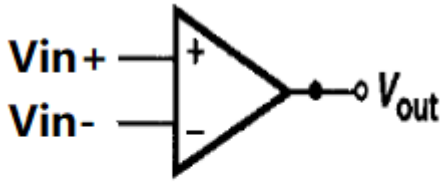
单端输出电平确定



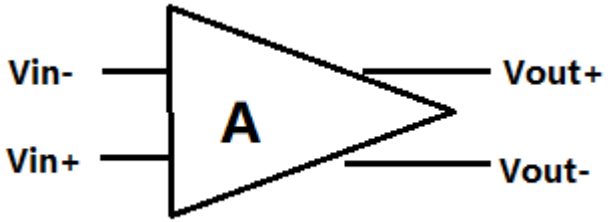
同侧输入与输出反向

- 低频小信号增益 $g_{mN}(r_{ON} \| r_{OP})$
- 图 (a) 有一个镜像极点。

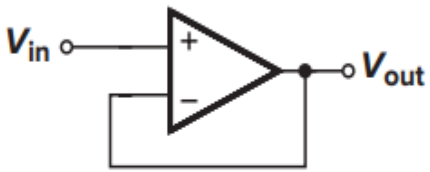
Fully differential OP, 电流源负载需要 CMFB!



与输出方向相同的输入为Vin+



例 9.4 求输入共模电压和闭环输出阻抗



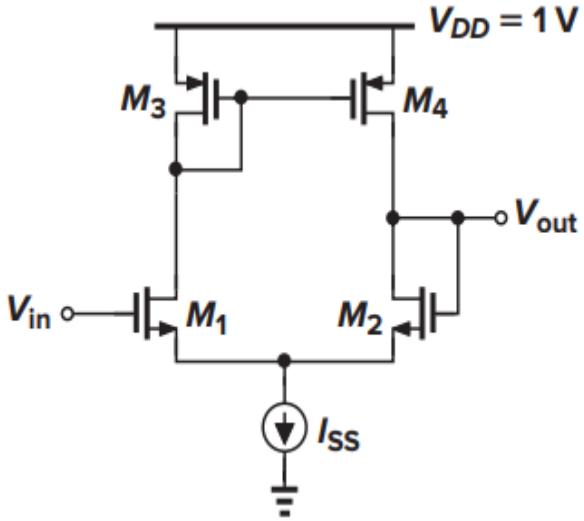


Figure 9.7

电压跟随器输入必须
在输出允许范围内

若开环增益很小，
则输入虚短不成立

设阈值电压V_{TH}=0.3V,
过驱动电压$V_{GS}-V_{TH}$=0.1V

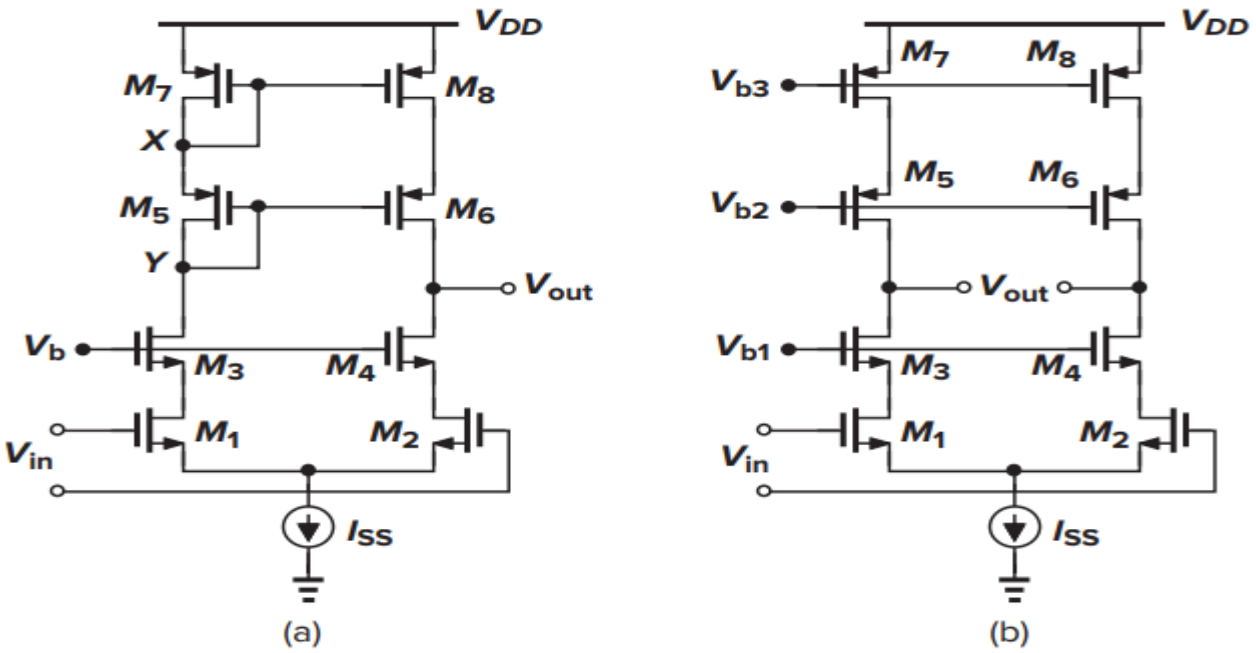
最小允许输入电压 $V_{in,min}=V_{GS1}+V_{ISS}=0.3+0.1+0.1=0.5$ V
最大允许输入电压 $V_{in,max}=V_{DD}-V_{GS3}+V_{TH}=1-(0.3+0.1)+0.3=0.9$ V
共模范围为 0.9-0.5=0.4V

闭环输出阻抗：与开环输出阻抗无关。

$$(r_{OP}\,||r_{ON})/[1+g_{mN}(r_{OP}\,||r_{ON})]=1/g_{mN}$$

闭环极点（设负载电容C_L）角频率：g_{mN}/C_L (rad/s)

高增益（输出阻抗）Cascode OP



Telescopic
套筒式

过驱动电压
VOD

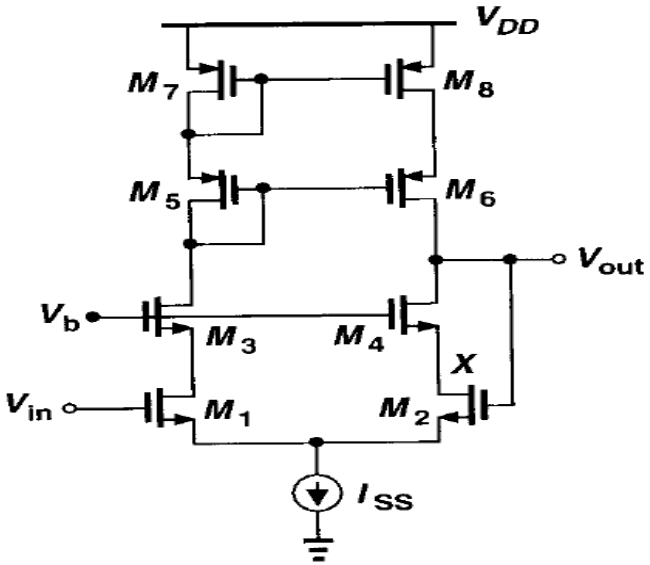
(a)电流镜负载，单端输出。
输入和输出范围均较小

(b)全差动结构，电流源负载。
输入范围小，需CMFB

图(b)全差动OP输出范围： $2[V_{DD} - (V_{OD1} + V_{OD3} + V_{ISS} + |V_{OD5}| + |V_{OD7}|)]$

增益 $A_v \approx g_{mN}[(g_{mN} r_{oN}^2) \,||\, (g_{mP} r_{oP}^2)]$

电流镜负载套筒式放大器实现单位增益缓冲器的限制



M2饱和区：$V_{out} \le V_X + V_{TH2}$

M4饱和区：$V_{out} \ge V_b - V_{TH4}$

Vb影响Vout和Vin范围

因 $V_X = V_b - V_{GS4}$,

故 $V_b - V_{TH4} \le V_{out} \le (V_b - V_{GS4}) + V_{TH2}$

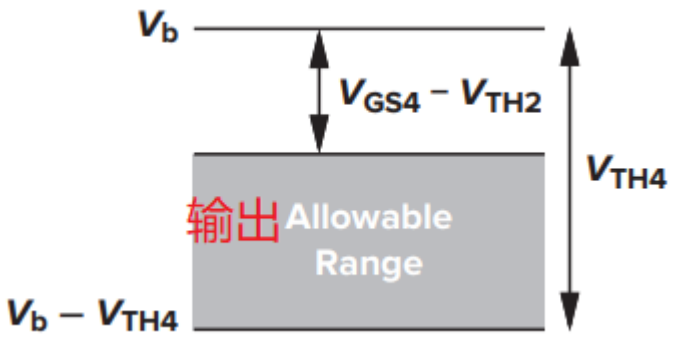
$$V_{omax} - V_{omin} = [V_b - (V_{GS4} - V_{TH2})] - (V_b - V_{TH4})$$

$$= V_{TH4} - V_{GS4} + V_{TH2} = V_{TH2} - V_{OD4}$$

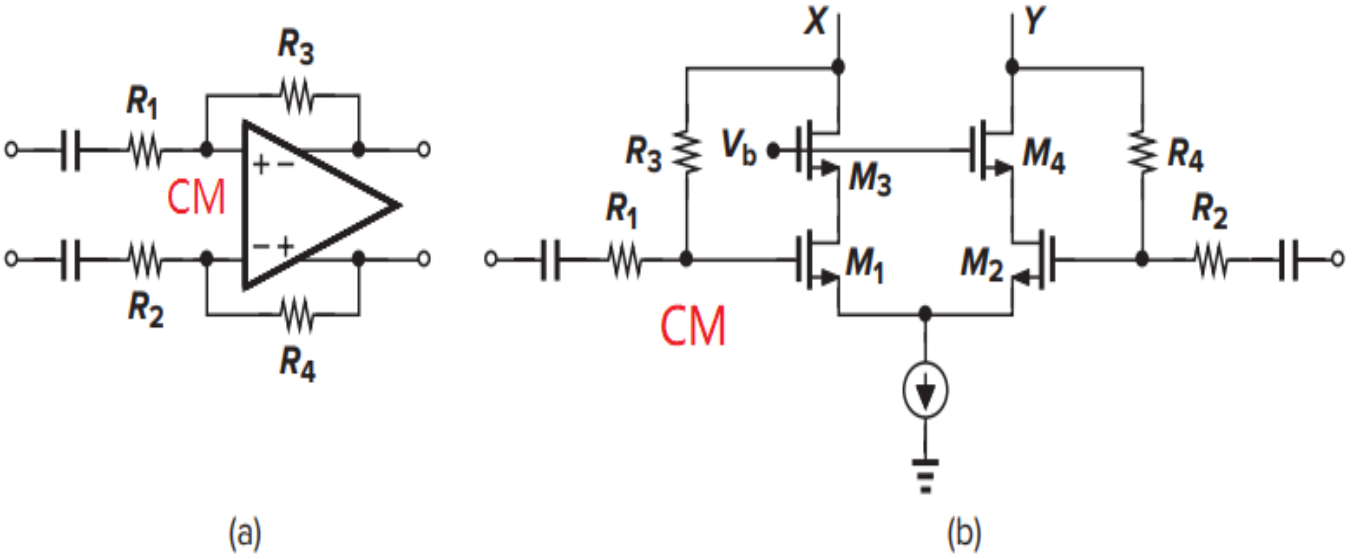
作为电压跟随器时，

输出（虚短输入）范围太小！

电压跟随器须工作在Vin和Vout共同有效的电压范围内



例9.6 套筒式运放的闭环增益和输出摆幅



高速或射频电路时输入CM电平可另由偏置电路设置（第五章）

Figure 9.10

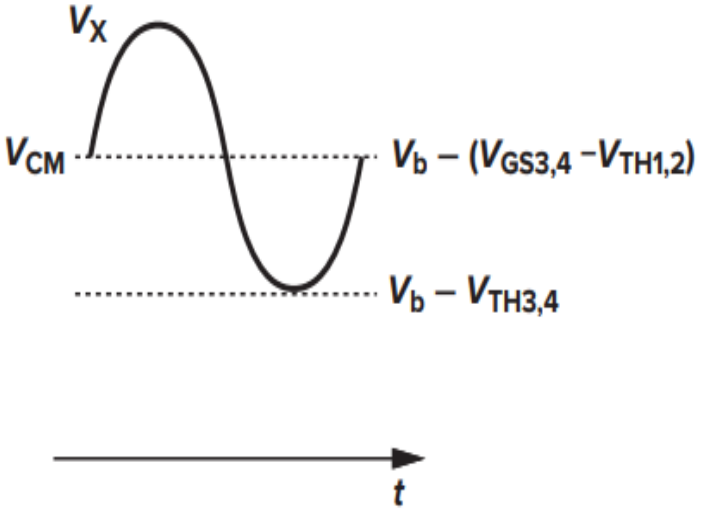
M3 饱和区：$V_X > V_b - V_{TH3}$

M1 饱和区：$V_{CM} < V_b - V_{GS3} + V_{TH1}$

闭环增益 $A_v = -\frac{R_3}{R_1}$

输出摆幅：$\pm(V_{TH1} + V_{TH3} - V_{GS3})$

$= \pm(V_{TH1} - V_{OD3})$



9.2.2 设计步骤 Design Procedure

The actual design methodology of an op amp somewhat depends on the specifications that the circuit must meet.

For example, a high-gain op amp may be designed quite differently from a low-noise op amp.

In most cases, some aspects of the performance, e.g., output voltage swings and open-loop gain, are of primary concern.

We will deal extensively with five parameters for each transistor: I_D, $V_{OD} = V_{GS} - V_{TH}$, W/L, gm, and r_O .

In the design of op amps (and many other circuits), it is helpful to begin with a power budget， the resulting design can readily be “scaled” for lower or higher power dissipations.

例 9.7 设计直筒式cascode全差动电路

V_{DD} = 3V, peak-to-peak differential output swing = 3V, power dissipation = 10mW, voltage gain = 2000. $\mu_n C_{ox}$ = 60 μA/V^2, $\mu_p C_{ox}$ = 30 μA/V^2, λ_n = 0.1 /V, λ_p = 0.2 /V (effective channel length of 0.5 μm), γ = 0, and $V_{THN} = |V_{THP}|$ = 0.7 V.

思路：支路I_D→V_{OD}→W/L→增益验证→修改W/L

注意：电流是根据输出压摆率计算得到的。

current mirrors : M7/M8, M9

3 mA to M9， 330 μA to M_{b1} and M_{b2}

X and Y swing by 1.5 Vpp

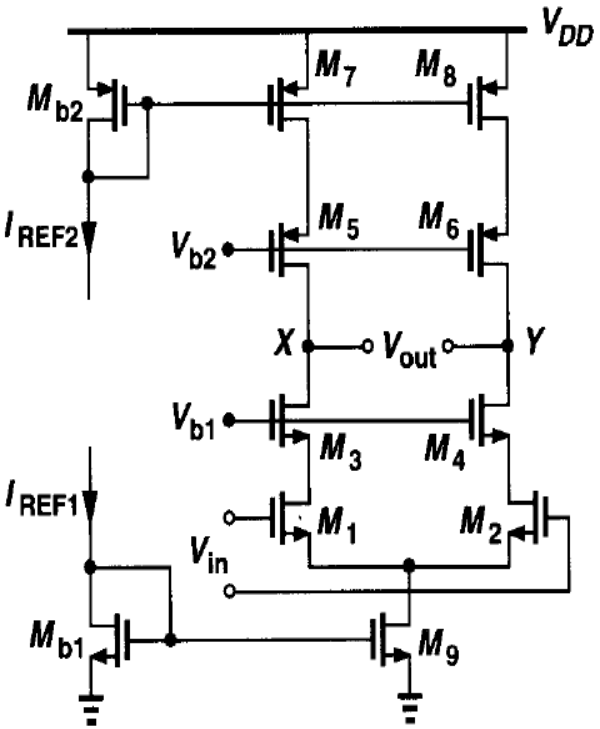
$|V_{OD7}| + |V_{OD5}| + V_{OD3} + V_{OD1} + V_{OD9} = 1.5$ V

choose $V_{OD9} \approx 0.5$ V

$V_{OD5}=V_{OD7}=0.3$V, $V_{OD1}=V_{OD3}=0.2$V

由此确定各MOS管宽长比

$$I_D = \frac{1}{2}\mu C_{OX}\frac{W}{L}(V_{GS} - V_{TH})^2$$



Example 9.7 (cont.)

$$(W/L)_{1-4} = 1250 \qquad (W/L)_{5-8} = 1111$$

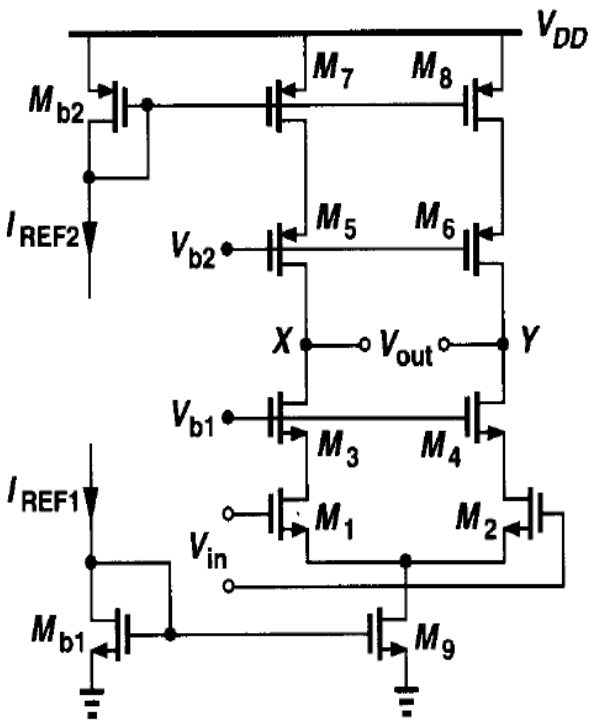
$$(W/L)_9 = 400$$

$$r_0 = \frac{1}{\lambda I_D}$$

$$g_m = \sqrt{2\mu C_{ox}\frac{W}{L} I_D}$$

$$A_v \approx g_{m1}[(g_{m3}r_{O3}r_{O1}) \| (g_{m5}r_{O5}r_{O7})]$$

=1416 < 2000



需要CMFB共模反馈电路确定输出直流电平。

使PMOS管长度增加 1 *倍*，宽长比不变，

则 λ_P减小为 1 半，r_{0P}增加 1倍，g_{mP}不变。

$A_v \approx 4000$

例 9.7 (cont.)：输入范围很小的问题

$V_{in,min} = V_{GS1} + V_{OD9} = V_{TH1} + V_{OD1} + V_{OD9} = 1.4\ V$

$V_{b1,min} = V_{GS3} + V_{OD1} + V_{OD9} =$（0.7+0.2）+0.2+0.5=1.6V

$$V_{b2,max} = V_{DD} - (|V_{GS5}| + |V_{OD7}|)$$

=3-(0.7+0.3+0.3)=1.7V

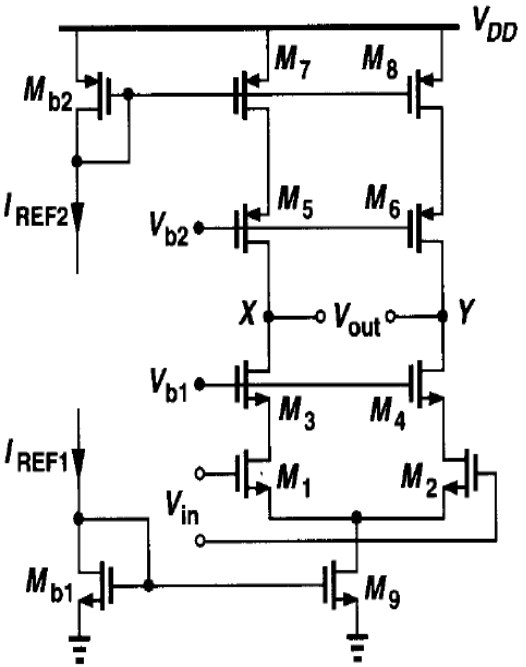
V_{outCM}受Vb1和Vb2限制:

$V_{b1} - V_{THn} < V_{outCM} < V_{b2} + V_{THp}$

即 $0.9 < V_{outCM} < 2.4V$，

VoutCM均值=1.65V

V_{inCM}下限（=1.4V）受V_{OD9}限制，
V_{inCM}上限（$=V_{b1}-V_{GS3}+V_{TH1}$）受V_{b1}限制，范围较小（Vb1确定了输出下限电压）。



V_{TH}=0.7,$V_{OD1,3}$=0.2
$V_{OD5,7}$=0.3,V_{OD9}=0.5

难以实现范围较大的电压跟随器

需要另有共模反馈电路CMFB确定输出工作点电压

9.2.3 线性缩放：宽度缩放，长度不变

导致功率缩放，增益不变、摆幅不变。

$$I_D = \frac{1}{2}\mu C_{OX}\frac{W}{L}(V_{GS} - V_{TH})^2$$

例如：

(1) 设I_D is doubled,

(2) W/L is doubled,

(3) $V_{GS} - V_{TH} = V_{OD} = V_{DSmin}$ is constant,
so are the allowable voltage swings,

(4) g_m is doubled,

(5) r_O is halved.

一般地，*使*电流增大，*则*电路速度加快（极点频率高），输入管g_m增大，输入参考噪声电压减小。

例：自动跟踪输入共模电压的偏置V_{b1}

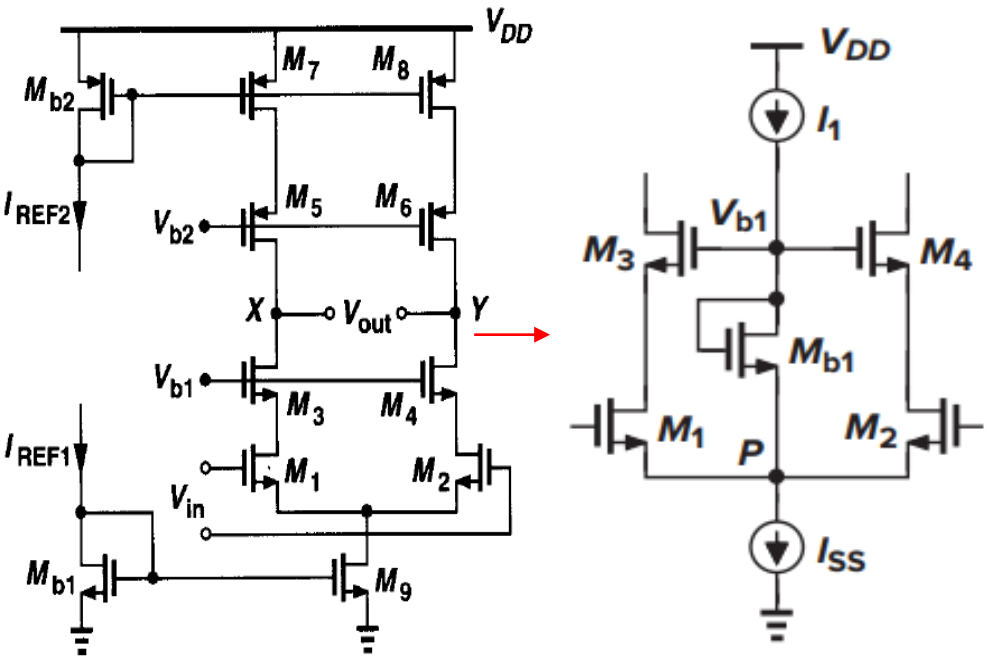
例：V_{b1}自动跟踪输入共模电平

$$V_P = V_{in,CM} - V_{GS1}$$

$$V_{b1} = V_P + V_{GS,b1}$$

故V_{b1} = （$V_{in,CM} - V_{GS1}$） + $V_{GS,b1}$
> $V_{in,CM} - V_{TH1} + V_{GS3}$ （M1饱和）

$$V_{GS,b1} > (V_{GS1} - V_{TH1}) + V_{GS3}$$

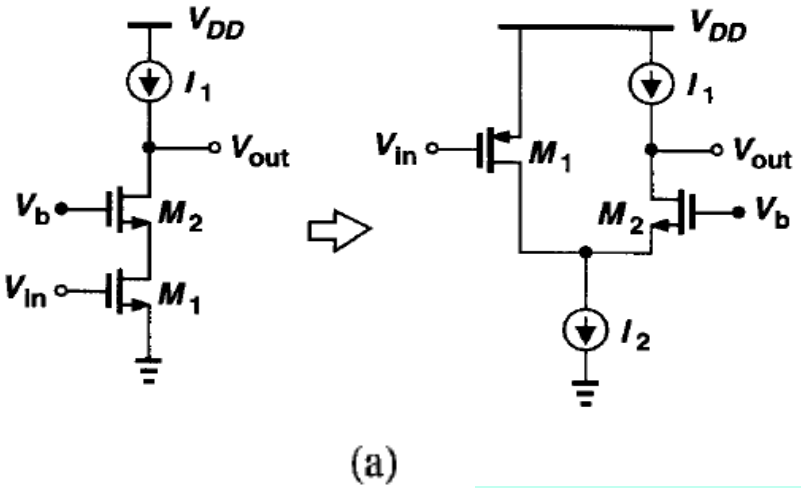


Mb1 is a narrow , long device，W/L很小

$$I_D = \frac{1}{2}\mu C_{OX}\frac{W}{L}(V_{GS} - V_{TH})^2$$

9.2.4 折叠式共源共栅 Folded cascode

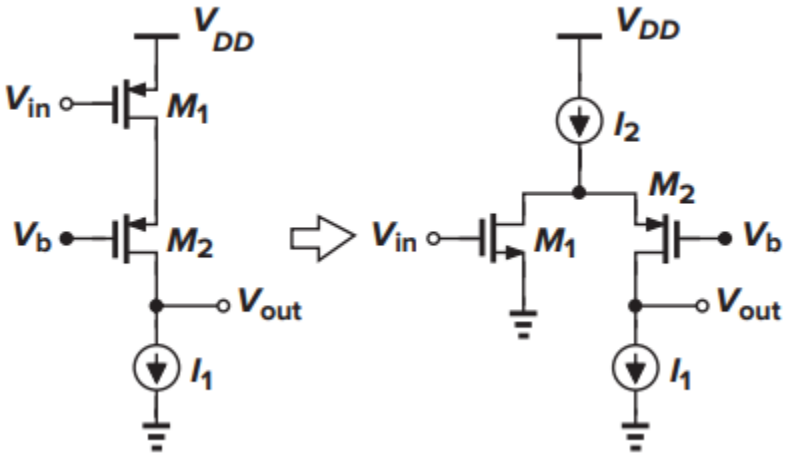
折叠CASCODE特点：输入信号范围大。



(a)

直筒式：
2个MOS类型相同。
输入信号电位较低。

折叠式：
2个MOS类型不同。
输入信号电位低。



(b)

直筒式：
输入信号电位较高。

折叠式：
输入信号电位高。

输出交变信号：gm1RoutVin

Differential folded-cascode

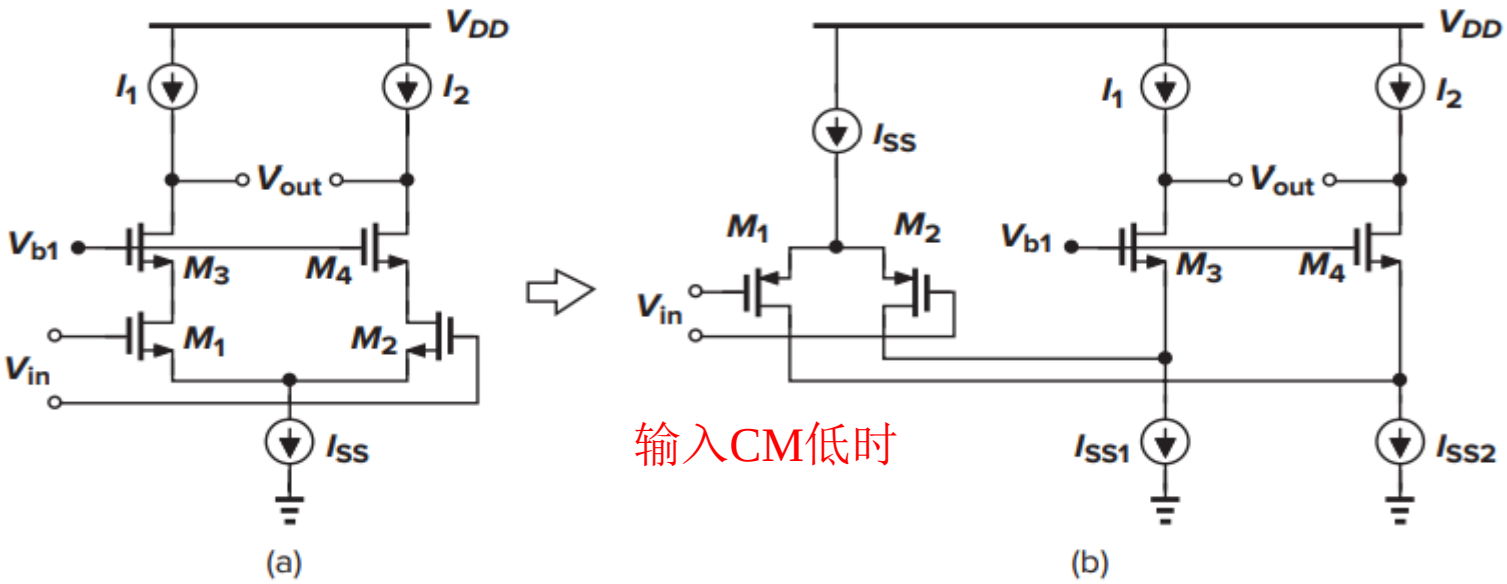


Figure 9.14 (a) Telescopic and (b) folded-cascode op amp topologies

折叠CASCODE输入共模范围大，输出范围也有所增大

折叠与直筒的区别：

（1）$I_{SS1} = I_{SS}/2 + I_{D3} = I_{SS}/2 + I_1$. The folded-cascode consumes more power.

（2）直筒式：$V_{GS1} + V_{ODSS} <$ input CM $< V_{b1} - V_{GS3} + V_{TH1}$,

折叠式：$V_{DD} - (V_{GS1} + V_{ODSS}) >$ input CM，V_{b1}尽量低（$V_{GS3}+V_{OD}$），输入和输出易满足。

folded-cascade OP 最大输出摆幅

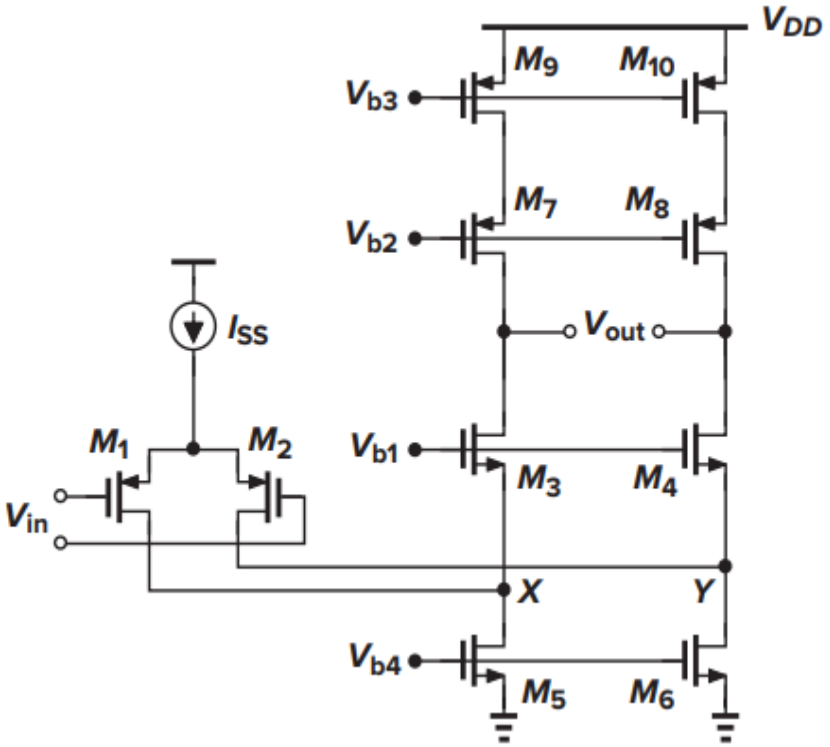


Figure 9.15 Folded-cascode op amp with cascode PMOS loads

在Vb2和Vb1合适情况下:

输出最低电平： $V_{OD3} + V_{OD5}$

输出最高电平： $V_{DD} -(|V_{OD7}|+|V_{OD9}|)$

单边摆幅：

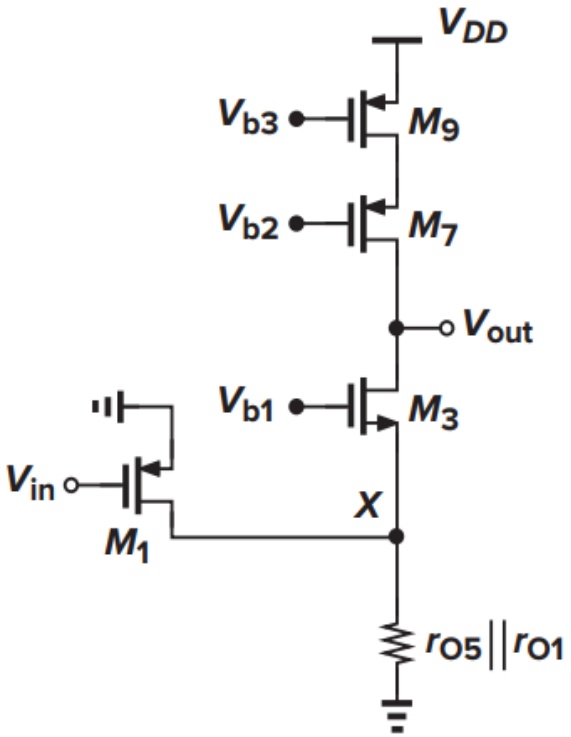
$V_{DD} -(|V_{OD7}|+|V_{OD9}|+ V_{OD3} + V_{OD5})$

差动输出摆幅=2倍单边摆幅。

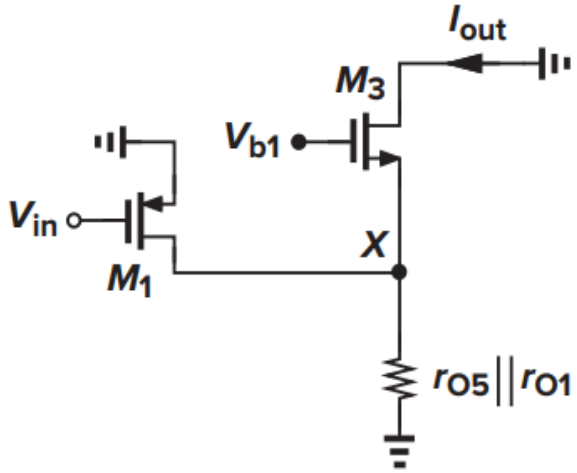
任何CASCODE OP输出阻抗都很大，除非已经构成V-V负反馈，否则电路级联时应注意后级电路需要有较大的输入阻抗。

折叠式CASCODE 的小信号增益

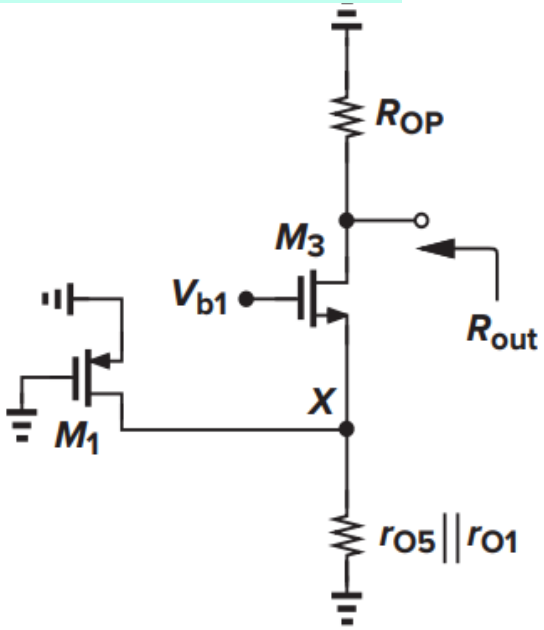
输出电压=输出短路电流*输出阻抗



(a)



(b)



(c)

$$G_m = \frac{I_{out}}{V_{in}} = \frac{g_{m1}V_{in}}{V_{in}} \times \frac{g_{m3}+g_{mb3}}{(r_{o5} \parallel r_{o1})^{-1}+(g_{m3}+g_{mb3})} \approx g_{m1}$$

$$|A_v| \approx g_{m1}\{[(g_{m3}+g_{mb3})r_{O3}(r_{O1}\|r_{O5})]\|[(g_{m7}+g_{mb7})r_{O7}r_{O9}]\}$$

高输入共模电平时的folded-cascode

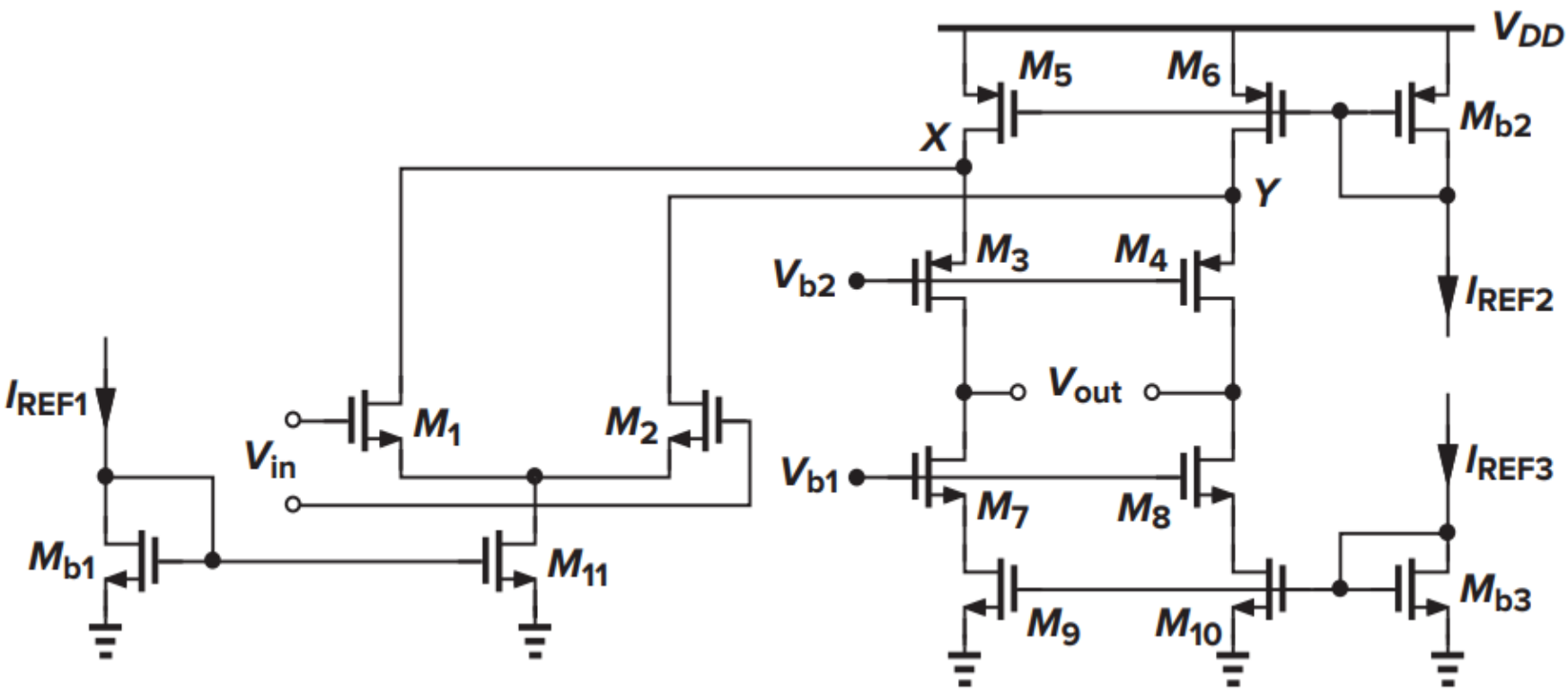
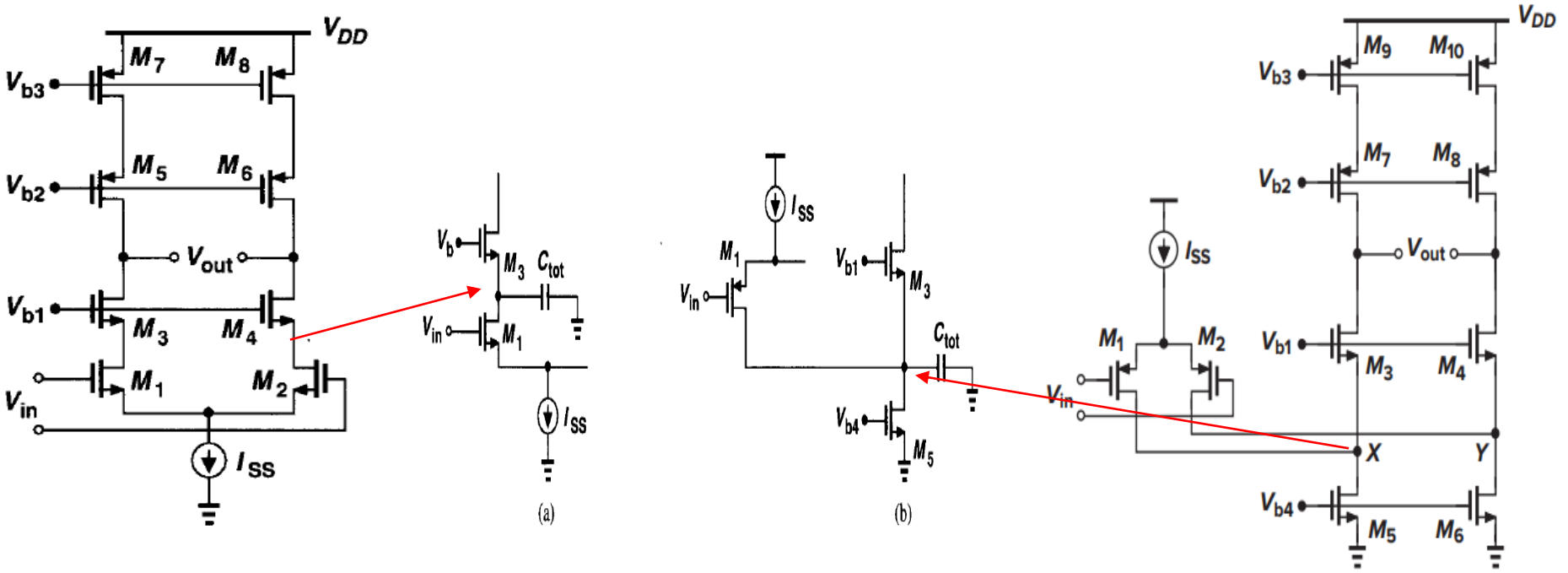


Figure 9.18 Realization of a folded-cascode op amp

与图9.15比较，增益大（NMOS输入管g_{m1}跨导大），
X点时间常数大(P管尺寸大即C_X大， 或g_{m3}小)；
NMOS输入管1/f 噪声较大（输入管为PMOS时1/f噪声较小）。

9.2.5 折叠式与直筒式的特性比较

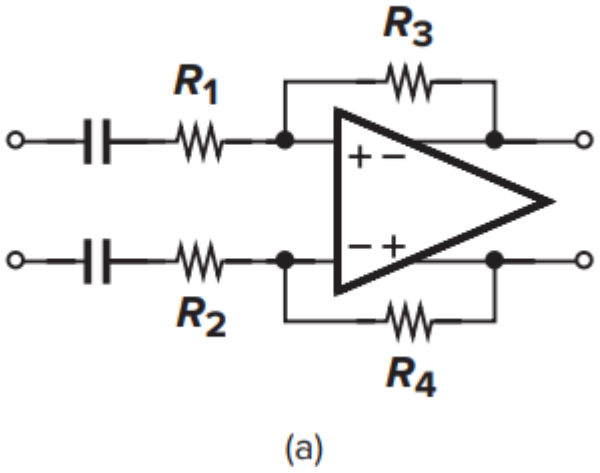


（1）直筒式带宽大，折叠式带宽小、增益较低；

（2）折叠式CASCODE输入共模范围大，输出范围稍大；可构成电压跟随器；

（3）折叠式功耗较大、噪声较大。

折叠式CASCODE COP特性（续）

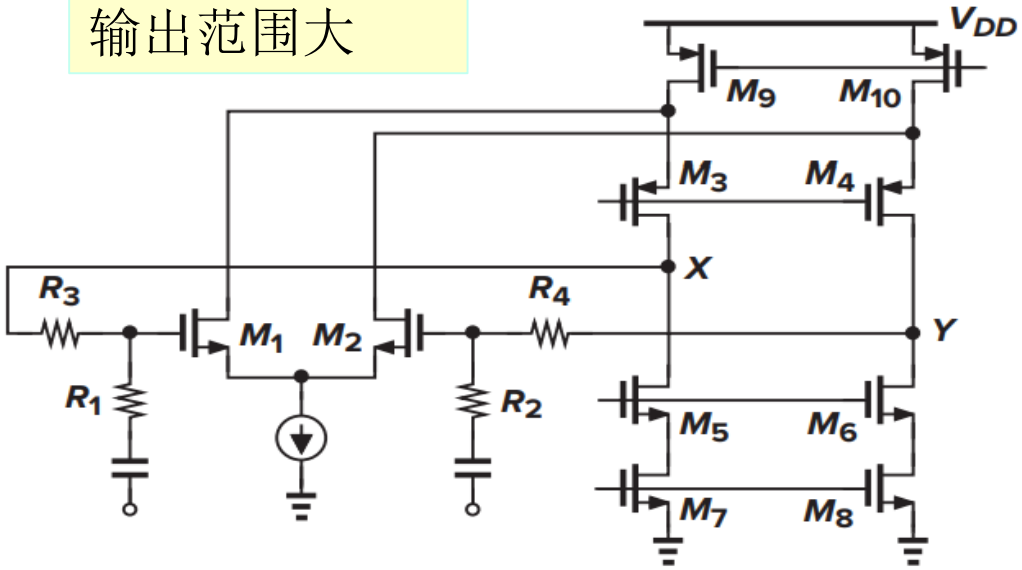


(a)

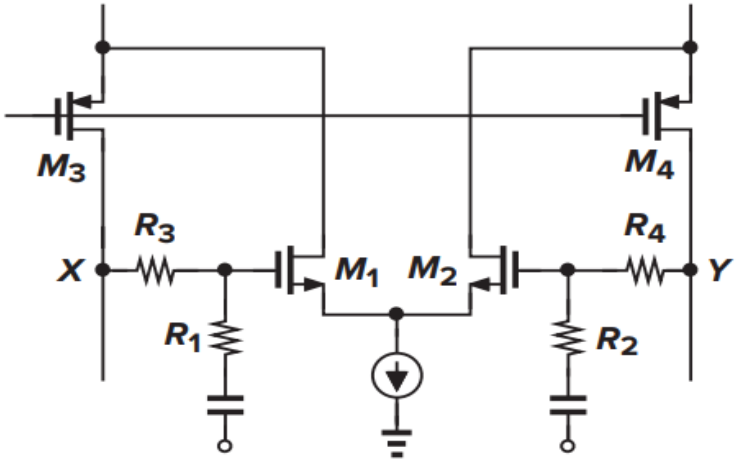
Figure 9.19
(a) Feedback amplifier
(b) implementation using a folded-cascode op amp
(c) alternative drawing to find allowable swings.

输入和输出共模电压相同。增益很高时，输入虚短，输入信号（M1和M2）栅极变化很小。

输出范围大



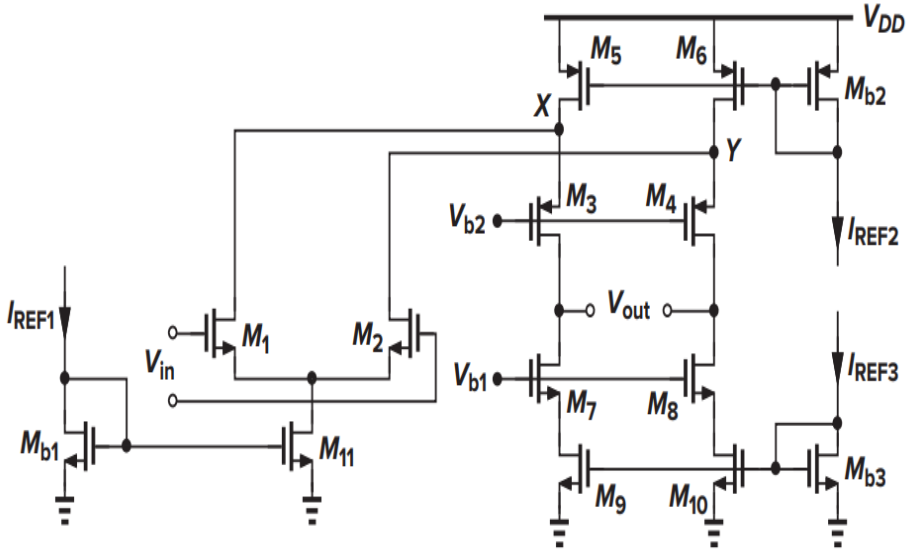
(b)



(c)

9.2.6 折叠式CASCODE OP 的设计

例9.9 Design a folded-cascode op amp with an NMOS input pair to satisfy the following specifications: V_{DD} = 3 V, differential output swing = 3 V, power dissipation = 10 mW, and voltage gain = 2000.



输出范围 → 输出支路各管过驱动电压→输入管V_{OD}

Begin with the power and swing specifications. Allocating 1.5 mA to the input pair, 1.5 mA to the two cascode branches。

开环应用时必须有 CMFB确定输出CM电平!但若构成电压跟随器，则可能利用其输入虚短特性(且有直流输入)确定其输出电平。

V_{TH} = 0.7V, 分配$V_{OD5,6}$ = 0.5V， $V_{OD3,4}$ = 0.4V, $V_{OD7\sim10}$ = 0.3V

解得： $(W/L)_{5,6}$ = 400, $(W/L)_{3,4}$ = 313, $(W/L)_{7-10}$ = 278.

Since the minimum and maximum output levels are equal to 0.6 V and 2.1 V, respectively, the optimum output common-mode level is 1.35 V.

例 9.9 (续) 折叠CASCODE OP设计

由第十章稳定性知识，运放构成电压跟随器是稳定性最不利情况

输入管的设计：

minimum input common-mode

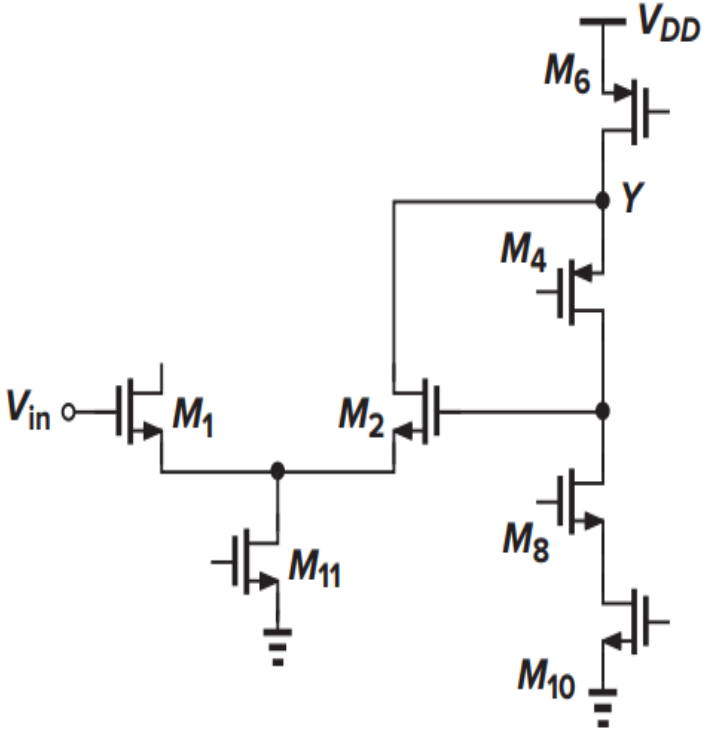
= $V_{GS1} + V_{OD11}$

if the input and the output CM levels are equal then $V_{GS2} + V_{OD11} = 1.35$ V

$V_{OD11} = 0.4$ V , $V_{GS1} = 0.95$ V,

obtaining $V_{OD1,2} = 0.95 - 0.7\ (V_{TH}) = 0.25$ V,

→ $(W/L)_{1,2} = 400$.

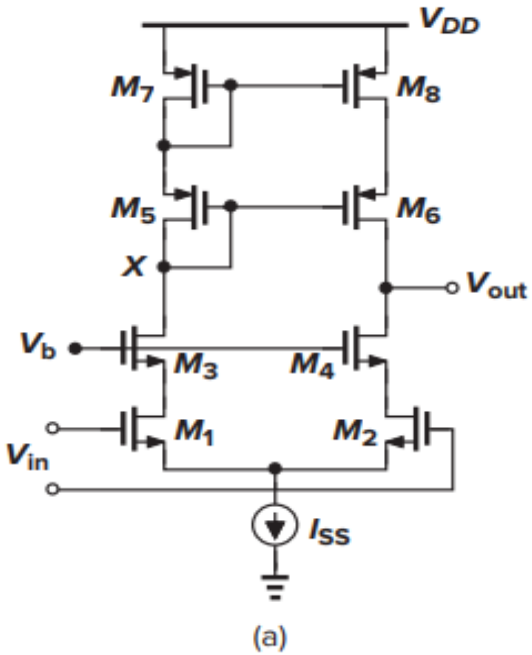


负反馈可能构成CMFB!

与输入是否有直流电平有关。

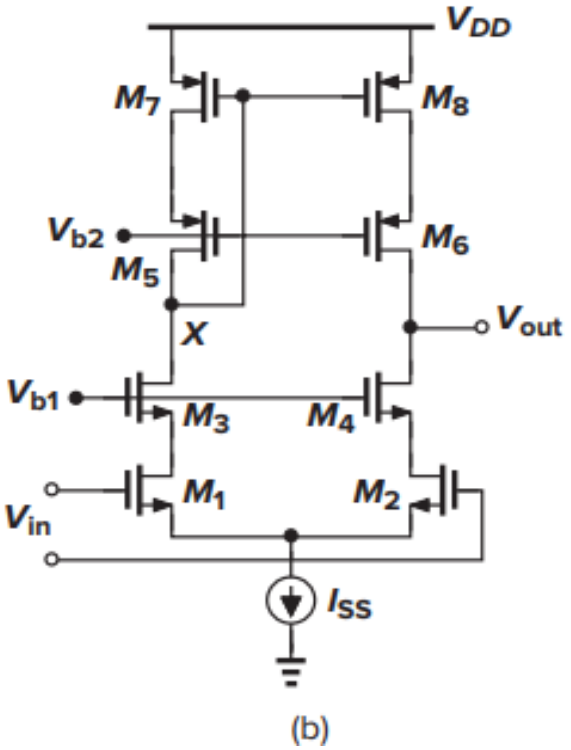
$$开环增益 A_{vopen} = \frac{V_{out}}{V_{in}} \approx g_{m1}\{g_{m4}r_{o4}(r_{o5} \,||\, r_{o2}) \,||\, g_{m8}r_{o8}r_{o10}\}$$

单端输出的cascode 电流镜运放



(a)

contains a mirror pole at node X



(b)

图(a)

$$V_X = V_{DD} - |V_{GS5}| - |V_{GS7}|,$$

maximum value of Vout:

$$V_{DD} - |V_{GS5}| - |V_{GS7}| + |V_{TH6}|$$

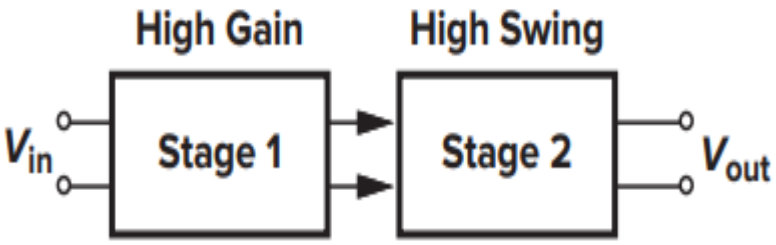
Vout最小值 =Vb-VTH4

>VODSS+VOD2+VOD4

图(b)

增大输出范围，通过Vb2将M7 and M8 are biased at the edge of the triode region

9.3 两级运放 two-stage OP amps



总增益=各级增益之积。
总带宽比每级带宽小。
输出级（输出阻抗较小，输出电压范围较大）更容易级联。

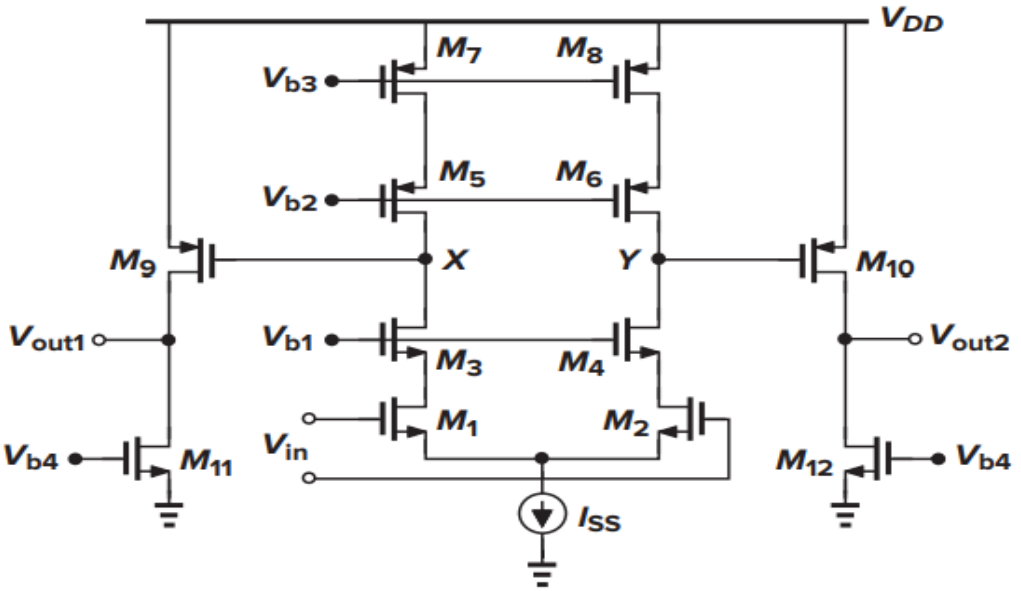


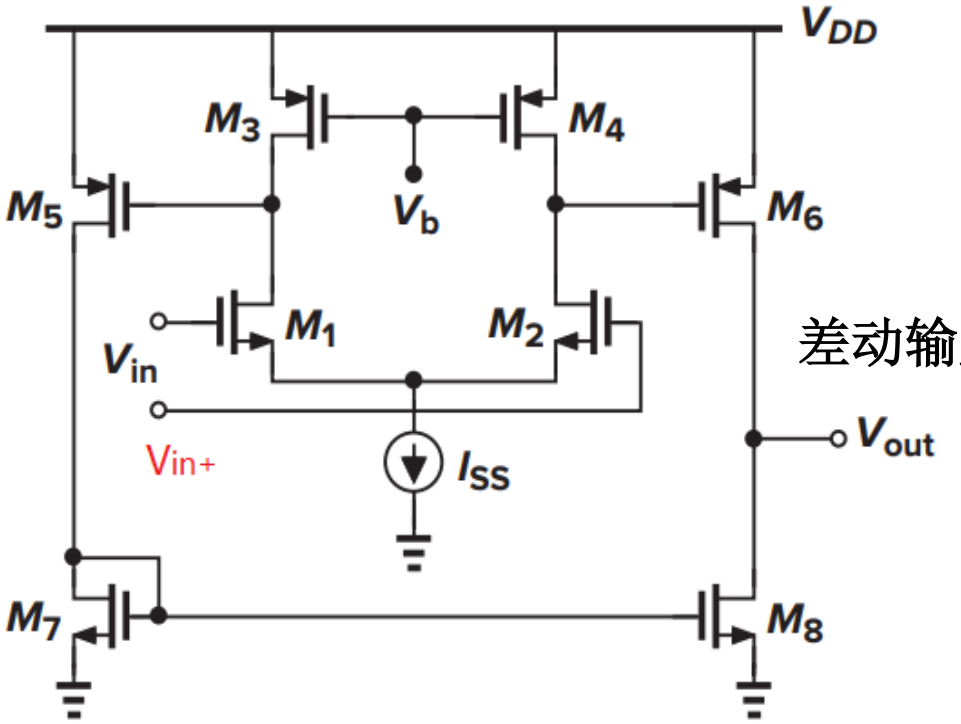
Figure 9.24 Two-stage op amp employing cascode

电流源负载运放一般Vout需CMFB，单边输出=$V_{DD} - |V_{OD5,6}| - V_{OD7,8}$

增益gain:

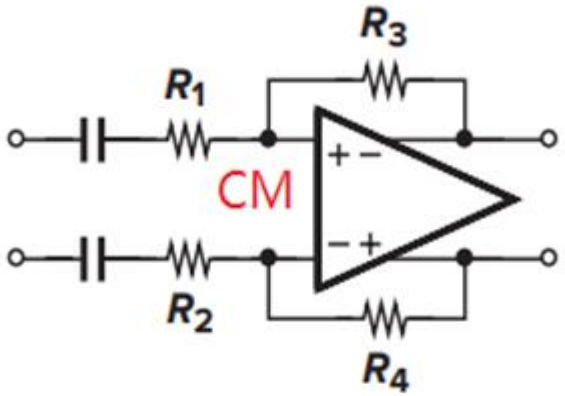
$$A_v \approx \{g_{m1,2}[(g_{m3,4} + g_{mb3,4})r_{O3,4}r_{O1,2}] \| [(g_{m5,6} + g_{mb5,6})r_{O5,6}r_{O7,8}]\}$$
$$\times [g_{m9,10}(r_{O9,10} \| r_{O11,12})]$$

单端输出的两级运放



若构成电压跟随器，Vout接Vin-;
则最小电压为$V_{GS1}+V_{ODSS}$

差动输入单端输出

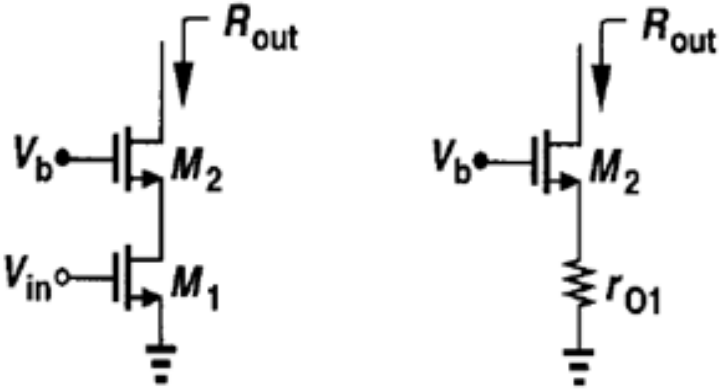


第一级放大电路（电流源负载）的直流输出电压不确定，一般（开环）需要**CMFB**；
但若外部有负反馈支路时，可能不需要专门的**CMFB**确定输出**CM**电平。

上图为全差动运放，有输入耦合电容**C**需要**CMFB**确定输出电平；若无**C**则不需要**CMFB**

9.4 增益提高：C-V反馈提高输出阻抗

提高低频增益gm（RD || Rout)：提高输出阻抗Rout，减小电流变化！



Vout在RD（上拉到电源）和Rout之间。

低压工艺不适合多级CASCODE

建模为电路跨导Gm约=gm电流源并联输出阻抗

设计思路：采用电流-电压负反馈和箝位电平增大输出阻抗。

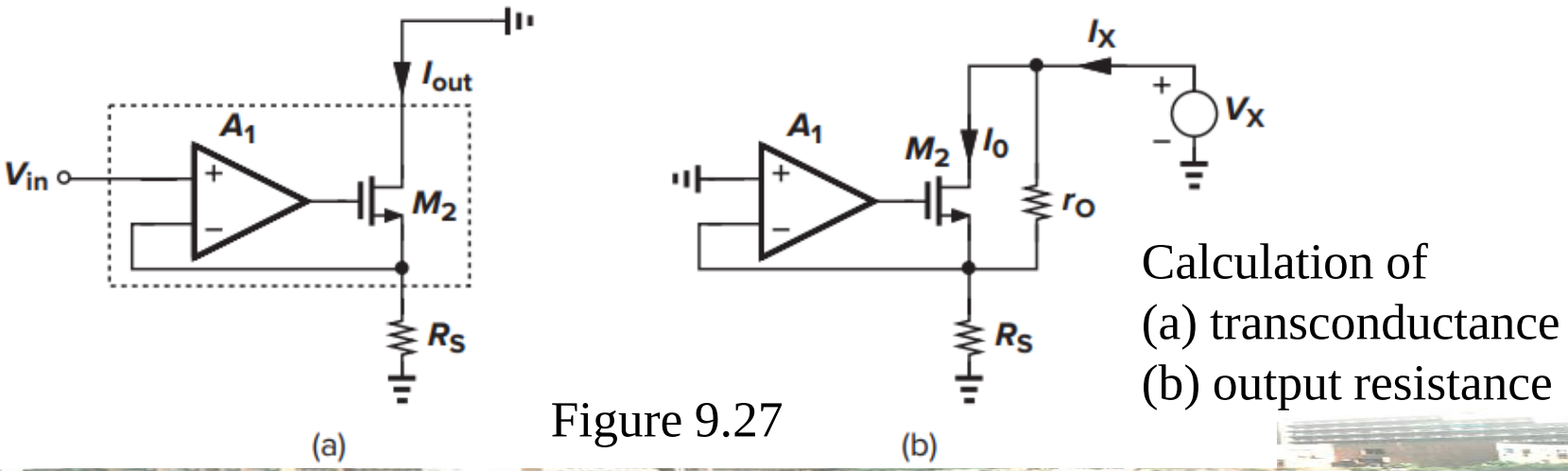
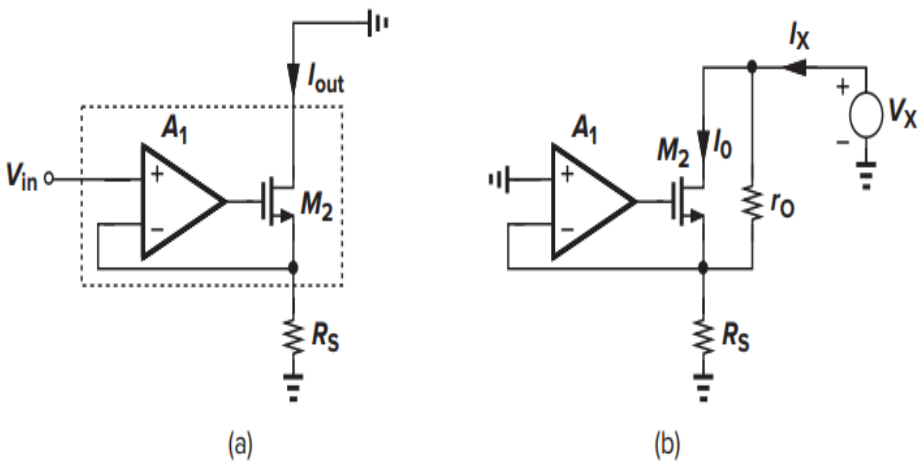


Figure 9.27

Calculation of
(a) transconductance
(b) output resistance

gain boosting（续）



图（a）：　　若计算跨导

$$I_{out} = g_m V_{GS2}$$
$$= g_m[(V_{in} - R_S I_{out})A_1 - R_S I_{out}]$$

实用电路 Vin一般不是如图所示

$$G_{mclosed} = \frac{I_{out}}{V_{in}} = \frac{A_1 g_m}{1 + (A_1 + 1) g_m R_S}$$

开环输出电阻：　　$g_m r_o R_S$ ，实为M_2的跨导g_{m2}和输出阻抗r_{o2}

反馈系数：　　$\beta = R_f (\because C - V$ 反馈$) = R_S$

图(b)，求闭环输出电阻 $\frac{V_X}{I_X}$，　$I_X = I_0 + I_{ro}$，其中：

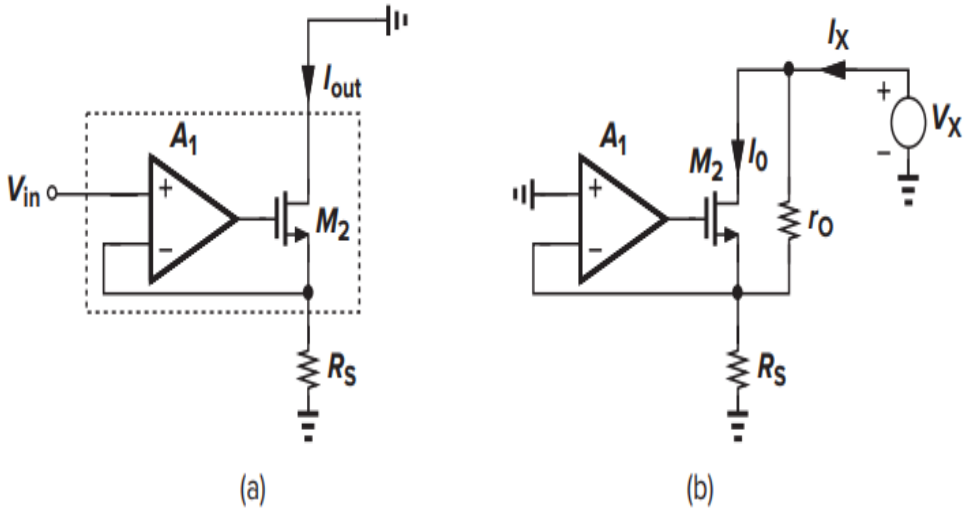
$$I_0 = g_m V_{GS2} = g_m(-A_1 R_S I_X - R_S I_X)\ ,\quad I_{ro} = \frac{V_X - R_S I_X}{r_o}$$

gain boosting（续2）

$$I_X = I_0 + I_{ro} = g_m(-A_1 R_S I_X - R_S I_X) + \frac{V_X - R_S I_X}{r_o}$$

得到闭环输出电阻（从MOS漏极）：

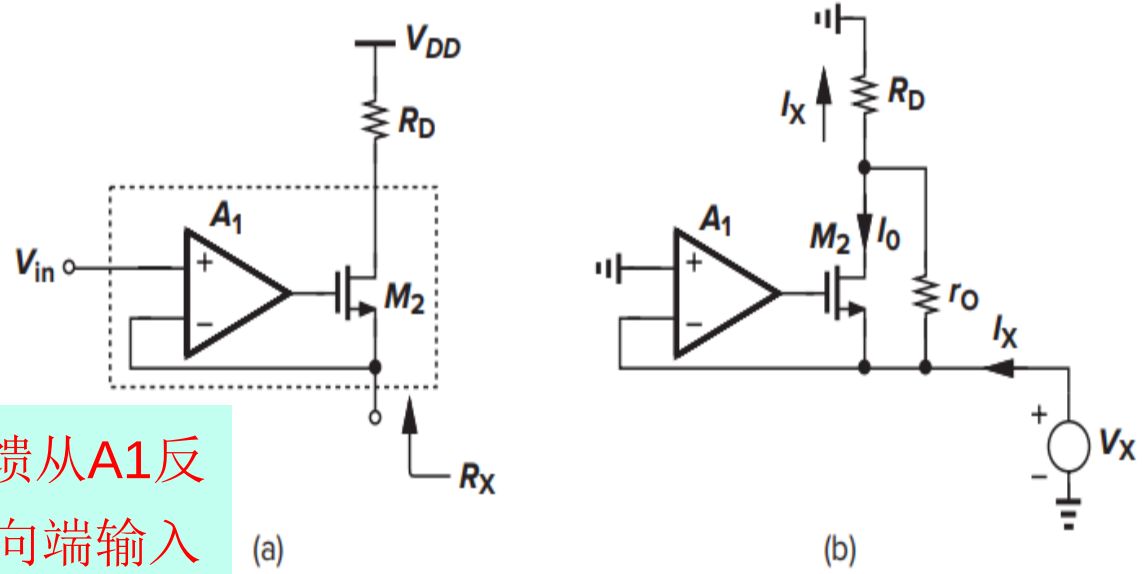
$$R_{out} = \frac{V_X}{I} = r_o + (A_1 + 1) g_m r_o R_S + R_S \approx A_1 g_m r_o R_S$$



若无A_1 （即V_{in} 直接连接到M_2 的G极）：

$$R_{out} = r_o + g_m r_o R_S + R_S$$

例9.11 增益提高MOS源级：很小输出电阻



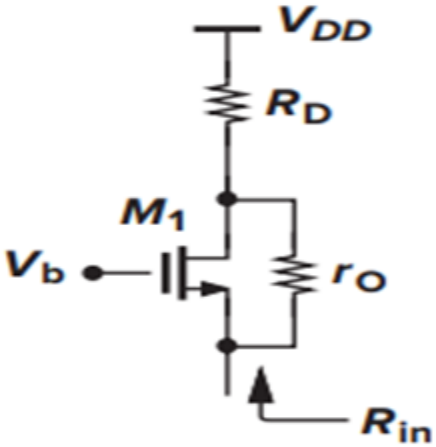
反馈从A1反向端输入

比较CG的图3.53和式（3.116）

Figure 9.28

$$\frac{I_X R_D - V_X}{r_O} + (-A_1 V_X - V_X) g_m + I_X = 0$$

$$R_X = \frac{R_D + r_O}{1 + (A_1 + 1) g_m r_O}$$

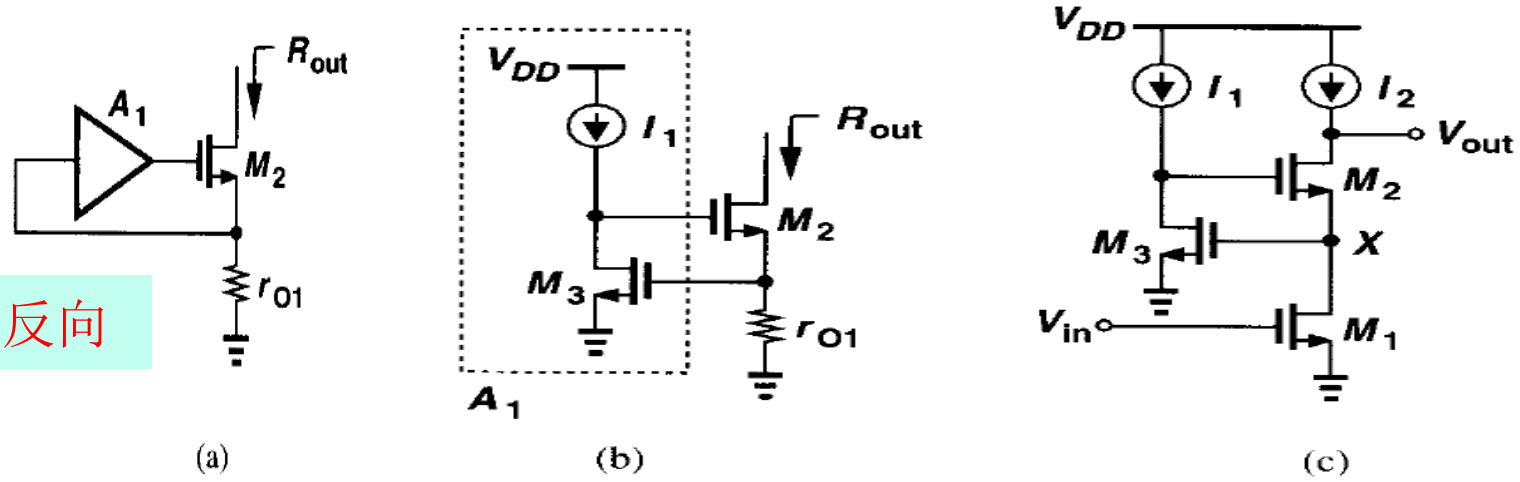


等效于MOS跨导提高了A1倍。

未计衬偏效应

$$R_{in} = \frac{V_X}{I_X} = \frac{R_D + r_o}{1 + (g_m + g_{mb}) r_o}$$

9.4.2 增益提高技术的电路实现



A1反向

(a) (b) (c)

半边电路的小信号通道

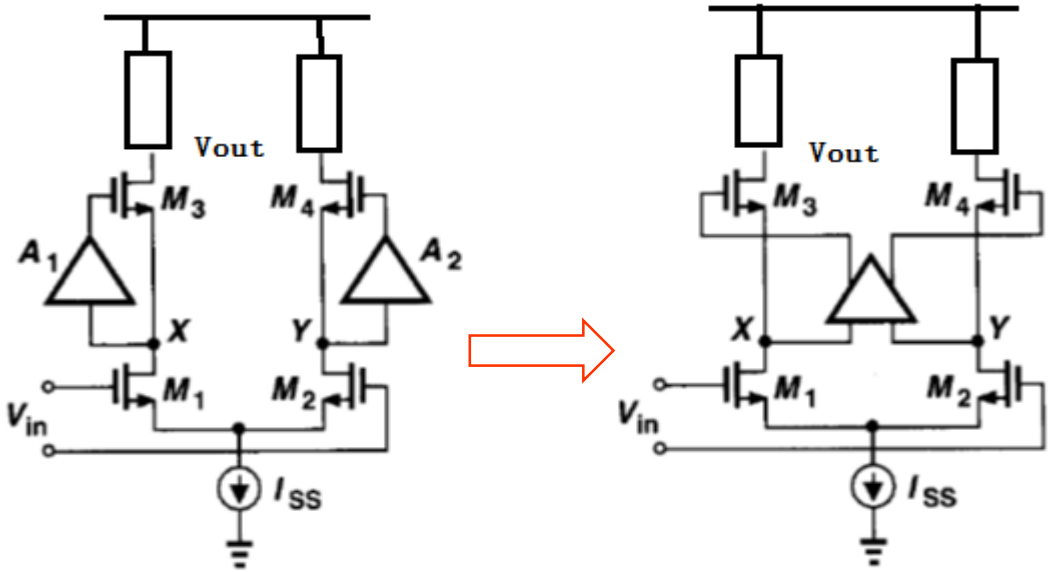
$$R_{out} \approx A_1 g_{m2} r_{O2} r_{O1}$$

假设理想电流源I1和I2，则

$$|A_v| \approx g_{m1}(g_{m2} r_{O2} r_{O1})(g_{m3} r_{O3}),$$

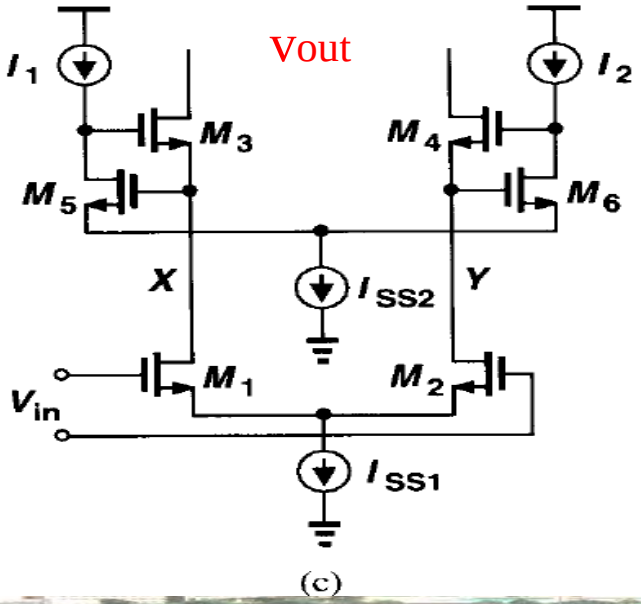
相当于3级CASCODE，但适合低压

差动电路的增益提高技术



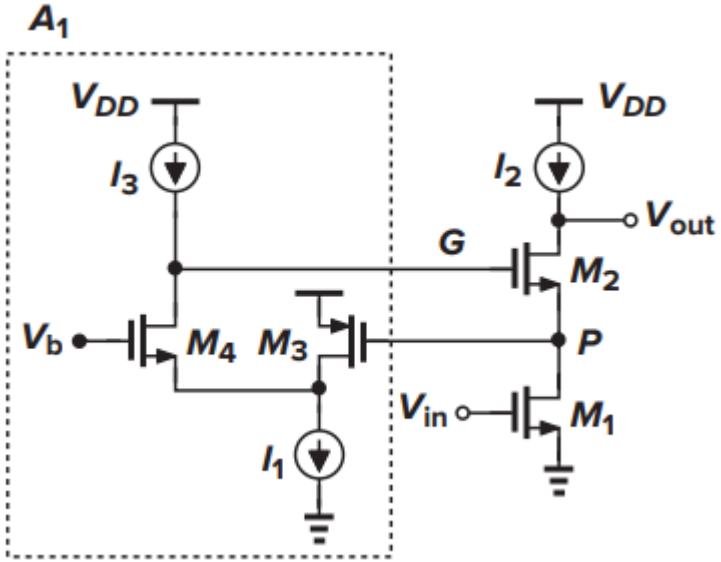
A_1和A_2反向放大器

单级差动放大器
同侧的输入与输出反向



M5或M6栅极X或Y限制（抬高）输出电平：
$V_X=V_{GS5}+V_{ISS}$，
使得Vout 范围减小；
Vx实际只需$2V_{OD}$，
因此该电路浪费V_{TH}

改进型：A1为折叠型



单边电路

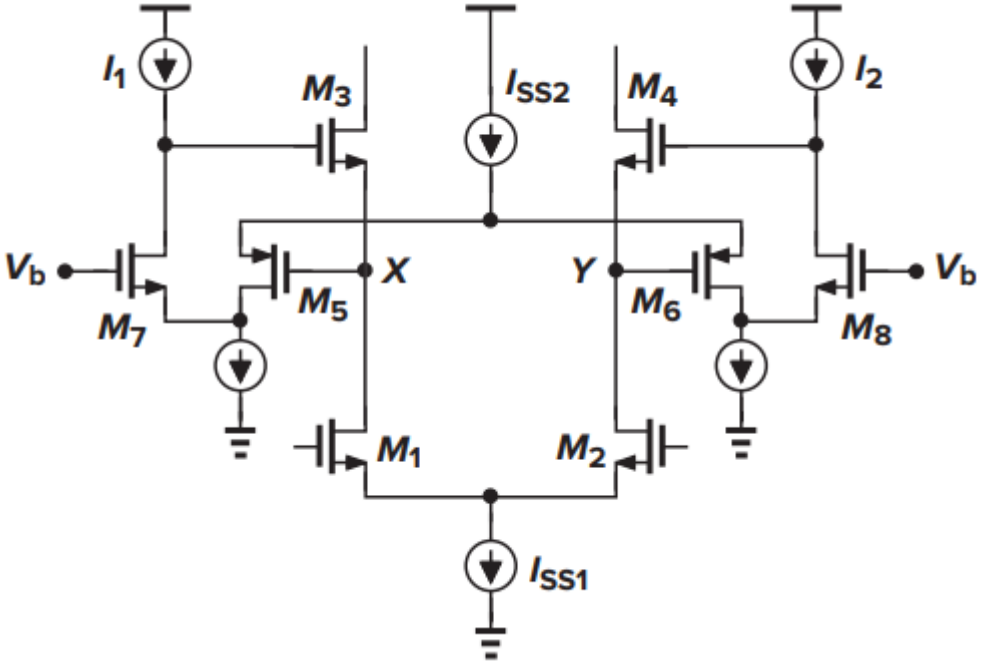
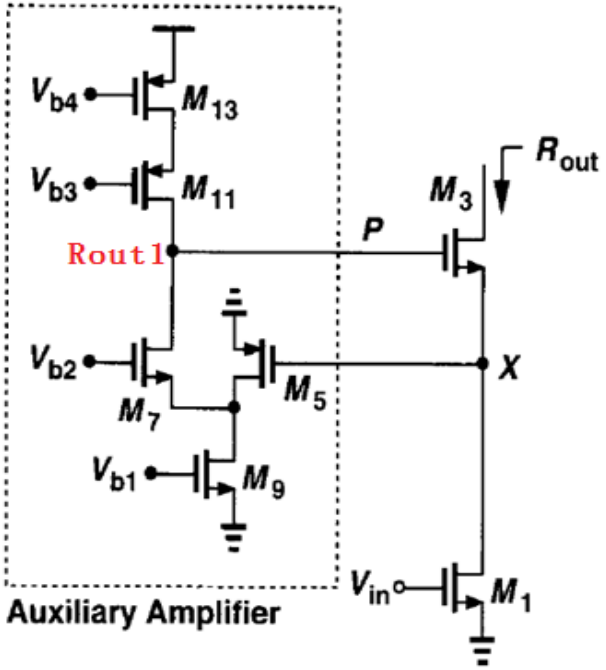


Figure 9.34 Folded-cascode circuit used as auxiliary amplifier.

差动电路（不包括M3漏极输出负载）

minimum allowable level of $V_X = V_{OD1} + V_{ISS1}$

例 9.14　计算输出阻抗Rout



增益与Rout成正比，
Rout与辅助放大器增益（幅度）成正比；
先求辅助放大器输出阻抗。

Figure 9.35　半边电路（小信号）

$$R_{out1} \approx \{g_{m7}r_{o7}(r_{o9} \,||\, r_{o5})\} \,||\, (g_{m11}r_{o11}r_{o13})$$

$$R_{out} \approx g_{m3}r_{o3} \times r_{o1} \times g_{m5}R_{out1}$$

$$= g_{m3}r_{o3}r_{o1} \times g_{m5}\{【g_{m7}r_{o7}(r_{o9} \,||\,||\, r_{o5})】 \,||\, (g_{m11}r_{o11}r_{o13})\}$$

输出端上下阻抗对称才能得到最大增益

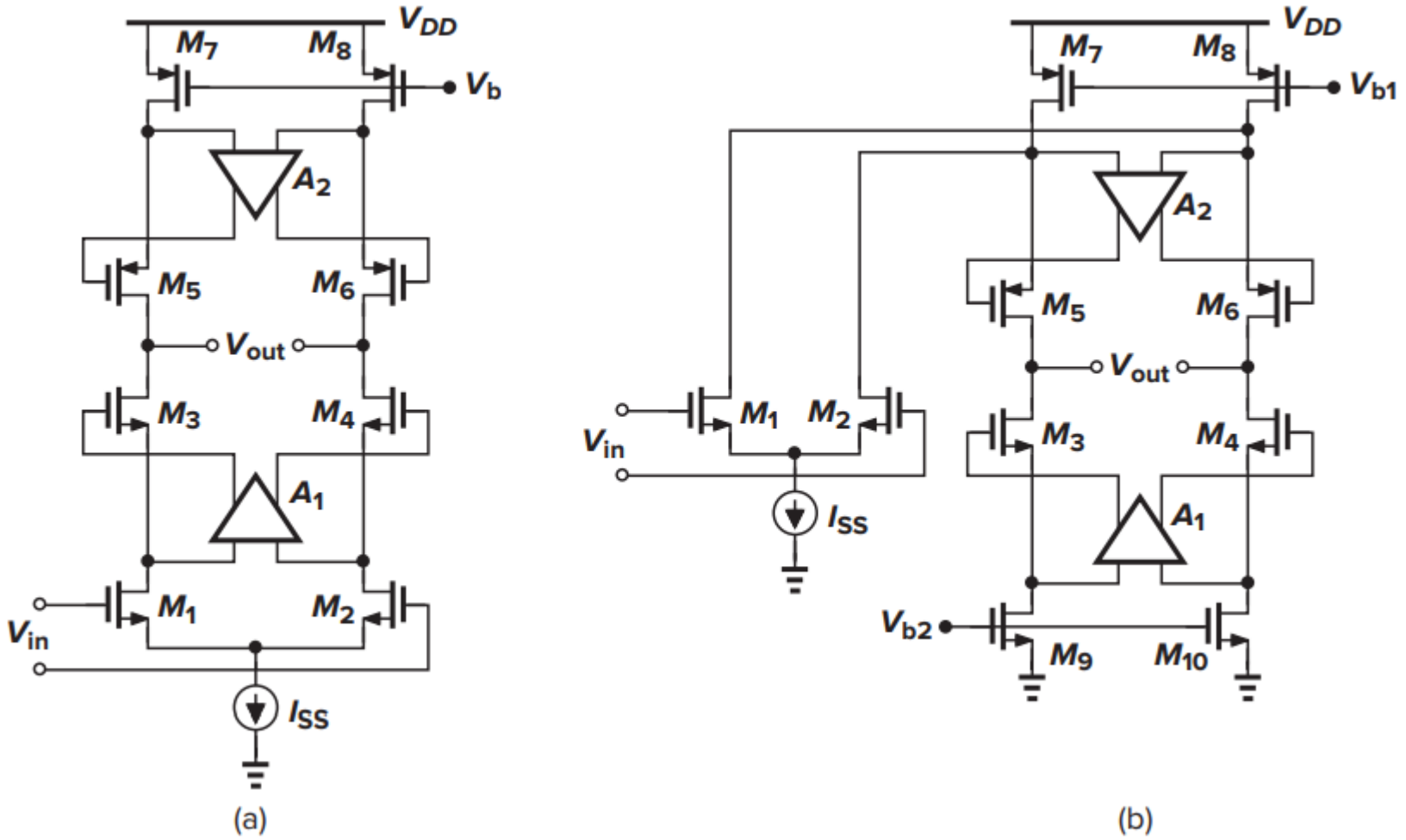


Figure 9.36 Gain boosting applied to both signal path and load devices

9.5 性能比较comparison

Table 9.1 Comparison of performance of various op amp topologies.

	Gain	Output Swing	Speed	Power Dissipation	Noise
Telescopic	Medium	Medium	Highest	Low	Low
Folded-Cascode	Medium	Medium	High	Medium	Medium
Two-Stage	High	Highest	Low	Medium	Low
Gain-Boosted	High	Medium	Medium	High	Medium

增益提高技术以功耗为代价，不符合现代便携式系统电路芯片设计的指导思想。

9.6 输出摆幅计算

仿真（测试）原理：进入线性区，增益下降。

估算依据：偏置电平和各管$V_{DS} > V_{OD}$；

单端摆幅 = 电源电压 - 轨到轨各管最小V_{DS}之和

若采用纳米管工艺，由于V_{OD}不很明确，需要通过仿真确定。

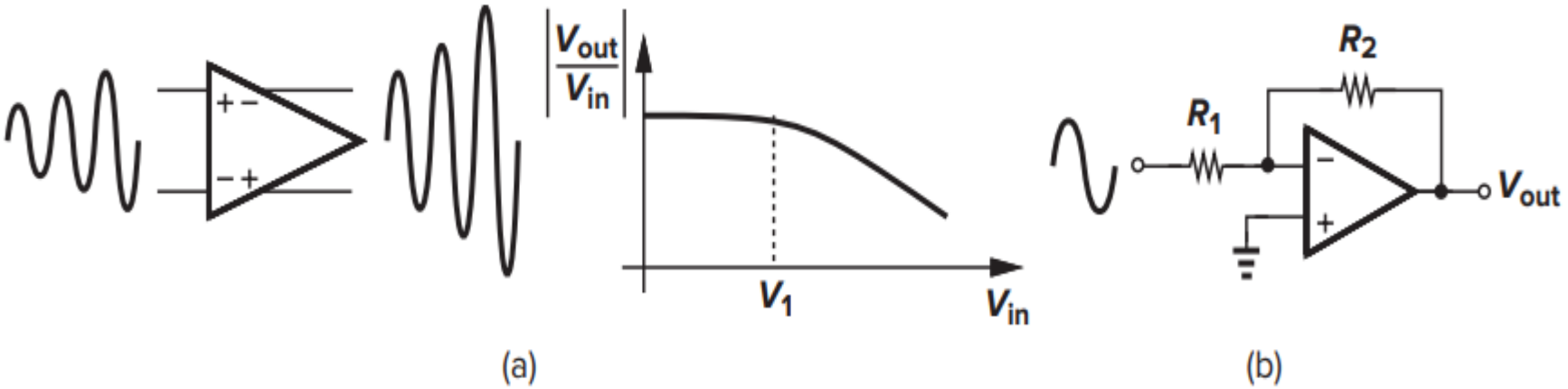
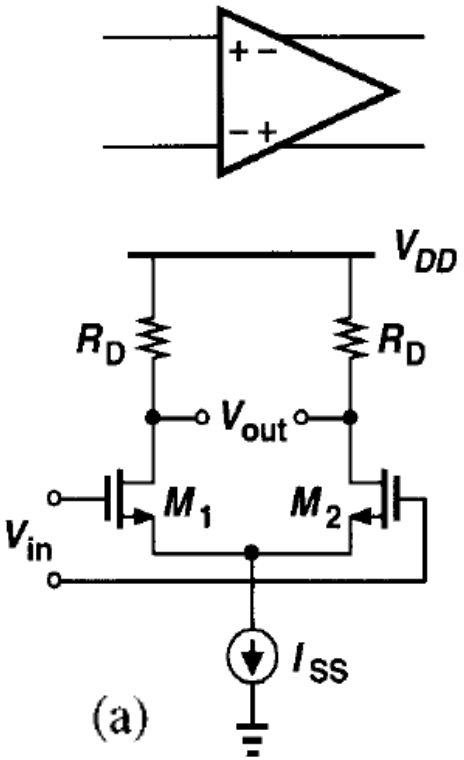


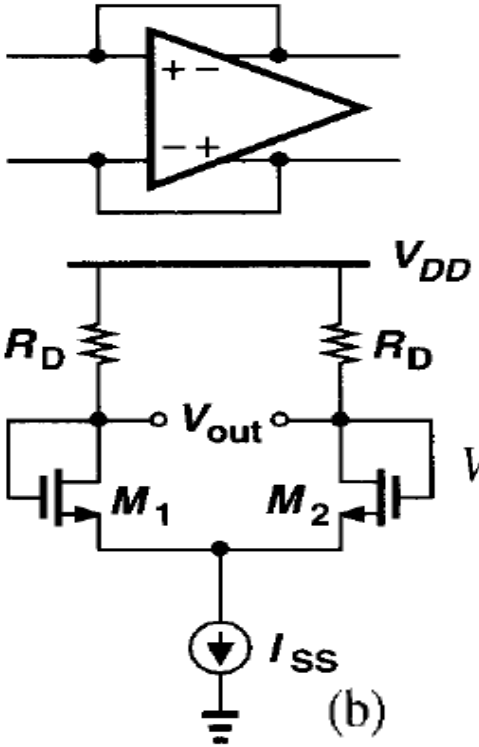
Figure 9.39 (a) Simulation of gain versus input amplitude (b) feedback amplifier

输入加正弦信号，测量输出失真（谐波），
例如失真1dB时的最大输出幅度。

9.7 共模反馈 CMFB

CMFB针对电流源负载的全差动电路，确定输出直流CM电平。





Common-Mode Feedback (CMFB)

$V_{DD} - I_{SS}R_D/2.$

输出共模电平确定

电流负载CM电平不确定

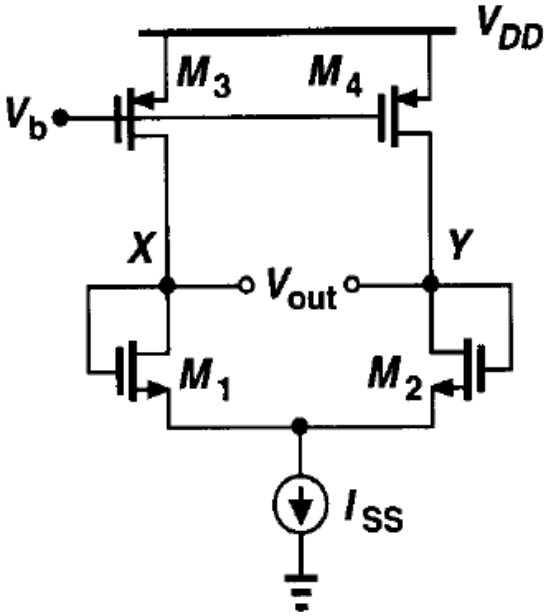
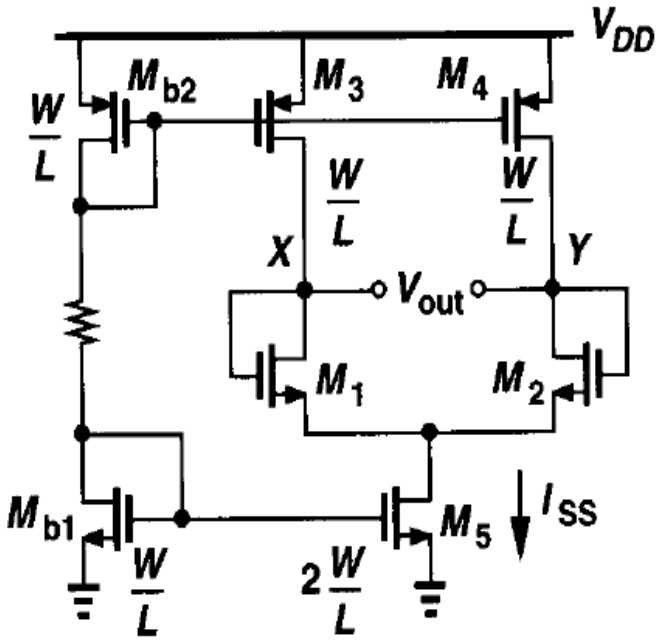


Figure 9.41



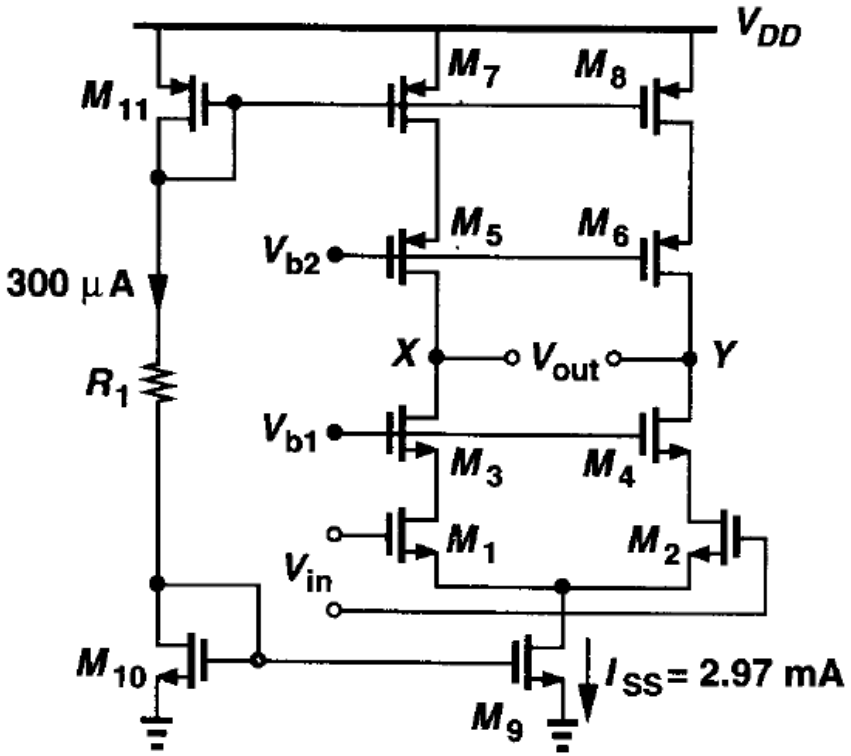
(b) effect of current mismatches.

共模电平不确定。并不是有反馈就能确定CM电平

mismatches in the PMOS and NMOS current mirrors create a finite error between $I_{D3,4}$ and $I_{SS}/2$

Differential feedback cannot define the CM level.

Example 9.16

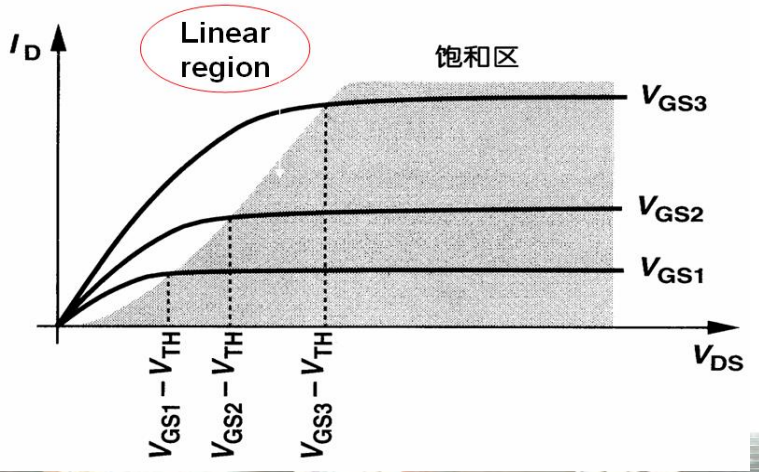


Suppose M_9 suffers from a 1% current mismatch with respect to M_{10}, producing I_{SS} = 2.97 mA rather than 3 mA.

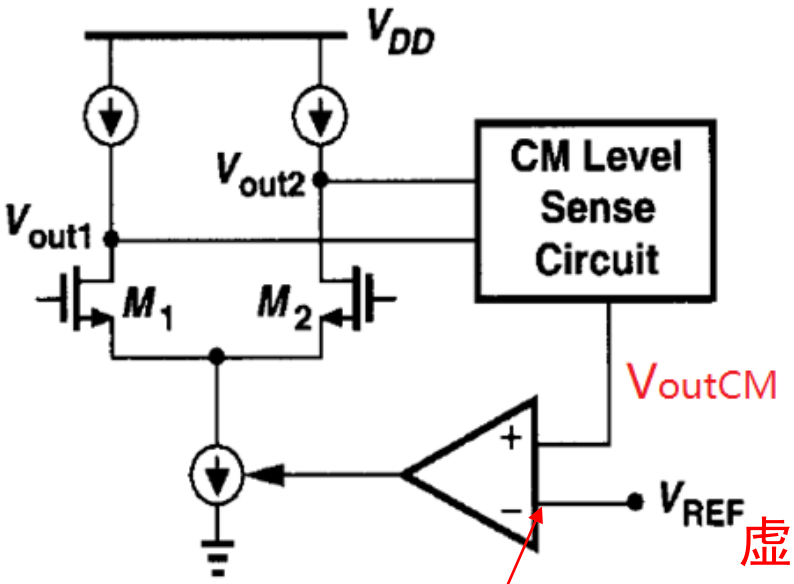
若MOS为非理想电流源，将被强制减少电流（使上下电流源总电流一致），将导致大电流的MOS管V_{DS}减少，该管进入线性区。

$$I_D = \frac{1}{2}\mu_n C_{OX}\frac{W}{L}(V_{GS} - V_{Tn})^2(1 + \lambda V_{DS})$$

则V_{DS}变化大



9.7.2 共模检测技术和CMFB原理性电路



虚短：

$V_{outCM}=V_{REF}$

Figure 9.44 Conceptual topology for common-mode feedback.

比较器输出电平范围要合适。

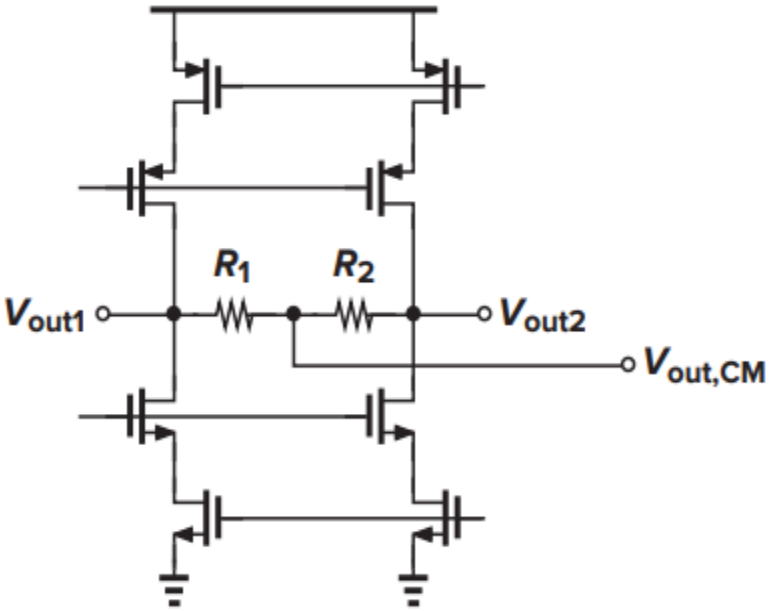
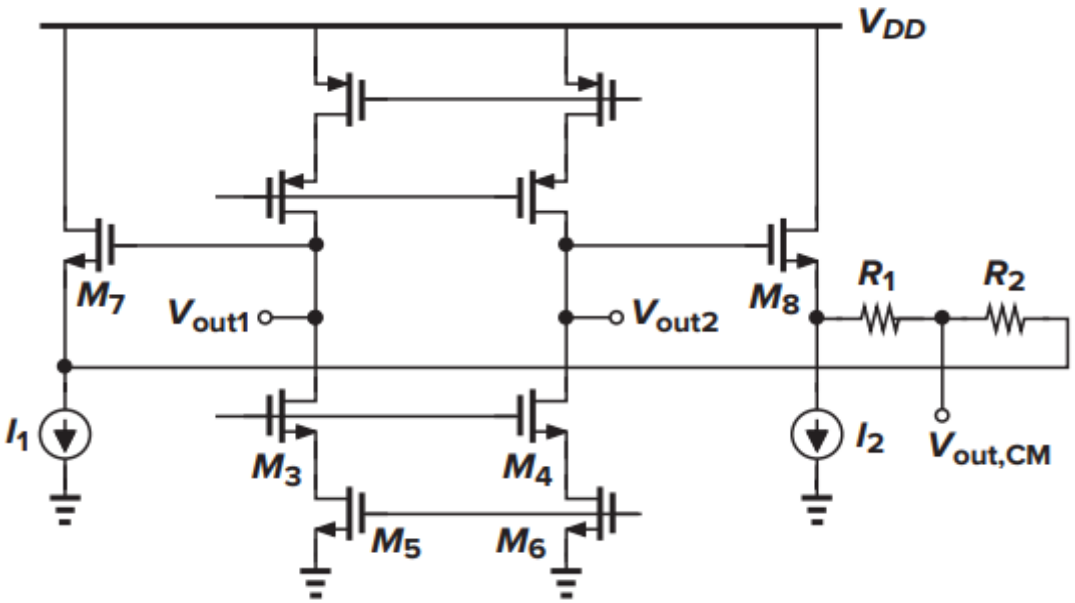


Figure 9.45 Common-mode feedback with resistive sensing

输出加源跟随器的CM检测电路



源极跟随器输出阻抗很小，R1和R2不必阻值很大。

与先前（图9.44）电路相比，本电路的CMFB比较器参考电压设置时，需要将$V_{out1,2}$直流CM电平相应地减小V_{GS8}

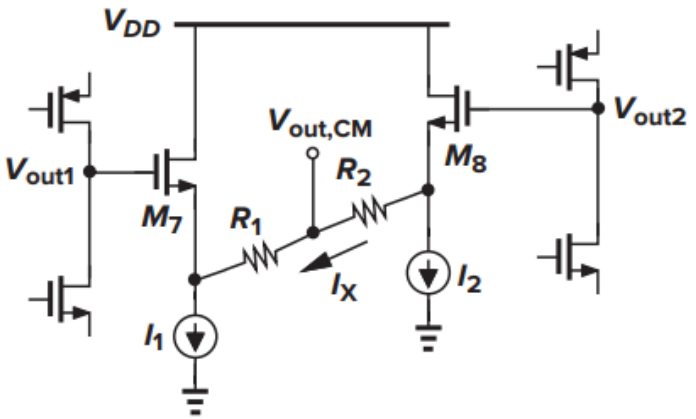
Figure 9.46 Common-mode feedback using source followers

如右图，应满足：

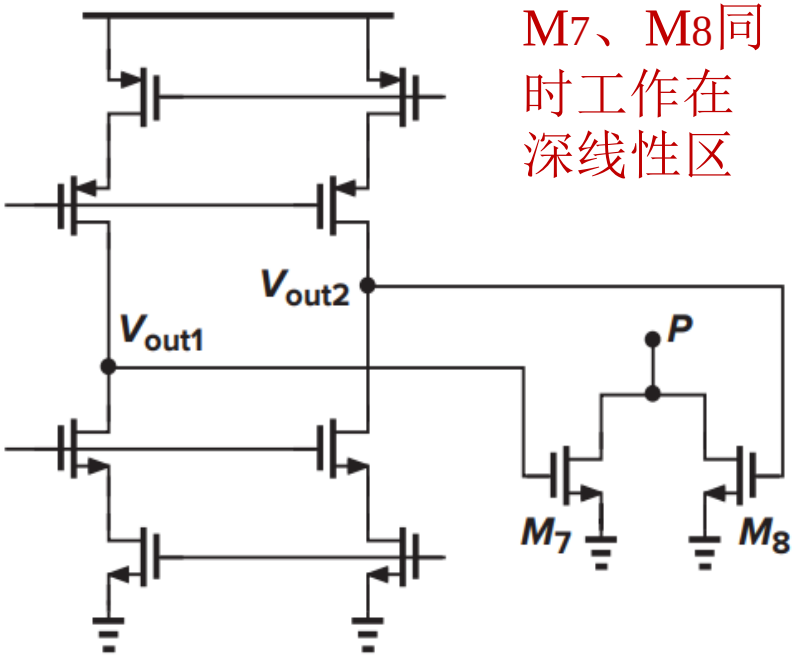
$$I_1 \approx \frac{V_{out2} - V_{out1}}{R_1 + R_2} + I_{D7}$$

$\therefore$ R_1和R_2以及I_1和I_2应足够大，

否则M_7和M_8没有正常电流即“挨饿”



另一种CM检测方法：三极管区测量CM



M7、M8同时工作在深线性区

$$R_{tot} = R_{on7} \| R_{on8}$$

$$= \frac{1}{\mu_n C_{ox} \frac{W}{L}(V_{out1} - V_{TH})} \Bigg\| \frac{1}{\mu_n C_{ox} \frac{W}{L}(V_{out2} - V_{TH})}$$

$$= \frac{1}{\mu_n C_{ox} \frac{W}{L}(V_{out2} + V_{out1} - 2V_{TH})}$$

$V_{out1}+V_{out2}=2V_{OCM}$与Rtot成反比

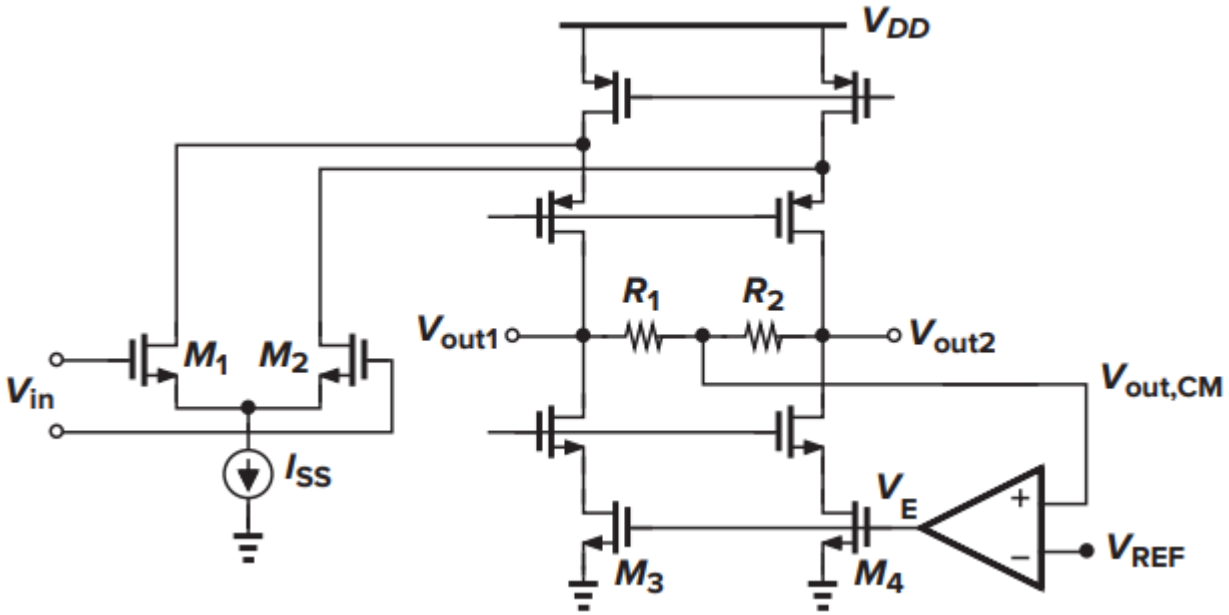
Figure 9.48 (a) Common-mode sensing using MOSFETs operating in the deep triode region,

设P点电位低，使M7、M8同时工作在深线性电阻区；

即：V_{out1}和V_{out2} >> $V_{TH7,8}+V_P$ （$V_P = V_{DS7,8}$），

输出变化幅度大时不易满足。

9.7.3 共模反馈技术



CMFB是负反馈；

控制输出支路。

本电路VoutCM 可加滤波电容，不破坏电路稳定性。

Figure 9.51 Sensing and controlling output CM level

使输出CM电平调整到设置的V_{REF}

控制输入电路的CMFB

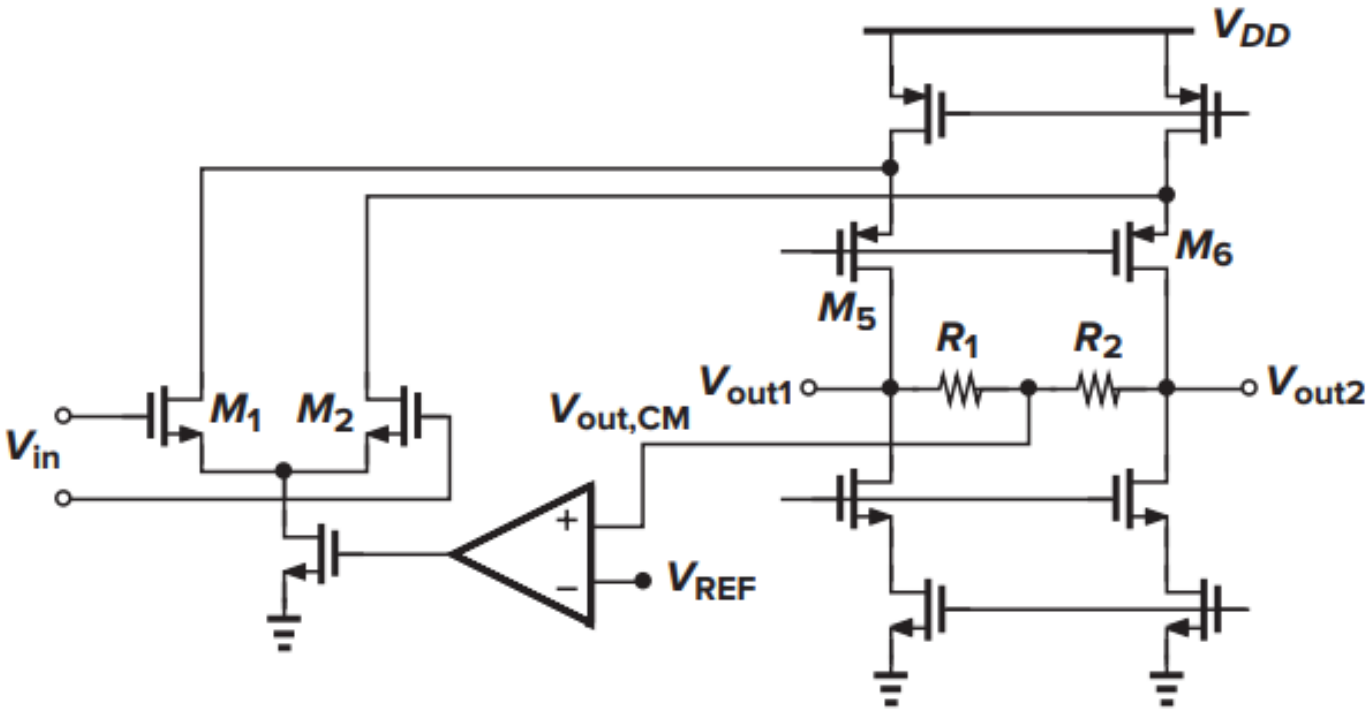
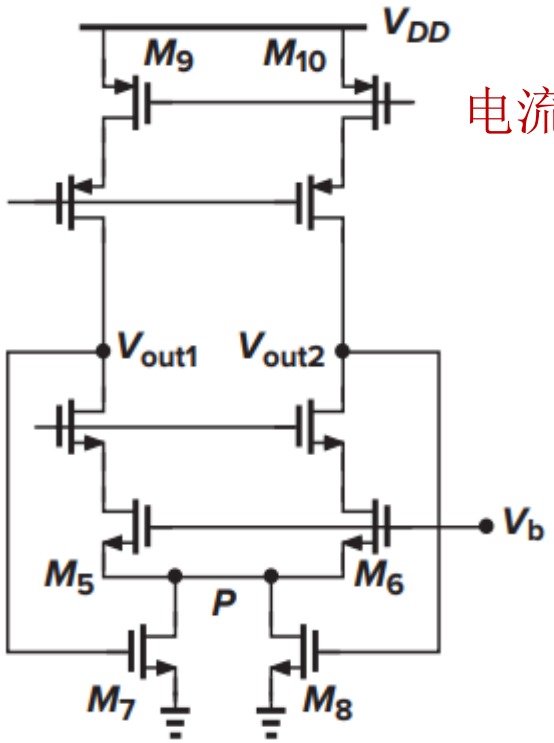


Figure 9.52 Alternative method of controlling output CM level.

CMFB调整输出CM电平的原理，
V_{outCM}可加C滤波，对信号和稳定性无影响。

深线性区电阻CMFB技术： 调节输出



电流源

if Vout1 and Vout2 rise, Ron7||Ron8 falls.

$I_{D9} = I_{D10} = I_D$,

$V_b - V_{GS5} = 2I_D(R_{on7}\|R_{on8})$,

即 $R_{on7}\|R_{on8} = (V_b - V_{GS5})/(2I_D)$

需设置Vb，使M7、M8工作在线性区，即P 点电位很低

$$R_{tot} = R_{on7}\|R_{on8}$$

$$= \frac{1}{\mu_n C_{ox}\left(\frac{W}{L}\right)_{7,8}(V_{out2} + V_{out1} - 2V_{TH})} = \frac{V_b - V_{GS5}}{2I_D}$$

前提：V_{out1}和V_{out2}变化范围不大，保证M7和M8在深线性区

$$V_{out1} + V_{out2} = \frac{2I_D}{\mu_n C_{ox}\left(\frac{W}{L}\right)_{7,8}} \frac{1}{V_b - V_{GS5}} + 2V_{TH}$$

$$V_{GS5} = \sqrt{2I_D/[\mu_n C_{ox}(W/L)_5]} + V_{TH5}.$$

缺点：不很准，受温度和工艺偏差影响；Vout1,2不能加滤波电容。

深线性区电阻CMFB技术，调节输入

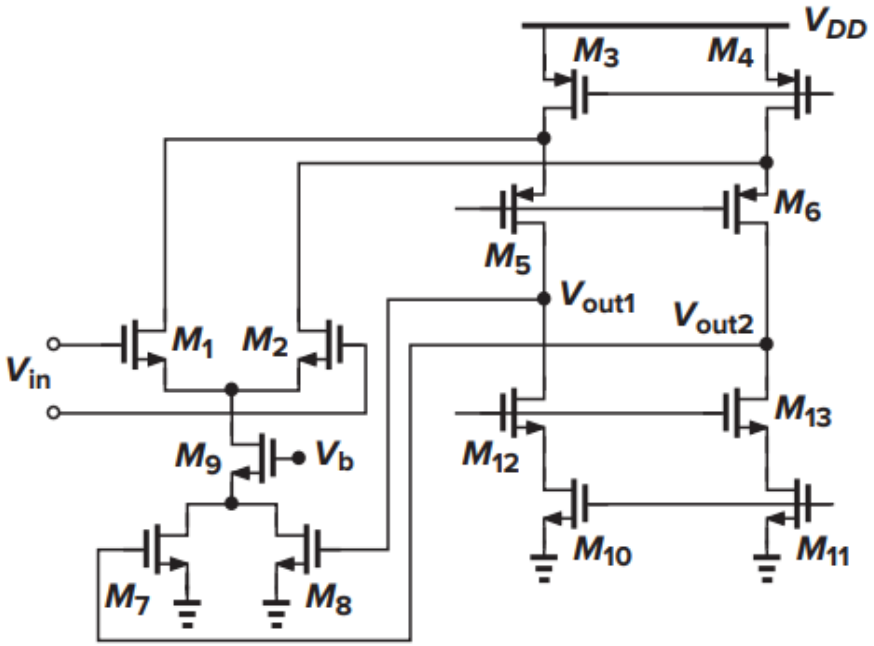
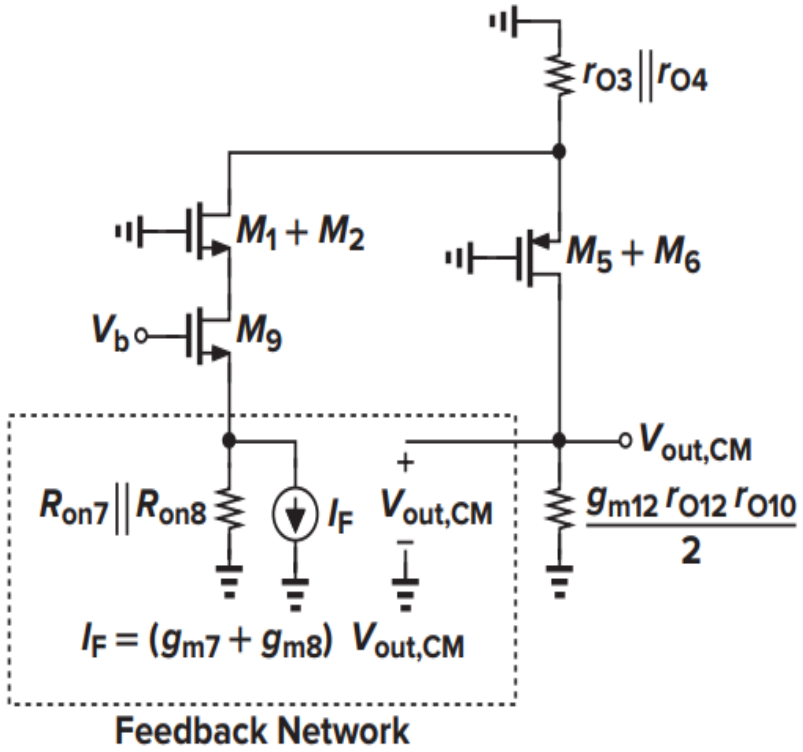


Figure 9.54 Alternative method of controlling output CM level.



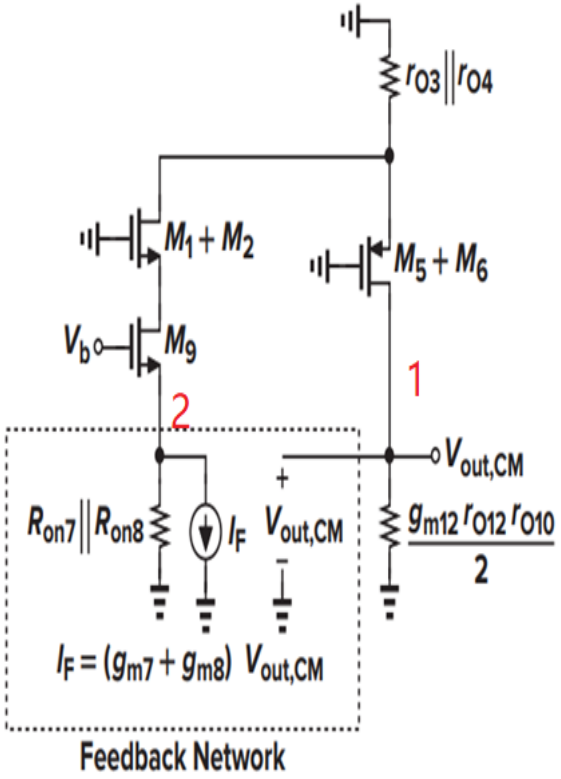
直流偏置V-V负反馈支路G模型：

$$I_1 = G_{11}V_1 + G_{12}I_2$$

$$V_2 = G_{21}V_1 + G_{22}I_2$$

$$\beta = \frac{V_2}{V_1}\Big|_{I2=0}$$

例9.18 深线性区电阻CMFB，调节输入



M_7 and M_8 must be in the triode region:

$g_{m7} = g_{m8} = \mu_n C_{ox} (W/L)_7 V_{DS7}$

$$\beta = \frac{V_2}{V_1}\Big|_{I2=0}$$

$$= -(g_{m7} + g_{m8})(R_{on7} \| R_{on8})$$

$$= -2\mu_n C_{ox} \left(\frac{W}{L}\right)_{7,8} V_{DS7,8} \cdot \frac{1}{2\mu_n C_{ox}(W/L)_{7,8}(V_{GS7,8} - V_{TH7,8})}$$

$$= -\frac{V_{DS7,8}}{V_{GS7,8} - V_{TH7,8}}$$

M9是源跟随器：dVb=dV2

$$\left|\frac{dV_{out,CM}}{dV_b}\right|_{closed} \approx \frac{V_{GS7,8} - V_{TH7,8}}{V_{DS7,8}}$$

$V_{DS7,8}$大好，则Vb变化对Vout影响小

深线性区电阻CMFB的部分偏置电路

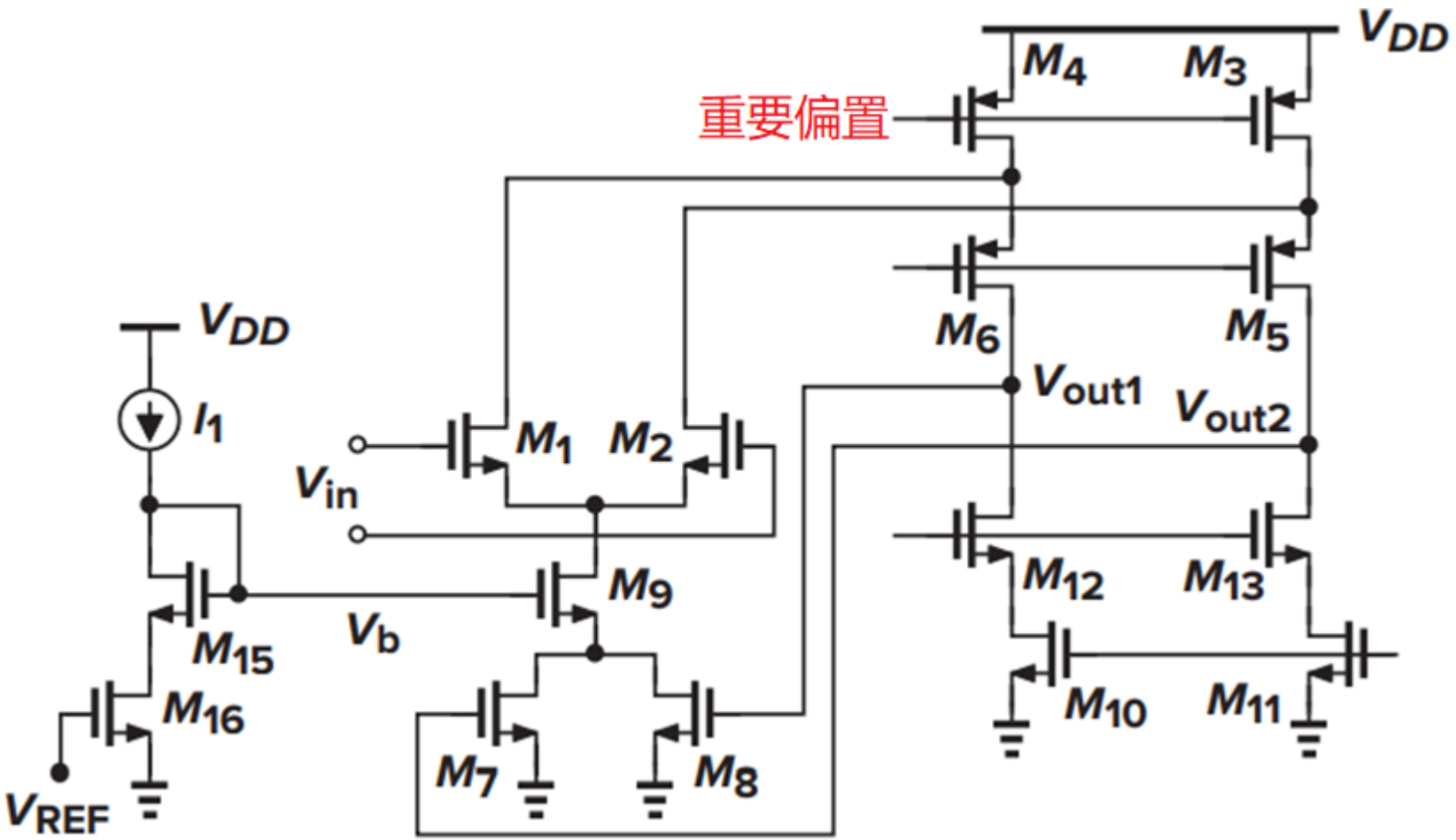


Figure 9.56 Modification of CMFB for more accurate definition of output CM level

深线性区电阻CMFB技术的偏置电路

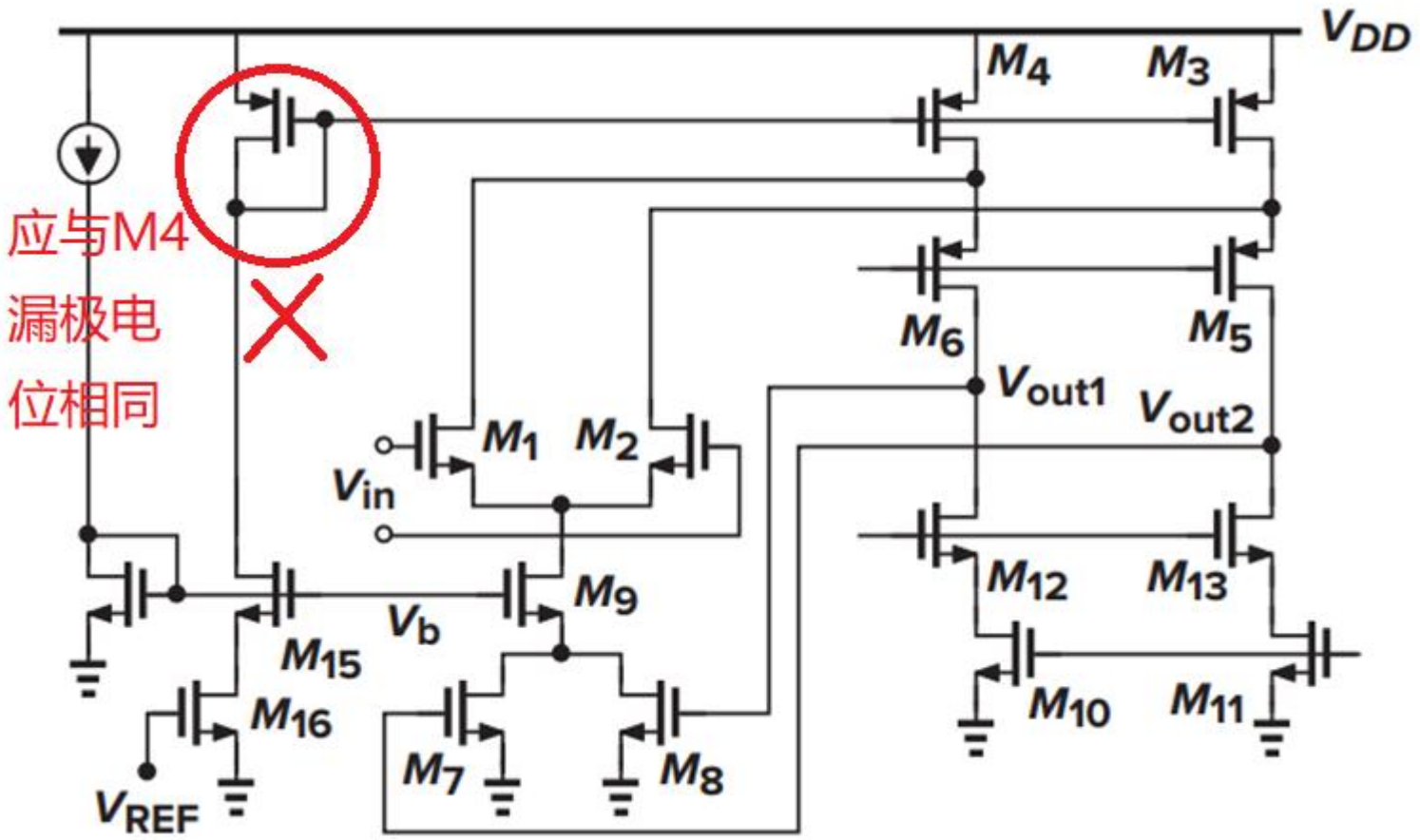


Figure 9.56 Modification of CMFB for more accurate definition of output CM level

改进的深线性区电阻CMFB技术

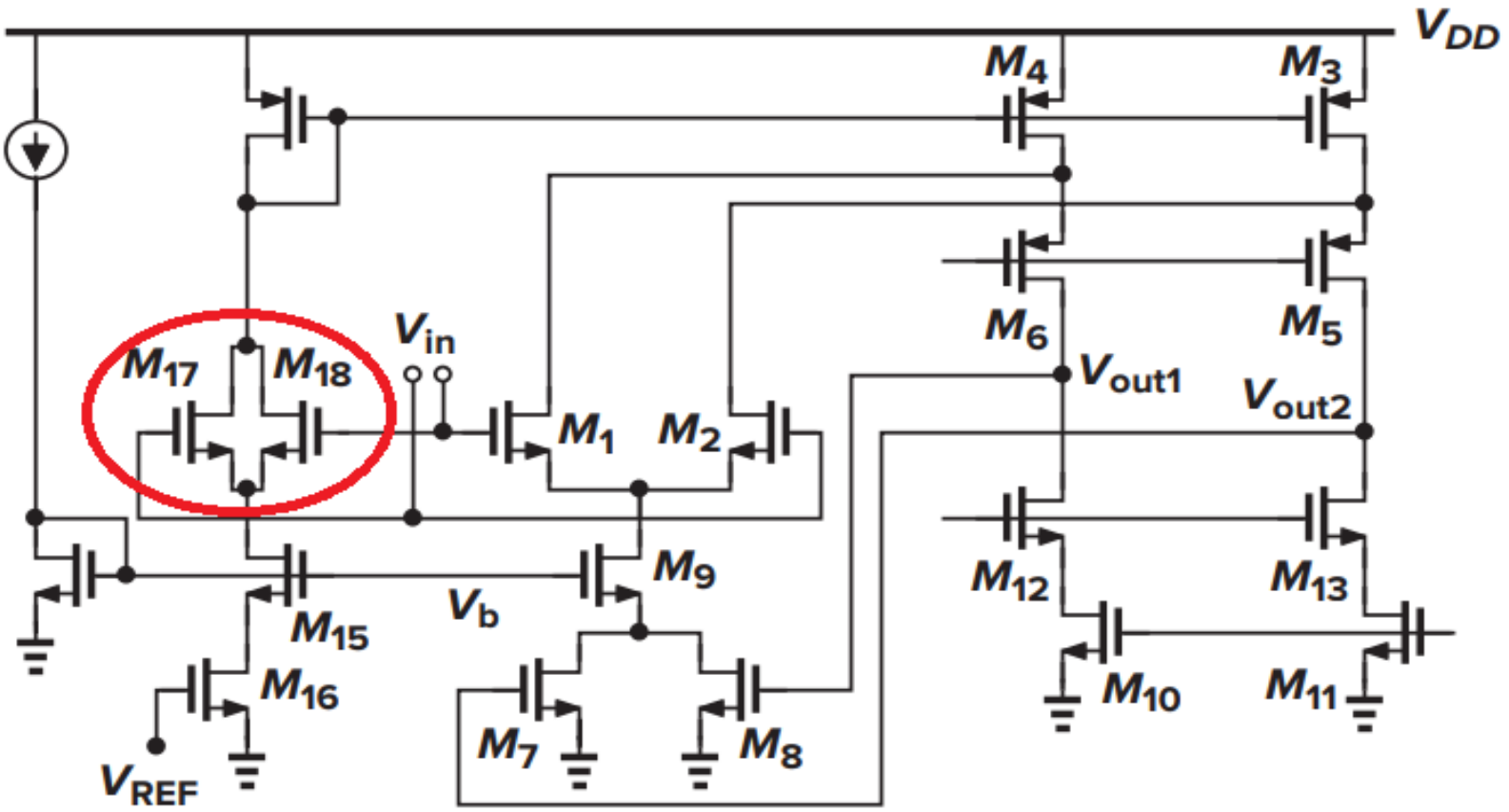
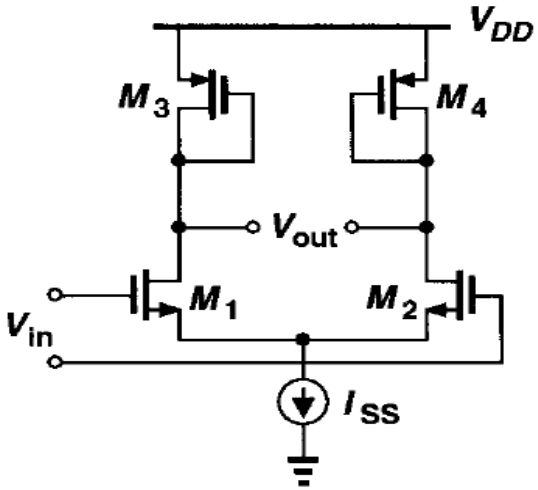


Figure 9.57 Modification to suppress error due to channel-length modulation

$(W/L)_{15} = (W/L)_9$, $(W/L)_{16} = (W/L)_7+(W/L)_8$

二极管负载（CM确定）简单差分对CMFB



图（a） 共模输出确定

Figure 9.58 (a) Differential pair using diode-connected loads

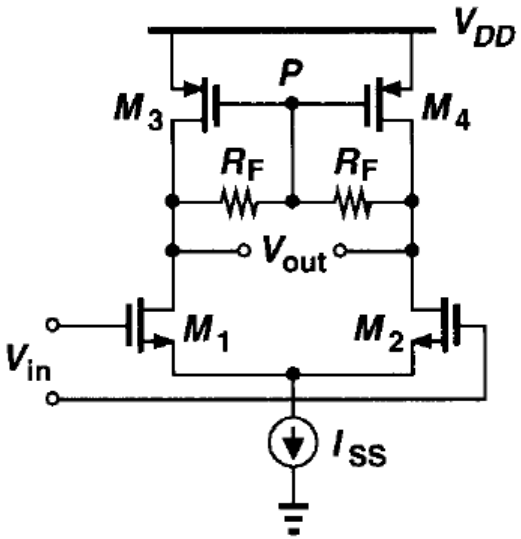


Figure 9.58 (b) resistive CMFB

图（b）对于共模信号，P点为电平确定的V_{OCM}，

$V_{OCM} = V_{DD} - |(V_{GS3} + V_{GS4})/2|$

M_3 and M_4 operate as diode-connected devices.

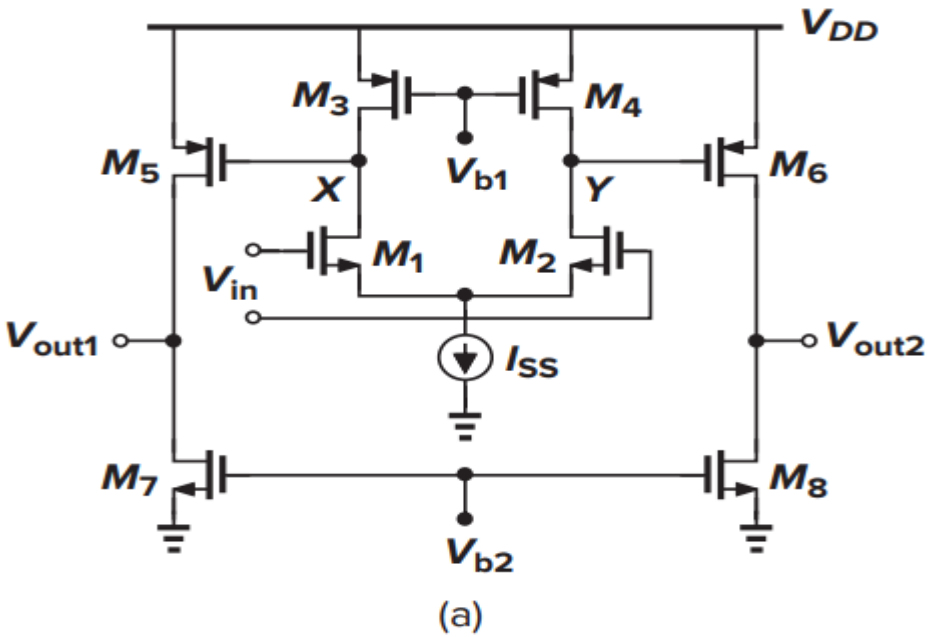
差动信号，**P为虚地**。增益为：$g_{m1,2}(r_{O1,2} \| r_{O3,4} \| R_F)$

单边最小输出$2V_{OD}$（前提V_{inCM} =？）；

最大输出：$V_{DD} - |V_{GS3}| + |V_{TH3}|$

9.7.4 两级运放中的共模反馈CMFB

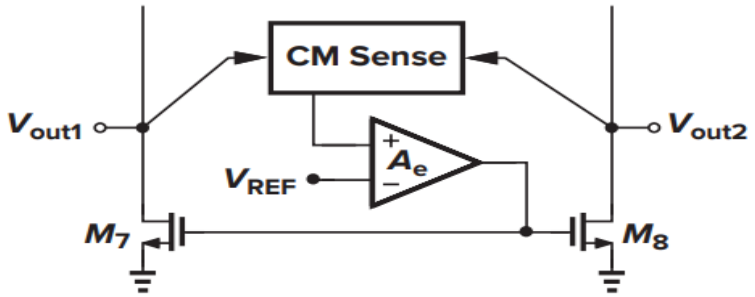
近似rail-to-rail output swings



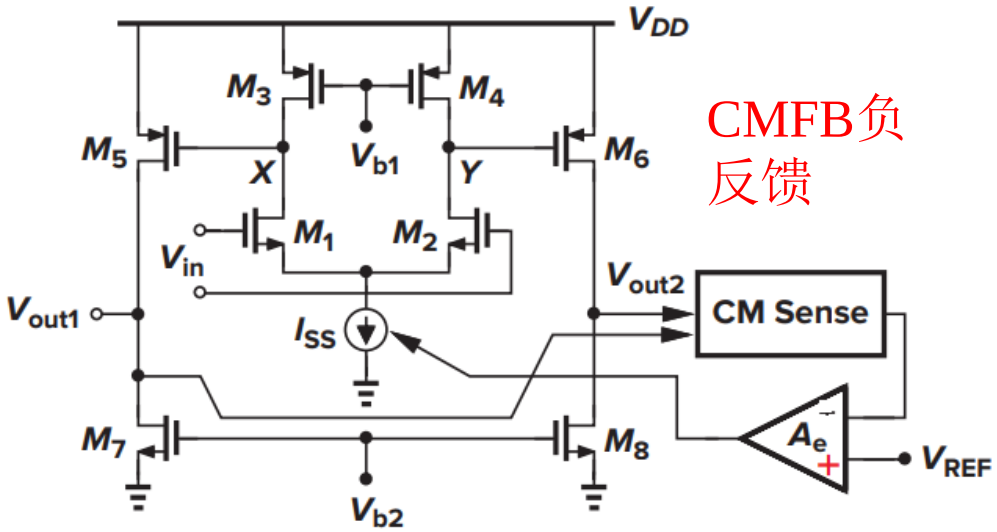
(a)

Figure 9.60 (a) Two-stage op amp, (b) CMFB around second stage, (c) CMFB from second stage to first stage.

图(b)对第一级输出X和Y电平没有进行反馈控制，不能保证全部MOS工作在饱和区，方法不可取



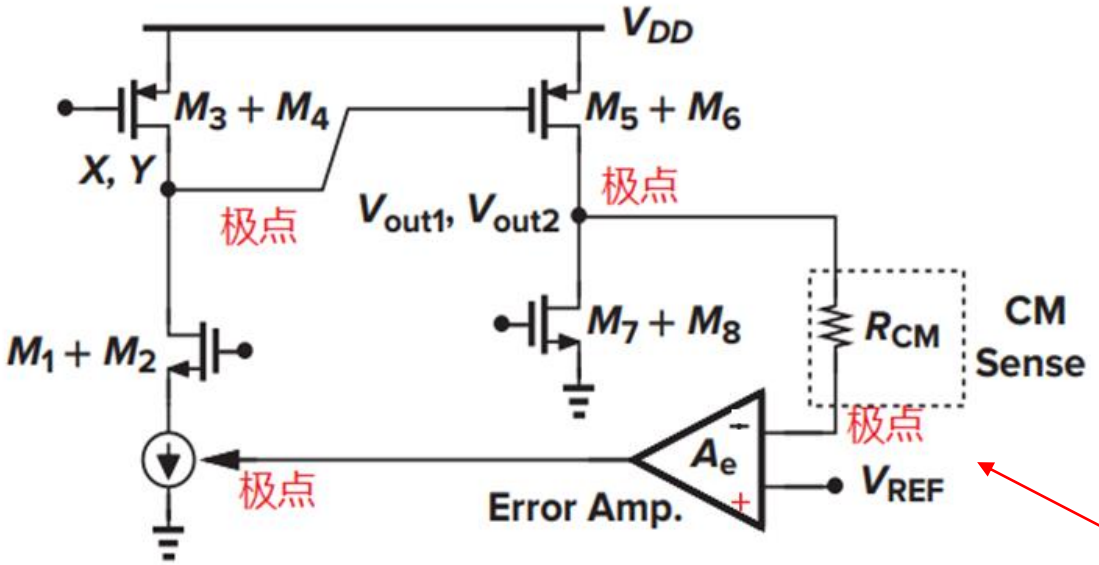
(b)



(c)

CMFB负反馈

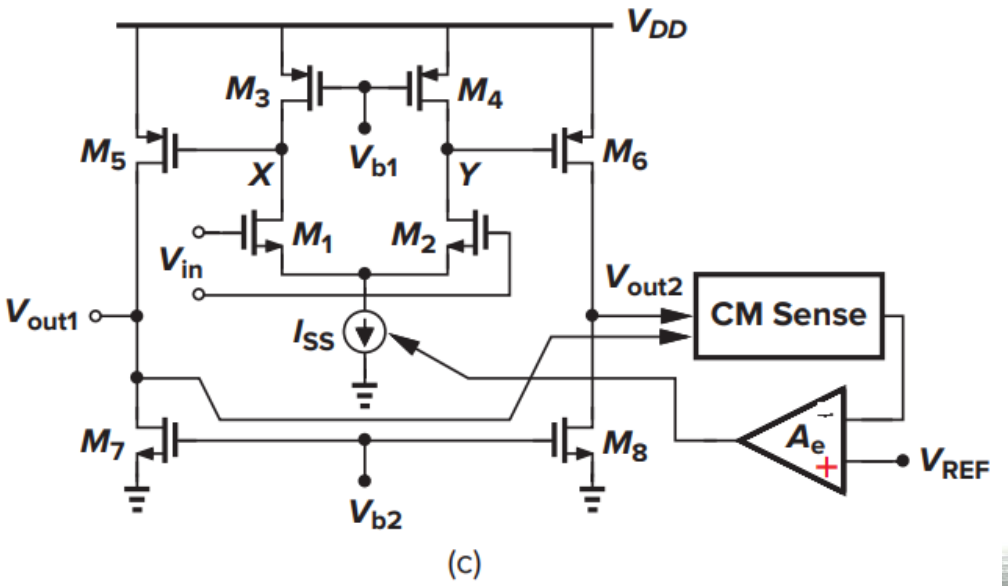
CMFB形成的多极点对系统稳定性不利



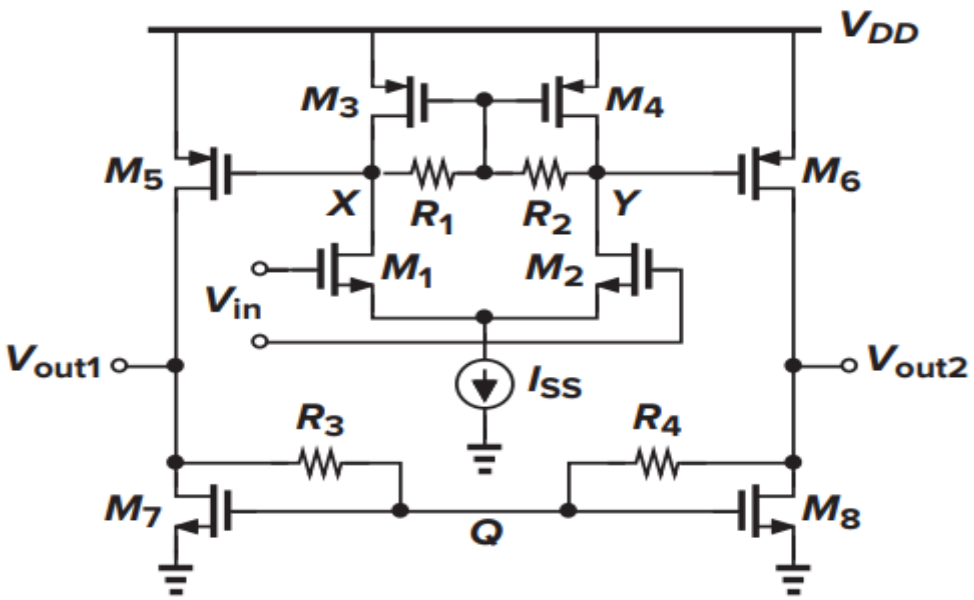
负反馈支路如有多极点，高频时可能会形成正反馈，引发自激振荡。

Figure 9.61 Equivalent CMFB loop to determine the number of poles

这里CM检测电路不能加C滤波



每级采用独立CMFB电路，避免多极点



M3和M5、M4 和M6是电流镜；

$V_Q = V_{outCM}$

电压增益：

$$A_V = g_{m1}(r_{O1} \| r_{O3} \| R_1) * g_{m5}(r_{O5} \| r_{O7} \| R_3)$$

output CM level is inevitably below $V_{DD}/2$, the output swings are limited

Figure 9.62 Simple CMFB loops around each stage.

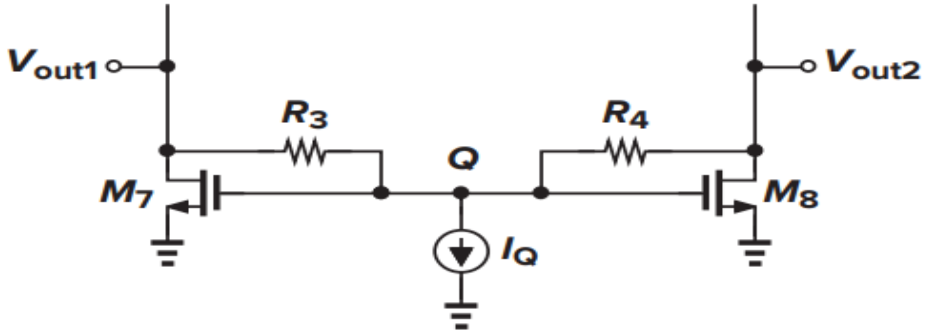
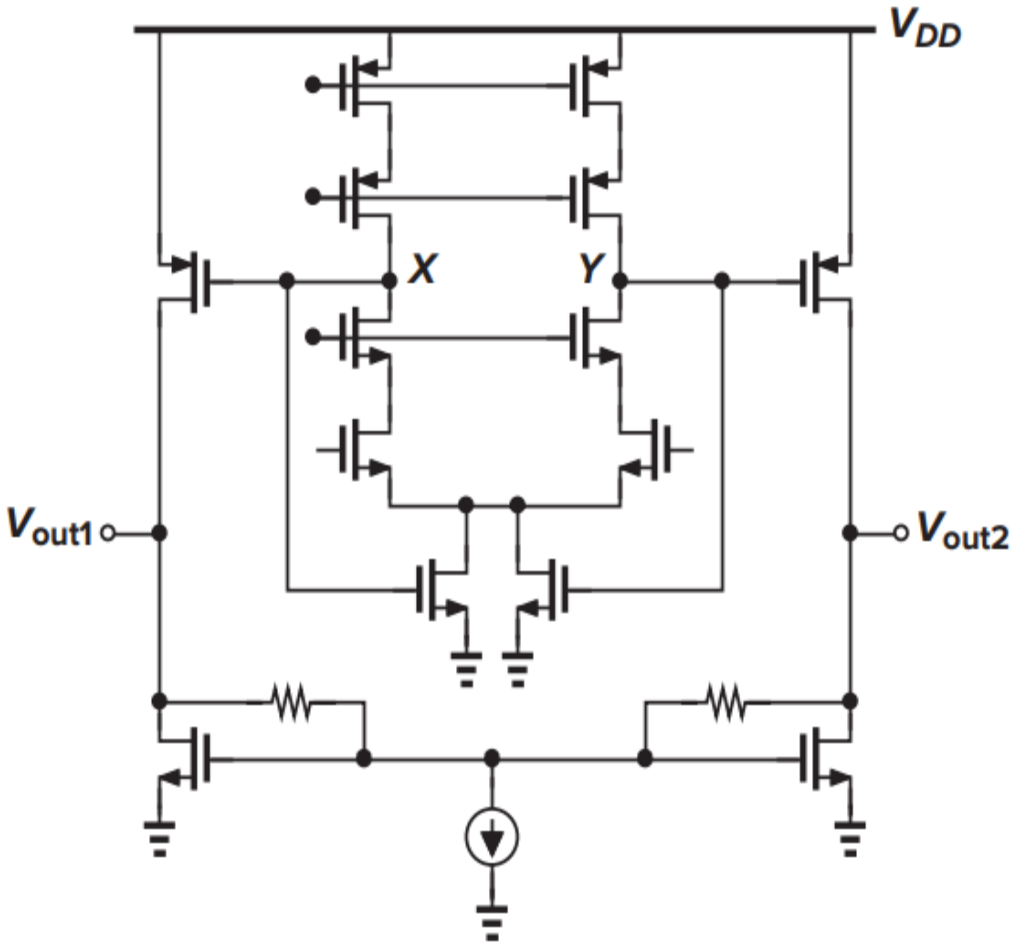


Figure 9.63 电路改进。

可使$V_{outCM} = V_{DD}/2$

且$V_{GS7,8} = V_Q$不高。

套筒式运放的CMFB



优点：
无需使用大电阻采样输出共模电压。

缺点：
尾电流源成为较小的线性区电阻，共模抑制较差。

Figure 9.64 CMFB loops around cascode and output stages

9.8 输入范围限制 input range limitations

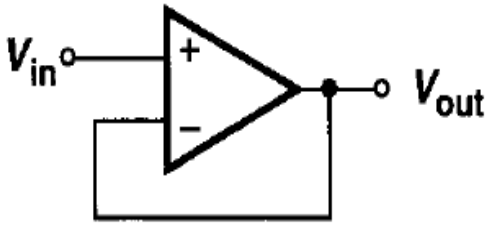
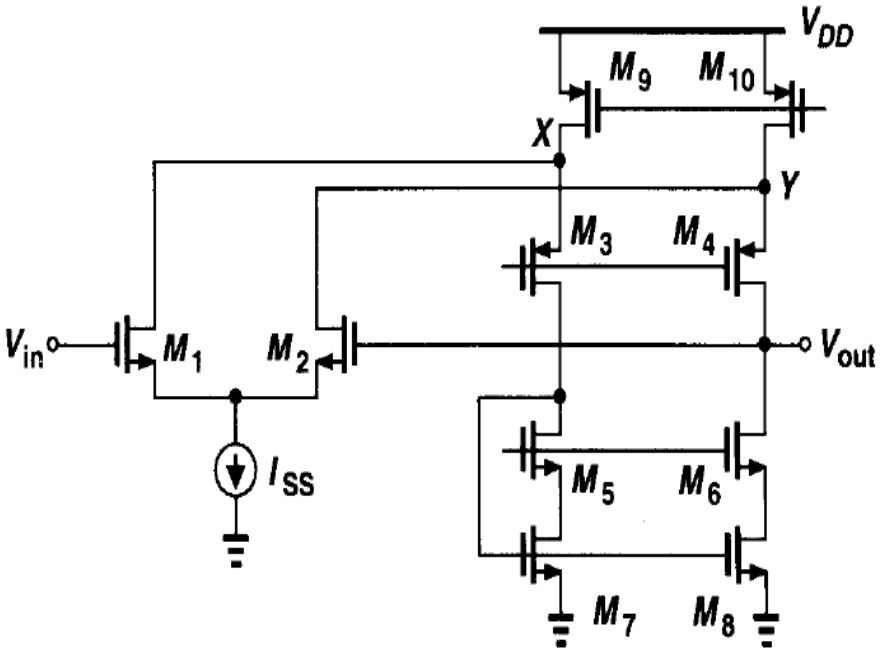


Figure 9.65 Unity-gain buffer

电压跟随器有最大带宽、最强驱动（输出阻抗小则负载能力强），最可能不稳定



电流镜单端输出

$V_{in,min} = V_{GS1,2} + V_{ISS} \approx V_{out,min} > V_{DS5,6} + V_{DS7,8}$

one threshold voltage higher than the allowable minimum provided by M_5+M_7

轨到轨输入运放的 输入CM range

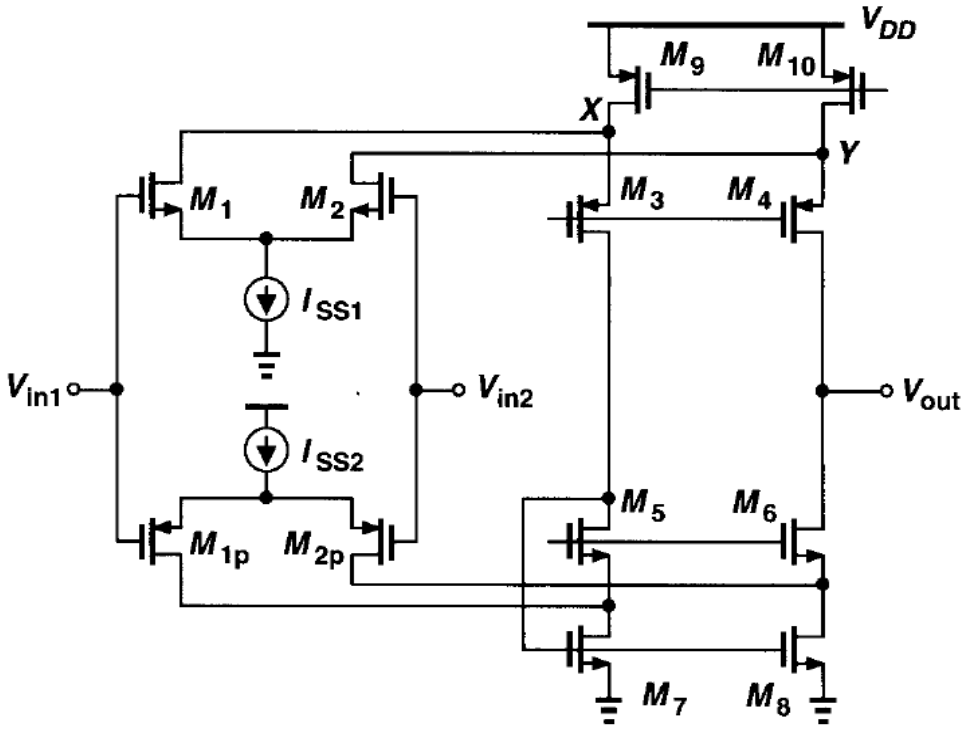


Figure 9.66 Extension of input CM range.

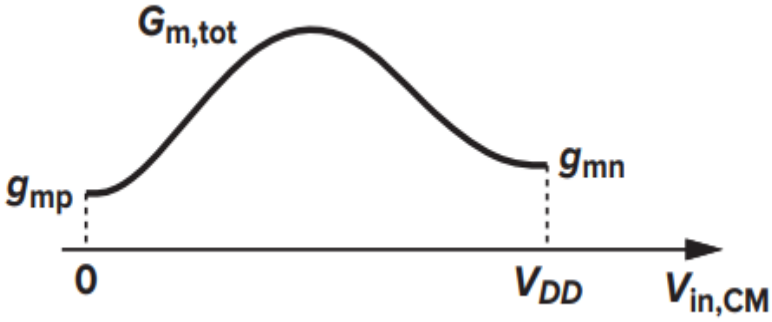


Figure 9.67 Variation of equivalent transconductance with the input CM level.

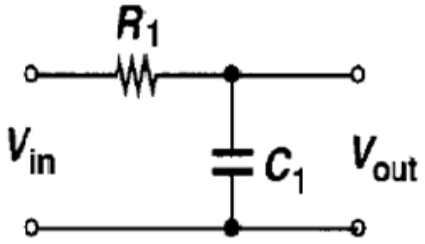
电流镜单端输出

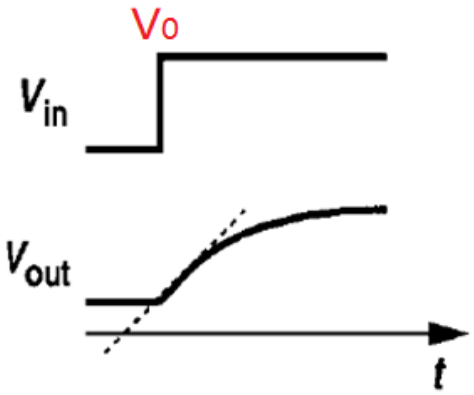
负反馈电路仅需要大的开环增益，只要环路增益足够大，闭环增益就与开环增益具体数值几乎无关。

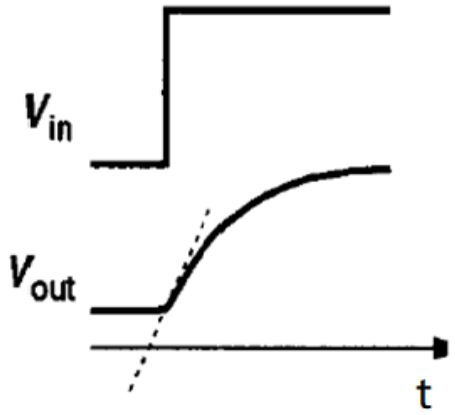
9.9 转换速率SR，大信号特性Tran仿真

SR： slew rate

转换速率与负载电容（包括反馈支路）有关。







$V_{out} = V_0[1-\exp(-t/\tau)]$

$\tau = RC$

$$\frac{dV_{out}}{dt} = \frac{V_0}{\tau}\exp\frac{-t}{\tau}.$$

t=0时，最大斜率称为压摆率

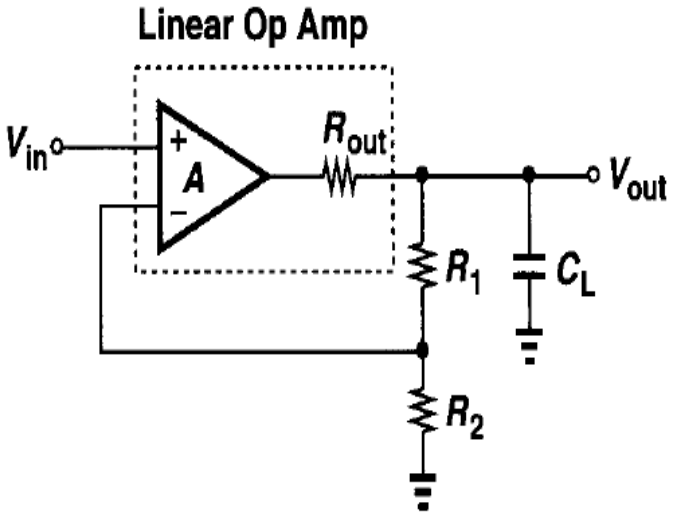
输出斜率应正比于输出（输入）幅度。

斜率上限（限制？）称为转换速率SR

若 $V_{out} = V_o \sin \omega t$, 则 $\left(\frac{dV_{out}}{dt}\right)_{t=0} = V_o\omega$

转换速率（与电路有关）可用来推算大信号带宽

Response of linear op amp to step input



$$\left[\left(V_{in} - V_{out}\frac{R_2}{R_1+R_2}\right)A - V_{out}\right]\frac{1}{R_{out}} = \frac{V_{out}}{R_1+R_2} + V_{out}C_L s$$

Assuming R1 + R2 >>Rout

$$\frac{V_{out}}{V_{in}}(s) \approx \frac{A}{\left(1+A\frac{R_2}{R_1+R_2}\right)\left[1+\frac{R_{out}C_L}{1+AR_2/(R_1+R_2)}s\right]}$$

如$R_1+R_2>>R_{out}$不满足，反馈支路有负载作用，修改A（反馈支路的加载）

$$V_{out} \approx V_0\frac{A}{1+A\frac{R_2}{R_1+R_2}}\left[1-\exp\frac{-t}{\frac{C_L R_{out}}{1+AR_2/(R_1+R_2)}}\right]u(t) \qquad (9.61)$$

V_o是输入阶跃幅度

Response of linear op amp to step input续

低频闭环增益：$A_{v,closed} = \dfrac{A}{1 + \dfrac{R_2}{R_1 + R_2} A}$

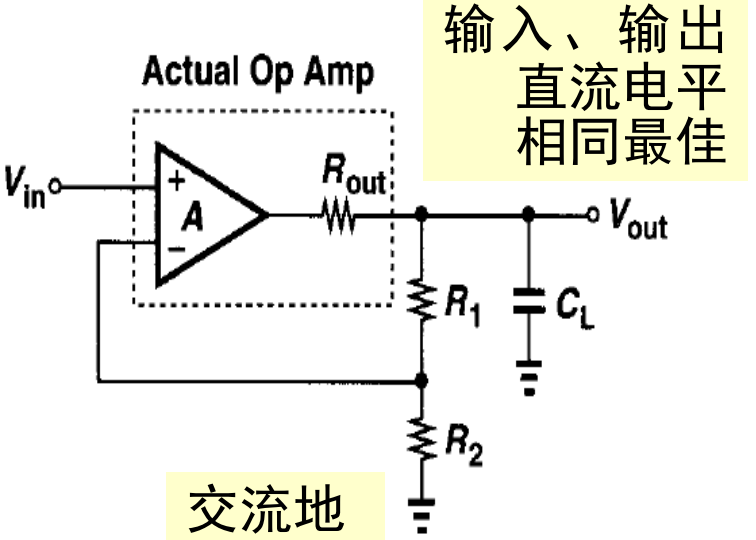
闭环时间常数：$\tau_{closed} = \dfrac{R_{out} C_L}{1 + \dfrac{R_2}{R_1 + R_2} A}$

闭环输出：$V_{out} = V_0 A_{v,closed} (1 - \exp \dfrac{-t}{\tau_{closed}})$

压摆率（可视为转换速率）：

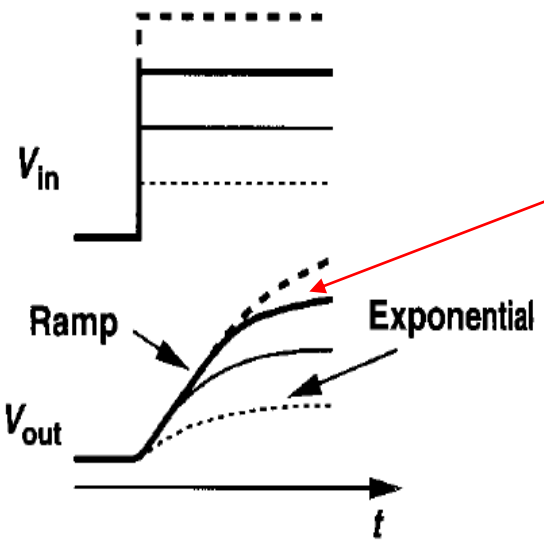
$$\left(\frac{dV_{out}}{dt} \right)_{t=0} = \frac{V_0 A_{v,closed}}{\tau_{closed}}$$

Response of linear op amp to step input (cont.)



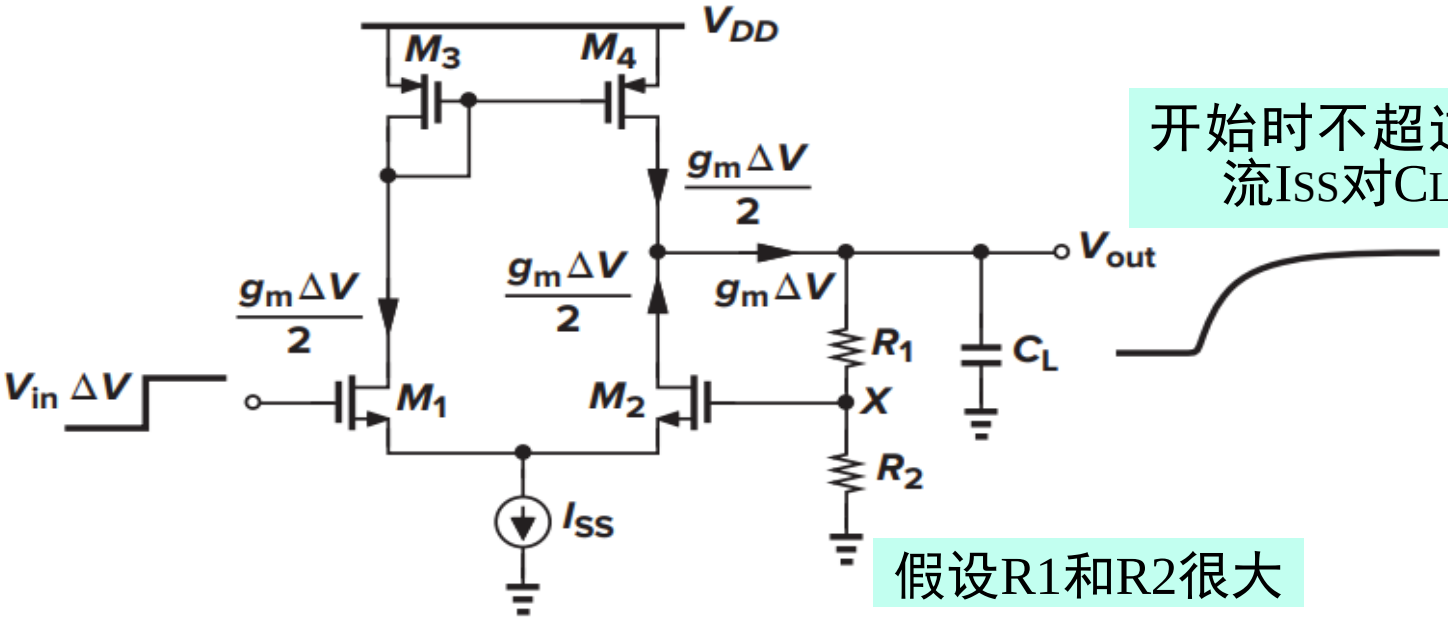
输入、输出直流电平相同最佳

交流地



大幅度阶跃输入时斜率不变

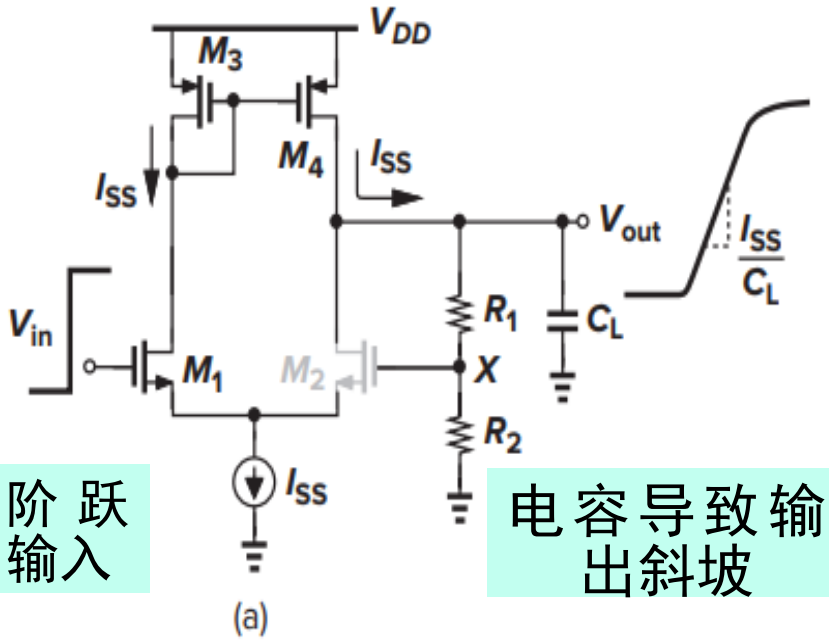
不同阶跃输入时，输出极限斜率称为**转换速率SR**



开始时不超过最大电流I_{SS}对C_L充电

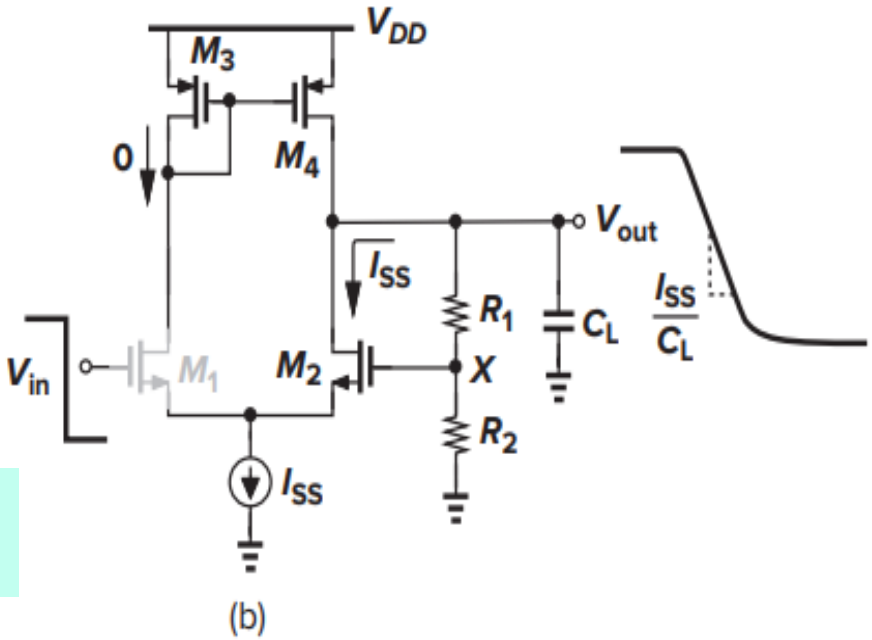
假设R1和R2很大

转换速率（SR）的起源



大 阶 跃 输入

电 容 导 致 输 出斜坡



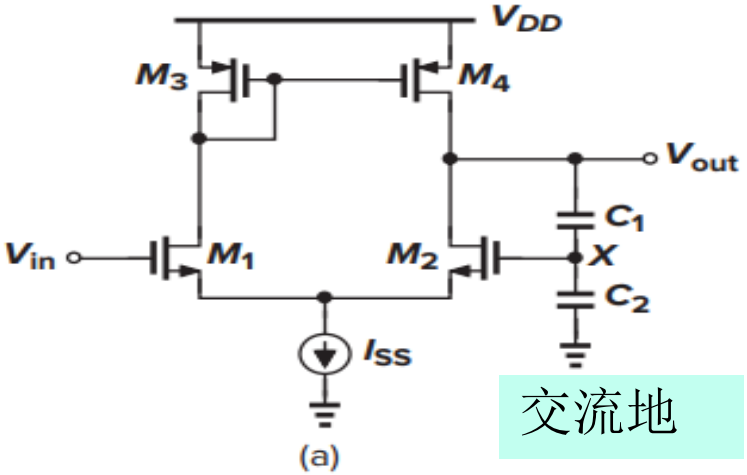
I_{SS}有限。输出最大充电斜率I_{SS}/C_L

转换速率表明，当输入高速大幅度信号时，输出信号存在失真(边沿变慢，表示大信号带宽变小)。

例 9.22 小信号阶跃响应和转换速率

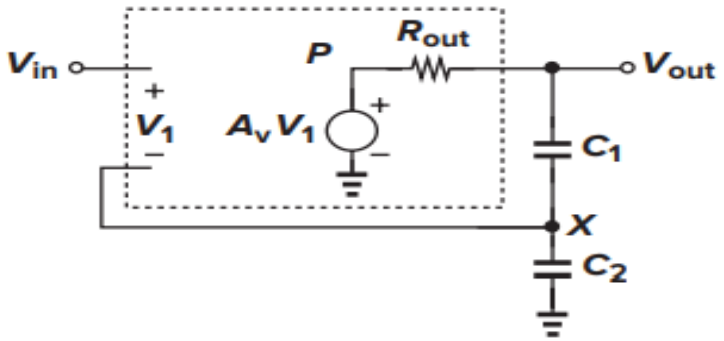
(a) Determine the small-signal step response of the circuit.

(b) Calculate the positive and negative slew rates



(a)

交流地



(b)

开环增益

$$A_v = g_{m1,2}(r_{O2} \| r_{O4})$$

开环输出阻抗：

$R_{out} = r_{O2} \| r_{O4}$

$$V_P = \left(V_{in} - \frac{C_1}{C_1 + C_2} V_{out} \right) A_v$$

转换速率与负载电容（包括反馈支路）有关。

Vout节点2支路电流相等

$$\left[\left(V_{in} - \frac{C_1}{C_1 + C_2} V_{out} \right) A_v - V_{out} \right] \frac{1}{R_{out}} = V_{out} \frac{C_1 C_2}{C_1 + C_2} s$$

例 9.22 小信号阶跃响应和转换速率(续)

重要参数：闭环输出幅度、时间常数

闭环增益

$$\frac{V_{out}}{V_{in}}(s) = \frac{A_v}{1 + A_v \dfrac{C_1}{C_1 + C_2} + \dfrac{C_1 C_2}{C_1 + C_2} R_{out} s}$$

$$= \frac{A_v / \left(1 + A_v \dfrac{C_1}{C_1 + C_2}\right)}{1 + \dfrac{C_1 C_2}{C_1 + C_2} R_{out} s / \left(1 + A_v \dfrac{C_1}{C_1 + C_2}\right)}$$

The response to a step of height V0 is given by

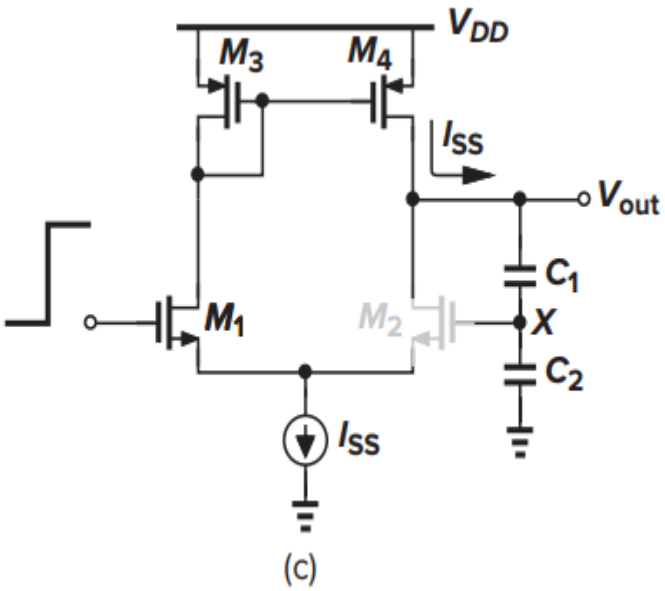
$$V_{out}(t) = \frac{A_v}{1 + A_v \dfrac{C_1}{C_1 + C_2}} V_0 \left(1 - \exp \frac{-t}{\tau}\right) u(t)$$

V_0是输入阶跃幅度。

V_0很大时，由于转换速率的限制，Vout不符合上式。

$$\tau = \frac{C_1 C_2}{C_1 + C_2} R_{out} / \left(1 + A_v \frac{C_1}{C_1 + C_2}\right)$$

例 9.22 小信号阶跃响应和转换速率(续)

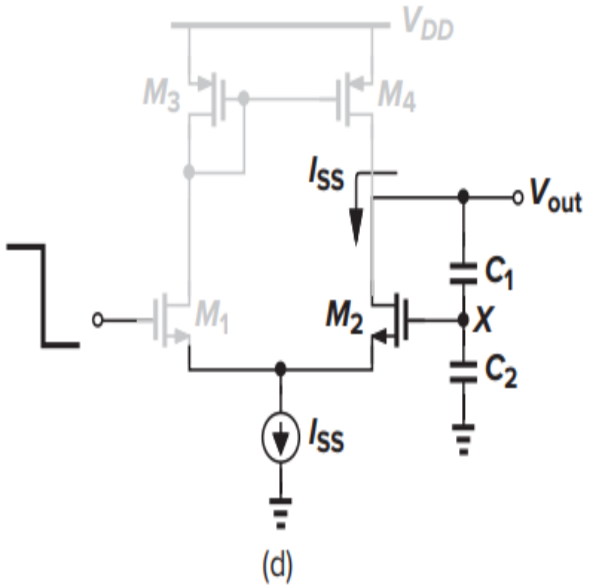


(c)

$$CdV = dQ = Idt$$

$$C = \frac{C_1 C_2}{C_1 + C_2}$$

初始Vout(0) = 0，
表示交变信号 = 0
实为CM直流电平



(d)

(c) 输出充电：
Vout(t)
= t * Iss/[C1C2/(C1 + C2)]
+ 初始CM电平

(d) 输出放电：
Vout (t)
= −t * Iss/[C1C2/(C1 + C2)]
+ 初始CM电平

Slew rate of telescopic(套筒) op

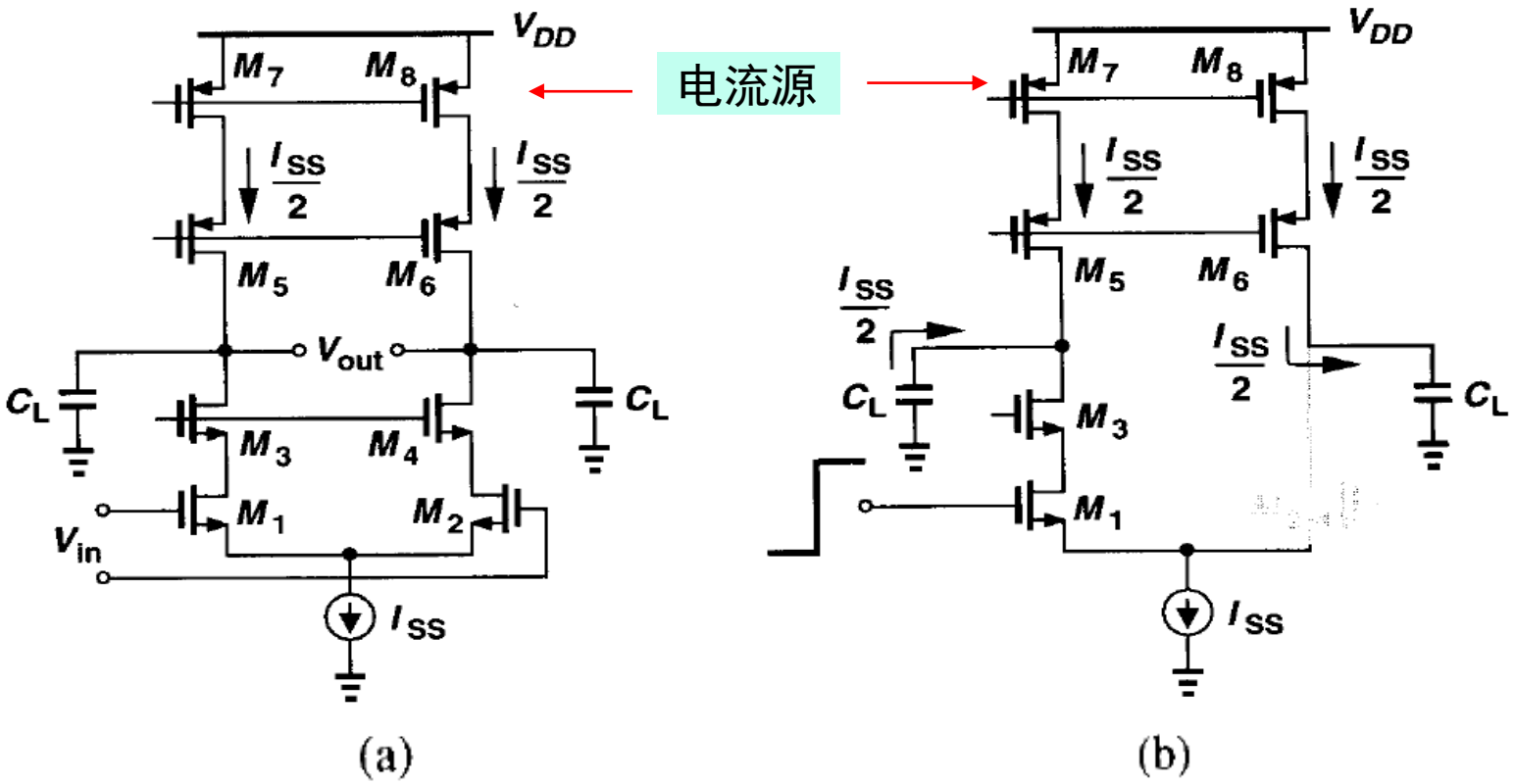


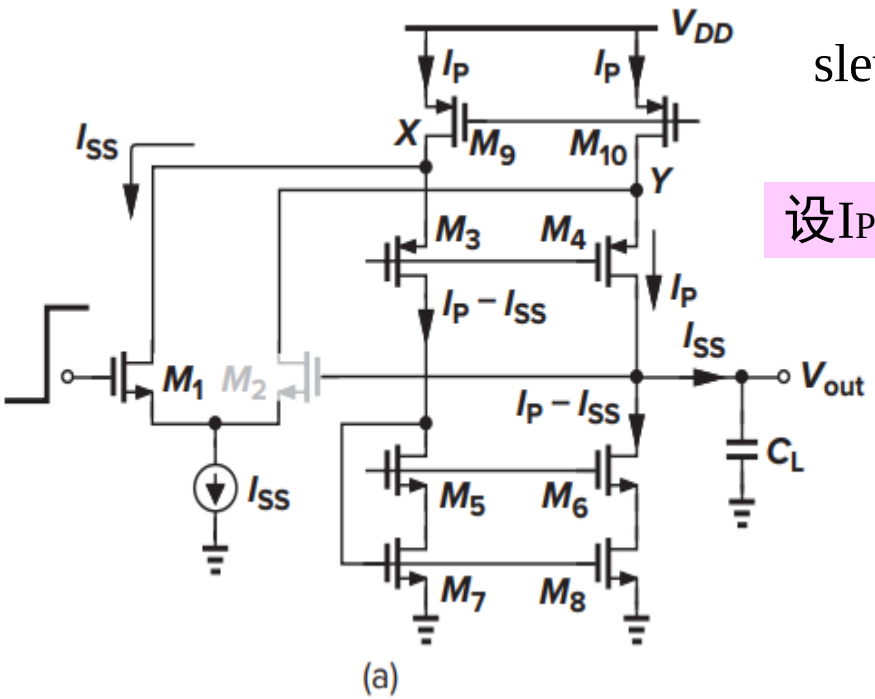
Figure 9.74 Slewing in telescopic op amp

单边输出转换速率：

$$\left.\frac{dV_{out1}}{dt}\right|_{t=0} = \frac{I_{SS}}{2C_L}$$

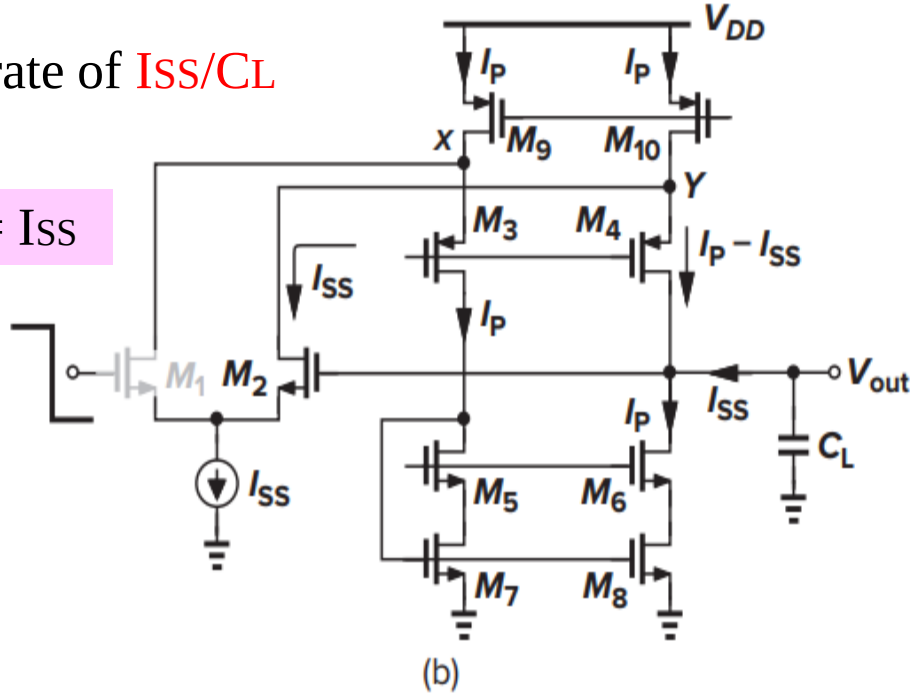
差分输出加倍。

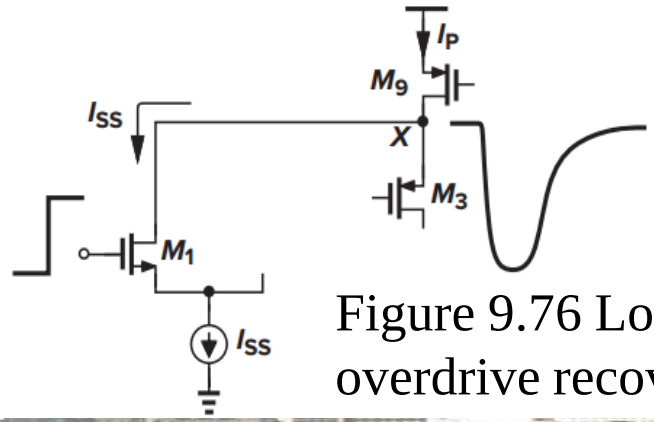
Slew rate of folded-cascode op



slew rate of ISS/CL

设IP >= ISS





若$I_{SS}/2 < I_P < I_{SS}$

注入输出电容的电流：
$I_{CL} = I_{D4} - I_{D6}$

因此实际电路选取：$I_P = I_{SS}$。
即4支路电流相同

Figure 9.76 Long settling due to overdrive recovery after slewing

9.10 电源抑制 Power Supply Rejection

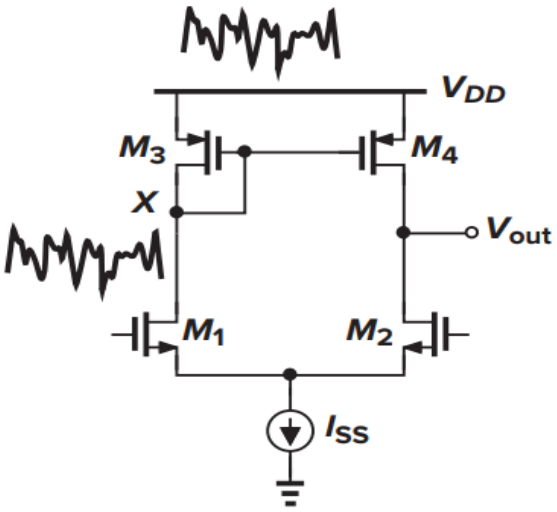


Figure 9.81

Power supply rejection ratio:

PSRR = |信号增益 / 电源到输出的增益|

电源噪声（共模，差分输入dVin=0即直流）
电源噪声到输出Vout的增益约为1

图9.81中，
V_{DD}噪声通过 $1/(2g_{m3})$与$2g_{m2}*r_{o2}*r_{oss}$分压得到Vout噪声， 电源到输出的噪声增益=1 。

低频增益: $|A_v| = g_{m2}(r_{O2} \| r_{O4})$

= PSRR 电源抑制比

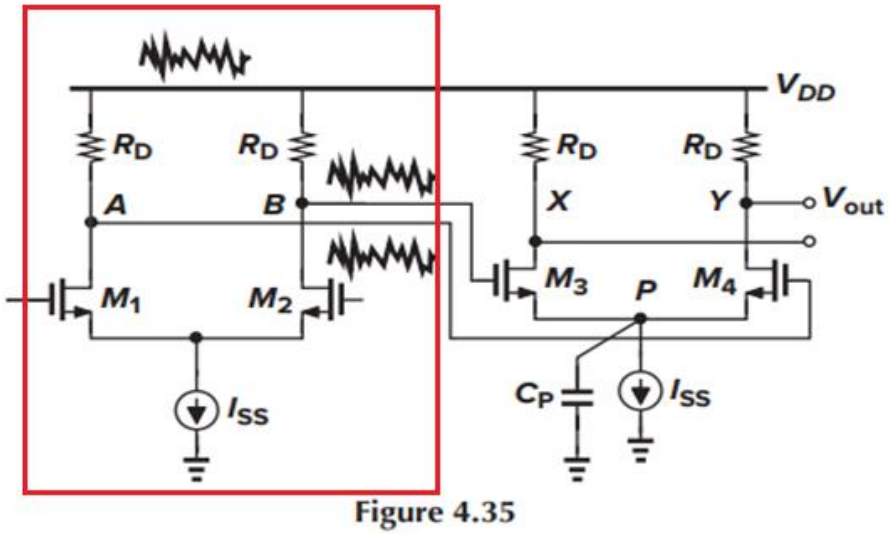


Figure 4.35

图4.35全差动电路中，
V_{DD}噪声通过 R_D与$g_{m2}*r_{o2}*r_{oss}$分压得到第一级的差动输出噪声，电源到输出的噪声增益=1 。

第一级低频增益$A_v = g_{m2} R_D$ = PSRR

例 9.25：闭环电路低频PSRR

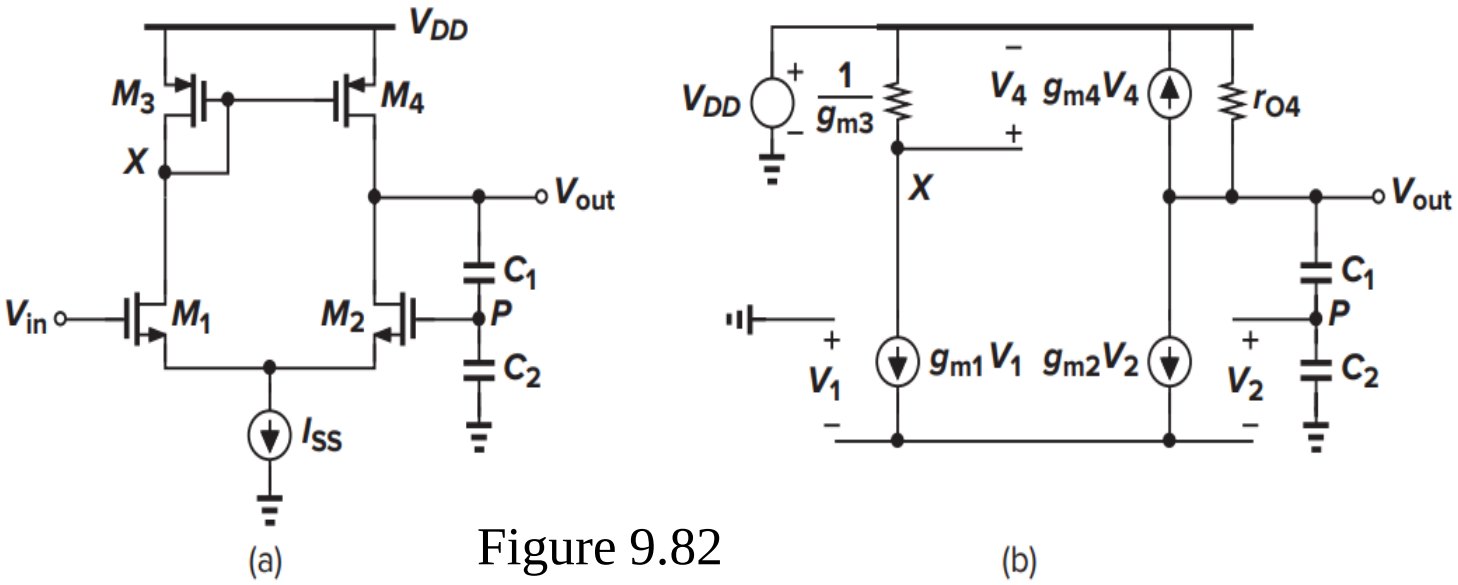


Figure 9.82

V_{out}通过r_{O4}引入V_{DD}噪声

电源噪声是共模

信号增益 = 1+C2/C1

$V_1 = V_{GS1}$，$V_2 = V_{GS2}$

思路：求解V_{out}节点总电流 = 0

$V_P - V_2 = -V_1$ → $V_{out}\dfrac{C_1}{C_1+C_2} - V_2 = -V_1$

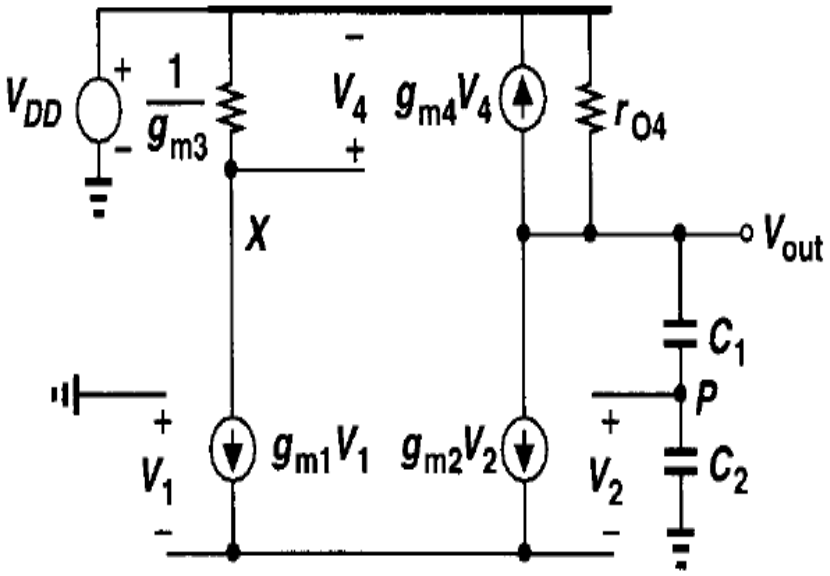
$g_{m1}V_1 + g_{m2}V_2 = 0$ → $V_1 = -V_2$

$$V_2 = \frac{V_{out}}{2}\frac{C_1}{C_1+C_2}.$$

例 9.25：闭环电路低频PSRR (cont.)

低频，忽略C上电流

$$-\frac{g_{m1}V_1}{g_{m3}}g_{m4}-\frac{V_{DD}-V_{out}}{r_{O4}}+g_{m2}V_2=0$$



r_{o2}有何影响？Vout向下看阻抗很大。

得到：

$$\frac{V_{out}}{V_{DD}}=\frac{1}{g_{m2}r_{O4}\dfrac{C_1}{C_1+C_2}+1}$$

Vout上噪声变小

$$PSRR=\frac{\text{信号增益}}{\text{电源到输出增益}}=\left(1+\frac{C_2}{C_1}\right)\left(g_{m2}r_{o4}\frac{C_1}{C_1+C_2}+1\right)$$

$$\approx g_{m2}r_{o4}\quad \text{稍增大}$$

本章知识要点

- 运算放大器的主要性能指标；
- 很大的放大器开环增益使得负反馈运放的两个输入端虚短、闭环运放增益精度较高；
- 一般采用Cascode放大器为运放高增益第一级；电流源负载需要共模反馈电路确定输出直流电平；但是对于电流源负载的差分输出级，若在应用时外加负反馈支路组成运算电路，则可利用该负反馈支路自动确定工作点，这时可能不需要CMFB电路；
- CMFB电路用瞬时电压极性法确认负反馈；
- 运放输出级需要大的电压动态范围和负载驱动（电流）能力；
- 设计非低噪放电路时，根据应用需求确定电路的输出转换速率（最大压摆率），进而确定尾电流源的电流；合理确定MOS的过驱动电压和工作点偏置电压，得到各MOS管宽长比，验证低频增益，调整宽长比。
- 运算放大器一般工作在负反馈状态；使用中若需要在输入端引入正反馈，则必须小于引入的负反馈，否则会发生自激振荡。