Timing Analysis: **Name:** **Student ID:**

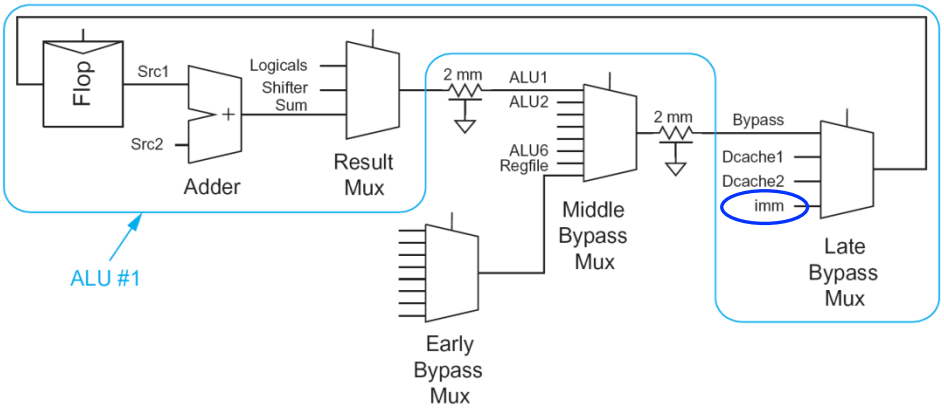

Figure 1 Itanium 2 ALU self-bypass path

The Integer Execution Unit of the Itanium 2 contains self-bypass paths for **six separate ALUs (Arithmetic Logic Unit), as shown in Figure 1. The path for one of the ALUs begins at registers (flip-flops) containing the inputs to an adder, as shown in the above figure.** The adder must compute the sum (or difference, for subtraction). A *result multiplexer* chooses between this **sum**, the output of the **logic** unit, and the output of the **shifter**. Then a series of *bypass multiplexers* selects the inputs to the ALU for the next cycle. The early bypass multiplexer chooses among results of ALUs from previous cycles and is not on the critical path. The 8:1 middle bypass multiplexer chooses a result from any of the **six ALUs**, **the early bypass mux**, or **the register** file. The 4:1 late bypass multiplexer chooses a result from **either of two results returning from the data cache**, the **middle bypass mux result**, or the **immediate operand from a register**. The late bypass mux output is driven back to the ALU to use on the next cycle. Because the six ALUs and the bypass multiplexers occupy a significant amount of area, the critical path also involves 2 mm wires from the result mux to middle bypass mux and from the middle bypass mux back to the late bypass mux.

For our example, the propagation delays and contamination delays of the path are given in the following Table. Suppose the **registers** are built from flip-flops with a **setup time of 50 ps**, **hold time of –7 ps**, **propagation delay of 70 ps**, and **contamination delay of 60 ps**, and the **55 ps clock skew** between flip-flops in the various ALUs.

Table 1 Combinational logic delays

Element	Propagation Delay	Contamination Delay
Adder	590 ps	100 ps
Result Mux	60 ps	35 ps
Early Bypass Mux	110 ps	95 ps
Middle Bypass Mux	80ps	55 ps
Late Bypass Mux	60ps	45 ps
2-mm Wire	100 ps	70ps

(1) What is the **minimum cycle time** at which the ALU self-bypass path will operate correctly?
(2) In the ALU self-bypass example with flip-flops from Figure 1, the earliest input to the late bypass multiplexer is the ***imm*** value coming from another flip-flop. Will this path experience any hold-time failures?
(3) How much **clock skew** can the system have before **hold-time** failures occurs?