# Exercise

1. Setup EDA Environment

   **% setdt vcs**
   **% setdt syn**

2. Simulating the behavioral description and RTL description of the GCD.

a) Copy the file **/js1/songch/DA_VLSI/DA_VLSI_Lab2.tgz** to your home directory.
b) Extract the files % **tar zxvf DA_VLSI_Lab2.tgz,** and enter **gcd** directory.
c) Build a simulator and simulate the **behavioral description** of Greatest Common Divisor (GCD).
   **% vcs -PP +lint=all +v2k -debug -line gcd_behavioral.v**
   **% ./simv**
   **Tips**: You can use the command '**./simv +a-in=72 +b-in=81**' to change the input integers.
d) Finish the **module definitions** for the registers in the RTL description of GCD. (Please refer to the verilog-basics-2 for the description of registers)
   1) **vcEDFF_pf** : a register with enable signal
   2) **vcRDFF_pf** : a register with reset signal
   3) **vcMux3** : a 3-to-1 multiplexer ( selection signals prefix is "A_SEL_", macro defined )
   4) **vcMux2** : a 2-to-1 multiplexer ( selection signals prefix is "B_SEL_", macro defined )
e) Build a simulator and simulate the RTL description of Greatest Common Divisor (GCD).

3. Blocking , non-blocking assignments comparison

a) Enter the directory **block**.
b) Read the source file **block.v , non-block.v , block_test.v** .
c) The file **block.v** described a module functioned "adding input signal value 2 in 2 clock cycles".
d) Simulate the test module, and find why module **block** and module **non-block** functioned inconsistently. **#tip:**If you cannot distinguish blocking and non-blocking assignments clearly, you'd better read the attachment **Verilog-Basics-2 in Lecture 3** linked from course homepages.
e) Modify the module **block** to make them function like **non-block** version module.
f) Re-simulate the test module, and observe their waveforms.

Please refer to **http://staff.ustc.edu.cn/~songch/da-ug.htm** for the following resources

1. Verilog-basics-2 in Lecture 3 Slides for the Verilog HDL.

**2. Documents for Design Compiler: http://202.38.80.152/dc_doc/tcoug.pdf (Synopsys Timing Constraints and Optimization User Guide)**

Please read the error information carefully if any.