A Ka-Band Low Phase Error CMOS VGA Using Current Steering Topology with Switched Capacitor

***Abstract*—A current steering variable gain amplifier (VGA) with switched-capacitor phase error compensation technique is presented in this paper. The principle of the proposed phase error compensation technique is analyzed and illustrated. A Ka-band 16-dB-tuning-range VGA using this technique is designed and verified in 65 nm CMOS technology. The post-layout simulation results show the phase error is less than 1.4° and the gain error is less than 0.18 dB with the peak gain of 7.3 dB over a wide frequency band of 32.5 GHz - 39 GHz. The VGA consumes 13 mW power from 1.2 V voltage. The chip area is 0.098 mm^2 excluding input/output pads.**

***Index Terms*—millimeter-wave, phased arrays, CMOS, VGA, current steering topology, phase error.**

I. Introduction

As the demand for high-data-rate communication booms, the phased-array technique in mm-wave wireless systems has become widely researched which achieves side lobe suppression and signal-to-noise ratio optimization [1]. Variable gain amplifier (VGA) is a key component of phased-arrays to realize gain controlling while compensating the loss caused by the phase shifter [2]. The VGA is supposed to be accurate in gain controlling and fine enough in gain compensating. Moreover, to avoid further calibration, the phase error of VGA is supposed to be minimized to maintain the beam point direction in a phased-array system [3].

Various VGA topologies have been reported these years while the current steering topology stands out for its stable input impedance as a result of the constantly biased common source stage. To further reduce the phase error, improvements have been proposed in [4]-[7]. One effective way is to replicate the topology into a topology with reversed phase to cancel the phase error together with the original topology which would enlarge the chip size and power consumption. Another method is bias-adjusting which requires relatively large area due to the essential digital-to-analog converters.

In this paper, a CMOS current steering VGA with switched capacitor is demonstrated to realize a wide gain control range of 16 dB with maximum 1.4° phase error and maximum 0.18 dB gain error across 32.5 GHz - 39 GHz on the 65 nm CMOS process.

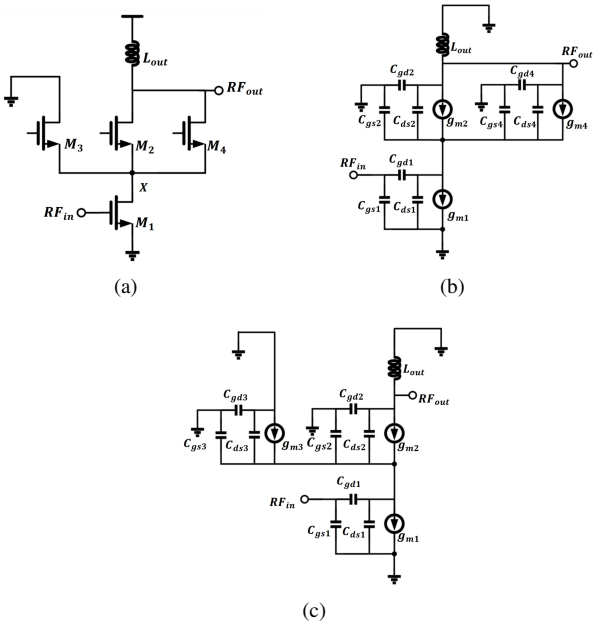

Fig. 1. Schematic of the conventional current steering VGA (a) and its small signal equivalent circuit in high gain mode (b) and low gain mode (c).

This paper is organized as follows. Section II analyzes the phase errors of the conventional current steering topology and the proposed current steering topology with switched capacitor to demonstrate the validity of the proposed topology. Section III shows the simulated results. Section IV draws the conclusion.

II. Phase Errors of Both Topologies

Fig. 1 shows the schematic of the current steering VGA topology (a) and its small signal equivalent circuit in the

$$H(s)_{wo/C_s,+} = \frac{(sC_{gd1}-g_{m1})\cdot[s(C_{ds2}+C_{ds4})+g_{m2}+g_{m4}]}{s\cdot\{s[(C_{gs2}+C_{gs4}+C_{ds1}+C_{gd1})\cdot(C_{gd2}+C_{gd4}+C_{ds2}+C_{ds4})+(C_{ds2}+C_{ds4})\cdot(C_{gd2}+C_{gd4})]+(g_{m2}+g_{m4})\cdot(C_{gd2}+C_{gd4})\}} \quad (1)$$

$$H(s)_{wo/C_s,-} = \frac{(sC_{gd1}-g_{m1})\cdot[sC_{ds2}+g_{m2}]}{s\cdot\{s[(C_{ds3}+C_{gs2}+C_{gs3}+C_{ds1}+C_{gd1})\cdot(C_{gd2}+C_{ds2})+C_{gd2}\cdot C_{ds2}]+g_{m2}\cdot C_{gd2}+g_{m3}\cdot(C_{gd2}+C_{ds2})\}} \quad (2)$$

$$H(s)_{w/C_s,+} = \frac{(sC_{gd1}-g_{m1})\cdot[s(C_{ds2}+C_{ds4})+g_{m2}+g_{m4}]}{s\cdot\{s[(C_{gs2}+C_{gs4}+C_{ds1}+C_{gd1})\cdot(C_{gd2}+C_{gd4}+C_{ds2}+C_{ds4})+(C_{ds2}+C_{ds4})\cdot(C_{gd2}+C_{gd4})]+(g_{m2}+g_{m4})\cdot(C_{gd2}+C_{gd4})\}} \quad (3)$$

$$H(s)_{w/C_s,-} = \frac{(sC_{gd1}-g_{m1})\cdot[sC_{ds2}+g_{m2}]}{s\cdot\{s[(C_{gs2}+C_{gs3\_T}+C_{ds1}+C_{gd1})+\frac{(sC_{ds3\_T}+g_{ds3})\cdot(sC_{gd3\_T}+sC_c)}{(sC_{ds3\_T}+g_{ds3})+(sC_{gd3\_T}+sC_c)}]\cdot(C_{gd2}+C_{ds2})+(sC_{ds2}+g_{m2})\cdot C_{gd2}\}} \quad (4)$$

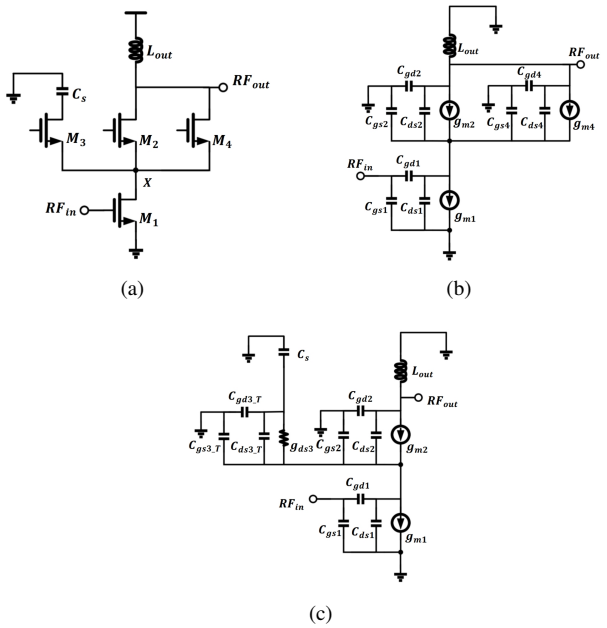

Fig. 2. Schematic of the proposed VGA (a) and its small signal equivalent circuit in high gain mode (b) and low gain mode (c).

high gain mode (b) and the low gain mode (c). The current steering VGA is consisted of a one-stage cascode amplifier composed by M_1, M_2 and a bleeding transistor M_3 as a gain-lowering path and a replicating transistor M_4 as an auxiliary path. The size of M_4 is configured to be equaled to that of M_3 to introduce same parasitic capacitors to the node X. Thus, at node X, the capacitance stays relatively constant under different gain modes [8].

Fig. 2 shows the schematic of the proposed current steering VGA with switched capacitor (a) and its small signal equivalent circuit in the high gain mode (b) and the low gain mode (c). The current steering VGA with switched capacitor is consisted of a cascode amplifier composed by M_1, M_2 and a switched capacitor C_s as a gain-lowering path together with M_3 and a replicating transistor M_4 as an auxiliary path.

It is worth noting that in the proposed topology, M_3 is working in the triode region as C_s blocks the DC current from drain to source while other transistors still in the saturation region. Therefore, as M_3 shifts from the saturation region to the triode region, the relating parasitic capacitance of the transistor would change.

The transfer functions under both modes of different topologies are written as (1)-(4) at the bottom of last page supposing L_{out} to be infinity for convenience. C_{gs}, C_{gd}, C_{ds} refer to the gate-source, gate-drain and drain-source parasitic capacitance of the transistor, respectively. C_{gs_T}, C_{gd_T}, C_{ds_T} refer to the gate-source, gate-drain and drain-source parasitic capacitance of the transistor in the triode region, respectively. g_m refers to the transconductance of the transistor. g_{ds} refers to the small signal admittance of the transistor in the triode region whose value equals to g_m of the transistor in the saturation region.

The transfer function of the proposed topology is the same as that of the conventional current steering topology in the high gain mode since the branch of M_3 could be omitted in the high gain mode.

From the transfer functions, the insertion phases of all modes could be derived as (5)-(8) at the bottom of this page. The phase of the proposed topology in the low gain mode is hard to be written as an expression because C_s introduces a new pair of zero and pole. Nevertheless, (5)-(8) share the same structure as:

$$\angle H(\omega) = \theta_1 + \theta_2 - \theta_3 - \theta_4 \tag{9}$$

The parasitic capacitance and the transconductance of a constantly biased transistor are both proportion to the size of the transistor for the first order. Therefore, the ratio of them would be constant. Thus, it could be derived that $\frac{C_{ds2}+C_{ds4}}{g_{m2}+g_{m4}}$ equals to $\frac{C_{ds2}}{g_{m2}}$. Then the focus is concentrated on θ_4 in different modes since θ_1, θ_2, θ_3 in (5)-(8) are unchanged respectively.

$$\begin{aligned}\angle H(\omega)_{wo/C_s,+} = \quad & \pi + \arctan(-\tfrac{\omega C_{gd1}}{g_{m1}}) + \arctan(\tfrac{\omega(C_{ds2}+C_{ds4})}{g_{m2}+g_{m4}}) - \tfrac{\pi}{2} \\ & -\arctan(\omega \tfrac{(C_{gs2}+C_{gs4}+C_{ds1}+C_{gd1})\cdot(C_{gd2}+C_{gd4}+C_{ds2}+C_{ds4})+(C_{ds2}+C_{ds4})\cdot(C_{gd2}+C_{gd4})}{(g_{m2}+g_{m4})\cdot(C_{gd2}+C_{gd4})})\end{aligned} \tag{5}$$

$$\begin{aligned}\angle H(\omega)_{wo/C_s,-} = \quad & \pi + \arctan(-\tfrac{\omega C_{gd1}}{g_{m1}}) + \arctan(\tfrac{\omega C_{ds2}}{g_{m2}}) - \tfrac{\pi}{2} \\ & -\arctan(\omega \tfrac{(C_{ds3}+C_{gs2}+C_{gs3}+C_{ds1}+C_{gd1})\cdot(C_{gd2}+C_{ds2})+C_{gd2}\cdot C_{ds2}}{g_{m2}\cdot C_{gd2}+g_{m3}\cdot(C_{gd2}+C_{ds2})})\end{aligned} \tag{6}$$

$$\begin{aligned}\angle H(\omega)_{w/C_s,+} = \quad & \pi + \arctan(-\tfrac{\omega C_{gd1}}{g_{m1}}) + \arctan(\tfrac{\omega(C_{ds2}+C_{ds4})}{g_{m2}+g_{m4}}) - \tfrac{\pi}{2} \\ & -\arctan(\omega \tfrac{(C_{gs2}+C_{gs4}+C_{ds1}+C_{gd1})\cdot(C_{gd2}+C_{gd4}+C_{ds2}+C_{ds4})+(C_{ds2}+C_{ds4})\cdot(C_{gd2}+C_{gd4})}{(g_{m2}+g_{m4})\cdot(C_{gd2}+C_{gd4})})\end{aligned} \tag{7}$$

$$\angle H(\omega)_{w/C_s,-} = \quad \pi + \arctan(-\tfrac{\omega C_{gd1}}{g_{m1}}) + \arctan(\tfrac{\omega C_{ds2}}{g_{m2}}) - \tfrac{\pi}{2} - \theta_{4,w/C_s,-} \tag{8}$$

$$\theta_{4,w/C_s,-}|_{C_s\to 0} = \arctan(\omega \tfrac{(C_{gs2}+C_{gs3\_T}+C_{gd3\_T}+C_{ds1}+C_{gd1})\cdot(C_{gd2}+C_{ds2})+C_{gd2}\cdot C_{ds2}}{g_{m2}\cdot C_{gd2}}) + \gamma \tag{10}$$

$$\theta_{4,w/C_s,-}|_{C_s\to \infty} = \arctan(\omega \tfrac{(C_{ds3\_T}+C_{gs2}+C_{gs3\_T}+C_{ds1}+C_{gd1})\cdot(C_{gd2}+C_{ds2})+C_{gd2}\cdot C_{ds2}}{g_{m2}\cdot C_{gd2}+g_{ds3}\cdot(C_{gd2}+C_{ds2})}) \tag{11}$$

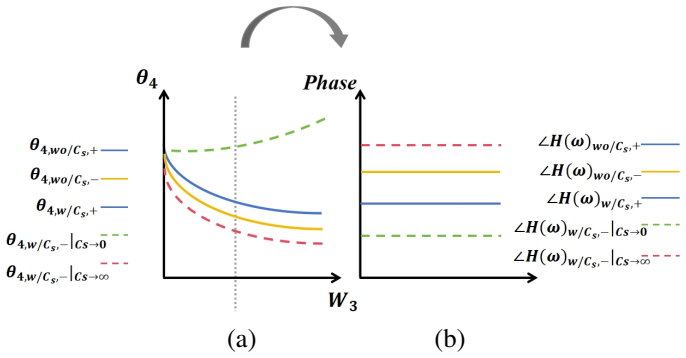

Fig. 3. Sketch of θ_4 on W_3 under different modes (a) and phases of different modes under certain W_3 (b).

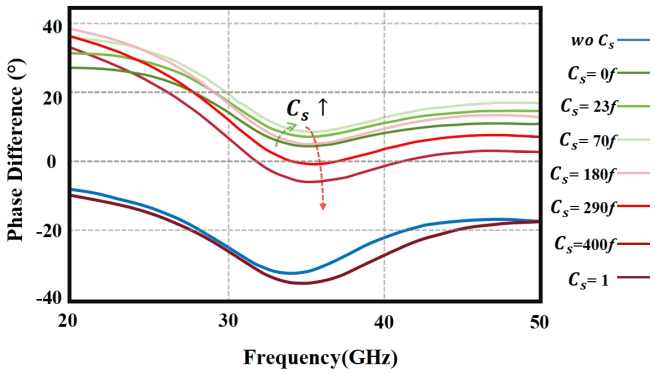

Fig. 4. Phase difference of the conventional topology and phase differences of the proposed topology sweeping the value of C_s.

For better analyzing, suppose C_s to be 0 and infinity and θ_4 in the low gain mode of the proposed topology could be written as (10), (11) at the bottom of last page where:

$$\gamma = \angle \frac{(SC_{ds3\_T} + g_{ds3}) \cdot (SC_{gd3\_T} + SC_c)}{(SC_{ds3\_T} + g_{ds3}) + (SC_{gd3\_T} + SC_c)} > 0 \qquad (12)$$

Based on the analysis of θ_4 of different modes and their first partial derivations on W_3, the sketch of θ_4 on W_3 could be drawn as Fig. 3.(a) which shows the relationship among θ_4 of different modes in both topologies. According to Fig. 3.(a), the relationship among the phases under different modes in different topologies with a certain configured M_3 could be depicted as Fig. 3.(b).

In the conventional current steering topology, the phase in the high gain mode would be constantly lower than that in the low gain mode and the phase error would rise as W_3 (W_4) increases. It is because the miller effect of the gate-drain parasitic capacitor of M_4. Though M_4 would balance the capacitance at node X to nearly the same under different gain modes, it introduces a certain miller capacitor to the output node in the high gain mode only while it could be omitted in the low gain mode. For those wide gain control range VGAs which requires greater W_3 (W_4), the drawback of the conventional topology on phase error would be more significant.

In the proposed topology, as C_s increases from 0 to infinity, the phase in the low gain mode varies continuously from somewhere higher than that of the high gain mode and ends somewhere lower than that of the high gain mode. That is to say, it must exists that a certain value of C_s which would minimize the phase error to zero. Since the miller capacitor at the output node which only effects in the high gain mode could not be eliminated, we mismatch the capacitance at node X to compensate the impact by configuring C_s in the gain-lowering path which only effects in the low gain mode.

The experimental results of VGAs in both topologies with input and output impedance matching networks are presented in Fig. 4 with the transistor parameters in Table I.

In the conventional current steering topology, the phase difference is negative. In the proposed topology, as C_s increases from zero, the phase difference would first rise to a peak from a positive value and then it would drop from the peak to a more negative value than that of the conventional topology. The phase difference of the conventional current steering topology is illustrated as the blue line while the process of rising and dropping of the phase difference of the proposed topology is illustrated as the fading green lines and the deepening red lines respectively in Fig. 4. It is demonstrated that with certain configuration of C_s, the phase difference would approach zero.

TABLE I
PARAMETERS OF THE TRANSISTORS

M_1 (W/L)	M_2 (W/L)	M_3 (W/L)	M_4 (W/L)
32μm/60nm	6μm/60nm	32μm/60nm	32μm/60nm

III. Measurement and Result

A Ka-band differential VGA in the proposed topology is demonstrated using the transistor parameters in Table I with transformer-based baluns to achieve broadband impedance matching. To better reach a reasonable C_s, an inductor is introduced to the inter-stage of the cascode amplifier which neutralizes the total capacitance at node X.

The proposed VGA is fabricated in 65 nm CMOS technology with a core area of 250 μm × 390 μm (0.098 mm^2). The layout of the VGA is shown in Fig. 5. The DC power is 13 mW from the 1.2 V supply.

The simulated S-parameters of the VGA in both gain modes are plotted in Fig. 6. The simulated gain peaks at 7.3 dB across a 3dB bandwidth of 32.5 GHz - 39 GHz. The input and output return loss of the VGA is less than 7 dB.

The phase difference and gain difference between both gain modes of the VGA are plotted in Fig. 7. Within the operating bandwidth, the phase error is no more than 1.4° and the gain control range is 16 dB with a variation of ± 0.18 dB.

The power compression point of the VGA in the high gain mode at 35 GHz is simulated as well. The output 1dB compression point is -0.85 dBm at 35 GHz.

TABLE II
COMPARISON BETWEEN PRIOR ARTS

Ref	Process	Bandwith (GHz)	DC Power (mW)	Peak Gain (dB)	Control Range (dB)	RMS Gain Error (dB)	Phase Error (°)	FEPE	OP1dB (dBm)	Chip area (mm^2)
[4]	65 nm	53-63	25	6	15	N/A	3	0.33	0	0.116
[6]	65 nm	38-40	38	22	16	N/A	2.67	2.68	2.5	0.37
[5]	65 nm	20-43	30.8	14.5	21.5	N/A	2	0.13	-16.5 (IP1dB)	0.34
[3]	40 nm	15-25	16	12	16	0.2	1.6	0.25	2.5	0.065
[7]	90 nm	22.7-29.7	7.4	19.2	23.7	0.94	4.5	3.65	5.8	0.383
This Work*	65 nm	32.5-39	13	7.5	16	0.18	1.4	0.19	-0.9	0.098

* Post-layout simulation

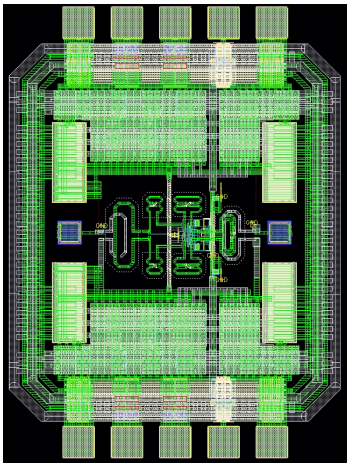

Fig. 5. Layout of the proposed VGA

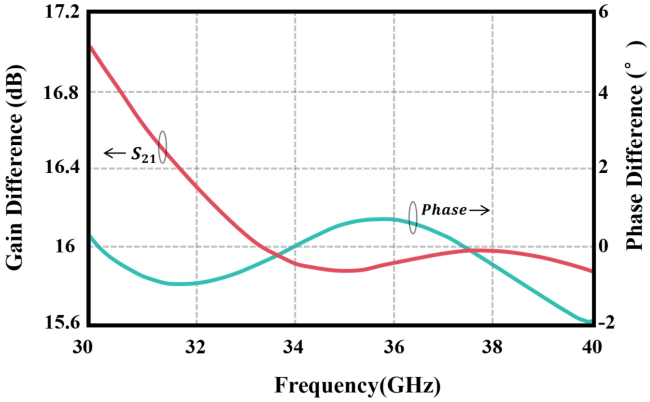

Fig. 7. Simulated gain difference and phase difference between both gain modes of the proposed VGA.

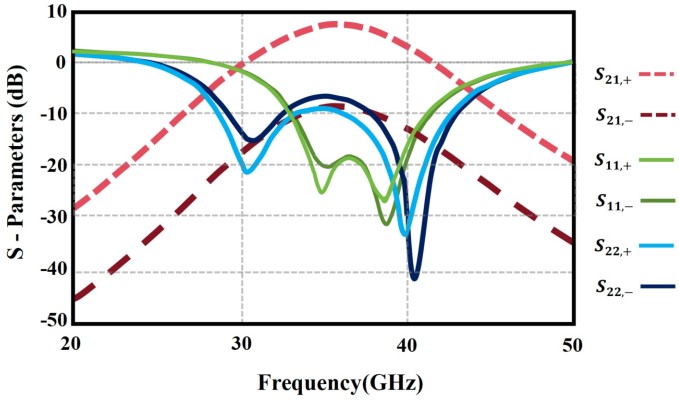

Fig. 6. Simulated S-parameters of the proposed VGA.

To indicate the ability for VGAs to work in high frequency with a small phase error in a wide band, a concept of frequency equivalent phase error (FEPE) is presented as [3]:

$$\text{FEPE} = \frac{\frac{\varphi_1}{f_1} + \frac{\varphi_2}{f_2}}{\frac{\text{BW}}{f_c}} \tag{13}$$

where φ_1, φ_2 refer to the largest and smallest phase error, respectively. f_1, f_2 refer to the frequency where φ_1, φ_2 occurs. BW refers to the bandwidth and f_c refers to the center frequency of the VGA.

The performance of the proposed VGA is summarized in Table II in comparison with prior arts. It is shown that the proposed VGA achieves a low phase error and a wide gain control range with a low gain error. In addition, the proposed topology is well-suited for high-frequency applications with wide bandwidth as indicated by the FEPE factor.

IV. CONCLUSION

In this paper, a current steering topology with switched capacitor is proposed. The mechanism of the switched capacitor is analyzed mathematically and demonstrated by simulation. A 65 nm CMOS VGA in the topology is demonstrated to realize a wide gain control range of 16 dB with maximum 1.4° phase error and maximum 0.18 gain error across 32.5 GHz - 39 GHz. The gain peaks at 7.3 dB with 13 mW power consumption from 1.2 V voltage. The chip area is 0.098 mm^2 excluding input/output pads.

REFERENCES

[1] J. -H. Tsai and Y. -T. Chen, "A 27–43 GHz CMOS Body-Biased Digital Current-Steering VGA With 4 Bit and Low Phase Shift," in IEEE Microwave and Wireless Technology Letters, vol. 33, no. 2, pp. 196-199, Feb. 2023, doi: 10.1109/LMWC.2022.3208631.

[2] Q. Zhang et al., "A Ka-Band CMOS Phase-Invariant and Ultralow Gain Error Variable Gain Amplifier With Active Cross-Coupling Neutralization and Asymmetric Capacitor Techniques," in IEEE Transactions on Microwave Theory and Techniques, vol. 70, no. 1, pp. 85-100, Jan. 2022, doi: 10.1109/TMTT.2021.3125326.

[3] C. -C. Yang et al., "A Low-Phase Error Cascode CMOS Variable Gain Amplifier With 180° Phase Control for Phase Array Systems," in IEEE Transactions on Microwave Theory and Techniques, vol. 70, no. 9, pp. 4187-4198, Sept. 2022, doi: 10.1109/TMTT.2022.3142158.

[4] D. Huang, L. Zhang, L. Zhang and Y. Wang, "A 60-GHz, 15-dB Gain Range Digitally Controlled Phase-Inverting VGA With 0-dBm OP1 dB and 3° Phase Variation in 65-nm CMOS," in IEEE Microwave and Wireless Components Letters, vol. 28, no. 9, pp. 819-821, Sept. 2018, doi: 10.1109/LMWC.2018.2854964.

[5] T. Wu, C. Zhao, H. Liu, Y. Wu, Y. Yu and K. Kang, "A 20 43 GHz VGA with 21.5 dB Gain Tuning Range and Low Phase Variation for 5G Communications in 65-nm CMOS," 2019 IEEE Radio Frequency Integrated Circuits Symposium (RFIC), Boston, MA, USA, 2019, pp. 71-74, doi: 10.1109/RFIC.2019.8701807.

[6] J. -H. Tsai and C. -L. Lin, "A 40-GHz 4-Bit Digitally Controlled VGA With Low Phase Variation Using 65-nm CMOS Process," in IEEE Microwave and Wireless Components Letters, vol. 29, no. 11, pp. 729-732, Nov. 2019, doi: 10.1109/LMWC.2019.2942013.

[7] J. -F. Chang and Y. -S. Lin, "7.4-mW, 22.7–29.7 GHz CMOS VGA With 23.7 dB (19.2 to 4.5 dB) Gain Tuning Range and 3.26 dB NFavg," in IEEE Microwave and Wireless Components Letters, vol. 32, no. 9, pp. 1075-1078, Sept. 2022, doi: 10.1109/LMWC.2022.3167707.

[8] Y. Yi, D. Zhao and X. You, "A Ka-band CMOS Digital-Controlled Phase-Invariant Variable Gain Amplifier with 4-bit Tuning Range and 0.5-dB Resolution," 2018 IEEE Radio Frequency Integrated Circuits Symposium (RFIC), Philadelphia, PA, USA, 2018, pp. 152-155, doi: 10.1109/RFIC.2018.8428833.