# Design and implementation of a test environment for a MPPCs reader multi-channel ASIC

Mauricio Montanares.
Universidad del Bío-Bío

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## About this work

▶ This work present the design and implementation of a testing platform for an ASIC (application specific integrated circuit).

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▶ The chip/ASIC was manufactured and needs to be tested, for do this, it is necessary to design, develop and implement a custom platform that allows the last.

## About this work

▶ This work present the design and implementation of a testing platform for an ASIC (application specific integrated circuit).

▶ The chip/ASIC was manufactured and needs to be tested, for do this, it is necessary to design, develop and implement a custom platform that allows the last.

▶ Testing environment/platform = Custom PCB + FPGA(custom digital logic).

## Overview of the design flow of the Integrated Circuits

## Post-Silicon validation. Why?

▶ On pre-silicon design verification its not possible to detect all design bugs.

▶ Several interactions between a design and the electrical state of a system are becoming significant (electrical bugs i.e signal integrity).

## Testing environment overview?

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## Chip overview and objectives

Ths chip/ASIC was disigned for be capable of read 4 SiPM (Silicon Photomultiplier, SiPM, Multi-Pixel Photon Counters, MPPC) in parallel and process these signals.

The objectives of the chip are:

▶ Be capable to read four MPPC, processed the inputs and convert this signals for **estimate the number of arrived photons**.

▶ **Measure the time when the photons arrived**.

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# Overview of the MPPC/SiMP detectors
What are SiMP/MPPCs?

▶ SiMP(Silicon Photomultiplier) = MPPC(Multi-Pixel Photon Counters)

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## Overview of the MPPC/SiMP detectors
What are SiMP/MPPCs?

▶ SiMP(Silicon Photomultiplier) = MPPC(Multi-Pixel Photon Counters)

▶ They are detectors consisting of multiple p-n silicon junctions that, when polarized with voltages close to their breakdown voltage, **can detect individual photons incident on their surface**.

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## Overview of the MPPC/SiMP detectors
What are SiMP/MPPCs?

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▶ They are detectors consisting of multiple p-n silicon junctions that, when polarized with voltages close to their breakdown voltage, **can detect individual photons incident on their surface**.

▶ The primary elements of the SiMP/MPPC are called pixels(photodiodes).

## Overview of the MPPC/SiMP detectors

### What are SiMP/MPPCs?

These devices are formed of a large number (hundreds or thousands) of microcells (independent between them).
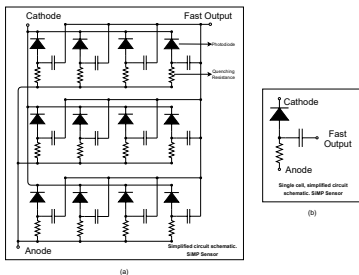


Figure: (a) Simplified circuit schematic of SiMP. (b) Single cell, simplified circuit schematic. SiMP Sensor. (On Semiconductors - 2021)

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## Overview of the MPPC/SiMP detectors

Operation mode

▶ When a photon arrives at the detector, activate some pixels, and if a pixel is activated, the pixel produces a signal out.

# Overview of the MPPC/SiMP detectors

## Operation mode

▶ When a photon arrives at the detector, activate some pixels, and if a pixel is activated, the pixel produces a signal out.

▶ When more than one photon arrives at the same time, the amplitude of the MPPC output will be the sum of the individual signals.
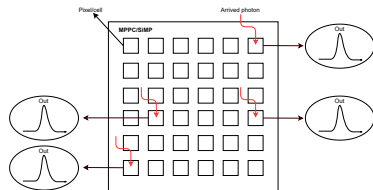


Figure: A high-level view of MPPC, arrived photons and pixel's outs (HAM, 2021)

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# Overview of the MPPC/SiMP detectors
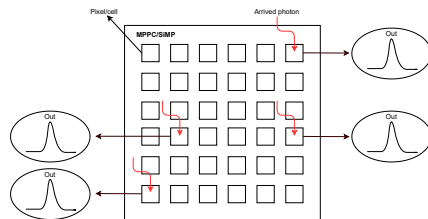
Operation mode



Figure: A high-level view of MPPC, arrived photons and pixel's outs
(HAM, 2021)

# Chip operation details

## Chip Features

▶ 4 Analog Channels based on transimpedance amplifiers (TIA)

▶ Every channel have three output VOUT-TIA, VOUT-INT, VOUT-DISC

▶ On chip DAC for precision adjust of polarization voltage (limmited to 1.8V)

▶ The chip (in theory) is capable to read from 1 to 3000 photons

## Chip Outputs
Description

We have 3 outputs for every channel, 12 outs in totally.
The outs are:

▶ VOUT-TIA: Direct out of TIA. This out is used to identify a
number greater than hundreds of triggered pixels

▶ VOUT-INT: Differntial output of the integrator. This output
is used to identify few triggered pixels.

▶ VOUT-DISC: Output from the discriminator circuit. It is used
to identify the moment when a signal arrives from the SiPM
(and can be used for estimate the number of arrived photons)

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# Chip Outs
## Block Diagram
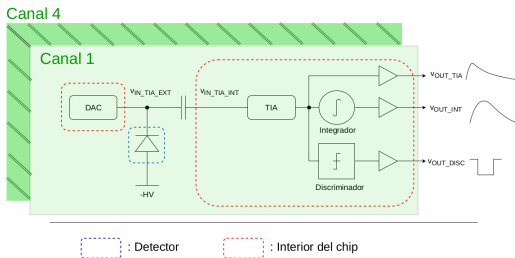


Figure: 1 of 4 channel of the chip. Image by R. Barraza

## Post Layout simulations
### For 1 photon

Renzo Barraza did some post layout simulations on his Master
Thesis.
For simulate the arrived of one photon to the detectors, was used a
current pulse of $0.1ns$ of duration and $4mA$ of amplitude.

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# Post Layout simulation TIA

For the arrived of one photon
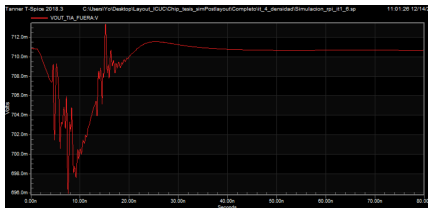


Figure: TIA voltage output. Image by R. Barraza

## Post Layout simulation Integrator
For the arrived of one photon
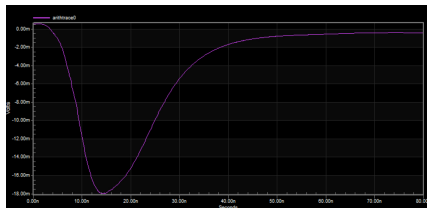


Figure: Integrator differential voltage output. Image by R. Barraza

## Post Layout simulation Discriminator

For the arrived of one photon



Figure: Discriminator voltage output. Image by R. Barraza

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## Multi-pixel trigger response

### Multiple arrived photons

For simulate the arrived of more than 1 photon, the amplitude of input signal was linearly scaled.

▶ 1 photon: 0.1$ns$ of duration and 4$mA$ of amplitude.

▶ 2 photons: 0.1$ns$ of duration and 8$mA$ of amplitude.

▶ 10 photons: 0.1$ns$ of duration and 40$mA$ of amplitude.

▶ 300 photons: 0.1$ns$ of duration and 1200$mA$ of amplitude.

▶ ...

### Note:

We can make a table to have the equivalence between charge[q]and number of photons based on the conditions of the experiments described by R.B

## The problems
Description of some of the problems

Verify the functionality of the chip.
Stimulus inputs and read the outputs of the chip. A post-silicon
verification. For these objectives, we need to be capable of doing
two things:

- ▶ Stimulus the inputs
- ▶ Read the outputs
- ▶ (and implement these last two things on real hardware with
  additional considerations for correct operation of the device)*

# How read the outputs of TIA and Integrator?
Methodologies described for R. Barraza

R. barraza in his Thesis proposes two methodologies:

▶ Peaking Time

▶ Max Amplitude

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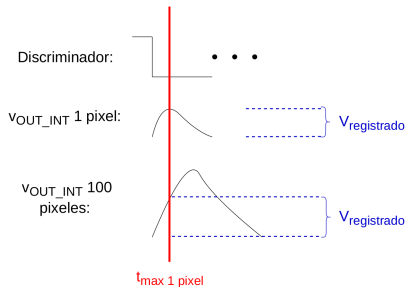
# Peaking Time



Figure: Peaking Time methodology. Image by R. Barraza

## Max Amplitude
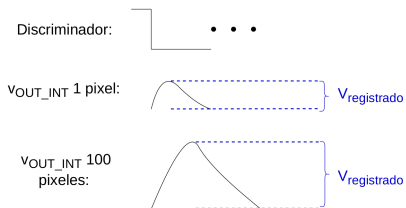


Figure: Max amplitude methodology. Image by R. Barraza

# Time over threshold

| Número de pixeles dis- parados | Duración de pulso del discriminador |
|---|---|
| 1 pixel | 11,4 ns |
| 2 pixeles | 17,68 ns |
| 3 pixeles | 21,24 ns |
| 7 pixeles | 31,65 ns |
| 11 pixeles | 38,07 ns |
| 29 pixeles | 54,88 ns |
| 47 pixeles | 65,88 ns |
| 199 pixeles | > 100 ns |

Figure: Time over threshold methodology. Table by R. Barraza
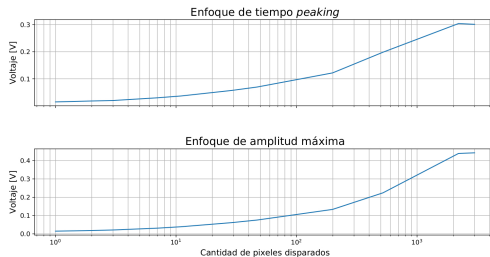
# Multi-pixel trigger TIA response

Methodologies comparison



Figure: TIA Methodologies comparison. Image by R. Barraza

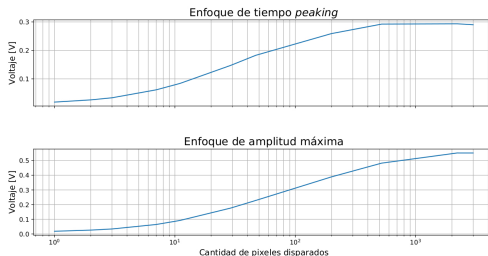# Multi-pixel trigger Integrator response

Methodologies comparison



Figure: Integrator Methodologies comparison. Image by R. Barraza

## Current pulse generator

It's possible to implement a circuit that permits to the user control
the input of charge to apply to the chip?

▶ How generate a current pulse? $I = C\frac{dV_i}{dt}$

▶ What elements we can control of the above equation? maybe
both..

▶ (how many levels of control we would like to have?)*

# Current pulse generator

1 charge option implementation

▶ For one option of charge



Figure: 1 Option charge generator

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# Current pulse generator simulation

1 option of current pulse simulation

▶ Simulation on LTspice
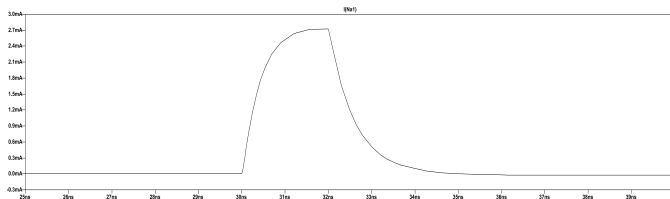


Figure: Simulation of 1 option current pulse generator

# Current pulse generator

Multi-Option current pulse generator implementation
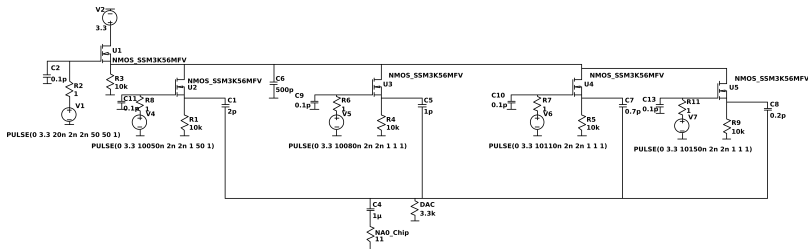
▶ For Multi-Option of current pulse



Figure: Multi-Option current pulse generator

## Current pulse generator
Multi-Option current pulse generator simulation
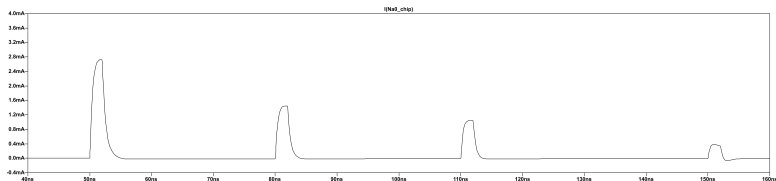
▶ Simulation on LTspice



Figure: Multi-Option current pulse generator simulation

# Current pulse generator. Simplified circuit
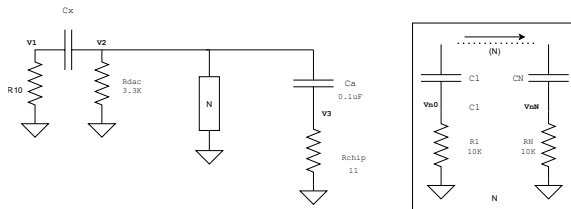
Multi-Option current pulse generator



Figure: Multi-Option current pulse generator. Simplified circuit

# Current pulse generator
Notes

- $\frac{dVi}{dt}$ depends of the *time on* value of the transistor
- It's not possible to generate pulses with the characteristics described in the thesis experiments
- But we can generate pulses where the equivalent area corresponds to the areas of the pulses described in the thesis. Equivalent charge.

# Read out circuit
TIA and Integrator output

The outputs TIA and INT (peak events) of the circuit are fast (ns).
For implement the second method (Max amplitude*) we can do:

- ▶ Peak detector
- ▶ Brute force (High speed ADC > 1GSPS)
- ▶ Dinamic comparator

## Selected option

I propose the use of a Dinamic Comparator for estimate the peak
of the signal out of TIA and Integrator.

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## Things that we know

▶ Relationship between charge[q] and number of photons

▶ It's possible control the charge changing the value of C

▶ We know the values of the output voltage of TIA and Integrator for some specific quantities of photons

▶ We know the duration of Discriminator pulse for some specific quantities of photons

# Read out circuit
Discriminator ouput

The output of Discriminator is more easy to measure using only a GPIO pin.

- ▶ FPGA GPIO (resolution of the rising or falling edge events is limited by the clock of the system)

# Read out circuit
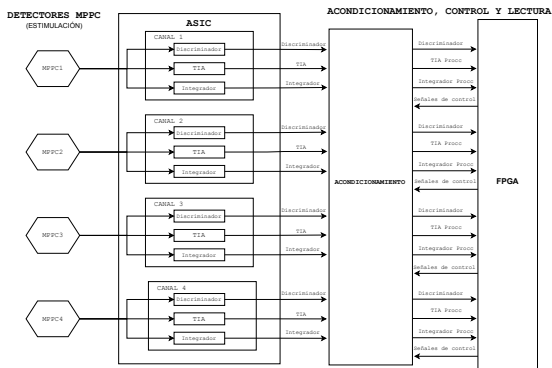## General block diagram



Figure: General block diagram of the system

# Read out circuit
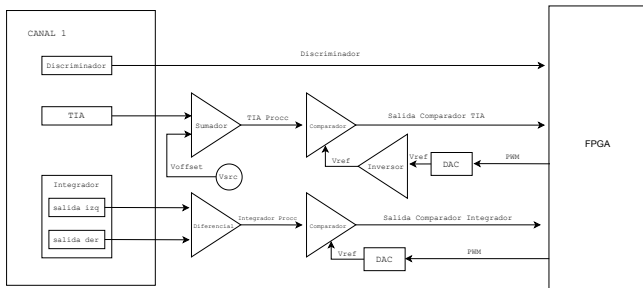Conditioning and Processing



Figure: Conditioning and processing block diagram

## Some Reference of the Read out circuit design

[1]. Orita, T., et al. "The current mode Time-over-Threshold ASIC for a MPPC module in a TOF-PET system." NIMA (2017) https://doi.org/10.1016/j.nima.2017.11.097

[2]. Orita, T., K. Shimazoe, and H. Takahashi. "The dynamic time-over-threshold method for multi-channel APD based gamma-ray detectors." NIMA (2015): 154-161