# A Dynamic Analysis of the Dickson Charge Pump Circuit

Toru Tanzawa and Tomoharu Tanaka

***Abstract*—Dynamics of the Dickson charge pump circuit have been analyzed. The analytical results enable the estimation of the rise time of the output voltage and that of the power consumption during boosting. By using this analysis, the optimum number of stages to minimize the rise time has been estimated as 1.4 $N_{\min}$, where $N_{\min}$ is the minimum value of the number of stages necessary for a given parameter set of a supply voltage, threshold voltages of transfer diodes, and a boosted voltage. Moreover, the self-load capacitance of the charge pump, which should be charged up at the same time as the output load capacitance of the charge pump, has been estimated as about one-third of the total charge pump capacitance. As a result, the equivalent circuit of the charge pump has been modified. The analytical results have been in good agreement with the simulation results by the iteration method, typically within 10% for the rise time and within 2% for the power consumption. In case of a charge pump with MOS transfer transistors, the analytical result of the rise time has agreed with the SPICE simulation within 10%.**

***Index Terms*— Charge pump circuit, equivalent circuit, optimum number of stages, power consumption, rise time.**

## I. Introduction

THE Dickson charge pump circuit [1] is currently used to generate a voltage higher than the supply voltage on chip. Power IC's require high voltages to switch MOS transistors, so that charge pumps with fewer than four stages are used [2], [3]. Di Cataldo *et al*. have analyzed dynamics of charge pumps with one or two stages [4] and with three stages [5] for high-speed switching of transistors. On the other hand, single-power EEPROM's require high voltages to apply to memory cells to rewrite data. So far, improved Dickson charge pump schemes [6]–[9] operable at low voltages have been developed for low-voltage EEPROM's. Such EEPROM's need charge pumps with more than three stages to generate rewriting voltages of 10–20 V from a supply voltage of 3–5 V. Recently, it became increasingly important to reduce the rise time for generating such high voltages because of the requirement of a data rewriting operation at high speed. However, the characteristics of a charge pump with an arbitrary number of stages is known only in steady state, not during boosting.

This paper describes a dynamic analysis of the Dickson charge pump circuit with an arbitrary number of stages. First, in Section II, the charge stored in each charge pump capacitor in steady state is derived as a function of the output voltage. Next, the total charge consumed by the charge pump during boosting is obtained by two different methods; by using the charge stored in each capacitor and by using the sum of the charge consumed by the charge pump in one cycle time. Then, combining these total charge estimations derived by the two methods, a recurrence formula for the output voltage is derived. As a result, the rise time and current consumption of a charge pump with an arbitrary number of stages can be calculated from the initial condition. The load capacitance of the charge pump itself is estimated and the equivalent circuit of the charge pump is modified. In Section III, the accurate rise time and current consumption are computed by the iteration method. In Section IV, in order to verify the dynamic analysis, its results are compared with the iteration method and the SPICE simulation. In Section V, it is shown that there are a number of stages to minimize the rise time under the condition of a given circuit area. Moreover, the power efficiency during boosting is obtained.

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## II. Dynamic Analysis

Fig. 1 illustrates the Dickson charge pump circuit. In [1], Dickson has discussed the charge pump operation in steady state when the output voltage is limited to a constant voltage. In steady state, the charge transferred from one capacitor to the next one just equals the charge transferred to the output. If the rise time of the output voltage is sufficiently long compared with the cycle time of the clocks driving the charge pump, or in other words, the output voltage rises "slowly," the charge pump will be kept steady state even during boosting. In this section, dynamics of the Dickson charge pump circuit are investigated by using only the steady state equations. In order to take the load capacitance of the charge pump itself into account, the total charge consumed by the charge pump is introduced.

A charge pump with an even number of stages is considered in this paper, but a similar analysis in the case of an odd-number-stage charge pump can be carried out.

The following assumptions are made.

1) Each diode and charge pump capacitor have constant values of $V_t$ and $C$, respectively.
2) The parasitic capacitance is negligibly small compared with the charge pump capacitance.
3) The cycle time of the input clocks $CLK1, 2$ driving the charge pump is sufficiently large for all RC time constant to be negligible and is set to be one.

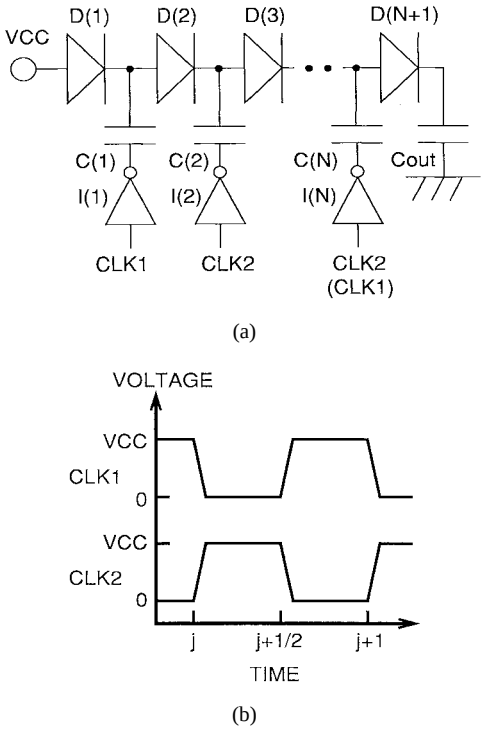



Fig. 1. (a) The Dickson charge pump circuit and (b) the driving clocks $CLK1, 2$. The clock driving the inverter $I(N)$ is $CLK2$ for even $N$ or $CLK1$ for odd $N$.

### A. Steady State

$q_{\rm out}$ is defined as the charge transferred from one capacitor to the next one during one cycle, and $Q(i)$ $(1 \le i \le N)$ is defined as the charges stored in the capacitors $C(i)$ at time $j$. The following relation holds under the condition that the diode $D(1)$ is cut off at time $j$:

$$Q(1) = C(V_{\rm cc} - V_t) \equiv CV_g \tag{1}$$

where $V_{\rm cc}$ is the supply voltage and $V_g$ represents the maximum voltage gain per stage. Next, from the condition that the diode $D(2)$ is cut off at time $j+1/2$ and the fact that the charges stored in the capacitors $C(1)$ and $C(2)$ at time $j+1/2$ are $Q(1) - q_{\rm out}$ and $Q(2) + q_{\rm out}$, respectively

$$V_{\rm cc} + \frac{Q(1) - q_{\rm out}}{C} - \frac{Q(2) + q_{\rm out}}{C} = V_t \tag{2}$$

the following relation holds using (1):

$$Q(2) = 2CV_g - 2q_{\rm out}. \tag{3}$$

Also, from the condition that the diode $D(3)$ is cut off at time $j$

$$V_{\rm cc} + \frac{Q(2)}{C} - \frac{Q(3)}{C} = V_t \tag{4}$$

the following relation holds using (3):

$$Q(3) = 3CV_g - 2q_{\rm out}. \tag{5}$$

Continuing the process, the general forms are expressed as

$$Q(2k-1) = (2k-1)CV_g - 2(k-1)q_{\rm out} \tag{6}$$

$$Q(2k) = 2kCV_g - 2kq_{\rm out} \tag{7}$$

where $1 \le k \le N/2$. Finally, from the condition that the diode $D(N+1)$ is cut off at time $j$

$$V_{\rm cc} + \frac{Q(N)}{C} - V_{\rm out} = V_t. \tag{8}$$

$Q(N)$ is represented by the output voltage of charge pump, $V_{\rm out}$, as

$$Q(N) = C(V_{\rm out} - V_g). \tag{9}$$

The relationship between (7) and (9) gives the output voltage-current characteristic

$$q_{\rm out} = \frac{C}{N}[(N+1)V_g - V_{\rm out}] \tag{10}$$

which has been derived by Dickson in [1]. From (6), (7), and (10), the charge stored in each charge pump capacitor is represented by

$$Q(2k-1) = \frac{2(k-1)}{N}C(V_{\rm out} - V_g) + CV_g \tag{11}$$

$$Q(2k) = \frac{2k}{N}C(V_{\rm out} - V_g). \tag{12}$$

### B. Total Supplied Charge

In this section, the rise time and the current consumption during boosting are derived. In order to derive the recurrence formula of the output voltage, the total charge consumed by the charge pump during boosting is obtained by two different methods; by using the charge stored in each capacitor and by using the sum of the charge consumed by the charge pump in one cycle time.

First, the total charge $Q_{\rm cc}^d(j)$ consumed by the charge pump during the arbitrary time $j$ is calculated using the charges stored in the charge pump capacitors as shown in (11) and (12).

The total charge $Q_{\rm cc}(k,j)$ $(1 \le k \le N)$ consumed by the inverter $I(k)$ driving the capacitor $C(k)$ during $j$ equals the total charge transferred from the capacitor $C(k)$ to the next one $C(k+1)$ through the diode $D(k+1)$ during $j$. Therefore, $Q_{\rm cc}(k,j)$ equals the total charge increase in the capacitors $C(k+1), C(k+2), \cdots, C(N)$ and $C_{\rm out}$ during $j$, where $C_{\rm out}$ is the output capacitance of the charge pump circuit. Similarly, the total charge $Q_{\rm cc}(0,j)$ supplied by the input voltage $V_{\rm cc}$ at the leftside in Fig. 1(a) equals the total charge increase in all capacitors including $C_{\rm out}$. Therefore, if $Q(i,j)$ and $Q_{\rm out}(j)$ are the charges stored in the capacitors $C(i)$ $(1 \le i \le N)$ and $C_{\rm out}$ at $j$, respectively, for $0 \le k \le N-1$

$$Q_{\rm cc}(k,j) = \sum_{i=k+1}^{N} [Q(i,j) - Q(i,0)] + [Q_{\rm out}(j) - Q_{\rm out}(0)] \tag{13}$$

and

$$Q_{\rm cc}(N,j) = Q_{\rm out}(j) - Q_{\rm out}(0). \tag{14}$$

The total consumed charge $Q_{cc}^d(j)$ is the sum of all charges $Q_{cc}(k,j)$ $(0 \le k \le N)$, so that

$$\begin{aligned} Q_{cc}^d(j) &= \sum_{k=0}^{N} Q_{cc}(k,j) \\ &= \sum_{k=1}^{N} k[Q(k,j) - Q(k,0)] \\ &\quad + (N+1)[Q_{out}(j) - Q_{out}(0)]. \end{aligned} \tag{15}$$

The following initial conditions can be assumed

$$Q(2k,0) = 0 \tag{16}$$

$$Q(2k-1,0) = CV_g \tag{17}$$

and

$$Q_{out}(0) = C_{out}V_g \tag{18}$$

which satisfy (11) and (12). Under the assumption that (11) and (12) hold during boosting, (15) results in

$$Q_{cc}^d(j) = (N+1)C_{load}(V_{out}(j) - V_g) \tag{19}$$

$$C_{load} \equiv C_{out} + C_{pump} \tag{20}$$

$$C_{pump} = \begin{cases} \frac{4N^2+3N+2}{12(N+1)}C, & \text{(for even } N) \\ \frac{4N^2-N-3}{12N}C, & \text{(for odd } N). \end{cases} \tag{21}$$

Another expression for $Q_{cc}^d(j)$ is derived below. Since the charge $q_{cc}^s$ supplied by the power supply in a cycle time in steady state is equal to the charge $q_{out}$ transferred to the capacitor $C(1)$ through the diode $D(1)$ plus the charge $Nq_{out}$ transferred from $N$ capacitors $C(k)$ $(1 \le k \le N)$ to the next ones, then

$$q_{cc}^s = (N+1)q_{out}. \tag{22}$$

Like the above equation in steady state, the relation between the supplied charge $q_{cc}^d(j)$ and the output charge increase $q_{out}(j)$ in a cycle time from $j$ to $j+1$ during boosting is assumed to be

$$q_{cc}^d(j) = (N+1)q_{out}(j). \tag{23}$$

Under the assumption that (10) holds even during boosting, the total supplied charge during $j$, $Q_{cc}^d(j)$, is given by

$$\begin{aligned} Q_{cc}^d(j) &= \sum_{m=0}^{j} q_{cc}^d(m) \\ &= (N+1)\sum_{m=0}^{j} \frac{C}{N}[(N+1)V_g - V_{out}(m)]. \end{aligned} \tag{24}$$

### C. Rise Time and Current Consumption

Combining (19) with (24)

$$C_{load}(V_{out}(j) - V_g) = \sum_{m=0}^{j} \frac{C}{N}[(N+1)V_g - V_{out}(m)]. \tag{25}$$

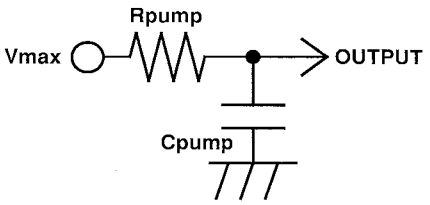



Fig. 2. The modified equivalent circuit of the charge pump. $V_{max} = (N+1)V_g$, $R_{pump} = N/C$, and $C_{pump} \approx NC/3$.

Since (25) holds for arbitrary $j$, the recurrence formula for the output voltage $V_{out}$ holds as follows:

$$C_{load}(V_{out}(j+1) - V_{out}(j)) = \frac{C}{N}[(N+1)V_g - V_{out}(j+1)]. \tag{26}$$

Using the initial condition of $V_{out}(0) = V_g$ from (18), (26) is solved as

$$V_{out}(j) = (N+1)V_g - NV_g\beta^j \tag{27}$$

$$\beta = \frac{1}{1 + \frac{C}{NC_{load}}}. \tag{28}$$

As a result, the rise time $T_r$ that the output voltage $V_{out}(j)$ raises from $V_g$ to $V_{pp}$, which satisfies $V_{out}(T_r) = V_{pp}$, is solved as

$$T_r = \frac{\ln\left[1 - \frac{V_{pp}-V_g}{NV_g}\right]}{\ln\beta} \tag{29}$$

where $N$ is the number of stages, $V_g$ is the maximum voltage gain per stage defined by (1), and $\beta$ is defined by (28). It is noted that this term should be multiplied by the cycle time of the driving clocks in practice, because (29) is expressed by the number of clock cycles. From (19), the mean current consumption $I_{cc}^d$ during $T_r$ can be obtained as

$$\begin{aligned} I_{cc}^d &\equiv Q_{cc}^d(T_r)/T_r \\ &= (N+1)C_{load}(V_{pp} - V_g)/T_r. \end{aligned} \tag{30}$$

Equations (29) and (30) are the main results of this paper.

$C_{load}$ can be regarded as the total load capacitance during boosting, so that $C_{pump}$ represents the self-load capacitance of the charge pump itself. $C_{pump}$ is about one-third of the total charge pump capacitance, $C_{pump} \approx NC/3$, and its error is less than 3% for even $N \ge 4$ and less than 7% for odd $N \ge 5$.

### D. Equivalent Circuit

Although the output voltage $V_{out}(j)$ is actually a staircase waveform, it can be regarded as a smooth function in case the rise time is sufficiently large compared with the cycle time of the driving clocks. In this case, (26) indicates the equivalent circuit of the charge pump as shown in Fig. 2. $R_{pump}$ represents the output series resistance of the charge pump and is given by $N/C$ (as mentioned above, this is multiplied by the cycle time of the driving clocks and has the same dimension as the resistor). $V_{max}$ is the maximum output voltage of the charge pump, $(N+1)V_g$. $C_{pump}$ expressed by (21) indicates the self-load capacitance of the charge pump and is connected in parallel with the output load capacitance $C_{out}$.

## III. Iteration Method

In this section, in order to compute the rise time and the current consumption accurately, only the cutoff condition of the transfer diodes and the charge conservation rule are used. A charge pump circuit with an even number of stages is also considered in this section.

### A. Rise Time

Since the charges $Q(2k-1,j)$ stored in the capacitors $C(2k-1)$ at time $j$ are transferred to the next ones $C(2k)$ by time $j+1/2$, the following relations hold if the charge conservation rule is assumed:

$$Q(2k-1,j)+Q(2k,j)=Q(2k-1,j+1/2)+Q(2k,j+1/2). \quad (31)$$

From the condition that the diode $D(2k)$ is cut off at time $j+1/2$

$$\frac{Q(2k,j+1/2)}{C}-\frac{Q(2k-1,j+1/2)}{C}=V_g. \quad (32)$$

Similarly, the charges $Q(2k,j+1/2)$ stored in the capacitors $C(2k)$ at time $j+1/2$ are transferred to the capacitors $C(2k+1)$ by time $j+1$. Then

$$Q(2k,j+1)+Q(2k+1,j+1)=Q(2k,j+1/2)+Q(2k+1,j+1/2) \quad (33)$$

$$\frac{Q(2k+1,j+1)}{C}-\frac{Q(2k,j+1)}{C}=V_g. \quad (34)$$

And also

$$Q_{\rm out}(j+1)+Q(N,j+1)=Q_{\rm out}(j+1/2)+Q(N,j+1/2) \quad (35)$$

$$\frac{Q_{\rm out}(j+1)}{C_{\rm out}}-\frac{Q(N,j+1)}{C}=V_g. \quad (36)$$

Furthermore

$$Q(1,j)=Q(1,j+1)=CV_g. \quad (37)$$

Eliminating the intermediate states at time $j+1/2$, $Q(k,j+1/2)$, and $Q_{\rm out}(j+1/2)$ from the above equations, for more than three stages, (38)–(43), shown at the bottom of the page, apply. Equations (40) and (41) hold for more than five stages, and $2\le k\le N/2-1$. The stored charges $Q(k,j)$, $(1\le k\le N)$, and $Q_{\rm out}(j)$ can be iteratively computed using the initial condition of (16)–(18). The rise time can be obtained by the time that the output voltage $Q_{\rm out}/C_{\rm out}$ rises from the initial voltage $V_g$ to the final voltage $V_{\rm pp}$. In case of a charge pump with one or two stages, the equations like the above can be analytically solved for each $Q(k,j)$ and $Q_{\rm out}(j)$, so that the rise time can be solved exactly [4]. On the other hand, the solution of the rise time for a charge pump with three stages can be obtained approximately rather than exactly because of the nonlinear equation for the rise time [5]. This approximation introduces an error of only a few percent to the solution.

### B. Current Consumption

The charge supplied to the charge pump during one cycle from $j$ to $j+1$, $q^d_{\rm cc}(j)$, is the sum of the charges supplied by the inverters $I(2k-1)$, which are the charge increases in the capacitors $C(2k)$, $Q(2k,j+1/2)-Q(2k,j)$, the charges supplied by the inverters $I(2k)$ and $I(N)$, which are the charge increases in the capacitors $C(2k+1)$ and $C_{\rm out}$, $Q(2k+1,j+1)-Q(2k+1,j+1/2)$ and $Q_{\rm out}(j+1)-Q_{\rm out}(j+1/2)$, respectively, and the charge supplied to the capacitor $C(1)$ by the input voltage, $Q(1,j+1)-Q(1,j+1/2)$. By using (31)–(37)

$$q^d_{\rm cc}(j)=(2CV_g-Q(2,j))-\sum_{k=2}^{N/2}(Q(2k,j)-CV_g)+\sum_{k=1}^{N/2-1}Q(2k+1,j+1)+(Q_{\rm out}(j+1)-Q_{\rm out}(j)). \quad (44)$$

Therefore, the total charge supplied to the charge pump during boosting, $Q^d_{\rm cc}(T_r)$, can be iteratively computed by

$$Q^d_{\rm cc}(T_r)=\sum_{j=0}^{T_r}q^d_{\rm cc}(j). \quad (45)$$

As a result, the current consumption during boosting, $I^d_{\rm cc}$, can be calculated by

$$I^d_{\rm cc}=Q^d_{\rm cc}(T_r)/T_r \quad (46)$$

using $T_r$ computed in Section III-A and $Q^d_{\rm cc}(T_r)$ computed by (45). The rise time and the current consumption computed

$$Q(2,j+1)=\frac{1}{4}[Q(2,j)+Q(3,j)+Q(4,j)-CV_g] \quad (38)$$

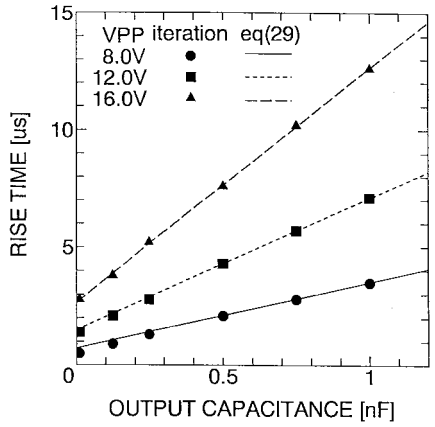
$$Q(3,j+1)=\frac{1}{4}[Q(2,j)+Q(3,j)+Q(4,j)+3CV_g] \quad (39)$$

$$Q(2k,j+1)=\frac{1}{4}[Q(2k-1,j)+Q(2k,j)+Q(2k+1,j)+Q(2k+2,j)-2CV_g] \quad (40)$$

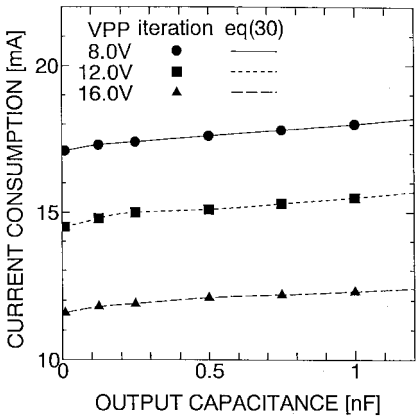
$$Q(2k+1,j+1)=\frac{1}{4}[Q(2k-1,j)+Q(2k,j)+Q(2k+1,j)+Q(2k+2,j)+2CV_g] \quad (41)$$

$$Q(N,j+1)=\frac{C}{2(C_{\rm out}+C)}[Q(N-1,j)+Q(N,j)+2Q_{\rm out}(j)-(2C_{\rm out}-C)V_g] \quad (42)$$

$$Q_{\rm out}(j+1)=\frac{C_{\rm out}}{2(C_{\rm out}+C)}[Q(N-1,j)+Q(N,j)+2Q_{\rm out}(j)+3CV_g] \quad (43)$$

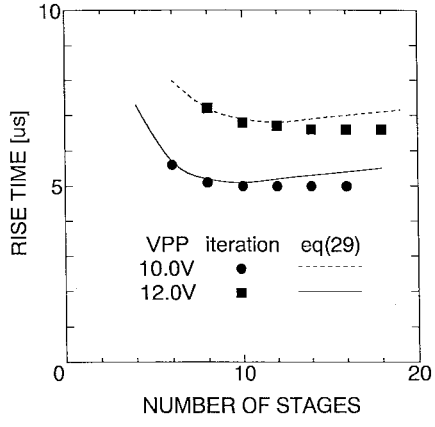



(a)

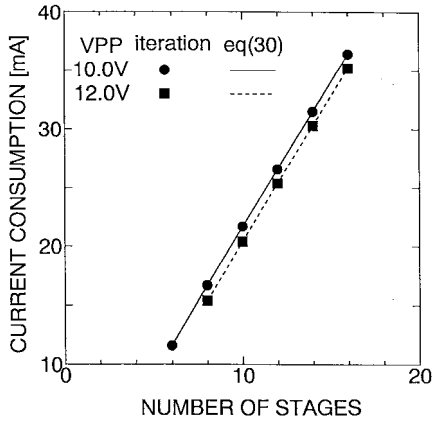



(b)

Fig. 3. Dependence of the (a) rise time and (b) current consumption on the output load capacitance under the condition of $N = 8$, $V_{cc} = 3.0$ V, $V_t = 0.6$ V, $C = 100$ pF, and the cycle time of driving clocks, $T_c = 100$ ns.




(a)




(b)

Fig. 4. Dependence of the (a) rise time and (b) current consumption on the number of stages under the condition of $V_{cc} = 3.0$ V, $V_t = 0.6$ V, $C = 100$ pF, $C_{out} = 1$ nF, and $T_c = 100$ ns.

in this section have been in good agreement with the SPICE simulation results within 5%. Therefore, the verification of the analytical results will be made by the comparison with the iteration method.

## IV. Verification of the Analysis

In this section, the analytical expressions are compared with the iteration method, the exact solutions in case of one and two stages, the approximate solution in case of three stages, and the SPICE simulation results for a charge pump with MOS transfer transistors.

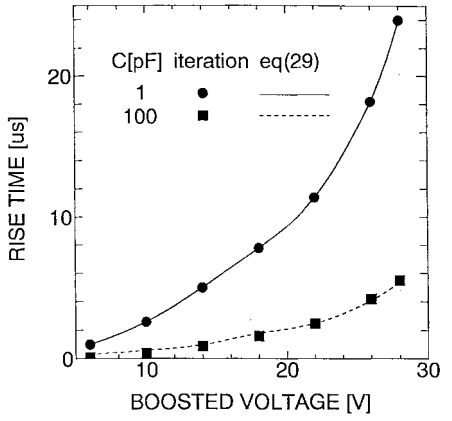
### *A. Comparison with the Iteration Method*

Figs. 3–6, respectively, show dependence of the rise time and current consumption on the output capacitance (Fig. 3), the number of stages (Fig. 4), the boosted voltage (Fig. 5), and the supply voltage (Fig. 6).

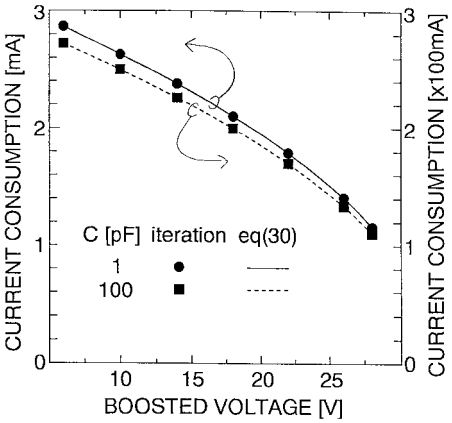
As shown in Fig. 3(a), the rise time increases proportionally to the output capacitance. The $y$-intersection in Fig. 3(a) indicates the rise time in case of no output load capacitance $(C_{out} = 0)$, and the self-load capacitance of the charge pump, which has been estimated by the analysis as about one-third of the total charge pump capacitance, is in good agreement with the iteration method. The current consumption during boosting has small dependence on the output capacitance, as shown in Fig. 3(b).

As shown in Fig. 4(a), the rise time iteratively computed by (38)–(43) is constant for a large number of stages while the rise time calculated by the analytical expression slightly increases with the number of stages because of the increasing self-load capacitance $C_{pump}$. Fig. 4(a) indicates the rise time does not depend on the excess number of stages in actual and the error of the analytical expression increases as the boosted voltage becomes much smaller than the maximum output voltage of $(N+1)V_g$. This suggests the assumption that the charge pump is kept steady state even during boosting does not hold in such a case. The constant rise time and the total supplied charge proportional to the number of stages result in a current consumption that is increasing with the number of stages [Fig. 4(b)]. The discrepancy between analytical and iterative results in Fig. 4(a) is attributed to the inaccuracy in the self-load capacitance $C_{pump}$, while this discrepancy does not appear in Fig. 4(b). This is because the discrepancy of the rise time $T_r$ is canceled by that of the total supplied charge $Q_{cc}^{d}(T_r)$ in (30), which is also increasing with the number of stages.

The rise time and the current consumption show a large dependence on the boosted voltage [Figs. 5(a) and (b)] and

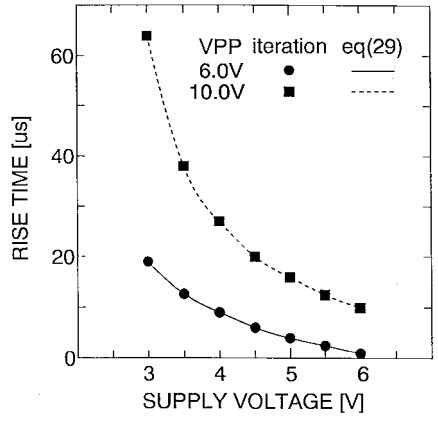



(a)

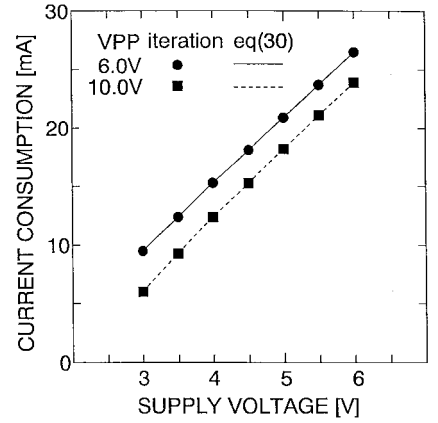



(b)

Fig. 5. Dependence of the (a) rise time and (b) current consumption on the boosted voltage under the condition of $N = 8$, $V_{cc} = 4.0$ V, $V_t = 0.6$ V, $C_{out} = 10$ pF, and $T_c = 100$ ns.




(a)




(b)

Fig. 6. Dependence of the (a) rise time and (b) current consumption on the supply voltage under the condition of $N = 4$, $V_t = 0.6$ V, $C = 100$ pF, $C_{out} = 10$ nF, and $T_c = 100$ ns.

the supply voltage [Figs. 6(a) and (b)]. Even in the case that the charge pump capacitance is ten times larger than the output capacitance as shown in Fig. 5 (in case of $C = 100$ pF and $C_{out} = 10$ pF), the analytical expression agrees with the iteration method.

Fig. 7 shows dependence of the rise time on the output voltage under the condition of no output load capacitance. In this case, the charge pump circuit has only a self-load capacitance. The analytical expression (29) in which the output capacitance $C_{out}$ is set to zero agrees with the iteration method in the case that the boosted voltage $V_{pp}$ is not much smaller than the maximum output voltage of $(N+1)V_g$. However, in the case of a small boosted voltage, the rise time given by the iteration method is independent of the number of stages. On the other hand, the rise time given by the analytical expression increases with the number of stages.

As mentioned above, the difference between the analytical expression and the iteration method increases as the boosted voltage becomes much smaller than the maximum output voltage of $(N+1)V_g$, or in other words, the number of stages becomes excessively large compared with the number of stages necessary for the boosted voltage. In such a case, the analytical results of (29) and (30) cannot be used. In a typical case that the boosted voltage is not smaller than one-fourth

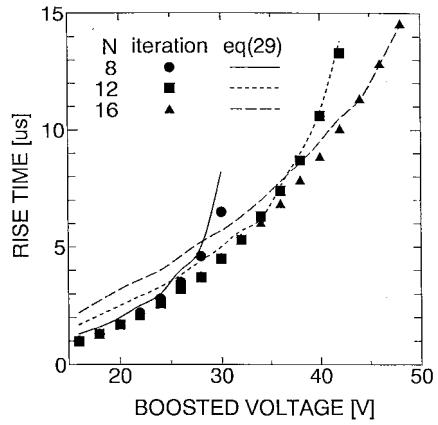



Fig. 7. Dependence of the rise time on the boosted voltage under the condition of $V_{cc} = 4.0$ V, $V_t = 0.6$ V, $C_{out} = 0$, and $T_c = 100$ ns.

of the maximum output voltage, the analytical results agree with the simulation results computed by the iteration method within 10% for the rise time and within 2% for the current consumption.

### *B. Comparison with [4] and [5]*

Di Cataldo *et al.* have analyzed dynamics of charge pumps with one or two stages [4] and with three stages [5]. The output

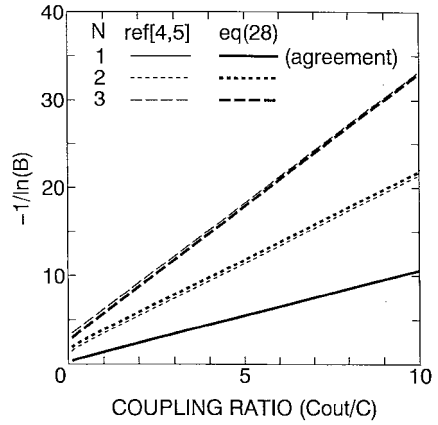



Fig. 8. Comparison of the analytical results with [4] and [5].

voltage has been derived like (27) by Di Cataldo *et al.*, where the factor $\beta$'s have been derived as

$$\beta = \begin{cases} \frac{K}{1+K}, & (\text{for } N=1) \\ \frac{1+2K}{2(1+K)}, & (\text{for } N=2) \\ \frac{3+5K+\sqrt{9+14K+9K^2}}{8(1+K)}, & (\text{for } N=3) \end{cases} \quad (47)$$

where $K$ is the coupling ratio $C_{\text{out}}/C$. $\beta$'s are the exact values in case of a charge pump circuit with one or two stages and the approximate value in case of that with three stages, respectively.

There is the difference of the rise time given by (29) with (28) and with (47) only in the factor $\beta$, so that the ratio between the rise time equals the ratio of $-(\ln\beta)^{-1}$. Fig. 8 shows dependence of the factor $-(\ln\beta)^{-1}$ on the coupling ratio $K$. Under the condition that the output capacitance is much larger than the charge pump capacitance, the factor $-(\ln\beta)^{-1}$ increases as $NC_{\text{out}}/C$ in both cases. The analytical expression agrees with the exact rise time in case of a one-stage charge pump. There are some differences in case of two- and three-stage charge pumps without the output load capacitance. However, the differences between the rise time given by (28) and by (47) in case of two and three stages are less than 2% under a condition of $K = 10$, for example.

As a result, the analytical expression can be also effective for charge pumps with fewer than four stages.

### C. Comparison with the Spice Simulation for a Charge Pump with MOS Transfer Transistors

In integrated circuits, transfer diodes used in the charge pump are realized by MOS transistors whose gate and drain terminals are shorted, as illustrated in Fig. 9. In this case, the body effect of transfer transistors should be taken into account in the cutoff condition such as in (1), (2), and so on [10]. In the Appendix, the analytical expression for the rise time is modified as (65). The characteristic of the MOS transfer transistor is specified by a body effect coefficient defined by (56), $\alpha$, and a threshold voltage at no back bias, $V_t$. In order to verify this analytical result, the SPICE simulation has been performed. The MOS transistor used in the SPICE simulation has $\alpha$ of 0.95 and $V_t$ of 0.3 V. Fig. 10 shows the dependence of

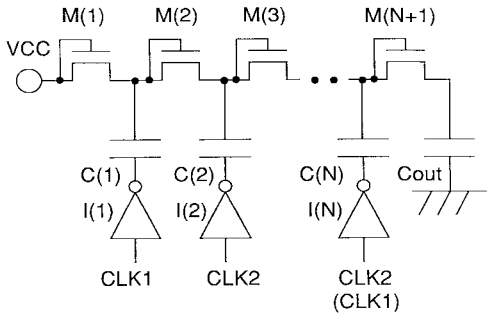



Fig. 9. The Dickson charge pump circuit with MOS transfer transistors.

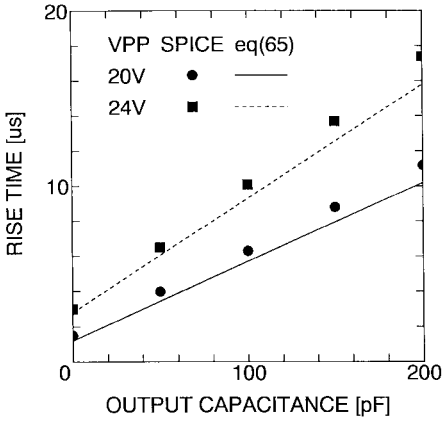



Fig. 10. Comparison of the analytical result with the SPICE simulation under the condition of $N = 8$, $C = 14$ pF, $V_{\text{cc}} = 5.0$ V, $T_c = 100$ ns, $\alpha = 0.95$, and $V_t = 0.3$ V.

the rise time on the output capacitance. The difference between the analytical result of (65) and the SPICE simulation result is less than 10%. As a result, the analytical expression is still effective for a charge pump with MOS transfer transistors.

## V. Discussion

### A. Determination of the Optimum Number of Stages

The self-load capacitance $C_{\text{pump}}$ is almost constant for a given circuit area which is proportional to the total charge pump capacitance $NC$. The output series resistance of the charge pump, $R_{\text{pump}} = N/C$, increases as the square of the number of stages $N$ in case of a given circuit area because the charge pump capacitance $C$ is inversely proportional to the number of stages. On the other hand, the maximum output voltage $V_{\max} = (N+1)V_g$ proportionally increases with the number of stages. As a result, there will be an optimum number of stages to minimize the rise time.

If the self-load capacitance of the charge pump $C_{\text{pump}}$ is set to be just one-third of the total charge pump capacitance $NC/3$ under the condition of a given circuit area

$$T_r \propto x^2 \ln[1 - 1/x] \quad (48)$$

where $x$ is $N/N_{\min}$. $N_{\min}$ is $(V_{\text{pp}} - V_g)/V_g$, which represents the minimum value of the number of stages necessary for a given parameter set of a supply voltage, threshold voltages of the transfer diodes, and a boosted voltage, so that the optimum

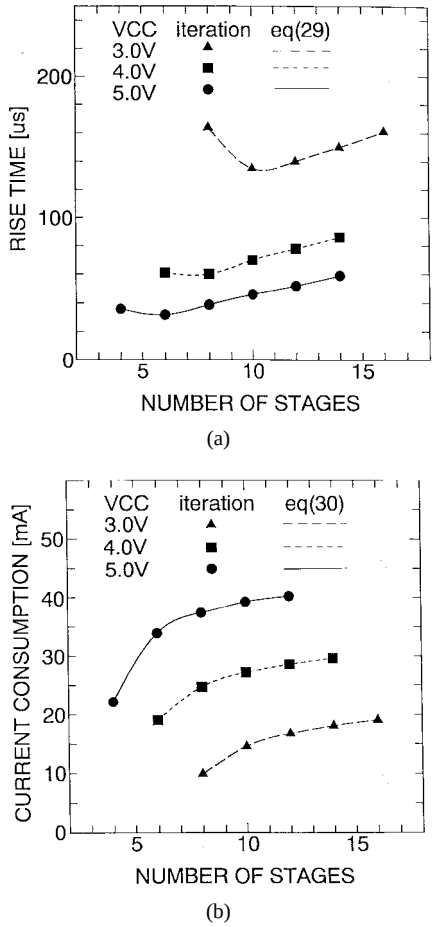



Fig. 11. Dependence of the (a) rise time and (b) current consumption on the number of stages under the condition of a constant circuit area $CN = 1$ nF and $V_{\rm pp} = 20.0$ V, $V_t = 0.6$ V, $T_C = 100$ ns, and $C_{\rm out} = 10$ nF.

number of stages to minimize the rise time $N_{\rm opt}$ is given by

$$N_{\rm opt} = 1.40 N_{\rm min}. \tag{49}$$

Fig. 11 shows the rise time and the current consumption under the condition of a constant circuit area. The rise time proportionally increases with the number of stages in case of a large number of stages. On the other hand, the rise time will be infinite in case of a number of stages as small as $N_{\rm min}$. As a result, there is an optimum number of stages in any case. The current consumption increases with the number of stages, so that a charge pump with an excessive number of stages increases not only the rise time but also the current consumption.

Fig. 12 shows the dependence of the optimum number of stages on the boosted voltage. The analytical expression represented by the continuous line agrees with the iteration method represented by the discrete dots. The optimum number of stages proportionally increases with the boosted voltage, as represented by (49).

Fig. 13(a) shows dependence of the optimum number of stages on the supply voltage. The optimum number of stages increases as the supply voltage decreases. As mentioned above, an increase of the number of stages results in an increase of the current consumption. Fig. 13(b) shows the total capacitance $C_{\rm tot} \equiv CN$ and the current consumption which are necessary

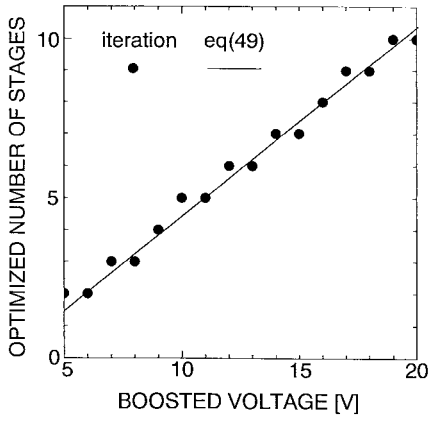



Fig. 12. Dependence of the optimum number of stages on the boosted voltage under the condition of a constant circuit area and $V_{\rm cc} = 3.0$ V, $V_t = 0.6$ V.

for a constant rise time of 63 $\mu$s. The circuit area and the current consumption at a supply voltage of 2 V are 17.9 and 5.1 times larger than those at 5 V, respectively.

### B. Power Consumption and Efficiency

The power consumption $P_{\rm in}$, the output power $P_{\rm out}$, and the power efficiency $R_{\rm power}$ during boosting are defined as

$$P_{\rm in} \equiv \sum_{j=0}^{T_r} q_{\rm cc}^d(j) V_{\rm cc}/T_r \tag{50}$$

$$P_{\rm out} \equiv \sum_{j=0}^{T_r} q_{\rm out}(j) V_{\rm out}(j)/T_r \tag{51}$$

$$R_{\rm power} \equiv P_{\rm out}/P_{\rm in}. \tag{52}$$

By using (27) for $V_{\rm out}(j)$, (10) for $q_{\rm out}(j)$, and (23) for $q_{\rm cc}^d(j)$, these values can be calculated as

$$P_{\rm in} = (N+1) C_{\rm load}(V_{\rm pp} - V_g) V_{\rm cc}/T_r \tag{53}$$

$$P_{\rm out} = \frac{1}{2} C_{\rm load}(V_{\rm pp}^2 - V_g^2)/T_r \tag{54}$$

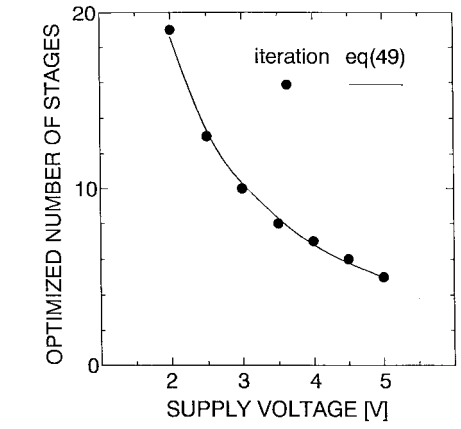
$$R_{\rm power} = \frac{V_{\rm pp} + V_g}{2(N+1)V_{\rm cc}}. \tag{55}$$

The power efficiency during boosting is about half of the power efficiency in steady state, which is given by $V_{\rm pp}/(N+1)V_{\rm cc}$.

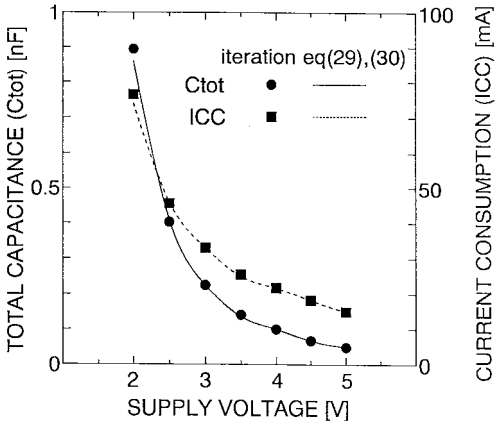
Fig. 13(c) shows dependence of the power consumption and the power efficiency on the supply voltage under the same condition as Fig. 13(b). As a result, not only the circuit area and the current consumption, but also the power consumption increase as the supply voltage decreases, unless the boosted voltage is scaled down according to the difference between the supply voltage and the threshold voltage of the transfer diode.

## VI. Conclusion

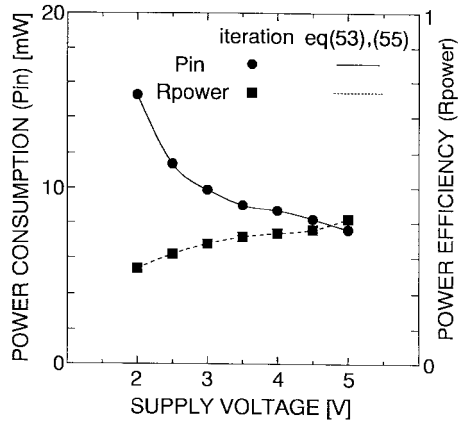
The analytical expressions for the rise time of the output voltage and the power consumption during boosting are derived. By using the analytical expressions, these value can be easily estimated. The optimum number of stages to minimize




(a)




(b)




(c)

Fig. 13. (a) Dependence of the optimum number of stages on the supply voltage under the condition of a constant circuit area and $V_{\rm pp} = 20.0$ V, $V_t = 0.6$ V. Dependence of (b) the total capacitance, $C_{\rm tot} = CN$, and the current consumption on the supply voltage and (c) the power consumption and efficiency under the condition that the rise time at any supply voltage is a constant value of 63 $\mu$s, $T_C = 100$ ns, and $C_{\rm out} = 10$ nF.

the rise time is given by 1.4 $N_{\rm min}$, where $N_{\rm min}$ is the minimum value of the number of stages necessary for a given parameter set of a supply voltage, threshold voltages of transfer diodes, and a boosted voltage. Moreover, the equivalent circuit of the charge pump has been modified by the self-load capacitance of the charge pump, which has been estimated as about one-third of the total charge pump capacitance.

## APPENDIX
## BODY EFFECT OF TRANSFER TRANSISTORS

As discussed in [10], the body effect of transfer transistors should be taken into account in the cutoff condition. The body effect of transfer transistors is expressed by a parameter $\alpha$ as

$$V_s = \alpha(V_d - V_t) \tag{56}$$

where $V_s$ is the source follower voltage, $V_d$ is the voltage applied on the drain terminal which is shorted to the gate terminal, and $V_t$ is the threshold voltage at no back bias [10]. Thus, the following equation should be used instead of (1):

$$Q(1) = \alpha C V_g. \tag{57}$$

Like (6), (7), and (9), the general forms are expressed by

$$Q(2k-1) = \sum_{i=1}^{2k-1} \alpha^i (CV_g - q_{\rm out}) - \alpha^{2(k-1)} q_{\rm out} \tag{58}$$

$$Q(2k) = \sum_{i=1}^{2k} \alpha^i \left( CV_g - \frac{q_{\rm out}}{\alpha} \right) \tag{59}$$

$$Q(N) = C\left( \frac{V_{\rm out}}{\alpha} - V_g \right). \tag{60}$$

Therefore, the output voltage-current characteristic with the body effect of transfer transistors is derived by

$$q_{\rm out} = C\left( \sum_{i=1}^{N+1} \alpha^i V_g - V_{\rm out} \right) \Big/ \sum_{i=1}^{N} \alpha^i \tag{61}$$

which has been derived by Witters *et al.* in [10]. In this case, the recurrence formula for the output voltage $V_{\rm out}$ holds as follow, instead of (26):

$$C_{\rm load}(V_{\rm out}(j+1) - V_{\rm out}(j)) = C\left( \sum_{i=1}^{N+1} \alpha^i V_g - V_{\rm out}(j+1) \right) \Big/ \sum_{i=1}^{N} \alpha^i \tag{62}$$

where the self-load capacitance $C_{\rm pump}$ included in the total load capacitance $C_{\rm load}$ in (62) is expressed by (63), shown at the top of the next page. Using the initial condition of $V_{\rm out}(0) = V_g$, (62) is solved as

$$V_{\rm out}(j) = \sum_{i=1}^{N+1} \alpha^i V_g - \left( \sum_{i=1}^{N+1} \alpha^i - 1 \right) V_g \beta^j. \tag{64}$$

Therefore, the rise time that the output voltage rises from $V_g$ to $V_{\rm pp}$ is

$$T_r = \ln\left[ 1 - (V_{\rm pp} - V_g) \Big/ \left( \sum_{i=1}^{N+1} \alpha^i - 1 \right) V_g \right] \Big/ \ln \beta. \tag{65}$$

If the transistors do not suffer from the body effect, i.e., $\alpha = 1$, (63) and (65) reduce to (21) and (29), respectively.

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$$C_{\text{pump}} = \begin{cases} \frac{1}{(N+1)(1-\alpha^N)} \left[ \frac{\alpha N^2+(N+1)^2-1}{4\alpha} - \frac{1-(N+1)\alpha^N+N\alpha^{N+1}}{(1-\alpha)^2} \right] C & (\text{for even } N) \\ \frac{1}{(N+1)(1-\alpha^N)} \left[ \frac{\alpha(N+1)^2+N^2-1}{4\alpha} - \frac{1-(N+1)\alpha^N+N\alpha^{N+1}}{(1-\alpha)^2} \right] C & (\text{for odd } N) \end{cases} \tag{63}$$

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