

MAURICIO MONTANARES SEPÚLVEDA
BSc Engineering

Test and characterization of a multichannel ASIC for reading signals generated by SiMP detectors



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Abstract

The development of integrated circuits is a complex task. This task can be divided into three major areas: design, manufacture, and verification. In the context of Professor Ángel Abusleme's research, the master's student Renzo Barraza has designed and shipped to manufacture a chip that aims to read 4 SiPM (Silicon Photomultiplier, SiPM, Multi-Pixel Photon Counters, MPPC) in parallel. If the configuration of these detectors is correct, they can detect individual incident photons on their surface. Hoping the designed chip can be tested with real detectors in the future and then be used in particle physics experiments requiring the reading of photomultipliers of silicon (SiMP / MPPC). The chip manufacturer has already and now corresponds the process of characterizing it and checking its operation. That is the test and verification process of the post-silicon circuit (post-silicon validation).

Because there are currently no solution-specific tests for this ASIC (Application Specific Integrated Circuit); This work proposes the design, test and validation of an embedded platform that will allow the characterization and verification of the chip functionalities. This test platform should allow the chip and detectors to be configured correctly and also, this verification circuit should permit to control chip inputs and outputs when needed, as well as be able to record the data from these outputs.

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1

Introduction

1.1 Integrated Circuits

When I discovered the world of integrated circuits (IC), how these work and how they are made, this blew my mind, and it's not for the complexity of the design and fabrication process. It was the fact that these things work!

An integrated circuit consists of a single-crystal chip of silicon, containing both active and passive elements and their interconnection (Millman and Halkias, 1972).

These chips (and their internal elements) are mounted entirely on a semiconductor material. You can have both active and passive 'ingredients' on a single chip, but these days the number of active components (transistors) is the significant majority on an integrated device.

In the late 1950s was conceived the idea of placing multiple electronic devices on the same substrate. In 60 years, the technology has evolved from producing simple chips containing a handful of components to fabricating flash drives with one trillion transistors and microprocessors comprising several billion devices (Razavi, 2005).

CMOS (Complementary Metal-Oxide Semiconductor) technology is the base of these devices, and the design of these circuits depends on the type of

circuit. They are two big categories: digital circuits and analog circuits (and the mixture of these two called mixed signal circuits). Each of these groups has a different technic of design. Perhaps you also have two big categories of design: analog design and digital design (and the mixture of these two called mixed signal design).

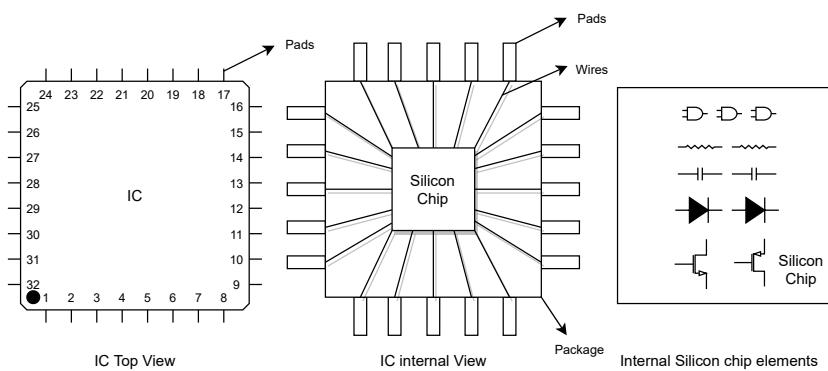


Figure 1.1: Integrated Circuit, different points of view

1.1.1 About the design of IC's

The proliferation of consumer electronics has been a driving factor in advancing integrated circuit (IC) design towards increasingly complex circuits and ever-smaller process technologies. The move towards design complexity has been aided by a mature and widely available set of Electronic Design Automation (EDA) tools in the digital domain. To take advantage of these tools circuit functions (e.g., signal processing) are implemented in the digital environment whenever possible (Galdames, 2021).

Analog and Digital integrated circuits (and also Mixed-signal) start from a top-down approach. Fig. 1.2 presented this graphically.

Three levels of abstraction can be readily identified during the design process (Galdames, 2021):

- The system-level, where system specifications are set, and functional blocks are identified.
- The circuit level, where circuit schematics are designed for each functional block.
- The layout level, where the circuit layout for all the functional blocks is designed, followed by floorplanning, placement, and global routing to generate the layout of the entire system.

After the design process, a next-level called *Post Silicon* arrives. At this level, the circuit, after manufactured, needs to be tested. The post-layout simulations are helpful to have an expected result in the post-silicon test. If this step fails, the IC is not ready for real-world applications, and the issues need to be identified (and corrected if possible). This Thesis concentrates on this stage and will be described a methodology for post-silicon verification for an ASIC(Application Specific Integrated Circuit).

1.1.2 About the fabrication of IC's

Fabricate an integrated circuit is complex and has many steps. This Thesis aims not to go deep into the Fabrication process of IC's; for that, we only will do a high-level overview of this process.

The fabrication of an Integrated Circuit (IC) it's a high-tech process. This process consists of a series of steps in which layers of the chip are defined through photo-lithography. The construction of an IC is based on layers of

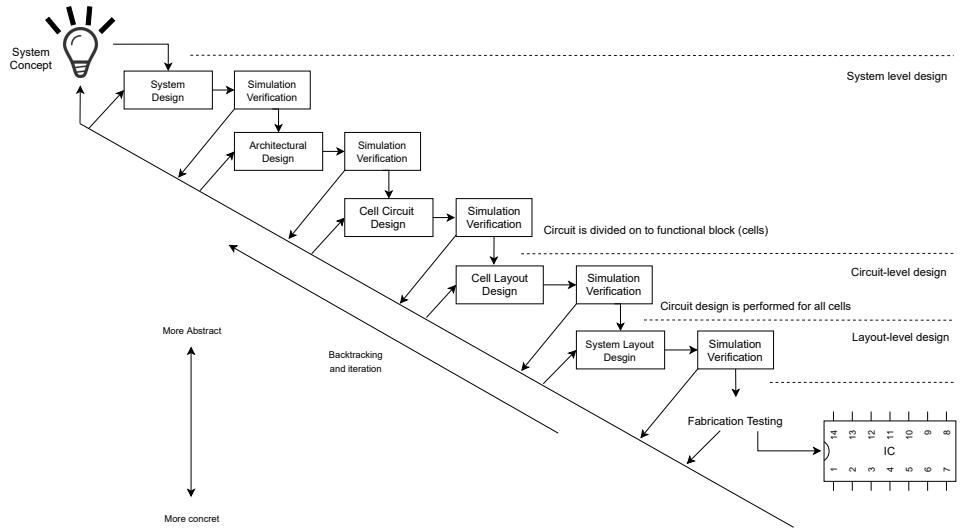


Figure 1.2: High-level view of the analog or mixed-signal design flow (Millman and Halkias, 1972; Galdames, 2021)

semiconductors, coppers, and other interconnected materials to form resistors, transistors, and other components. Transistors are fabricated on thin silicon wafers that serve as a mechanical support and an electrical common point called the substrate (Uyemura, 2012). For example, a cross-section view of a CMOS inverter is in Fig. 1.3. This image shows the different layers like n+ diffusion, p+ diffusion, polysilicon, metal, and silicon oxide. The fabrication consists of printed elements above the p-substrate(wafer) using different layers and interconnects these elements with metal.

In this diagram (Fig. 1.3), the inverter is built on a p-type substrate. The

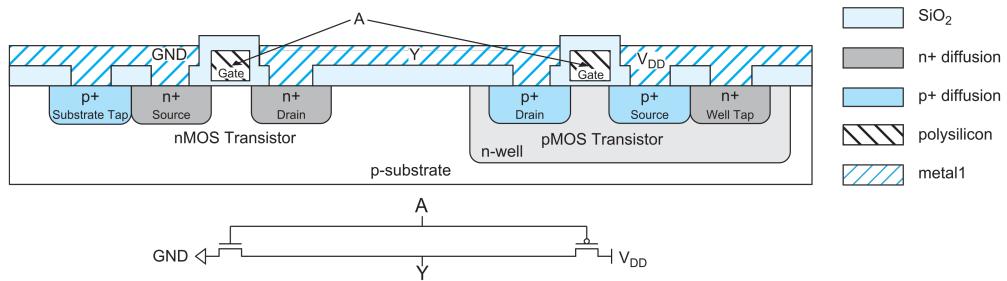


Figure 1.3: Inverter circuit. Cross-section view and schematic (Uyemura, 2012)

pMOS transistor requires an n-type body region, so an n-well is diffused into the substrate in its vicinity. The inverter could be defined by a hypothetical set of six masks: n-well, polysilicon, n+ diffusion, p+ diffusion, contacts, and metal.

Building another element (active or passive) can be done with the same process but with different steps. The lithography permits create a high level of complex IC's, and the cost is efficient. That is the reason why this process is the standard in the Silicon industry. (Razavi, 2005)

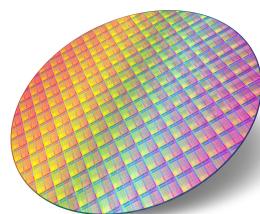


Figure 1.4: Silicon Wafer(p-substrate). Courtesy of WaferWorld

1.2 The verification process of IC's

In standard industrial practice today, analog, digital and mixed-signal circuits are still essentially verified based on repeated-simulations methodologies.

Verification is classified into two principal clusters depending on the moment when the verification is done: pre-silicon validation and post-silicon testing and test generation (Gielen et al., 2019) .

It is crucial to make a distinction between verification levels (pre-silicon and post-silicon):

- The pre-silicon design validation, which focuses on validating the correctness in the functionality of a design (Nahir et al., 2010).
- Post-silicon test generation, which focuses on verifying the correctness in the functioning of a fabricated (sub)system (Nahir et al., 2010).

1.2.1 Pre-silicon verification

If we examine Fig. 1.2 , it is possible to see different steps of verification. These stages are essential after every design step because it is crucial to detect all the possible problems after the fabrication process.

Simulation and verification steps are performed at each level to account for undesired effects (e.g., layout parasitics) and detect potential problems. If the design fails to meet specifications at some point in the design flow, redesign iterations are performed (Galdames, 2021).

Analog, Digital, and Mixed-signal circuit verification at design time can broadly be categorized into two approaches: formal methods and simulation-

based techniques. These approach are described bellow, and are based on (Gielen et al., 2019).

- Formal methods attempt to validate in some formal manner if the designed circuit is satisfying the correctness constraints. They typically step away from physics-based AMS (Analog/mixed-signal) simulations try to work at a higher level of circuit abstraction, as this can lead to a significant speed-up in design validation time, be it that they can suffer from inaccuracies due to this abstraction.
- Simulation-based techniques, on the other hand, start from the physics of the devices within the circuit and validate the design by sampling its performance through simulating the circuit several times under different inputs and conditions. This has the benefit that it takes many more physical details into account. However, since these simulations are time-intensive, this comes at the cost of an extensive validation time. In addition, the limited set of simulations carried out does not guarantee formally that the design is correct under all circumstances.

These days exist dedicated software for simulate and verified every step of the design process. The industry typically uses simulation-based validation as the default method.

This industry extended process has the benefit that the circuit is represented very reliably (up to the precision of the device models used and the parasitics incorporated in the netlist). However, the downside is that the simulation time can be excessively long, especially for transient simulations or simulating for time-dependent reliability (Gielen et al., 2019).

1.2.2 Post-silicon validation

Later the manufactured process is ready (Fig. 1.2), a new verifying stage is crucial to be sure of the correct functionality of the IC. This stage is denominated post-silicon validation. See the Fig. 1.5

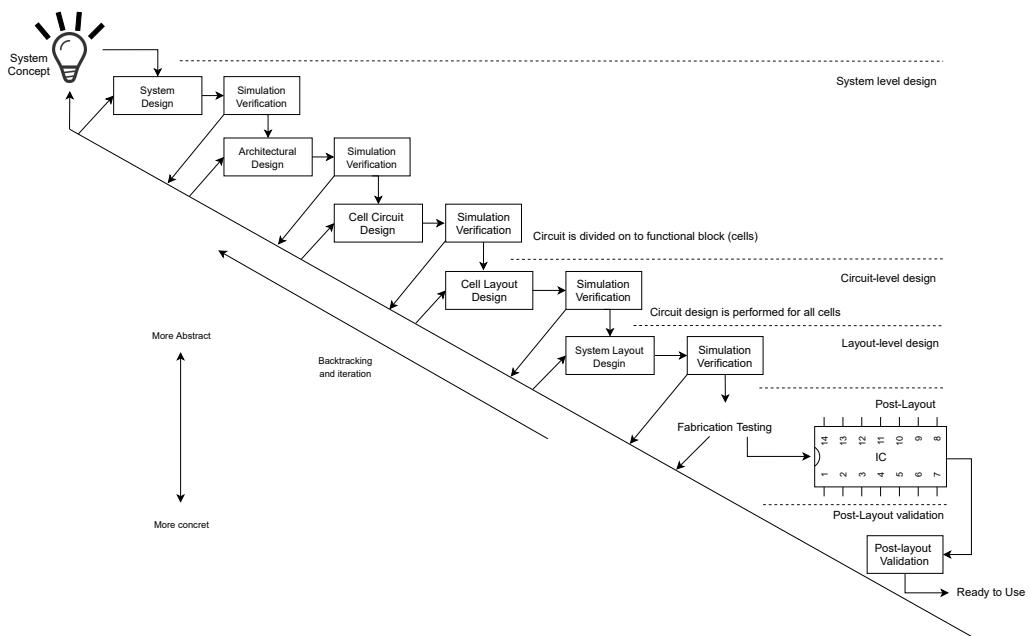


Figure 1.5: High-level view of the analog or mixed-signal design flow and Post-silicon validation stage context

Post-silicon validation involves operating one or more manufactured chips in actual application environments to validate correct behaviors over specified operating conditions. The objective is to ensure that no bugs escape to the field (Mitra et al., 2010).

Validation (post-silicon) has significant overlap with pre-silicon design

verification and manufacturing (or production) testing. Traditionally, most hardware design bugs are detected during pre-silicon verification and manufacturing defects are targeted by manufacturing testing.

While both manufacturing testing and pre-silicon verification continues to be essential. Post-silicon validation is becoming extremely necessary because of several unique aspects. These aspects are showed in Table 1.1 and are based on Mitra et al. (2010).

Table 1.1: Why post-silicon validation?

Reasons why post-silicon validation is fundamental	
1	We cannot rely on pre-silicon design verification alone to detect all design bugs. Simulation is several orders of magnitude slower than actual silicon. Formal verification is very useful for certain situations, such as the verification of individual arithmetic units or protocols, it faces scalability challenges for full chip-level verification. Hence, bugs that escape pre-silicon design verification are often detected during post-silicon validation.
2	In advanced technologies, several interactions between a design and the electrical state of a system are becoming significant, e.g., signal integrity (cross-talk and power-supply noise), thermal effects, and process variations. Such interactions can result in incorrect behaviors and are often referred to as electrical bugs. Accurate modeling of all these physical effects is usually very difficult during pre-silicon design verification.
3	Unlike manufacturing defects, post-silicon bugs may be caused by subtle interactions between a design and physical effects (the so-called electrical bugs) or by design errors (the so-called logic bugs). It may be very difficult to create accurate and effective fault models for such bugs.
4	Unlike manufacturing testing, where the primary objective is to detect defects, post-silicon validation involves localizing, root causing, and fixing bugs. Bug localization generally dominates post-silicon validation effort and costs.

Pre-silicon verification and post-silicon validation environments have fun-

damentally different characteristics.

Simulations at the pre-silicon levels are highly controllable, repeatable, observable, and hence easy to debug. On the other hand, it is maddeningly slow, limiting the depth and breadth of coverage that can be achieved even with farms of high-performance compute servers. Post-silicon validation is almost the inverse - extremely fast, but with very coarse controllability, uncertain reproducibility, very limited observability, and is very difficult to debug. The lack of controllability and observability makes it challenging to get meaningful coverage data with which to implement a coverage directed validation methodology (Nahir et al., 2010).

These differences are recapitulated and exhibit in Table 1.2. It should also be considered that post-silicon validation also suffers from platform stability and electrical and circuit issues, increasing the problem.

Table 1.2: Pre-silicon vs Post-silicon

Pre-silicon verification	Post-silicon validation
Observable	Very limited observability
Highly controllable	Coarse controllability
Repeatable	Problematic reproducibility
Easy to debug	Difficult to debug
Slow(simulation)	Extremely fast

While many methods and tools have been developed and are widely used in industry to both formally validate and automatically generate tests (ATPG) for digital subsystems, the AMS(Analog/mixed-signal) verification tools are lagging (Guo et al., 2015).

This Thesis is focused on an analog/mixed-signal ASIC and its verification. The inherent obstacles of verifying analog circuits lie in the facts that

(Gielen et al., 2019; Nahir et al., 2010):

- There is no practical or commonly used method to formally describe their function, whereas commercial simulators are used extensively in all design steps.
- The performance of analog circuits is parametrically sensitive to all kinds of inequalities (process, supply, temperature, aging), which makes their verification complex.
- The influence of fabrication defects on analog circuit functionality is less predictable.

Pre-silicon tools give better control over the corners we want to hit. This control is not there in post-silicon tools. Presently it is tough to measure our coverage in post-silicon validation. Moreover, these methods are based on the assumption that we know all the paths we want to cover in the hardware, which we do not. We require developing and implementing the stimuli available in pre-silicon for the post-silicon experiments (Nahir et al., 2010).

It is seldom to see a unified plan for verification and validation (especially on AMS). We need to act on specifics parts of the circuit that need to be tested. When and how to do it.

We can propose an easy and high-level view example: Suppose a chip, this device was stimulated in post-layout simulations with some known inputs, and the chip outs were collected. These data were checked for the designer, and the behavior of the circuit accomplishment the design specifications. So the circuit will be fabricated.

Once the chip fabrication is ready, it's the moment to do a Post-silicon test. Recreated(in real life) the original stimulus (used in post-layout simulation) and use these signals for stimulus the chip inputs. The outs(in Post-silicon test) can be measured and compared with the data collected from the releases in the post-layout simulation. See the Fig. 1.6

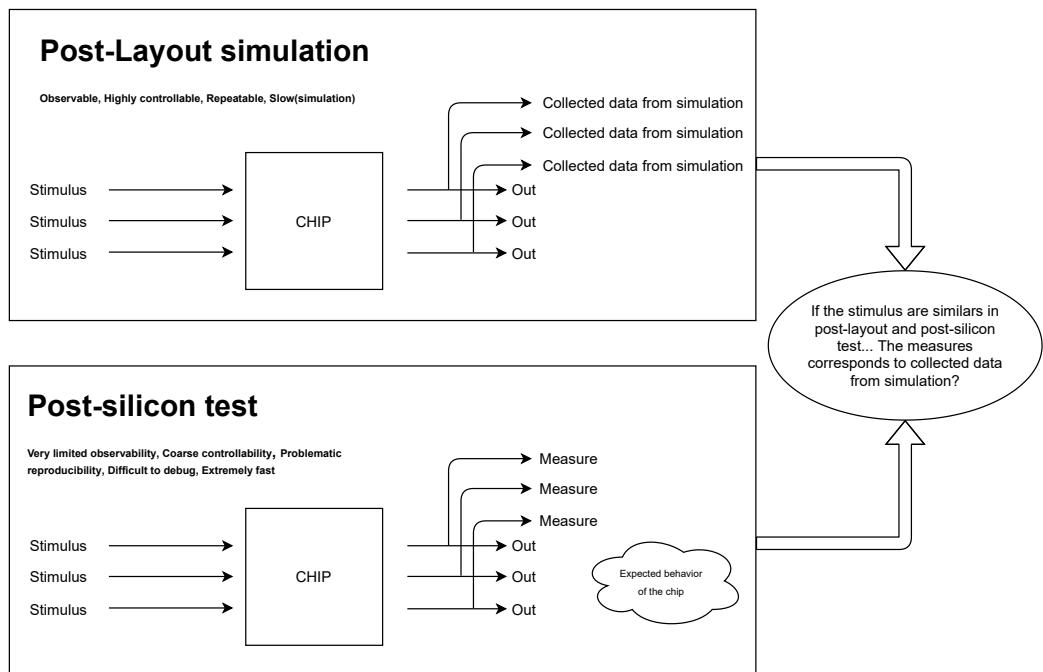


Figure 1.6: High-level example view of Post-silicon test

1.3 About the Silicon Photomultipliers

Silicon photomultipliers (Silicon Photomultiplier, SiPM, Multi-Pixel Photon Counters, MPPC) are detectors consisting of multiple p-n silicon junctions that, when polarized with voltages close to their breakdown voltage, can detect individual photons incident on their surface (Altamirano, 2021). As stated in Sadygov et al. (2006), a silicon photomultiplier is a monolithic

solid-state photodetector composed of an array of hundreds or thousands of photodiodes put in parallel. These are independent of each other and are connected to a common read node (fast output).

The primary elements of the SiMP are called pixels (photodiode, see Fig. 1.7b). In the case of the SiMP model "MICROFCSMTPA-10010-GEVB" (ON (2021)), this device is formed of a large number (hundreds or thousands) of microcells. Each microcell is an avalanche photodiode with its own quench resistor and a capacitively coupled fast output. Fig. 1.7a.

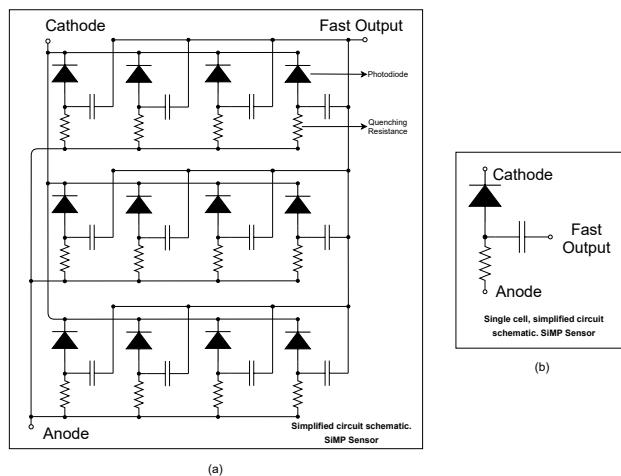


Figure 1.7: (a) Simplified circuit schematic of SiMP. (b) Single cell, simplified circuit schematic. SiMP Sensor. (ON (2021)).

1.3.1 Operation mode

When a photon arrives at the detector, activate some pixels, and if a pixel is activated (for an incident photon), the pixel produces a signal out. Each pixel of the MPPC produces the same out amplitude when a photon is detected. A representation of this is shown in Fig. 1.8.

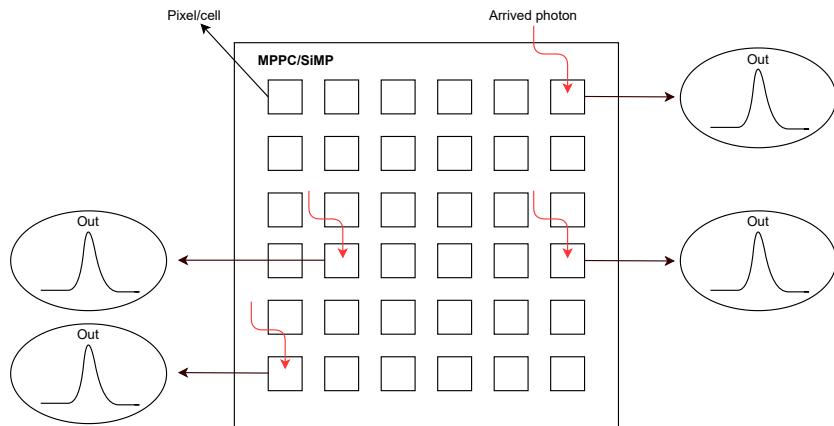


Figure 1.8: A high-level view of MPPC, arrived photons and pixel's outs (HAM, 2021).

And what happens if more than one photon arrives at the same time? In this scenario, the pixel's output signal will be the same as that for one photon, but the amplitude of the MPPC output will be the sum of the individual cell signals.

Fig. 1.9 shows output pulses from the MPPC obtained when it was illuminated with the pulsed light at photon counting levels and then amplified with a linear amplifier and observed on an oscilloscope. As can be seen from the figure, the pulses are separated from each other according to the number of detected photons such as one, two, etc (HAM, 2021). Measuring the height of each pulse allows estimating the number of detected photons.

1.3.2 Performance of MPPC's

It is not the focus of this Thesis to go deeper into MPPC/SiMP features, but there are some crucial details(performance considerations) to keep in mind.

The bibliography (Shen, 2012; Gomi et al., 2007; Sadygov et al., 2006)

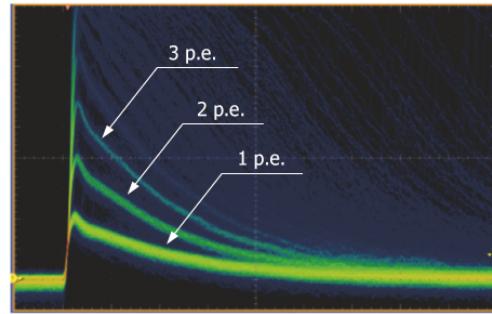


Figure 1.9: Pulse waveforms when using a linear amplifier (HAM, 2021).

usually uses some terminology for reference to the performance issues of the MPPC. Some of these characteristics are: photon detection efficiency (PDE), dark count rate (DCR), single-photon timing resolution (SPTR), after-pulse, and cross-talk probability, as well as their temperature coefficient

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2

A short introduction to the custom ASIC for reading SiMP detectors

The chip is a multichannel ASIC and has four analog channels with four outputs each. Of these four outputs, 3 are analog signals, and one is digital.

Renzo Barraza has designed a chip that aims to read 4 SiPM (Silicon Photomultiplier, SiPM, Multi-Pixel Photon Counters, MPPC) in parallel. If the configuration of these detectors is correct, they can detect individual incident photons on their surface.

2.1 Description and features of the ASIC

This IC can read 4 SiMP detectors in parallel, process these measurements internally, and through 4 outputs (3 analog and one digital), deliver information on the number of photons that arrived at each detector. The number of photons that arrived at the detectors must be extracted from the analog and digital signals (chip outputs). These estimates and their methods are described in detail in section 3.2.

Some relevant characteristics of the ASIC:

- The chip has four analog channels for 4 MPPC (SiMP) detectors.

A short introduction to the custom ASIC for reading SiMP detectors

- Each analog channel has an 8-bit DAC, which allows the user of the readout circuit to fine-tune the gains of the SiPM by adjusting its bias voltage, in addition to compensating for the dark noise mentioned in chapter (Altamirano, 2021) . Due to the limitations of CMOS technology, the maximum voltage that can be delivered is close to 1.8V (relative to ground). This limitation prevents the Chip itself from being able to directly bias the MPPC detectors.

Fig. 2.1 is a graphical summary of these points.

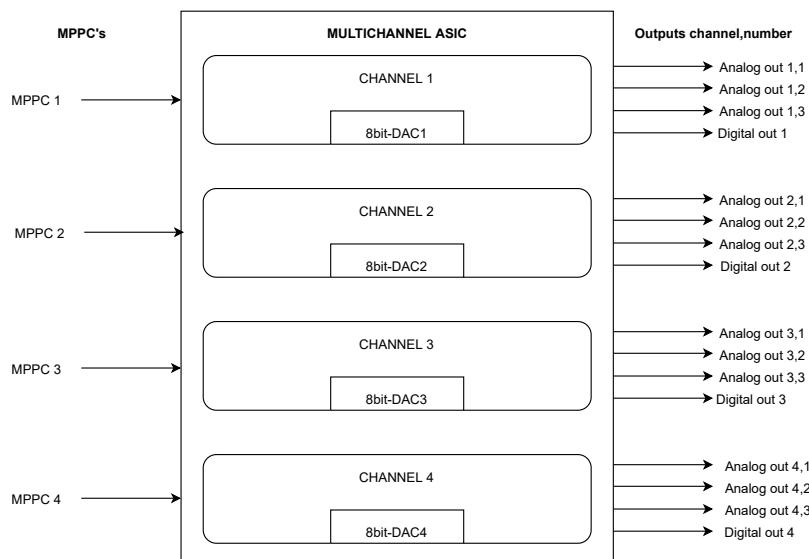


Figure 2.1: ASIC high-level overview

2.2 Inputs and on-chip signal processing

The chip has four analog inputs and four outs, three analogs and one digital output. In details:

This ASIC has four channels, and each channel has one analog input. Those inputs are connected to the MPPC's, and when photons arrive at the detectors, a flow of charge is produced and the chip reads this current using a specific circuit.

The reading circuit for the SiMP detectors corresponds to an open-loop transimpedance amplifier (TIA) type circuit, which the chip designer justifies based on the objectives proposed in the thesis presented by R. Barraza (Altamirano, 2021).

A high-level circuit representation of the above is shown in Fig. 2.2, where "-HV" is a high negative voltage, and it is used to polarize the detectors.

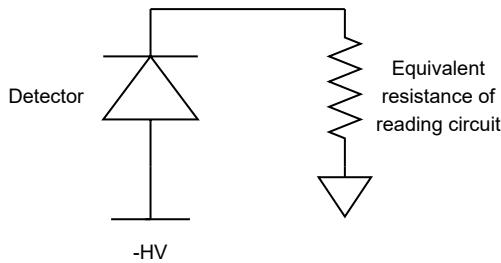


Figure 2.2: Read out circuit representation (Altamirano, 2021)

Employing the TIA is possible to read the flow of charge (coming from the detector, drift current), and after processing the voltage output signal of the TIA (Fig. 2.3). Using the voltage output is possible to obtain information about how many photons arrived at the detector. The methods for doing that are described in section 3.2

2.2.1 Post-TIA Processing

Once the TIA has read the signal, two things must be measured:

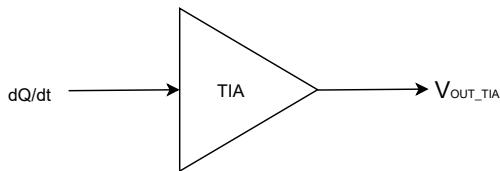


Figure 2.3: Transimpedance Amplifier (TIA)

1. The instant the charge is received.
2. Number of pixels activated in the detector.

To know the first one, the designer of the chip decided to implement a discriminator circuit. This circuit is activated when the voltage signal produced by the TIA indicates that one or more pixels have been triggered/activated in the detector. The output of the discriminator, therefore, delivers a digital signal (on/off transition) and this signal lasts as long as the MPPC continues to provide current. The information supplied by the discriminator can be used to know the number of pixels activated in the detector. Additionally, the designer decided to implement an extra circuit block to improve the results. This new circuit is an integrator circuit, and its purpose is to integrate the output voltage signal of the TIA. The information that provides this block can be added to that already delivered by the discriminator to read more accurately the number of activated pixels (Altamirano, 2021).

A representation of the internal component of each of the four channels is shown in Fig. 2.4 and shows that the signal produced by the SiMP connects to the VIN_TIA_EXT node. The potential of this node can be altered due the voltage produced by the DAC of the channel(four channels, and each channel has one DAC). This DAC is capable of doing a fine-adjusting of the SiPM bias voltage (with the limitations of CMOS technology explained in

section 2.1)

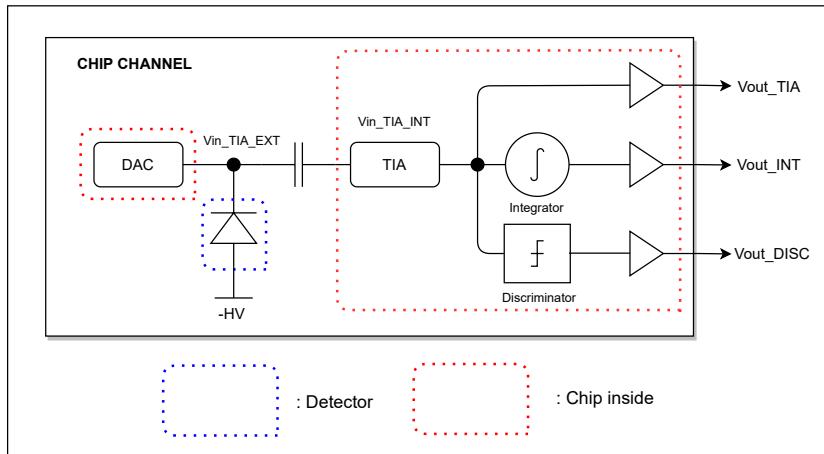


Figure 2.4: Internal components of each of the four channels in the ASIC (Altamirano, 2021).

2.3 Description of the chip outputs

The chip for each channel has four outputs:

- $V_{OUT_INT_DER}$ and $V_{OUT_INT_IZQ}$: These are the differential outputs of the integrator (V_{OUT_INT} in the figure). This output is used to identify few triggered pixels.
- V_{OUT_TIA} : Direct output of the TIA. It is employed to identify a number greater than hundreds of triggered pixels.
- V_{OUT_DISC} : It is the output of the discriminator. It serves to identify the moment when a signal arrives from the SiPM and can also be used to identify a neighborhood bounded by triggered pixels.

These points are based on the description of the outputs given by the designer of the ASIC in (Altamirano, 2021). In Fig. 2.4, it is possible to observe the outputs of one channel.

3

Post-layout simulations and estimation methodologies for counting photons using the ASIC

In Fig. 1.2, the last verification step is called post-layout verification. At this stage, the designer did appropriate simulations based on the problem specification described on chapter 2. These simulations were used to estimate the number of photons arrived at the detector and the time of this event. For this, the designer of the chip used methods that will be described in this chapter.

3.1 Post layout simulations

Using software and some techniques described in section 1.2, the designer simulates some conditions for validating the behavior of his circuit. The ASIC is designed to be capable of two main things: estimate the number of photons arrived at the detector and the time of this event.

To do these two things, simulated the arrival of photons is necessary. So, how to do that?

3.1.1 Single-photon arrival simulation

The author of the circuit used as an input signal a current pulse of 0.1ns with an amplitude of $4mA$. This, because the electrical charge delivered by said current pulse is equivalent to the charge delivered by 1 pixel triggered in the *Hamamatsu S14160-3050HS* detector.

The aforementioned current pulse was used for stimulating the channels of the ASIC. The response of the circuit and the outs are exhibited in the figures 3.1, 3.2 and 3.3.

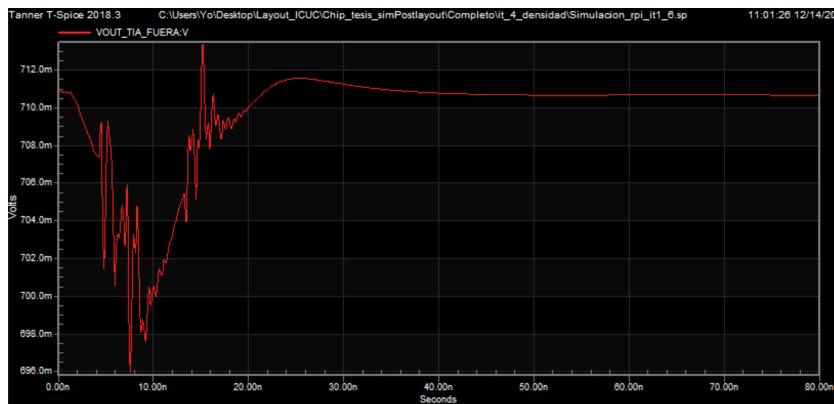


Figure 3.1: TIA Out for one pixel activated (Altamirano, 2021)

3.1.2 Multi-photon arrival simulation

The current pulse used for simulating the arrival of one photon is linearly scaled for simulating more arrival photons (more pixels activated). This linearly scaled affects just the signal's amplitude, but the duration of this signal is equal for every quantity of simulated photons (Table 3.1).

For example, to simulate the activation of two pixels of the detector (MPPC/SiMP), the current pulse will be a pulse of 0.1ns with an ampli-

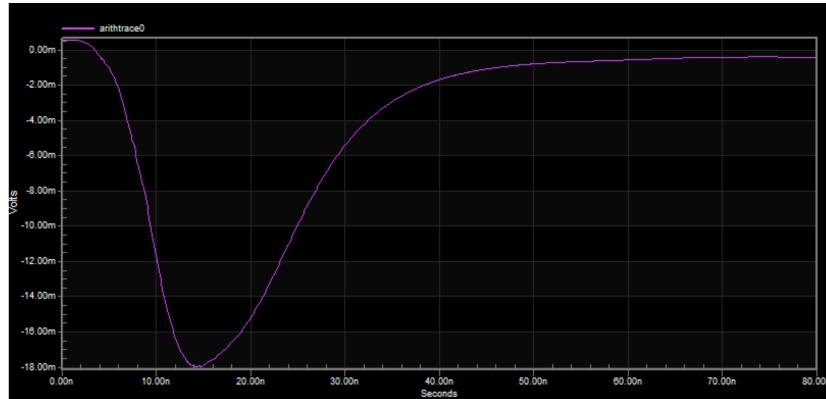


Figure 3.2: Integrator Out fo one pixel activated (Altamirano, 2021)



Figure 3.3: Discriminator Out for one pixel activated (Altamirano, 2021)

tude of $8mA$. In the case of simulating the activation of four pixels, the current pulse will be a pulse of $0.1ns$ with an amplitude of $16mA$. And so on. Table 3.1, Fig 3.4 and Fig 3.5 summarize this.

The third column of Table 3.1 shows the equivalent charge for a pulse of $0.1ns$ with this correspondence amplitude. That data will be necessary for the next chapters.

Generate a pulse whit the values of amplitude and duration of $0.1ns$ can be challenging. Nevertheless, it is possible to produce a pulse that the

Table 3.1: Pixels, Current and Charge relation

Pixels	Current[mA]	Charge[q]
1	4	4E-13
2	8	8E-13
3	12	1.2E-12
4	16	1.6E-12
5	20	2E-12
6	24	2.4E-12
7	28	2.8E-12
8	32	3.2E-12
9	36	3.6E-12
10	40	4E-12
...
1000	4000	4E-10
...
2000	800	8E-10
...
3000	12000	1.2E-09

integration area will be equivalent to the equivalent charge for n number of pixels, following the current equation 3.1.

$$\frac{dQ}{dt} = C \frac{dv}{dt} \quad (3.1)$$

3.2 Chip signal reading. How to read/interpret the analog outputs of the chip?

On Altamirano (2021), two methodologies are mentioned to measure the outputs and estimate the number of activated pixels. We will refer to these as:

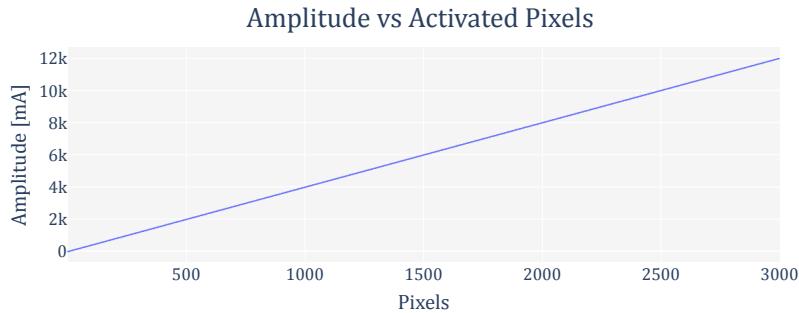


Figure 3.4: Current Amplitude vs activated pixels.

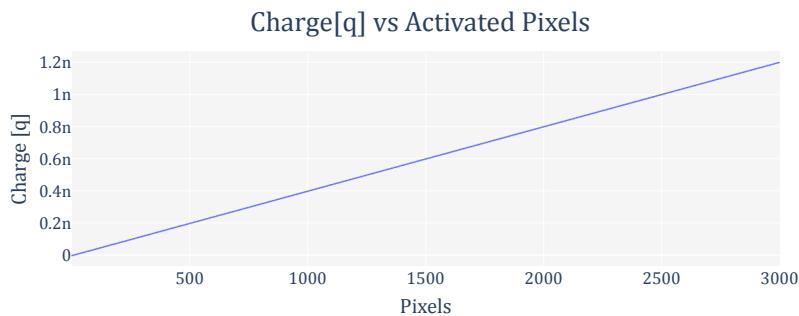


Figure 3.5: Charge vs activated pixels.

1. Peaking time approach
2. Maximum amplitude approach

3.2.1 Peaking time approach

This approach has two stages: calibration and measurement. Calibration is done with just one pixel activated ($N = 1$). At this point, a time difference Δt is measured between the moment of the discriminator trigger (V_{out_DISC} transition on / off) and the moment of maximum amplitude (*peaking time*) of the V_{out_INT} output for one activated pixel. The next measurements (when N increase) will be performed with the same *peaking time* measured

in the calibration stage ($N = 1$). It is essential to mention that for a small N , therefore a low amplitude input signal, this method works well, but as N increases, the transistors leave their region of linearity, which will cause imprecision in the measurement of the valid maximum of the V_{out_INT} signal Altamirano (2021). This approach can be seen in the following Fig 3.6.

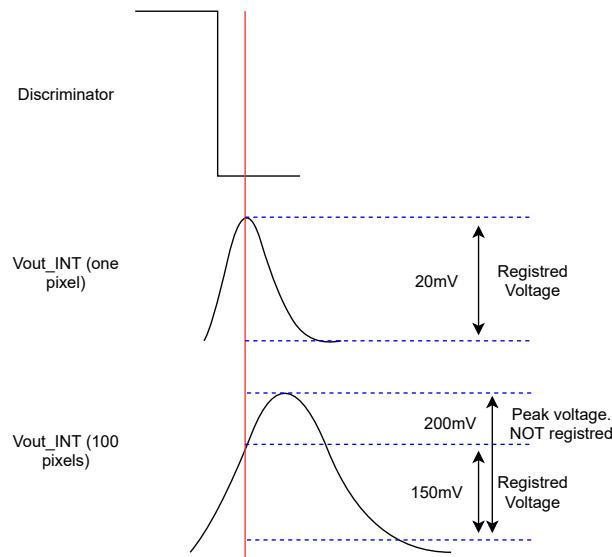


Figure 3.6: Peaking time approach (Altamirano, 2021). Voltages on the figure are just referential examples.

3.2.2 Maximum amplitude approach

The second approach is to assume that the user will identify the maximum amplitude of the analog outputs. Therefore the maximum value of said signals is recorded regardless of when this occurs; This approach can be seen in the following Fig 3.7.

In addition to these two methods, it is possible to use the digital signal

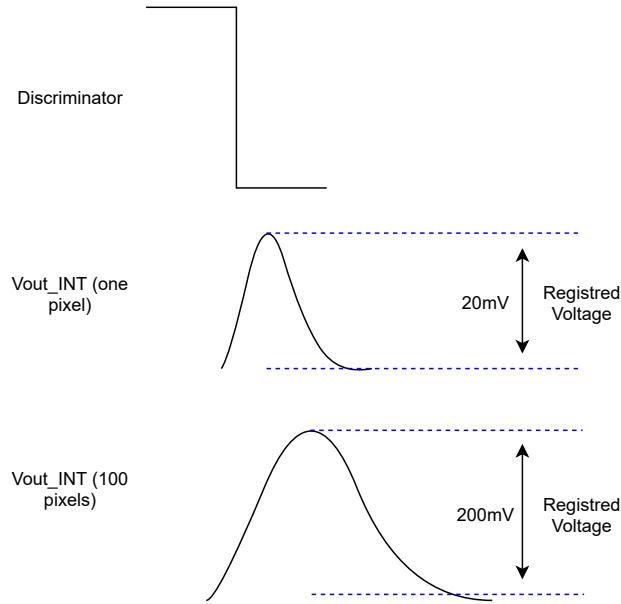


Figure 3.7: Maximum amplitude approach (Altamirano, 2021). Voltages on the figure are just referential examples.

from the discriminator and, depending on the duration of the pulse, estimate the number of pixels triggered using the *Time Over Threshold* method. This method is described in Orita et al.; Bagliesi et al. (2011); Altamirano (2021) and is used in circuits of similar applications. The method consists of relating the duration of the digital pulse with a certain number of activated pixels.

3.2.3 Performance of methodologies

The following Figs 3.8, 3.9 shows the performance of both methodologies when measuring the outputs of the TIA and integrator. Additionally, the duration of the discriminator pulses to identify the number of pixels it is showed in Table 3.2.

The chip designer mentions that based on their results, it can be stated

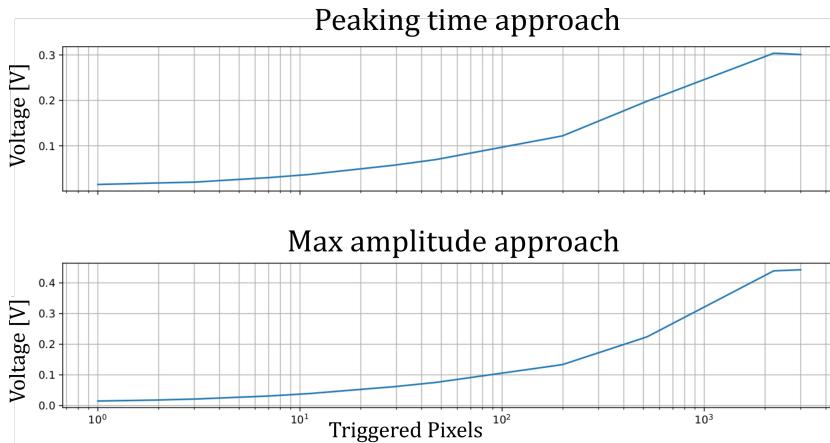


Figure 3.8: Results of the approach. TIA out (Altamirano, 2021).

that: Both measurement approaches of the integrator cannot resolve differences of 1 triggered pixel, but it can resolve differences of 2 triggered pixels. This capacity degrades as more amplitude signals are received from the SiPM. A summary of the ability to resolve multiple pixels using the various analog outputs is provided below and it is summarized on Tables 3.3 and 3.4.

- It should be noted that the TIA data are not reliable with few pixels because there the oscillations caused by the digital buffer abnormally. It is worth recalling that TIA output is intended to deliver information of hundreds or more pixels.
- Based on the data mentioned above, using the *Time Over Threshold* technique to resolve signals of few pixels becomes necessary.

Table 3.2: Duration of discriminator pulses according to number of pixels triggered in the detector

Number of activated pixels	Discriminator pulse duration [ns]
1	11.4
2	17.68
3	21.24
7	31.65
11	38.07
29	54.88
47	65.88
199	>100

Table 3.3: Ability to resolve pixels of the TIA.

Number of triggered pixels in the detector	Resolution capacity of pixels measuring maximum of the signal(max amplitude approach)	Pixel resolution capacity measuring at the moment of maximum signal for 1 pixel (peaking time approach)
1 - 11	2	2
11 - 29	3	3
29 - 47	10	6
47 - 199	10	20
199 - 521	35	100
521 - 2207	250	Not distinguished
2207 - 3000	Not distinguished	Not distinguished

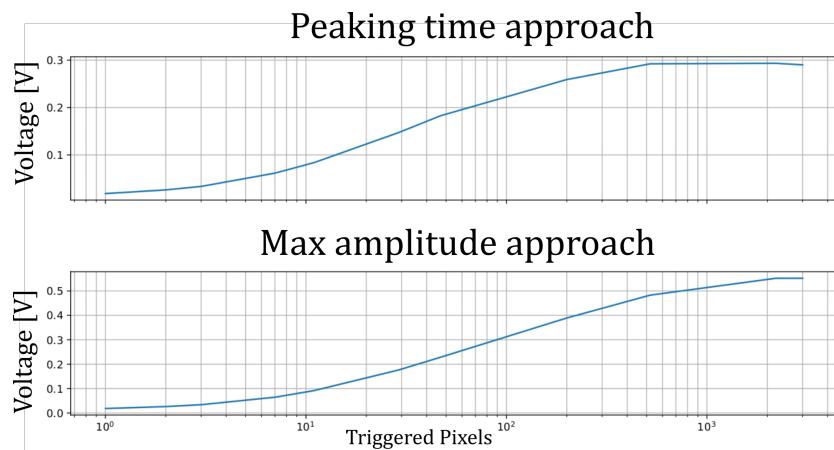


Figure 3.9: Results of the approach. Integrator out (Altamirano, 2021).

Table 3.4: Ability to resolve pixels of the Integrator.

Number of triggered pixels in the detector	Resolution capacity of pixels measuring maximum of the signal(max amplitude approach)	Pixel resolution capacity measuring at the moment of maximum signal for 1 pixel (peaking time approach)
1 - 2	1	1
2 - 3	1	2
3 - 7	1	1
47 - 199	2	2
11 - 29	3	3
29 - 47	4	4
47 - 199	7	8
199 - 521	9	11
521 - 2207	20	40
2207 - 3000	575	Not distinguished

4

Proposed environment for testing the chip

The process of validation and characterization of the chip necessarily requires a suitable test environment. This test environment must have the capabilities to properly condition the circuit to stimulate the inputs and analysis of the outputs. Additionally, the test environment must provide stimulation signals and do a proper registration of the outputs. With the recorded information of the outputs and using the estimation methods described in section 3.2, estimating the number of triggered pixels will be possible. In the practice, this environment will be an specific board with all the necessary elements for the characterization and validation process.

In previous works, Orita et al.; Bagliesi et al. (2011); Galdames (2021) a circuit is designed and printed on a plate, which allows the IC to be correctly conditioned to proceed with the stimulation of the inputs and analysis of the outputs. The ASIC designer proposes as future work the design of a PCB (printed circuit board) to validate and test the ASIC.

The design of this characterization and validation environment is set out below. Details related to the implementation of the methods will be presented in this chapter.

The validation environment must have:

- A negative HV(high voltage) generator for the correct polarization of

the detectors.

- Current pulse generator for stimulating the inputs.
- Mechanisms for the control and reading of analog and digital data that allow the implementation of the pixel estimation methodologies described in the section.

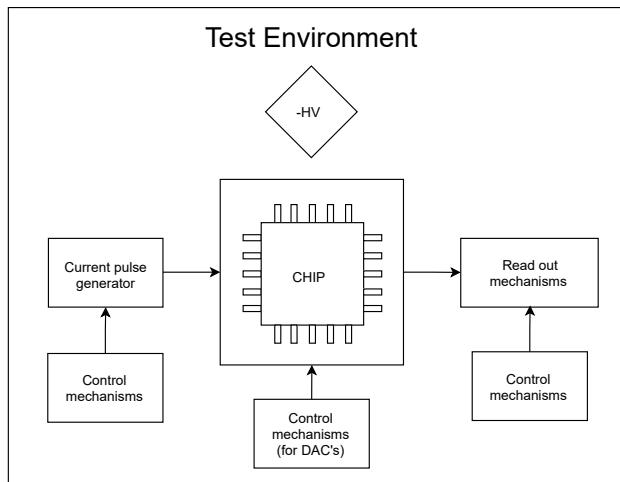


Figure 4.1: Block diagram and high-level view of the test and characterization environment.

4.1 Negative HV generator

A negative HV generator is used for the correct polarization of the detectors. The specifications of the "*MICROFCSMTPA-10010-GEVB*" detectors indicate a reverse bias voltage close to -24V. The PCB must supply this voltage. Based on the specifications of the detector datasheet, this high-negative voltage must be generated by a Charge Pump type circuit.

The Charge Pump (CP) is an electronic circuit that converts the supply voltage VDD to a *DC* output voltage $Vout$ that is several times higher than VDD . Unlike the other traditional $DC - DC$ converters, which employ inductors, *CP* are only made of capacitors and switches (or diodes) [1]. *CP* under specific conditions can also produce a voltage lower than the input voltage, generating a negative voltage.

They are different topologies of charge pump circuits, and the majority of these are based on multiplication stages. The idea behind the behavior of these types of power sources is to use semiconductor elements (diodes or transistors) combined with two complementary control signals to guide the direction of the current connecting and disconnecting different stages of the circuit to produce an increment (or decrements) of the output voltage.

For example, on Tanzawa and Tanaka (1997) the authors analyze the dynamics of a Dickson *CP* circuit. The topology of the circuit doubler voltage is presented in Fig 4.2.

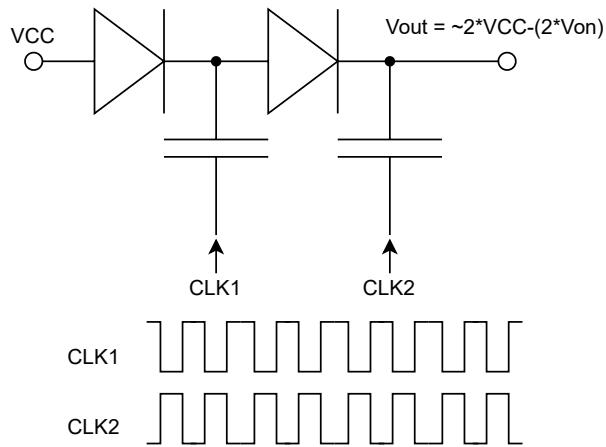


Figure 4.2: Dickson CP, voltage doubler and complementary clock (digital) signals (Tanzawa and Tanaka, 1997).

To improve the results of this topology is recommended to use *Schottky diodes* because the parameter V_{on} is smaller than other diodes(Palumbo and Pappalardo, 2010). It is also possible to use transistors instead of diodes, this is a very popular practice to implement these *CP* sources in integrated circuits.

For example a Dickson charge pump with MOSFET implementation is shown in Fig. 4.3. It is a typical n-stage Dickson charge pump. The input $CLK1$ and $CLK2$ are two out-of-phase clocks with amplitude V_{clk} . These two clocks will increase the potential voltage in capacitors by transferring charges in the capacitor chains through diode-connected MOS transistors. The coupling capacitors will be charged and discharged during each half clock cycle (Lin, 2012a).

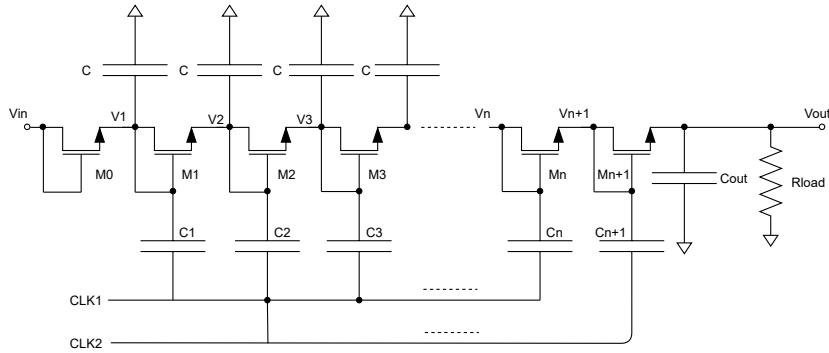


Figure 4.3: A typical n-stage Dickson charge pump (Lin, 2012a).

On equation 4.1 voltage V_t is related to the node voltage of each stage and the voltage difference between the voltages of the nth stage and $(n+1)th$ nodes is given by:

$$\Delta V = V_{n+1} - V_n = V'_{clk} + V_t \quad (4.1)$$

On 4.2 C_s as the stray capacitance at each node and C are the coupling capacitances. The voltage gain V'_{clk} can be express as:

$$V'_{clk} = \left(\frac{C}{C + C_s} \right) V_{clk} \quad (4.2)$$

For an N stage charge pump, the voltage at the output node is as follow:

$$V_{out} = V_{DD} + N(V'_{clk} - V_t) - V_t \quad (4.3)$$

The equation above is the ideal output voltage when there is no output charge and no output current delivered. When the charge pump is connected to an output load, the load current at a clock frequency f , is given by (Lin (2012a)):

$$I_{out} = f(C + Cs)V_L \quad (4.4)$$

V_L is the voltage drop per stage for supplying the load current. Therefore, the output voltage will be reduced an $N \cdot V_L$ voltage. So the output voltage with load will be rewrite as follow (Lin (2012a)):

$$V_{out} = V_{DD} + N \left(\frac{C}{C + C_s} \right) V_{clk} - V_t - \frac{I_{out}}{f(C + Cs)} - V_t \quad (4.5)$$

Equations 4.1 ,4.2 , 4.3, 4.4 and 4.5 are based on Lin (2012a)

This type of circuit is easy to find as integrated circuits, where manufacturers guarantee certain output values for specific conditioning parameters. For example, the LTC3261 is a high voltage inverting charge pump that operates over a wide 4.5V to 32V input range and can deliver up to 100mA of output current, and the output voltage will be $-V_{in}$. Based on the datasheet,

this IC is a good option for implement the HV negative source (Lin, 2012b).

4.2 Current pulse generator for stimulating the inputs

Before using real detectors, the outputs of these sensors must be emulated in such a way as to have control over the timing of the current pulse triggering. Having control over the pulse triggering moment is essential to perform the characterization and validation of the ASIC. To achieve this, a charge generator circuit will be required.

The current signals used in the post layout simulations (Chapter 3) have amplitudes ranging from $4mA$ to $12A$, with a duration of $0.1ns$ for any of the amplitude values in Table 3.1. Current pulses of the same order of magnitude as the signals used in the post-layout simulations (ns) must be generated for testing purposes.

The chip is designed to read charge (and the current associated with this flow of charge), so the fundamental objective will be to generate current pulses where the delivered charge can be related to N of activated pixels using the linear relationship mentioned in section 3.1.2 and 3.1. The chip designer's suggestion will be used as a reference in his thesis to generate this pulse. Using the current equation 3.1 will consist of use one capacitor to generate the charge.

On equation 3.1, we can see that the current in the (ideal) capacitor depends on two factors: C (capacitance of the capacitor) and $\frac{dV}{dt}$. To regulate the current pulse, we must control at least one of these factors.

4.2.1 Different voltage values for charging C

Using electronic keys, it is possible to charge and discharge a capacitor in a controlled way. The capacitor, under certain conditions, must be connected to a voltage V , charged, and therefore generate a current $i = C \frac{dV}{dt}$ (accumulating a charge $Q = CV$, and then discharged to the ground.

To achieve this charge and discharge, two digital signals will be used to control a pair of electronic switches (Mosfets). These transistors will have the function of controlling the charge and discharge of the capacitor.

Figure 4.4(a) shows the circuit at the transistor level where $M1$ and $M2$ are the electronic keys, clk_1 and clk_2 are the control signals, V is the voltage source, C_x is a capacitor in charge of accumulating charge that will be delivered to the chip (R_{chip}), R_{dac} is the equivalent resistance of the internal DAC of the chip channel, C_a is the coupling capacitor mentioned in section 2.3 (Fig 2.4) which must have a value of $1uF$ and R_{Chip} is the equivalent input resistance ASIC (11 ohm) Altamirano (2021)

Figure 4.4(b) shows the control signals. The figure 4.4(b) and 4.4(d) shows the circuit of the Fig 4.4(a) at the switch level. Where the first stage (b) is the charge and delivery of the current pulse to R_{chip} and stage (d) is the discharge of capacitors to the ground.

Note that C_x and R_{dac} make up a high pass filter, and C_a and R_{chip} are another high pass filter (see Fig 4.4 (a,b,d)). Where the equivalent transfer function for these two filters in series will be:

$$Hs_1 \cdot Hs_2 = \frac{s}{s + \frac{1}{R_{dac}C_x}} \cdot \frac{s}{s + \frac{1}{R_{chip}C_a}} \quad (4.6)$$

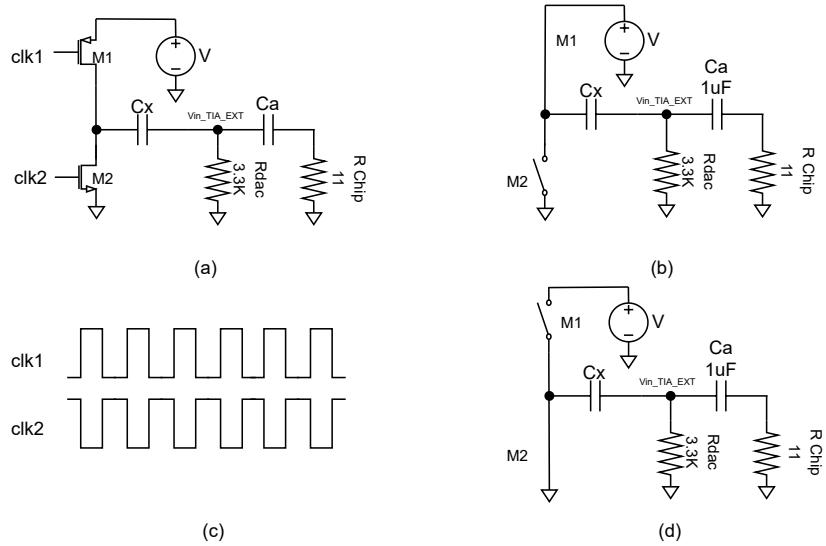


Figure 4.4: (a) Circuit at the transistor level-view. (b) 1st stage, charging the capacitors. (c) Digital control signals(referential). (d) Second stage, discharging capacitors to the ground.

And for example, supposing that we assign a value of 350pF to C_x , the transfer function is as:

$$Hs_1 = \frac{s}{s + 8.658 \cdot 10^5} \quad (4.7)$$

$$Hs_2 = \frac{s}{s + 9.091 \cdot 10^4} \quad (4.8)$$

$$Hs_1 \cdot Hs_2 = \frac{s^2}{s^2 + 9.567 \cdot 10^5 + 7.871 \cdot 10^{10}} \quad (4.9)$$

Analyzing the resulting system, we can see that the function poles are distant, not interfering with each other. We can also notice that the pole of the filter generated by C_a and R_{chip} will not affect the current pulse(Fig 4.5). The latter is reinforced when analyzing the frequency behavior of both

filters in series (Fig 4.6), considering that the current pulse will be above the frequencies of $10^8 Hz$.

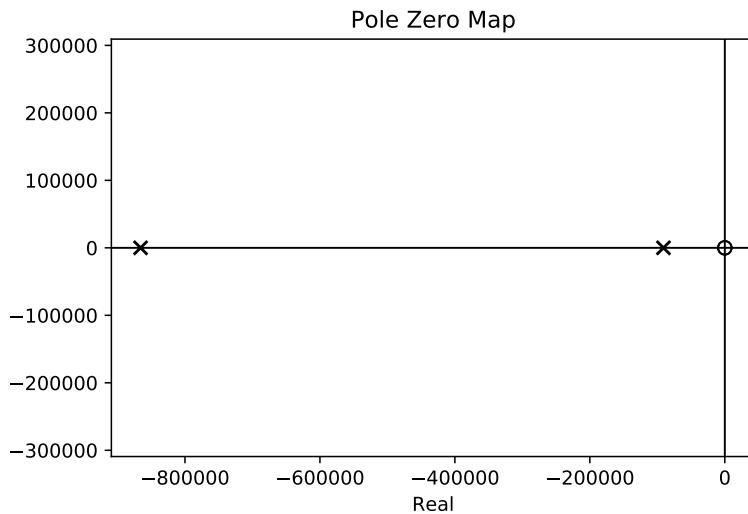


Figure 4.5: Map of poles and zeros of the equation 4.9

The capacitor C_x must accumulate a charge Q according to the equation of current $Q = CV$, where the extremes of the values (minimum and maximum) are found in Table 3.1. Considering the previous equation, we note that a voltage V must be selected (which corresponds to the voltage V of Fig 4.4a). This voltage must be set to different values so that from an exact value of C_x , different values of charge Q can be generated. They are many forms to set a voltage, it can be used from a voltage divider adjusted with a potentiometer to voltages set by a DAC (Digital to Analog Converter) to establish this voltage. The DAC option will be chosen because it has precision, output stability and monotony assured by the manufacturer, fundamental parameters if we are looking for accuracy in the generation of Q charge.

For the election of the DAC, we must ensure some specific parameters.

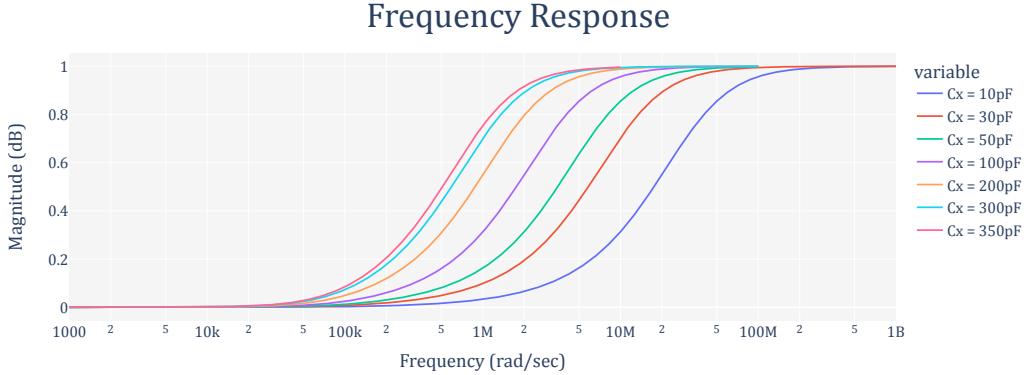


Figure 4.6: Frequency response pulse current circuit generator for different values of C_x

The resolution, the maximum voltage delivered, maximum short-circuit current are examples of some parameters.

From an application view, the resolution of the DAC depends on the number of bits and of the reference voltage. For example, considering a 4-bit DAC (Fig 4.7, Table 4.1) and considering a reference voltage $V_{ref} = V_{ref} = 3.3V$. The resolution will be given by the equation 4.10.

$$Resolution = \frac{V_{ref}}{2^n - 1} \quad (4.10)$$

, resulting in a minimum step of 0.22V. Another example and using the same equation 4.10 but in this case for a 12-bit DAC, the minimum step-size (resolution), with $V_{ref} = 3.3V$, will be 0.8mV.

The converter's resolution will be essential so that using the charge equation $Q = CV$ it is possible to generate voltages that allow having load values equal to or less than one pixel (4E-13, Table 3.1). Assuming a 12-bit DAC

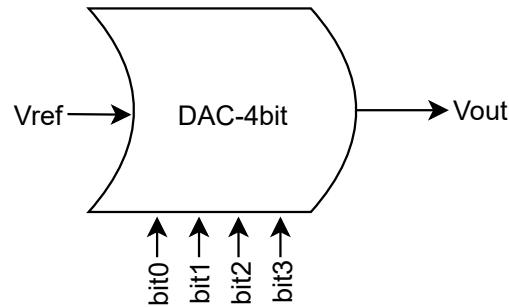


Figure 4.7: Example of 4bit-DAC

Table 4.1: 4bit-DAC reference outputs

Bits	Vout
0000	0
0001	0.22
0010	0.44
0011	0.66
...	...
1101	2.86
1110	3.08
1111	Vref

$C_x = 300\text{pF}$, $V_{ref} = 3.3V$, the minimum charge generated will be:

$$Q_{min} = V_{min} \cdot C_x = 0.8mV \cdot 350\text{pF} = 2.4E - 13 \quad (4.11)$$

. Resulting in a charge value of less than one pixel 3.1.

The highest voltage delivered by the DAC will be approximately equal to the reference voltage of the DAC. It is relevant to consider this maximum voltage since if one seeks to comply with the maximum charge generation expressed in Table 3.1, C_x is fixed. This voltage must be greater than or

equal to:

$$V = \frac{Q_{max}}{C}, C = C_x \quad (4.12)$$

For a maximum charge value of 1.2E-9 and $C_x = 350\text{pF}$, it is $V = 3.4V$. Therefore, for a fixed C_x value and to generate the maximum load from Table 3.1, a DAC must deliver a maximum voltage greater than or equal to $3.4V$.

The short-circuit current is a value given by the converter manufacturer in the datasheet. This parameter is vital in order not to damage the DAC when the current pulses are generated. Based on Spice simulations, a short-circuit current value greater than 200mA is recommended.

The circuit of Fig 4.4(a) was simulated in Lt-Spice with commercial transistors, considering various input voltages from $100mV$ to $3V$ with a step of $200mV$. Control signals were shown in Fig 4.8. In Fig 4.9 the voltage corresponding to the connection node between the source and the source of the transistors M1 and M2, respectively, is shown. It is important to note that these transistors are operating in Triode-region because $V_{ds} \leq V_{gs} - V_t$.

Fig 4.10 shows the current pulses generated by the clk1 and clk2 control signals. Note that there are negative and positive currents. In the simulation, the current from R_{chip} to the circuit was measured; therefore the negative currents go to the chip.

4.3 Control and reading mechanisms for output data.

The chip outputs are fast, on the order of nanoseconds. To implement the estimation methods presented in Chapter 3, one must be able to correctly

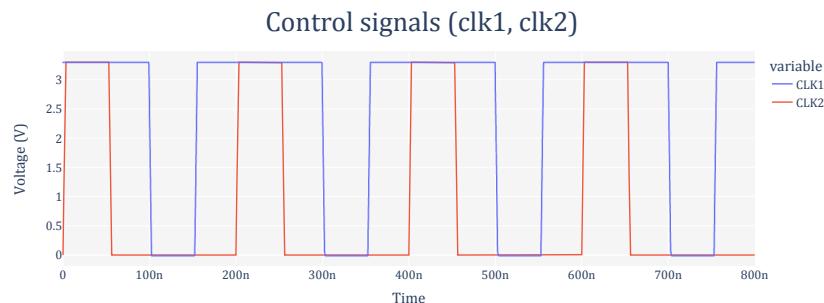


Figure 4.8: Spice simulation, control signals for M1 and M2

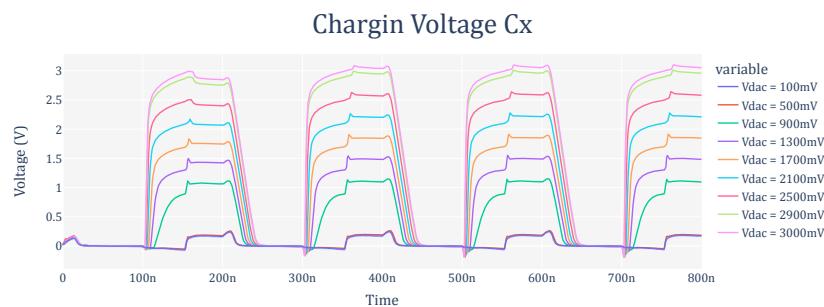


Figure 4.9: Spice simulation, charging voltage (common node between transistors M1 and M2)

read and process the information provided by the circuit outputs.

Analyzing post-layout simulations, the following questions arise:

1. How to read the signals of Fig 3.1, 3.2, 3.3
2. How do you know when to read?
3. How much information is necessary to capture to proceed with the estimation methods mentioned in section 3.2?

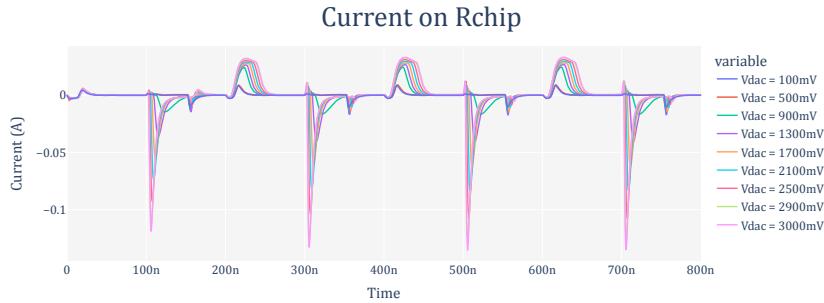


Figure 4.10: Spice simulation, current to the chip

4.3.1 How to read the output signals of the chip?

To answer question this question, it is necessary to remember that the circuit has digital (V_{out_disc}) and analog outputs (V_{out_TIA} , V_{out_INT}). The mechanism for read this signals will be different and it'll be described in this section.

Digital Outs

The digital outputs deliver information by changing their logic state (on/off transition and vice-versa). The information provided by this signal is the time of occurrence of the arrival of photons to the detector and also can be used for extract information about the approximate number of activated pixels. To detect the time of occurrence (pulse event), it is necessary to identify where the digital signal changes from high to low. Correctly capturing this information requires an additional circuit that detects with sufficient temporal definition (< 5ns according to simulation data shown in Table 3.2) the on/off transition moment. To estimate the number of activated pixels, it is necessary to count how long (after the on / off transition) the discriminator signal is in a low state before changing to a high state. The duration of

the V_{out_DISC} signals will depend proportionally on the amount of charge read by the chip. In Table 3.2, you can read the results for specific numbers of activated pixels. Therefore, correctly capturing this information requires an additional circuit that detects this event with sufficient resolution.

Analog

The signals V_{out_TIA} and V_{out_DISC} have information encoded in amplitude, that is to say, that the maximum value measured from its initial value provides information. The data delivered by these signals correspond to the number of activated pixels and was explained in more detail in chapter 3. These analog signals are non-periodic events, and their moment of occurrence can be controlled by the activation of the charge generator circuit. Like the V_{out_DISC} outputs, the duration of the V_{out_TIA} and V_{out_DISC} signals will depend proportionally on the amount of charge read by the chip. The results recorded in the post-layout simulations shown in Fig 3.1, 3.2, provide us with relevant information regarding the scenario of a triggered pixel. This event will produce the fastest and lowest amplitude outputs.

4.3.2 How do you know when to read?

To answer the second question, which mentions knowing when to read, it is necessary to remember that the charge generation process can be controlled in its entirety, so it can be predicted when there will be relevant information to read from the V_{out_DISC} and V_{out_TIA} outputs. This means that it is not necessary to read or monitor the analog outputs permanently. It must also have a controllable reading system. That is to say; it allows to

start and end the reading at certain times. For the digital signal of the discriminator circuit, it is only necessary to have a circuit that detects the transition moments *on-off* and *off-on*. See Fig 4.13.

4.3.3 How much information is necessary to capture to proceed with the estimation methods mentioned in section 3.2?

Question three refers to how much information is necessary to use the methodologies outlined in section 3.2. In Altamirano (2021) it is recommended to use the second approach (max amplitude) to take full advantage of the capabilities of the ASIC. For this reason, we will focus on this methodology and how it is possible to obtain enough information to implement it.

The approach called **Maximum amplitude** requires a reading system capable of recording the maximum amplitude of analog signals. To achieve this, it is necessary to digitally store the analog information, allowing its later analysis. This analog-digital conversion necessarily requires a specialized circuit called analog to digital converter.

About the Analog to Digital Converters

Analog to Digital Converters (ADC) are circuits that belong to mixed-signal circuits, and these devices transform the analog signal into a digital signal using different techniques. There are various types of ADC, each architecture employing different methodologies to achieve the conversion. Some of these ADC classes are Flash, SAR, Delta-Sigma. Regardless of the type of ADC, their functionality is to transform a continuous analog signal to a discrete

signal composed of digital samples (Fig. 4.12). Every ADC performs at least three processes. These processes are:

- analog signal sampling.
- signal quantization.
- signal encoding.

The sampling process depends on the sampling period of the ADC (generally expressed in samples per second, SPS). This parameter is relevant when selecting an ADC. Depending on the maximum frequencies of the analog signals, at least twice the maximum frequency (Nyquist) must be sampled to recover a signal and avoid Aliasing. In practice, it is recommended at least ten times the Nyquist frequency.

The quantization of analog signals is the assignment of discrete values to the samples acquired in the sampling process. This quantization depends directly on the number of bits that the ADC has. For example, an 8-bit ADC has 2^8 possible values to assign to the sampled values. These 2^8 possible values depend on a reference voltage, this voltage being an input of the ADC. In general, the quantization process depends on the ADC selected, and the manufacturers explain these details in the device datasheets.

An example of 4bit ADC is shown in Fig. 4.11

The quantization process involves a quantization error. This error has a form of random noise. It is uniformly distributed around $\pm \frac{1}{2} LSB$ with zero mean and standard deviation given by the equation (Lutenberg (2012)):

$$\sigma = \frac{1}{\sqrt{Nbits \cdot LSB}} \quad (4.13)$$

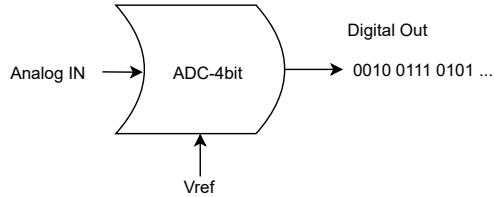


Figure 4.11: 4bit ADC. High level view.

LSB is the Least Significant Bit (quantization step), which corresponds to the distance between two adjacent levels in a quantization. This error implies in certain situations an approximation when quantizing. For example, when the sample is between two values (of the 2 Nbits), it should be approximated to the closest (See Fig. 4.12). This error decreases according to equation 4.13 as the number of bits in the converter increases. The encoding consists of transforming the quantized values to binary digital values, and that can be stored in a memory or be delivered to another digital circuit.

In addition to these parameters already mentioned there are others, such as the maximum bandwidth of the converter, a parameter that indicates up to which frequencies the attenuation will be less than $-3dB$. We also find the acquisition time, a parameter expressed in units of time and refers to how many units of time after sampling the signal are quantified.

In our case, the analog signals are of the order of nanoseconds, which, based on *Nyquist*, would imply selecting an ADC of the order of GSPS, in addition to having sufficient bit resolution to quantify the samples accurately and have a bandwidth higher than the $200MHz$, so that the Discriminator and Integrator signals are not attenuated. Using an ADC with the characteristics mentioned above would work to obtain enough information to allow the application of the maximum breadth methodology, but the associated cost is

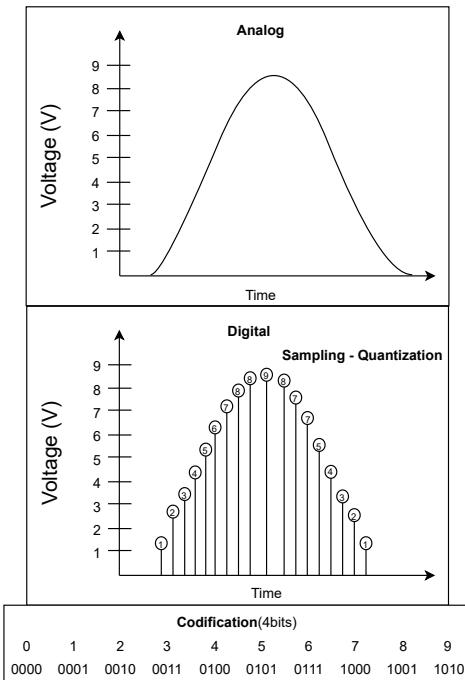


Figure 4.12: Analog to digital conversion example.

high. Remember that the generation of analog signals depends on the charge generator circuit, which makes the process controllable and reproducible in time. Considering this, a technique called sub-sampling can be applied. This technique will be described in section 4.3.4.

4.3.4 Sub-sampling

This technique consists of sampling a signal (which is fast for the acquisition system) repeatedly at different points in time. This technique allows the reconstruction of the original signal without the need of fast ADC. Applying this technique depends on knowing, and being able to control, the moment of arrival of the signals to be processed. They must also have precise control and reading mechanisms. The ADC to implement this technique can be

slower than that required by the Nyquist theorem, but it must guarantee a fast acquisition time that allows sampling at precise moments and a correct bandwidth so as not to attenuate the chip signals.

For the characterization of the ASIC, the charge generation process is controllable and repeatable, so it is possible to implement this technique with the appropriate elements.

In Fig 4.13 three graphs are shown in time, where the upper graph is the trigger signal for the charge generator circuit, the middle signal is a representation of one of the chip outputs, and the graph below It is the response of the digital output of the ASIC when the readed charge by the chip is equal or greater than the equivalent charge of one activated pixel.

The sub-sampling process of the signal in the middle graph is graphically expressed in Fig 4.14, wherein Fig 4.14(a) is shown at a certain point in time, Fig 4.14(b) at another, and so on until the different samples can reconstruct a significant part of the original signal (Fig 4.14(f)). Each of the samples can be an average of samples taken simultaneously to correct any noise that may exist.

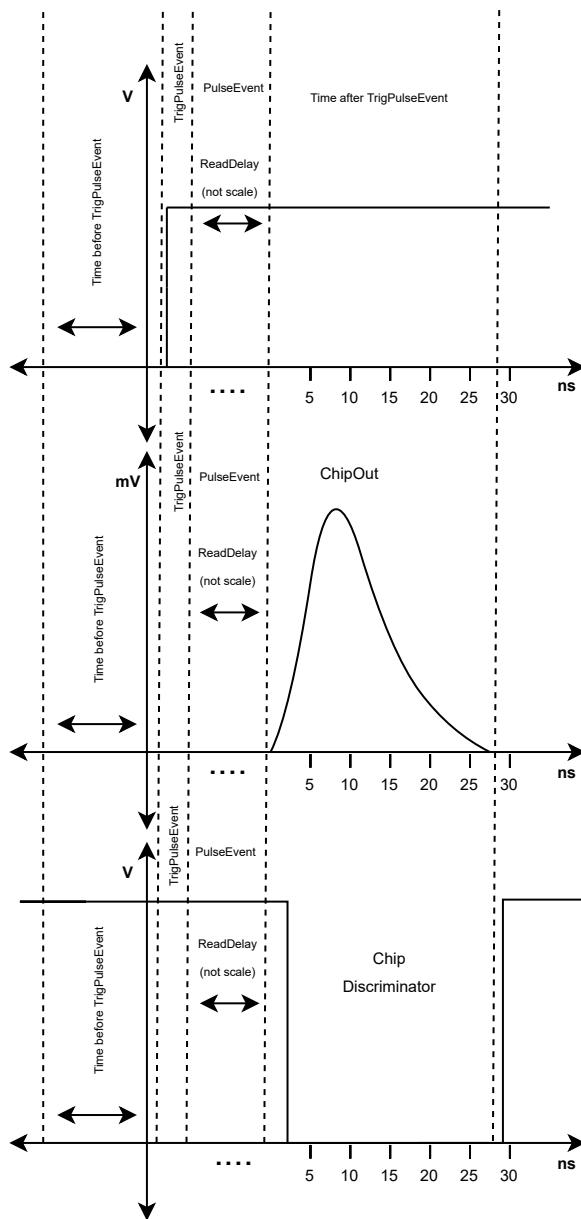


Figure 4.13: Succession of events in time

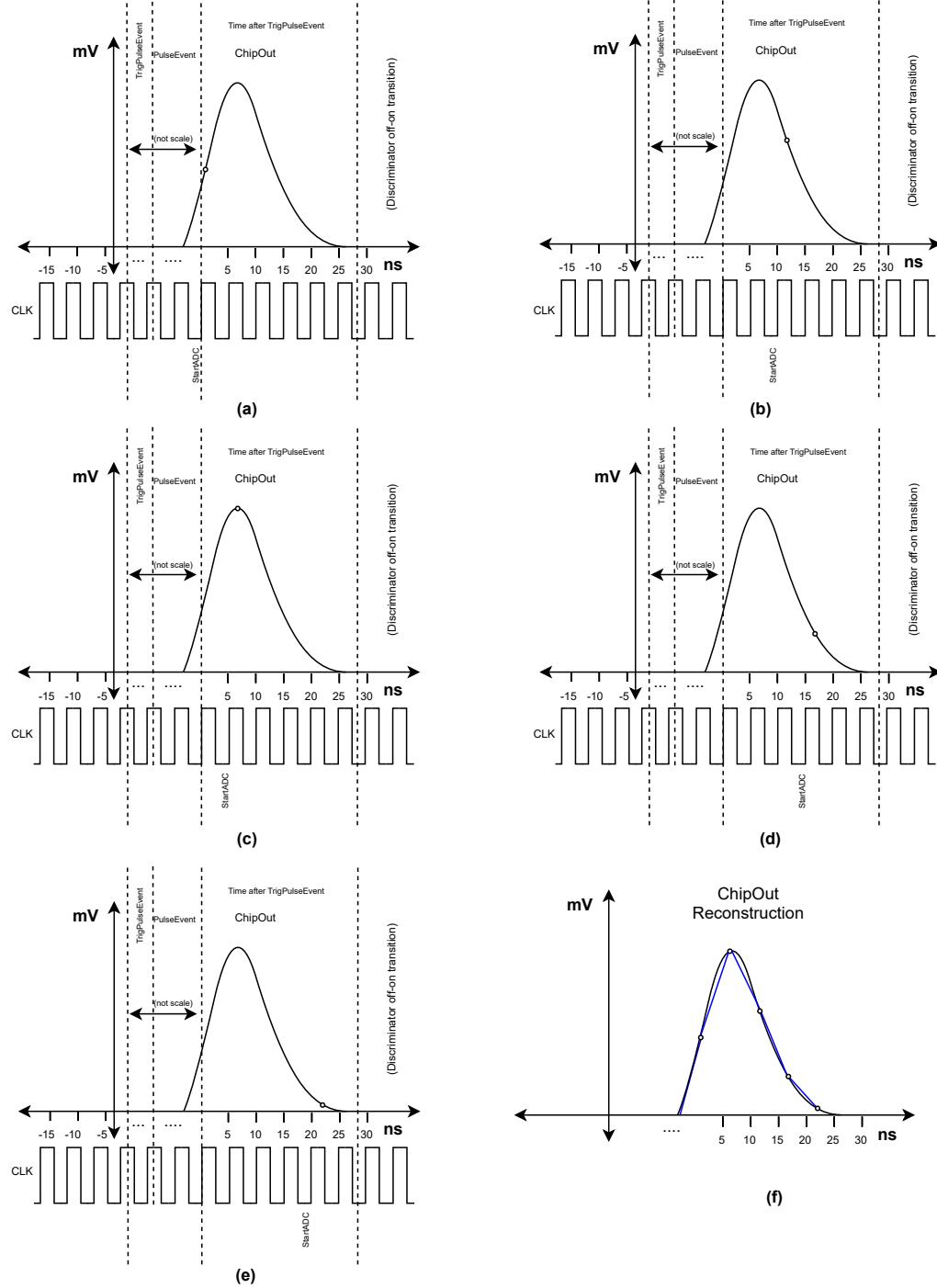


Figure 4.14: Sub-sampling methodology.

Implementation of the test environment

To implement the methods described in the previous chapters, it is necessary to have a system that allows the control of events with nanosecond precision that provides flexibility and re-configurations in some instances. Given the requirements, the use of an FPGA (field-programmable gate array) is proposed to implement the control mechanisms of the circuit characterization and verification process. The FPGA chosen is part of the Zynq-7000 family (Zybo Board).

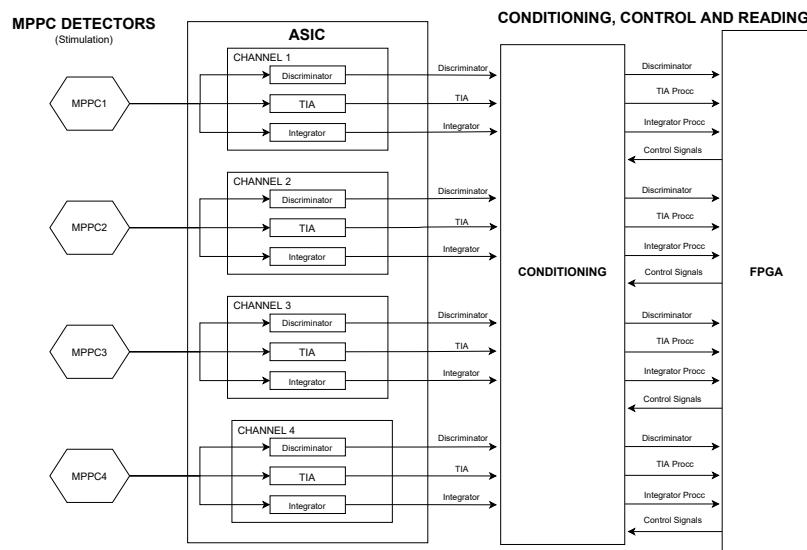


Figure 5.1: Global view of the testing system.

A global view of the test system can be seen in Fig 5.1; it is possible to see

the MPPC detectors, the Chip and each of its channels, the outputs, a signal conditioning block, and finally, the FPGA. In the initial verification process, the MPPCs will be replaced by the charge generator circuit of section 4.2. This circuit will be part of a PCB where other elements necessary for the test process will be soldered, the elaboration of this board and its specific components will be soldered. Will be presented in a later chapter.

The conditioning stage includes the analog to digital conversion of the analog signals of the Chip as well as the DAC that allows controlling the voltage V of the charge generator circuits described in section 4.2, Fig 4.4.

It is also essential to consider that the chip has 12 analog outputs, and each one delivers information. According to the requirements of this thesis, it is not necessary to read all these signals in parallel, which allows only one ADC to be used for the entire system. However, a suitable multiplexer is required to achieve those mentioned above. The multiplexer must have a low input capacitance and a bandwidth large enough not to attenuate the chip-out signals. Reading the digital signals (discriminator circuit out) requires a digital circuit that will be implemented in the FPGA, which will detect the transition from high to low state and count how many times elapses will elapse until the transition from low to high state. The definition of the account of this circuit will be proportional to the FPGA clock speed. In this case, it will be 5ns, justified time if the data in Table 3.2 are analyzed.

In addition to the counter circuit, the FPGA must have other custom logic blocks, which allow, for example, to store information from the ADC quickly (on each clock edge) and be delivered to the user when requested. There must also be logical blocks in charge of controlling the converters (ADC-

DAC) to control their operation according to the mechanisms described in the datasheets of each component. Remember that the ASIC also has 4 DACs, one for each channel. The control of these blocks must also be considered in the custom blocks to be designed. In Fig 5.2, the conditioning stage and internal blocks of the FPGA can be seen in more detail. Note that the FPGA has two internal blocks, Custom logic, and Zynq Processor System. Zynq Processor System is the Xilinx manufacturer's designation for its SoC (System on Chip). In the words of the manufacturer: "Xilinx provides the Processing System IP Wrapper for the Zynq®-7000 to accelerate your design and its configuration for your embedded products. The Processing System IP is the software interface around the Zynq-7000 Processing System. The Zynq-7000 family consists of a system-on-chip (SoC) style integrated processing system (PS) and a Programmable Logic (PL) unit, providing an extensible and flexible SoC solution on a single die. The Processing System IP Wrapper acts as a logic connection between the PS and the PL while assisting you to integrate custom and embedded IPs with the processing system using the Vivado IP integrator."

Using this system, it is possible to interact with different peripherals of the ARM Cortex-A9 processor(UART, SPI, GPIOs) to facilitate the acquisition and control of custom logic through the AXI bus.

Specific components are :

- ADC: LTC2245 (Linear Technolgy)
- DAC: AD5344 (Analog devices)
- MUX: DG1207 (Maxim integrated)

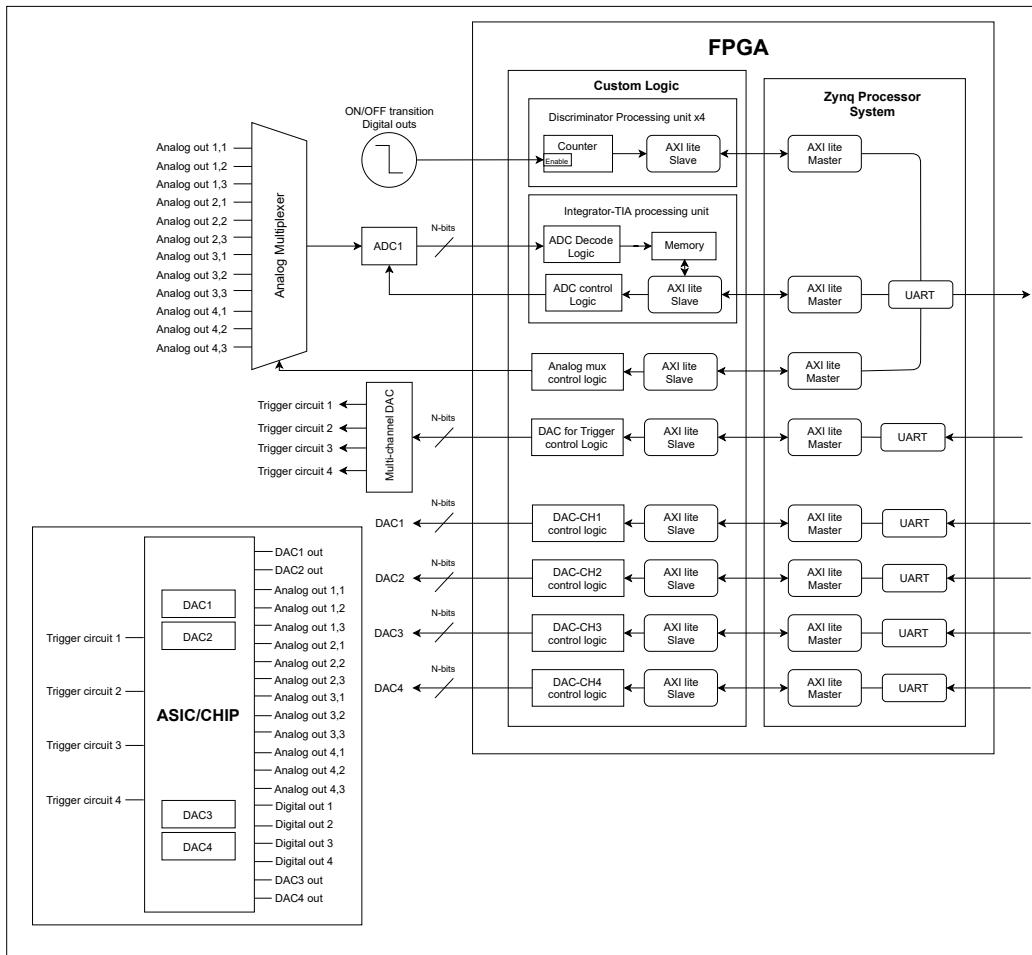


Figure 5.2: System implementation view.

6

Conclusions and future work

Based on the data provided by the chip designer in his Thesis (Altamirano, 2021), it is possible to use this information to devise a test scenario for the ASIC. The test environment must be adjusted to the physical requirements of the Chip for its correct functioning and operation. The work presented so far provides ideas and justifications for how it is planned to implement the integrated circuit characterization and validation environment. The justifications and requirements have been based in the great majority on the Thesis provided by the designer and works related to the verification of circuits with similar purposes.

6.1 Future work

As future work remains, the implementation of the digital blocks in charge of reading and controlling the elements of Fig 5.2 and the design and manufacture of a PCB where the ASIC and the other components necessary to carry out testing and characterization experiments will go.

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