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Nuclear Physics B (Proc. Suppl.) 215 (2011) 344–348
NUCLEAR PHYSICS B PROCEEDINGS SUPPLEMENTS
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A custom front-end ASIC for the readout and timing of 64 SiPM photosensors

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A new class of instruments – based on Silicon PhotoMultiplier (SiPM) photosensors – are currently under development for the next generation of Astroparticle Physics experiments in future space missions. A custom front-end ASIC (Application Specific Integrated Circuit) for the readout of 64 SiPM sensors was specified in collaboration with GM-IDEAS (Norway) that designed and manufactured the ASIC. Our group developed a custom readout board equipped with a 16 bit ADC for the digitization of both pulse height and time information. A time stamp, generated by the ASIC in correspondence of the threshold crossing time, is digitized and recorded for each channel. This allows to define a narrow time window around the physics event that reduces significantly the background due to the SiPM dark count rate. In this paper, we report on the preliminary test results obtained with the readout board prototype.

1. INTRODUCTION

In the recent years, the introduction of the Silicon PhotoMultiplier (SiPM) – a new solid-state photosensor operating in quenched Geiger mode [1–5] – has been followed by an intense work of research and development worldwide, leading to significant advances in this field as in the case of the Digital SiPM concept [6]. The application of SiPM photosensors as a potential replacement of traditional photomultipliers spans many different detection techniques in particle physics.

In this paper, we focus on the impact of this new device in the detection of Cherenkov light, a field that may require the capability to deal with very low light levels. Differential Cherenkov detectors – as the Ring Imaging Cherenkov (RICH) or the Detection of Internally Reflected Cherenkov Light (DIRC) – are based on the imaging of specific patterns of Cherenkov light, generated by the passage of a charged particle through a radiator, onto a detection plane structured into cells or pixels. For particles carrying one unit of electric charge (Z=1), the number of photons hitting a single pixel can fluctuate around a quite small average value, thus requiring photosensors with single-photon detection capability.

Arrays of SiPM devices, with a variety of different pixel sizes and covering sensitive areas of several tens of square millimeters, have been manufactured [7–10], but the typical dark count rates at room temperature (or with moderate cooling) are still too large to isolate the hits originated by the Cherenkov emission from the background noise in the image.

A way to circumvent this problem is to take advantage of the synchronous emission of photons radiated into the Cherenkov cone with respect to the random distribution of the SiPM dark counts in time. The need to record the arrival time of each photon hitting the photodetector array, lead to the specifications for a new front-end ASIC capable of providing (in addition to a pulse height measurement) an accurate time-stamp for each SiPM readout channel. This feature allows to select pixels carrying useful information on the Cherenkov image within a narrow "time-window" relative to an external trigger or relying on the self-triggering capabilities of the device. As a result of the application of the time filtering, the contrast of the image can be improved providing

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0920-5632/$ – see front matter
doi:10.1016/j.nuclphysbps.2011.04.049

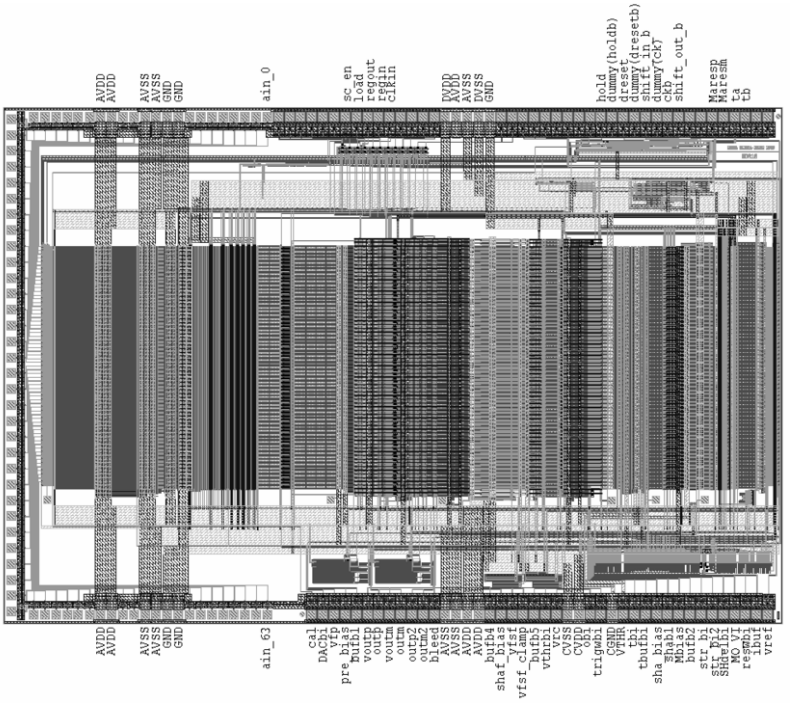

Figure 1. Overview of the VATA64-HDR16 ASIC.

a better efficiency to identify the Cherenkov pattern.
In this paper, we briefly describe the main functionalities of the new ASIC and a few preliminary results obtained with our first prototype test board.

2. VATA64-HDR16: a front-end ASIC for SiPM readout

The VATA64-HDR16 is a 64 channel front-end ASIC based on the VATA architecture (for a short review on the early history of ASICs for High Energy Physics see for instance [11]) and tailored for SiPM read-out. It has been specified in collaboration with GM-IDEAS [12] that developed the ASIC under a 0.35μm CMOS manufacturing process with an epitaxial protection against SEE effects in space applications. An overview of the ASIC can be found in Fig. 1.
All the ASIC main operational parameters can be programmed by downloading a "slow control" configuration after power-up.

The analog signal processing takes place in the front-end channels of the device, while the read-out is handled in the back-end. Each channel consists of a charge sensitive preamplifier, a fast shaper for triggering and timing and a slow shaper to provide a charge measurement. The output of the fast shaper is fed into a discriminator. The architecture of the channel readout is shown in Fig. 2.
At power-on, a threshold can be set and individually adjusted for each cannel.
In auto-trigger mode, whenever a channel exceeds its threshold value, the (auto-)trigger signal is asserted. The trigger can be output to the global off-chip trigger line and may also be used to generate an on-chip Sample-and-Hold (SH) signal.
A Time-To-Analogue-Converter (TAC) is implemented as a voltage ramp initiated by the trigger

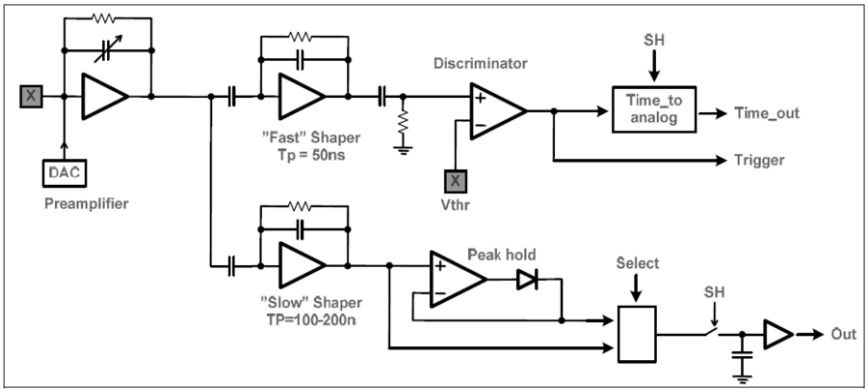

Figure 2. Architecture of one front-end channel of the VATA64-HDR16 ASIC.

and sampled with the SH signal. The slow shaper is followed by a Peak & Hold device.

The outputs of all channels are readout via two multiplexers running in parallel, one for the sampled slow shaper charge measurement and one for the TAC values. The output of both multiplexers is made available via differential output current buffers. The ASIC can be sampled in three different ways:

- external sampling: this is the traditional VA sampling method;
- internally generated sampling based on an internal trigger: a SH signal is issued at a programmable time delay;
- internally generated sampling based on an external trigger: the ASIC senses the TA/TB lines to check if any other ASIC has triggered. The SH signal is issued at a programmable time delay.

With the ASIC in "self-triggering" mode, whenever a channel exceeds its threshold it starts a new time measurement that is stopped after a programmable delay by the SH signal. In this way, we can measure the time differences between the first triggering channel and the other channels that have been hit. This functionality allows to define an offline "time window" to select events characterized by a number of hits detected simultaneously.

3. The VATA64-HDR16 test board

We developed a dedicated test-board, the VAB-HDR16 (see Fig. 3), equipped with all the circuitry for signal conditioning, digitization and readout. For the readout of the current output

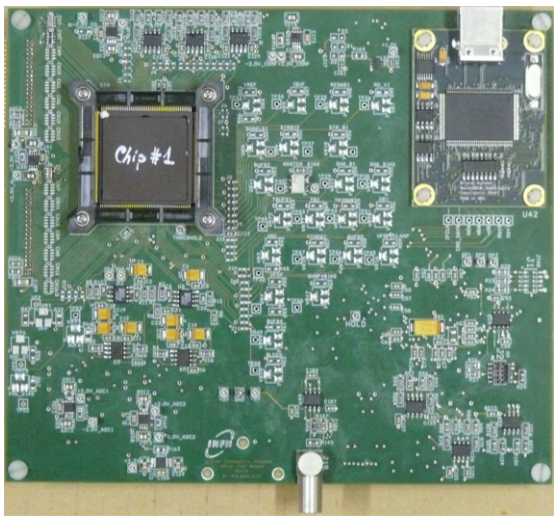

Figure 3. The VATA-HDR16 test board.

buffers of the ASIC, two stages are used: the first one is a voltage feedback amplifier for current-to-voltage conversion, while the second one consists of a fully differential input and differential output device.
For the analog to digital conversion, we used a 16 bits, 1 MSPS, fully differential ADC. All configuration, control and readout signals were generated by an Altera FPGA of the Cyclone II family: the EP2C8T144. Our test-board is equipped with an USB 2 interface with a PC to download the configuration bits of the VATA64-HDR16, to read/write registers and to readout the digitized data.

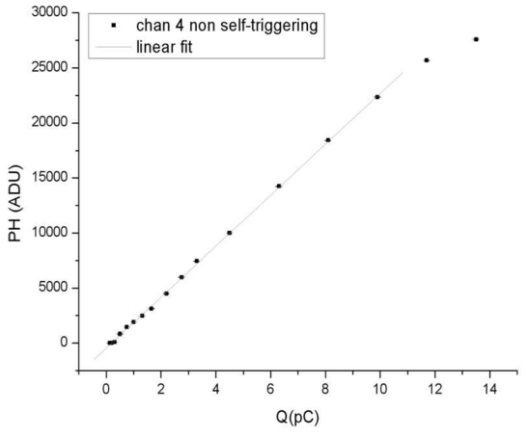

Figure 4. Measurement of the pulse height linearity of the ASIC.

4. Tests of the VATA64-HDR16 with the VAB-HDR16

We report here on the preliminary tests performed in our lab to verify the functionality of the board and the ASIC. All the measurements reported below – relative to the pulse height linearity and the time response of the ASIC – were performed with no SiPM devices connected to the test board.

Pulse height linearity tests were performed injecting known values of charge into the ASIC input. The VATA64-HDR16 showed a linear response for charges up to 12 pC (Fig. 4). For larger charges, a saturation effect was observed. The pedestal rms width could be lowered to $\sigma \sim$ 1 fC with simple EMI reduction precautions by shielding the board.

The result of a test on the linearity of the time measurement is reported in Fig. 5. The first triggering channel was set to produce a constant time output t_{max} whose value was set via the programmable SH time delay. We injected charge in a second channel at various delays with respect to the first one: the generated time-stamp showed a good linearity up to several hundreds of nanoseconds.

The width of the time pedestal was found to be around $\sigma \sim 4$ ADC units, i.e. 160 ps. (Fig. 6).

5. Conclusions

The basic functionalities of a new ASIC, specifically designed for SiPM readout, were tested using a custom test board. In a following paper we will report on our measurements – both in the lab and at a dedicated beam test – with SiPM photodetectors connected to the ASIC. At present, we are integrating the new ASIC readout into SiPM-based prototypes of RICH and DIRC Cherenkov detectors.

Acknowledgments

The authors would like to thank Altera Inc. for supporting the project through the Altera University program. This work has been funded by the Istituto Nazionale di Fisica Nucleare (INFN) in Italy in cooperation with GM-Ideas.

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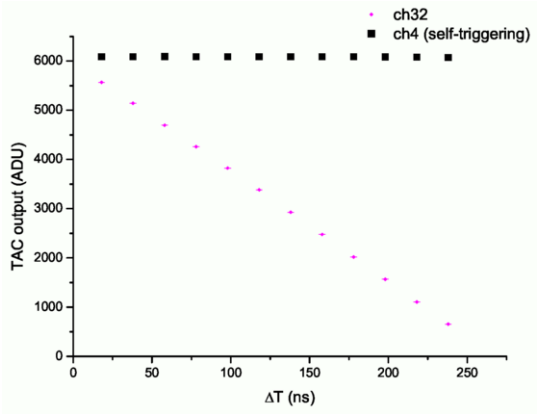

Figure 5. Measurement of the time linearity of the ASIC. The anti-correlation shown in the figure is due to the offset in the time-stamp of the first trigger which occurs at t_{max}

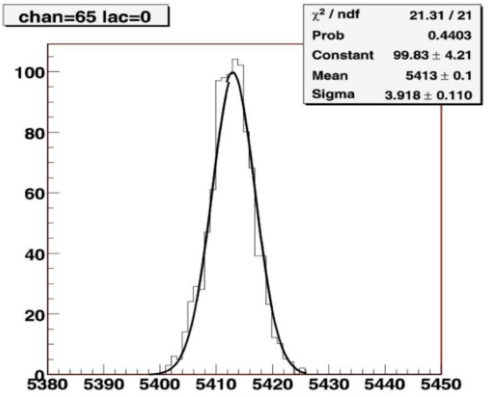

Figure 6. A typical time pedestal of one channel of the board during charge injection tests.

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