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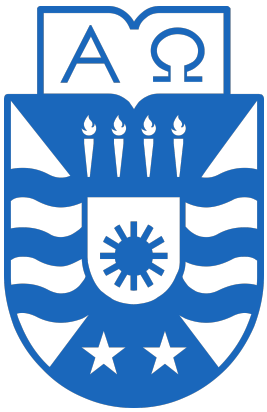
Test and verification of a multichannel ASIC for reading SiMP detectors



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Abstract

The development of integrated circuits is a complex task. This task can be divided into three major areas: Design, manufacture, and verification. In the context of Professor Ángel Abusleme's research, the master's student Renzo Barraza has designed and shipped to manufacture a chip that aims to read 4 SiPM (Silicon Photomultiplier, SiPM, Multi-Pixel Photon Counters, MPPC) in parallel. If the configuration of these detectors is correct, they can detect individual incident photons on their surface. Hoping the designed chip can be tested with real detectors in the future and then be used in particle physics experiments requiring the reading of photomultipliers of silicon (SiMP / MPPC). The chip manufacturer has already and now corresponds the process of characterizing it and checking its operation. That is the test and verification process of the post-silicon circuit (Post-silicon validation).

This work proposes the design of an embedded platform. It will allow verifying the functionalities of the chip because there are currently no solution-specific tests for this ASIC (Application-specific integrated circuit). This test platform should allow the chip and detectors to be configured correctly. SiMP would allow testing with real detectors. Also, this verification circuit should permit to control chip inputs and outputs when needed, as well as be able to record the data from these outputs.

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1 The Chip

The Chip is a multichannel ASIC and has four analog channels with four outputs each. Of these four outputs, 3 are analog signals, and one is digital.

1.1 Description and features of the ASIC

This IC can read 4 SiMP detectors in parallel, process these measurements internally, and through 4 outputs (3 analog and one digital), deliver information on the number of photons that arrived at each detector. The number of photons that arrived at the detectors must be extracted from the analog and digital signals (chip outputs). These estimates and their methods are described in detail in Chapter ...

Specifying some things:

- The Chip has four analog channels for 4 MPPC (SiMP) detectors.

- Each analog channel has an 8-bit DAC, which allows the user of the readout circuit to fine-tune the gains of the SiPM by adjusting its bias voltage, in addition to compensating for the dark noise mentioned in chapter ... . Due to the limitations of CMOS technology, the maximum voltage that can be delivered is close to 1.8V (relative to ground). This

limitation prevents the Chip itself from being able to directly bias the MPPC detectors.

Fig. 1.1 is a graphical summary of these points.

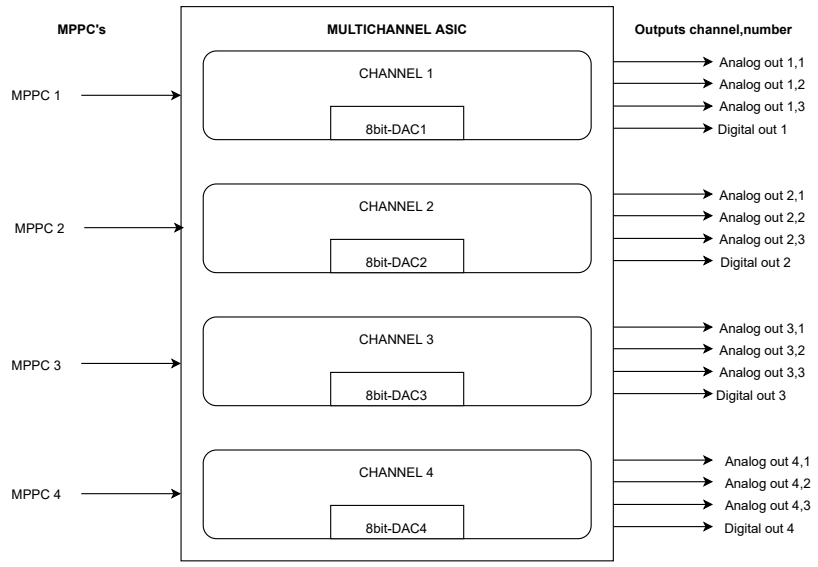

Figure 1.1: ASIC high-level overview

1.2 Inputs and on-chip signal processing

The Chip has four analog inputs and three outs, three analogs and one Digital output. In details:

This Chip has four channels, and each channel has one Analog input. Those inputs are connected to the MPPC's, and when photons arrive at the detectors, a flow of charge is produced and the Chip reads this current using a specific circuit.

The reading circuit for the SiMP detectors corresponds to an open-loop transimpedance amplifier (TIA) type circuit, which the chip designer justifies based on the objectives proposed in his Thesis (Altamirano, 2021). On the Chip are four TIA's, each one for every channel.

A high-level circuit representation of the above is shown in Fig. 1.2, where "-HV" is a High negative voltage, and it is used to polarize the detectors.

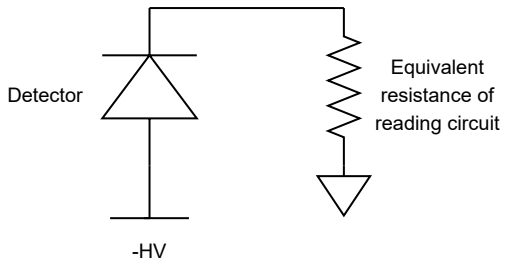

Figure 1.2: Read out circuit representation (Altamirano, 2021)

Employing the TIA is possible to read the flow of charge (coming from the detector), and after processing the voltage output signal of the TIA (Fig. 1.3). Using the voltage output is possible to obtain information about how many photons arrived at the detector. The methods for doing that are described in chapter ...

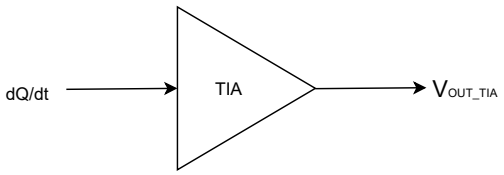

Figure 1.3: Transimpedance Amplifier (TIA)

1.2.1 Post-TIA Processing

Once the TIA has read the signal, two things must be measured:

1. The instant the charge is received.

2. Number of pixels activated in the detector.

To know the first one, the designer decided to implement a discriminator circuit. This circuit is activated when the voltage signal produced by the TIA indicates that one or more pixels have been triggered in the detector. The output of the discriminator, therefore, delivers a digital signal (on/off transition). This signal lasts as long as the MPPC continues to provide current. The information supplied by the discriminator can be used to know the number of pixels fired in the detector. Additionally, the designer decided to implement an extra circuit block to improve the results. This new circuit is an integrator, and its purpose is to integrate the voltage signal of the TIA. The information that provides this block can be added to that already delivered by the discriminator to read more accurately the number of activated pixels (Altamirano, 2021).

A representation of the internal component of each of the four channels is shown in Fig. 1.4

Fig. 1.4 shows that the signal produced by the SiMP connects to the VIN_TIA_EXT node. The potential of this node can be altered due to the effect of the DAC. This DAC is capable of doing a fine-adjusting of the SiPM bias voltage (with the limitations of CMOS technology explained in section 1.1)

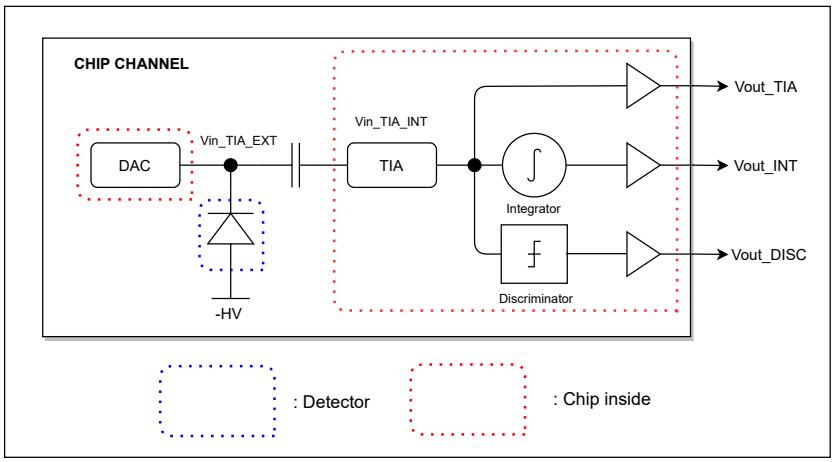

Figure 1.4: Internal components of each of the four channels (Altamirano, 2021).

1.3 Outputs

The Chip for each channel has four outputs:

- VOUT_INT_DER and VOUT_INT_IZQ: These are the differential outputs of the integrator (VOUT_INT in the figure). This output is used to identify few triggered pixels.
- VOUT_TIA: Direct output of the TIA. It is employed to identify a number greater than hundreds of triggered pixels.
- VOUT_DISC: It is the output of the discriminator. It serves to identify the moment when a signal arrives from the SiPM and can also be used to identify a neighborhood bounded by triggered pixels.

These points are based on the description of the outputs gives by the designer of the ASIC in (Altamirano, 2021). In Fig. 1.4, it is possible to observe the outputs of one channel.

2

Results of post-layout simulations and estimation methodologies

In Fig. **??**, the last verification step is called post-layout verification. At this stage, the designer did appropriate simulations based on the problem specification described on chapter 1. These simulations were used to estimate the number of photons arrived at the detector and the time of this fact. For this, the author of the Chip used methods that will be described in this chapter.

2.1 Post layout simulations

Using software and some techniques described in section **??**, the designer simulates some conditions for validating the behavior of his circuit. The Chip is designed to be capable of two main things: Estimate the number of photons arrived at the detector and the time of this fact. To do these two things, simulated the arrival of photons is necessary. So, how to do that?

2.1.1 Single-photon arrival simulation

The author of the circuit used as an input signal a current pulse of 0.1 ns with an amplitude of 4 mA. This, because the electrical charge delivered by

said current pulse is equivalent to the charge delivered by 1 pixel triggered in the Hamamatsu S14160-3050HS detector.

The aforementioned current pulse was used for stimulating the channels of the ASIC. The response of the circuit and the outs are exhibited in the figures 2.1, 2.2 and 2.3.

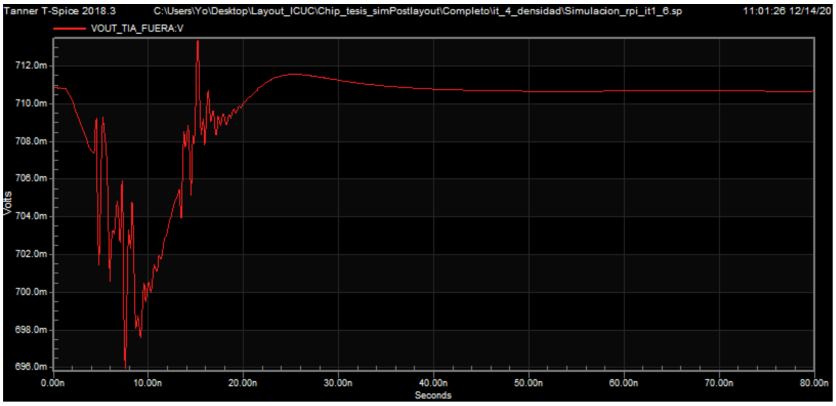

Figure 2.1: TIA Out. One pixel activated (Altamirano, 2021)

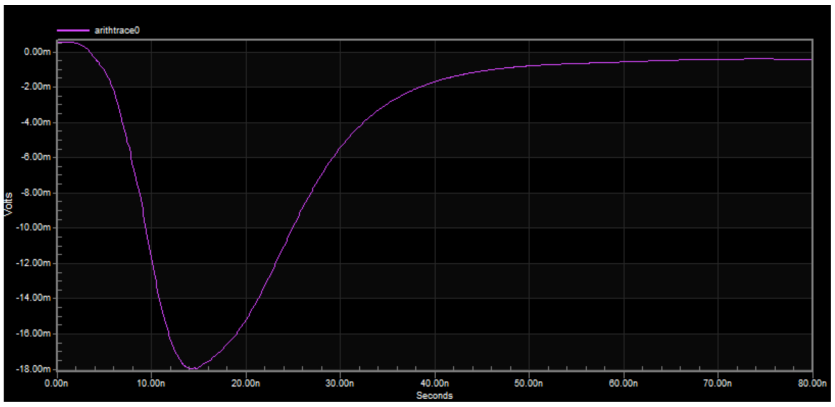

Figure 2.2: Integrator Out. One pixel activated (Altamirano, 2021)

Figure 2.3: Discriminator Out. One pixel activated (Altamirano, 2021)

2.1.2 Multi-photon arrival simulation

The current pulse used for simulating the arrival of one photon is linearly scaled for simulating more arrival photons (more pixels activated). This linearly scaled affects just the signal's amplitude, but the duration of this signal is equal for every quantity of simulated photons (Table 2.1).

For example, to simulate the activation of two pixels of the detector (MPPC/SiMP), the current pulse will be a pulse of 0.1 ns with an amplitude of 8 mA. In the case of simulating the activation of four pixels, the current pulse will be a pulse of 0.1 ns with an amplitude of 16 mA. And so on. Table 2.1, Fig 2.4 and Fig 2.5 summarize this.

The third column of table X shows the equivalent charge for a pulse of 0.1 ns with this correspondence amplitude. That data will be necessary for chapter X because generate a pulse whit the values of amplitude and duration of 0,1ns can be challenging. Nevertheless, it is possible to produce a pulse that the integration area will be equivalent to the equivalent charge for n number of pixels, following the current equation 2.1.

Table 2.1: Pixels, Current and Charge relation

Pixels	Current[mA]	Charge[q]
1	4	4E-13
2	8	8E-13
3	12	1.2E-12
4	16	1.6E-12
5	20	2E-12
6	24	2.4E-12
7	28	2.8E-12
8	32	3.2E-12
9	36	3.6E-12
10	40	4E-12
...	...	...
1000	4000	4E-10
...	...	...
2000	800	8E-10
...	...	...
3000	12000	1.2E-09

$$\frac{dQ}{dt} = C\frac{dv}{dt} \tag{2.1}$$

2.2 Chip signal reading. How to read/interpret the analog outputs of the Chip?

In the thesis, two methodologies are mentioned to measure the outputs and estimate the number of activated pixels. We will refer to these as:

1. Peaking time approach

2. Maximum amplitude approach

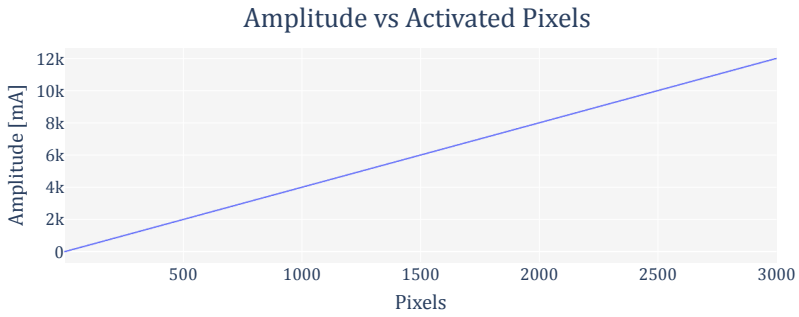

Figure 2.4: Current Amplitude vs activated pixels.

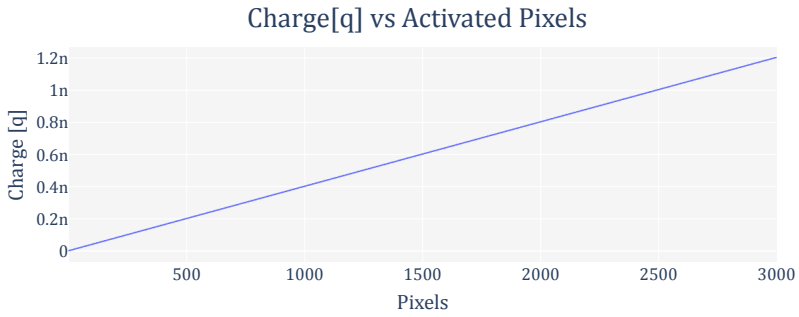

Figure 2.5: Charge vs activated pixels.

2.2.1 Peaking time approach

This approach has two stages: Calibration and Measurement. Calibration is done with just one pixel fired. At this point, a time difference is measured between the moment of the discriminator trigger (Vout_DISC transition on / off) and the moment of maximum amplitude (peak value) of the Vout_INT output for a pixel. The measurement is performed with the peaking time calculated in the calibration stage. The Vout_INT signal will be measured after the time delta calculated for N triggered pixels. It is essential to mention that for a small N (number of activated pixels) (therefore a low amplitude input signal), this method works well, but as N increases, the transistors leave

their region of linearity, which will cause imprecision in the measurement of the valid maximum of the Vout_INT signal. This approach can be seen in the following Fig 2.6.

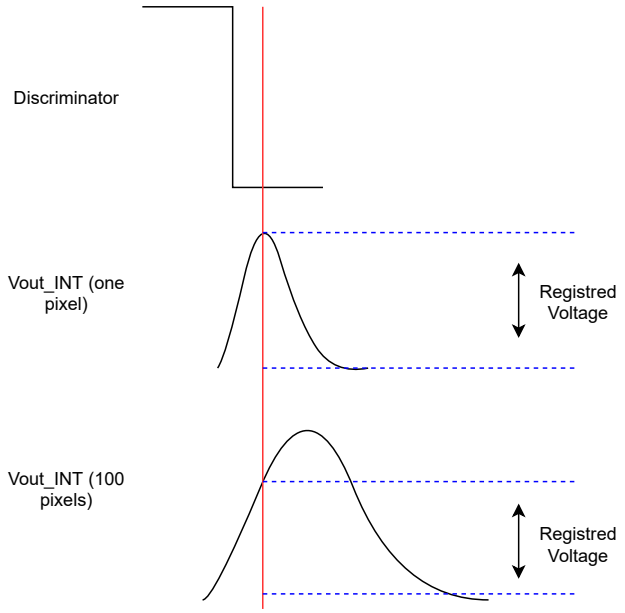

Figure 2.6: Peaking time approach (Altamirano, 2021).

2.2.2 Maximum amplitude approach

The second approach is to assume that the user will identify the maximum amplitude of the analog outputs. Therefore the maximum value of said signals is recorded regardless of when this occurs; This approach can be seen in the following Fig 2.7.

In addition to these two methods, it is possible to use the digital signal from the Discriminator and, depending on the duration of the pulse, estimate the number of pixels triggered using the Time Over Threshold method. This method is described in Orita et al.; Bagliesi et al. (2011); Altamirano (2021)

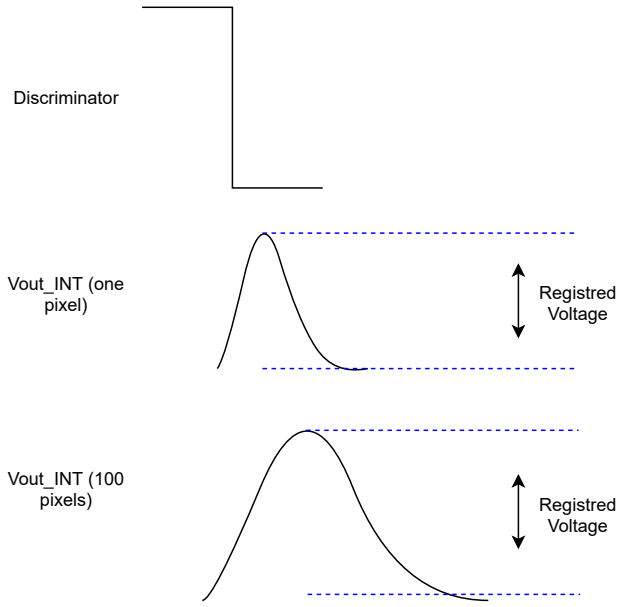

Figure 2.7: Maximum amplitude approach (Altamirano, 2021).

and is used in circuits of similar applications. The method consists of relating the duration of the digital pulse with a certain number of activated pixels.

2.2.3 Performance of methodologies

The following Figs 2.8, 2.9 shows the performance of both methodologies when measuring the outputs of the TIA and Integrator. Additionally, the duration of the discriminator pulses to identify the number of pixels it is showed in Table 2.2.

The chip designer mentions that based on their results, it can be stated that: Both measurement approaches of the integrator cannot resolve differences of 1 triggered pixel, but it can resolve differences of 2 triggered pixels. This capacity degrades as more large signals are received from the SiPM. A summary of the ability to resolve multiple pixels using the various analog

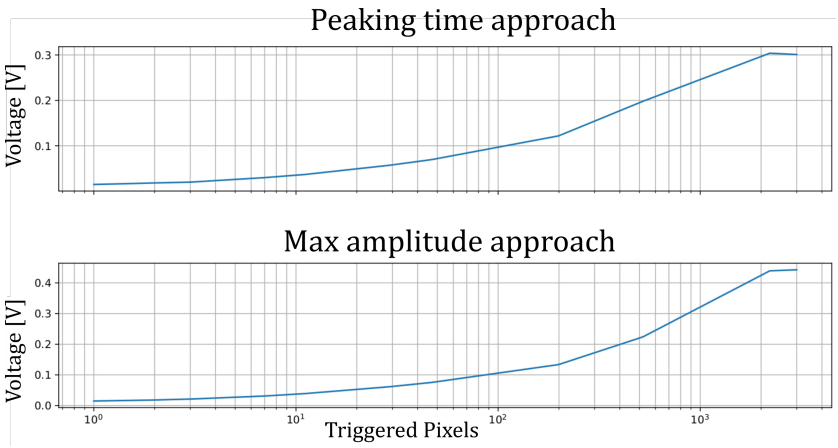

Figure 2.8: Results of the approach. TIA out (Altamirano, 2021).

outputs is provided below and it is summarized on Tables 2.3 and 2.4.

- It should be noted that the TIA data are not reliable with few pixels because there the oscillations caused by the digital buffer abnormally the amplitude of the signal. Remember that the TIA output is intended to deliver information of hundreds or more pixels.

- Based on the data mentioned above, using the Time over threshold technique to resolve signals of few pixels becomes necessary.

Table 2.2: Duration of discriminator pulses according to number of pixels triggered in the detector

Number of activated pixels	Discriminator pulse duration [ns]
1	11.4
2	17.68
3	21.24
7	31.65
11	38.07
29	54.88
47	65.88
199	>100

Table 2.3: Ability to resolve pixels of the TIA.

Number of triggered pixels in the detector	**Resolution capacity of pixels measuring maximum of the signal(max amplitude approach)**	**Pixel resolution capacity measuring at the moment of maximum signal for 1 pixel (peaking time approach)**
1 - 11	2	2
11 - 29	3	3
29 - 47	10	6
47 - 199	10	20
199 - 521	35	100
521 - 2207	250	Not distinguished
2207 - 3000	Not distinguished	Not distinguished

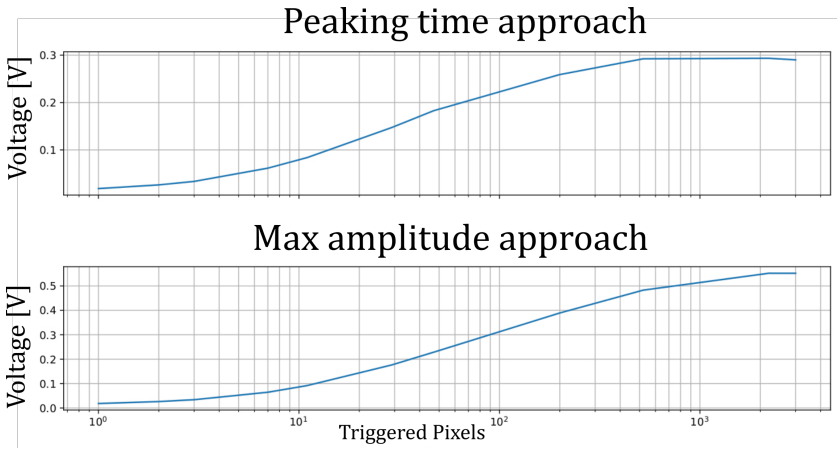

Figure 2.9: Results of the approach. Integrator out (Altamirano, 2021).

Table 2.4: Ability to resolve pixels of the Integrator.

Number of triggered pixels in the detector	**Resolution capacity of pixels measuring maximum of the signal(max amplitude approach)**	**Pixel resolution capacity measuring at the moment of maximum signal for 1 pixel (peaking time approach)**
1 - 2	1	1
2 - 3	1	2
3 - 7	1	1
47 - 199	2	2
11 - 29	3	3
29 - 47	4	4
47 - 199	7	8
199 - 521	9	11
521 - 2207	20	40
2207 - 3000	575	Not distinguished

3

Validation Environment

The process of validation and characterization of the Chip necessarily requires a suitable test environment. This test environment must have the capabilities to properly condition the circuit to stimulate the inputs and analysis of the outputs. Additionally, the test environment must provide stimulation signals and be able to record outputs. With the recording of the outputs and using the estimation methods described in section 2.2, estimating the number of triggered pixels will be possible.

In previous works, Orita et al.; Bagliesi et al. (2011); Galdames (2021) a circuit is designed and printed on a plate, which allows the IC to be correctly conditioned to proceed with the stimulation of the inputs and analysis of the outputs. The ASIC designer proposes as future work the design of a PCB (printed circuit board) to validate and test the ASIC.

The design of this characterization and validation environment is set out below. The details related to the implementation of the methods presented in this chapter are exposed in Chapter ....

The validation environment must have:

- A negative HV(high voltage) generator for the correct polarization of the detectors.
- Current pulse generator for stimulating the inputs.

- Mechanisms for the control and reading of analog and digital data that allow the implementation of the pixel estimation methodologies described in the section

3.1 Negative HV generator

A negative HV generator it is for the correct polarization of the detectors. The specifications of the "MICROFCSMTPA-10010-GEVB" detectors indicate a reverse bias voltage close to -24V. The PCB must supply this voltage. Based on the specifications given by Professor Abusleme, this voltage must be generated by a Charge Pump type circuit.

The Charge Pump (CP) is an electronic circuit that converts the supply voltage VDD to a DC output voltage Vout that is several times higher than VDD. Unlike the other traditional DC-DC converters, which employ inductors, CPs are only made of capacitors and switches (or diodes) [1]. CP under specific conditions can also produce a voltage lower than the input voltage, generating a negative voltage.

They are different topologies of charge pump circuits, and the majority of these are based on multiplication stages. The idea behind the behavior of these types of power sources is to use semiconductor elements (diodes or transistors) combined whit two complementary control signals to guide the direction of the current connecting and disconnecting different stages of the circuit to produce an increment (or decrement) of the output voltage.

For example, on Tanzawa and Tanaka (1997) the authors analyze the dynamics of a Dickson CP circuit. The topology of the circuit doubler voltage is presented in Fig 3.1.

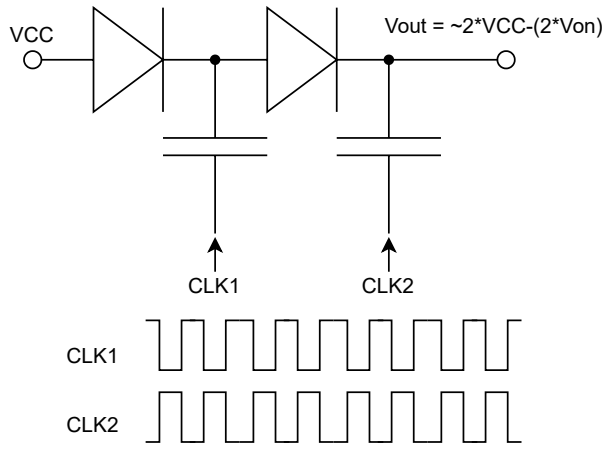

Figure 3.1: Dickson CP, voltage doubler and complementary clock (digital) signals (Tanzawa and Tanaka, 1997).

To improve the results of this topology is recommended to use Schottky diodes because the parameter V_{on} is smaller than other diodes(Palumbo and Pappalardo, 2010). It is also possible to use transistors instead of diodes, this is a very popular practice to implement these CP sources in integrated circuits.

For example a Dickson charge pump with MOSFET implementation is shown in Fig X. It is a typical n-stage Dickson charge pump. The input CLK and CLKB are two out-of-phase clocks with amplitude V CLK . These two clocks will increase the potential voltage in capacitors by transferring charges in the capacitor chains through diode-connected MOS transistors. The coupling capacitors will be charged and discharged during each half clock cycle (Lin, 2012a).

The voltage difference between the voltages of the nth stage and $(n+1)th$ nodes is given by:

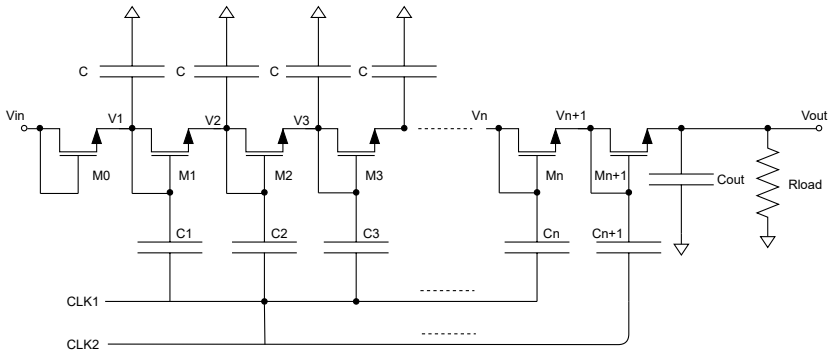

Figure 3.2: A typical n-stage Dickson charge pump (Lin, 2012a).

$$\Delta V = V_{n+1} - V_n = V'_{clk} + V_t \tag{3.1}$$

Where the voltage gain can be express as:

$$V'_{clk} = \left(\frac{C}{C + C_s}\right) V_{clk} \tag{3.2}$$

For an N stage charge pump, the voltage at the output node is as follow:

$$V_{out} = V_{DD} + N(V'_{clk} - V_t) - V_t \tag{3.3}$$

The equation above is the ideal output voltage when there is no output load and no output current delivered. When the charge pump is connected to an output load, the load current at a clock frequency f , is given by (Lin (2012a)):

$$I_{out} = f(C + Cs)V_L \tag{3.4}$$

V_L is the voltage drop per stage for supplying the load current. Therefore, the output voltage will be reduced an $N * V_L$ voltage. So the output voltage

with load will be rewrite as follow (Lin (2012a)):

$$V_{out} = V_{DD} + N\left(\frac{C}{C + C_s}\right)V_{clk} - V_t - \frac{I_{out}}{f(C + Cs)} - V_t \tag{3.5}$$

Equations 3.1, 3.2, 3.3, 3.4 and 3.5 are based on Lin (2012a)

This type of circuit is easy to find as integrated circuits, where manufacturers guarantee certain output values for specific conditioning parameters. For example, the LTC3261 is a high voltage inverting charge pump that operates over a wide 4.5V to 32V input range and can deliver up to 100mA of output current, and the output voltage will be -Vin. Based on the datasheet, this IC is a good option for implement the HV negative source (Lin, 2012b).

3.2 Current pulse generator for stimulating the inputs

Before using real detectors, the outputs of these sensors must be emulated in such a way as to have control over the timing of the current pulse triggering. Have dominion over the pulse triggering moment is essential to perform the characterization and validation of the ASIC. To achieve this, a load generator circuit will be required.

The current signals used in the post layout simulations (section x) have amplitudes ranging from 4mA to 12A, with a duration of 0.1ns for any of the amplitude values in Table 2.1. Current pulses of the same order of magnitude as the signals used in the post-layout simulations (ns) must be generated for testing purposes. The chip is designed to read current, so the fundamental thing will be to generate current pulses where the delivered load (-integral

current-) can be related to N of activated pixels using the linear relationship mentioned in section 2.1.2 and 2.1. The chip designer's suggestion will be used as a reference in his thesis to generate this pulse. Using the current equation (equation!) will consist of the capacitor to generate the charge.

From equation 2.1, we can see that the current in the (ideal) capacitor depends on two factors C (capacitance of the capacitor) and $\frac{dV}{dt}$. To regulate the current pulse, we must control at least one of these factors.

3.2.1 Multi-option C values

The equation X allows the current to be varied by changing the values of C. It is possible to have several values of capacitors that for a fixed and known $\frac{dV}{dt}$ generate an amount of charge equal to $Q = CV$. If C varies, the load and consequently the current will change. An analog multiplexer circuit can be used that connects different values of capacitors to one source. When the source is turned on a current is generated. $i = C\frac{dV}{dt}$.

This idea is discarded at first because a circuit that is in charge of multiplexing the signals will add additional capacitance's that negatively influence the generation of the pulses. Furthermore, this multiplexer would be required to have a sufficiently large bandwidth not to attenuate the pulsating signals, making the implementation complexity.

3.2.2 Different charging voltage values for C

Using electronic keys, it is possible to charge and discharge a capacitor in a controlled way. The capacitor, under certain conditions, must be connected to a voltage V, charged, and therefore generate a current $i = C\frac{dV}{dt}$ (accumu-

lating a charge $Q = CV$), and then discharged to the ground.

To achieve this charge and discharge, two complementary digital signals will be used to control a pair of electronic switches (Mosfets). These transistors will have the function of controlling the charge and discharge of the capacitor.

Figure 3.3(a) shows the circuit at the transistor level where M1 and M2 are the electronic keys, clk1 and clk2 are the control signals, V is the voltage source, C_x is a capacitor in charge of accumulating charge that will be delivered to the Chip (R_{chip}), R_{dac} is the equivalent resistance of the internal DAC of the Chip channel, C_a is the coupling capacitor mentioned in section 1.3 (Fig 1.4) which must have a value of 1uF (Altamirano, 2021) and R_{Chip} is the equivalent input resistance ASIC (11 ohm, Altamirano (2021))

Figure 3.3(b) shows the complementary control signals. The figure 3.3(b) and 3.3(d) shows the circuit of the Fig 3.3(a) at the switch level. Where the first stage (b) is the charge and delivery of the current pulse to R_{chip} and stage (d) is the discharge of capacitors to the ground.

Note that C_x and R_{dac} make up a high pass filter, and C_a and R_{chip} are another high pass filter (see Fig 3.3 (a,b,d)). Where the equivalent transfer function for these two filters in series will be:

$$Hs_1 \cdot Hs_2 = \frac{s}{s + \frac{1}{R_{dac}C_x}} \cdot \frac{s}{s + \frac{1}{R_{chip}C_a}} \tag{3.6}$$

And for example, supposing that we assign a value of 350pF to C_x, the transfer function is as:

$$Hs_1 = \frac{s}{s + 8.658 \cdot 10^5} \tag{3.7}$$

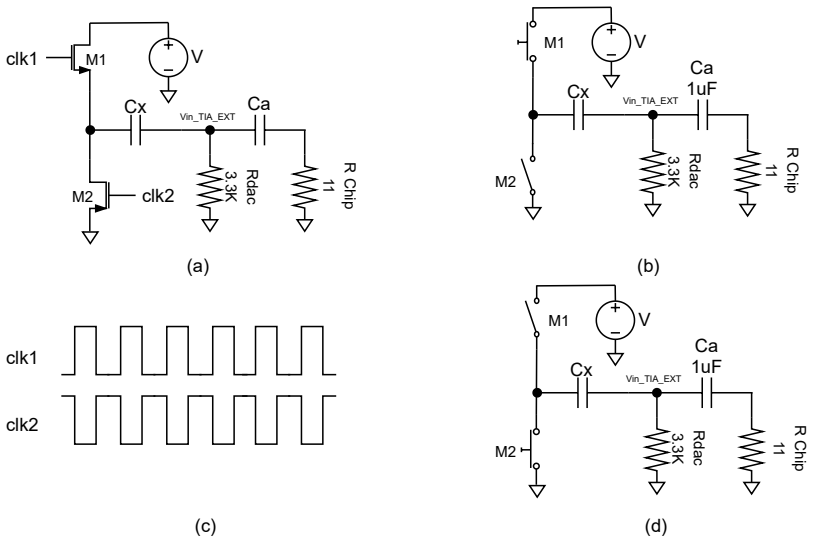

Figure 3.3: (a) Circuit at the transistor level-view. (b) 1st stage, charging the capacitors. (c) Complementary control signals. (d) second stage, discharging capacitors to the ground

$$Hs_2 = \frac{s}{s + 9.091 \cdot 10^4} \tag{3.8}$$

$$Hs_1 \cdot Hs_2 = \frac{s^2}{s^2 + 9.567 \cdot 10^5 + 7.871 \cdot 10^{10}} \tag{3.9}$$

Analyzing the resulting system, we can see that the function poles are distant, not interfering with each other. We can also notice that the pole of the filter generated by C_a and R_{chip} will not affect the current pulse(Fig 3.4). The latter is reinforced when analyzing the frequency behavior of both filters in series (Fig 3.5), considering that the current pulse will be above the frequencies of $10^8 Hz$.

The capacitor C_x must accumulate a charge Q according to the equation $Q = CV$, where the extremes of the values (minimum and maximum) are

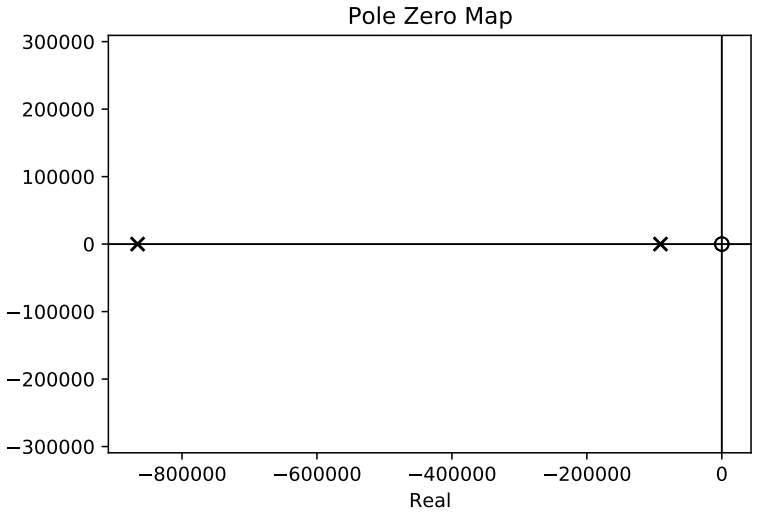

Figure 3.4: Map of poles and zeros of the equation 3.9

found in Table 2.1. Considering the previous equation, we note that a voltage V must be selected (which corresponds to the voltage V of Fig 3.3a). This voltage must be set to different values so that from an exact value of C_x, different values of load Q can be generated. It can be used from a voltage divider adjusted with a potentiometer to voltages set by a DAC (digital to analog converter) to establish this voltage. The DAC option will be chosen because it has precision and output stability assured by the manufacturer, fundamental parameters if we are looking for accuracy in the generation of Q charge.

For the election of the DAC, we must ensure three things. The resolution, the maximum voltage delivered, maximum short-circuit current.

The resolution of the DAC depends on the number of bits and the reference voltage. For a 4-bit DAC (Fig 3.6, Table 3.1) and considering a voltage

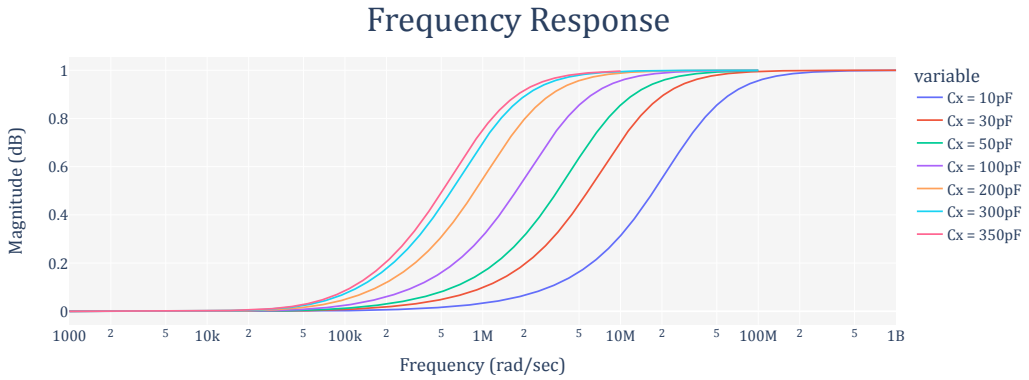

Figure 3.5: Frequency response pulse current circuit generator for different values of C_x

$V_{ref} = 3.3V$ the resolution will be given by:

$$Resolution = \frac{V_{ref}}{2n - 1} \tag{3.10}$$

, resulting in a minimum step of 0.22V. For a 12-bit DAC, the minimum step (with $V_{ref} = 3.3V$) will be $0.8mV$.

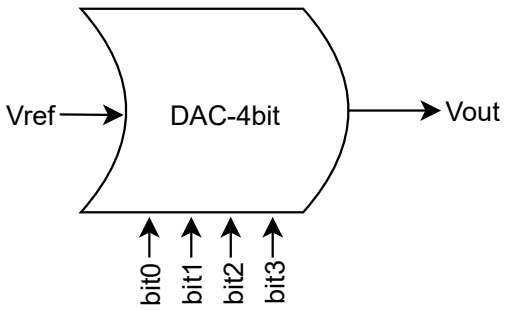

Figure 3.6: Example of 4bit-DAC

The converter's resolution will be essential so that using the load equation $Q = CV$ it is possible to generate voltages that allow having load values equal to or less than one pixel (4E-13, Table 2.1). Assuming a 12-bit DAC,

Table 3.1: 4bit-DAC reference outputs

Bits	Vout
0000	0
0001	0.22
0010	0.44
0011	0.66
...	...
1101	2.86
1110	3.08
1111	Vref

$C_x = 300pF$, $V_{ref} = 3.3V$, the minimum load generated will be:

$$Q_{min} = V_{min} * C_x = 0.8mV * 350pF = 2.4E - 13 \tag{3.11}$$

.Resulting in a charge value of less than one pixel 2.1.

The highest voltage delivered by the DAC will be approximately equal to the reference voltage of the DAC. It is essential to consider this maximum voltage since if one seeks to comply with the maximum load generation expressed in Table 2.1, C_x is fixed. This voltage must be greater than or equal to:

$$V = \frac{Q_{max}}{C}, C = C_x \tag{3.12}$$

For a maximum load value of 1.2E-9 and $C_x = 350pF$, it is $V = 3.4V$. Therefore, for a fixed C_x value and to generate the maximum load from Table 2.1, a DAC must deliver a maximum voltage greater than or equal to $3.4V$.

The short-circuit current is a value given by the converter manufacturer in the datasheet. This parameter is essential in order not to damage the DAC when the current pulses are generated. Based on Spice simulations, a

short-circuit current value greater than 100mA is recommended.

The circuit of Fig 3.3(a) was simulated in Lt-Spice with commercial transistors, considering various input voltages from $100mV$ to $3V$with a step of $200mV$. Control signals were shown in Fig 3.7. In Fig 3.8 the voltage corresponding to the connection node between the source and the source of the transistors M1 and M2, respectively, is shown. It is important to note that these transistors are operating in Triode-region because $V_{ds} \leq V_{gs} - V_t$.

Fig 3.9 shows the current pulses generated by the clk1 and clk2 control signals. Note that there are negative and positive currents. In the simulation, the current from RChip to the circuit was measured; therefore the negative currents go to the Chip.

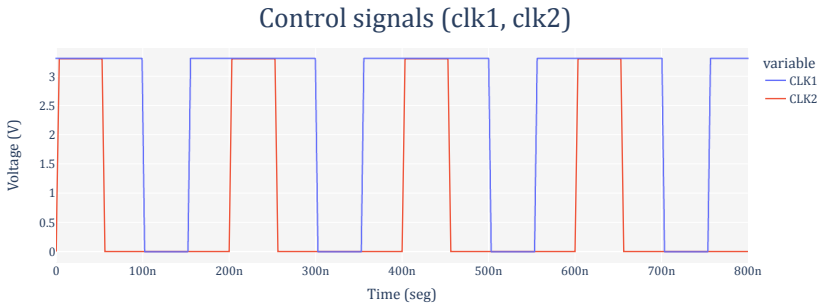

Figure 3.7: Spice simulation, control signals for M1 and M2

3.3 Control and reading mechanisms for output data.

The chip outputs are fast, on the order of nanoseconds. To implement the estimation methods presented in Chapter 2, one must be able to correctly read and process the information provided by the circuit outputs.

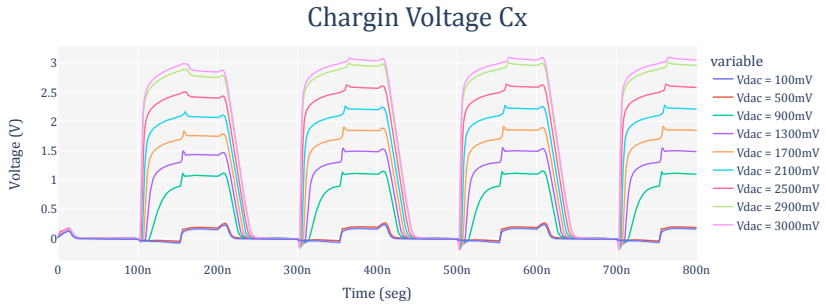

Figure 3.8: Spice simulation, charging voltage (between transistors M1 and M2)

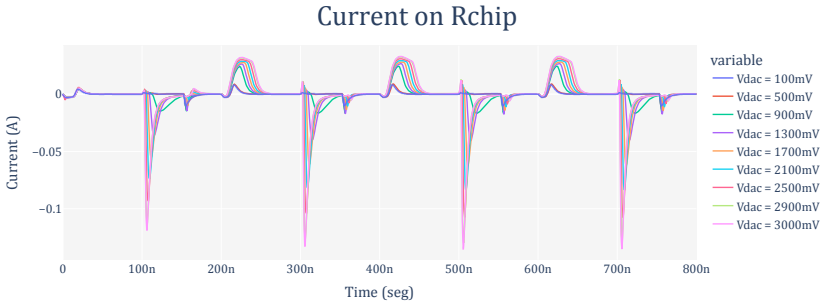

Figure 3.9: Spice simulation, current to the Chip

The following questions arise:

1. How to read the signals of Fig 2.1, 2.2, 2.3
2. How do you know when to read?
3. How much information is necessary to capture to proceed with the estimation methods mentioned in section 2.2?

3.3.1 How to read the signals of Chapter 2?

To answer question 1, it is necessary to remember that the circuit has digital $(\text{Vout}_disc) and analog (Vout_TIA, Vout_INT) outputs$.

Digital Outs

The digital outputs deliver information by changing their logic state (in this case, an on/off transition). The information provided by this signal is the time of occurrence of the arrival of photons to the detector and the approximate number of activated pixels. To detect the time of occurrence (pulse event), it is necessary to identify where the digital signal changes from high to low. Correctly capturing this information requires an additional circuit that detects with sufficient temporal definition ($<$ 5ns according to simulation data shown in Table 2.2) the on/off transition moment. To estimate the number of activated pixels, it is necessary to count how long (after the on / off transition) the discriminator signal is in a low state before changing to a high state. The duration of the Vout_DISC signals will depend proportionally on the amount of charge read by the Chip. In Table 2.2, you can read the results for specific numbers of activated pixels. Therefore, correctly capturing this information requires an additional circuit that detects this event with sufficient resolution.

Analog

The signals Vout_TIA and Vout_DISC have information encoded in amplitude, that is to say, that the maximum value measured from its initial value provides information. The data delivered by these signals correspond to the number of activated pixels and was explained in more detail in Chapter 2. These analog signals are non-periodic events, and their moment of occurrence can be controlled by actuating the load generator circuit. Like the Vout_DISC outputs, the duration of the Vout_TIA and Vout_DISC

signals will depend proportionally on the amount of load read by the Chip. The results recorded in the post-layout simulations shown in Fig 2.1, 2.2, provide us with relevant information regarding the scenario of a triggered pixel. This event will produce the fastest and lowest amplitude outputs.

3.3.2 How do you know when to read?

To answer question 2, which mentions knowing when to read, it is necessary to remember that the charge generation process can be controlled in its entirety, so it can be predicted when there will be relevant information to read from the Vout_DISC and Vout_TIA outputs. This means that it is not necessary to read or monitor the analog outputs permanently. It must also have a controllable reading system. That is to say; it allows to start and end the reading at certain times. For the digital signal of the Discriminator, it is only necessary to have a circuit that detects the transition moments on-off and off-on. See Fig 3.12.

3.3.3 How much information is necessary to capture to proceed with the estimation methods mentioned in section 2.2?

Question 3 refers to how much information is necessary to use the methodologies outlined in section 2.2. In Altamirano (2021) it is recommended to use the second approach (max amplitude) to take full advantage of the capabilities of the ASIC. For this reason, we will focus on this methodology and how it is possible to obtain enough information to implement it.

The approach called Maximum amplitude requires a reading system capable of recording the maximum amplitude of analog signals. To achieve this, it is necessary to digitally store the analog information, allowing its later analysis. This analog-digital conversion necessarily requires a specialized circuit called Analog to digital converter.

Analog to digital converter

Analog-Digital Converters (ADC) are circuits that belong to mixed-signal circuits, and these devices transform the analog signal into a digital signal using different techniques. There are various types of ADCs, each architecture employing different methodologies to achieve the conversion. Some of these ADC classes are Flash, SAR, Delta-Sigma. Regardless of the type of ADC, their functionality is to transform a continuous analog signal to a discrete signal composed of digital samples (Fig X). Every investor performs at least three processes. These processes are:

- Analog signal sampling.
- Signal quantization.
- Signal encoding.

The sampling process depends on the sampling period of the ADC (generally expressed in samples per second, SPS). This parameter is relevant when selecting an ADC. Depending on the maximum frequencies of the analog signals, at least twice the maximum frequency (Nyquist) must be sampled to recover a signal and avoid Aliasing. In practice, it is recommended at least ten times the Nyquist frequency.

The quantization of analog signals is the assignment of discrete values to the samples acquired in the sampling process. This quantization depends directly on the number of bits that the ADC has. For example, an 8-bit ADC has 2^8 possible values to assign to the sampled values. These 2^8 possible values depend on a reference voltage, this voltage being an input of the ADC. In general, the quantization process depends on the ADC selected, and the manufacturers explain these details in the device datasheets.

An explample of 4bit ADC is shown in Fig X

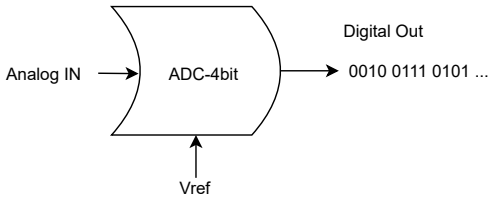

Figure 3.10: 4bit ADC. High level view.

The quantization process involves a quantization error. This error has a form of random noise. It is uniformly distributed around $\pm\frac{1}{2}LSB$ with zero mean and standard deviation given by the equation (Lutenberg (2012)):

$$\sigma = \frac{1}{\sqrt{Nbits * LSB}} \tag{3.13}$$

LSB is the Least Significant Bit (quantization step), which corresponds to the distance between two adjacent levels in a quantization. This error implies in certain situations an approximation when quantizing. For example, when the sample is between two values (of the 2 Nbits), it should be approximated to the closest (See Fig X). This error decreases according to equation 3.13 as the number of bits in the converter increases. The encoding consists of

transforming the quantized values to binary digital values, and that can be stored in a memory or be delivered to another digital circuit.

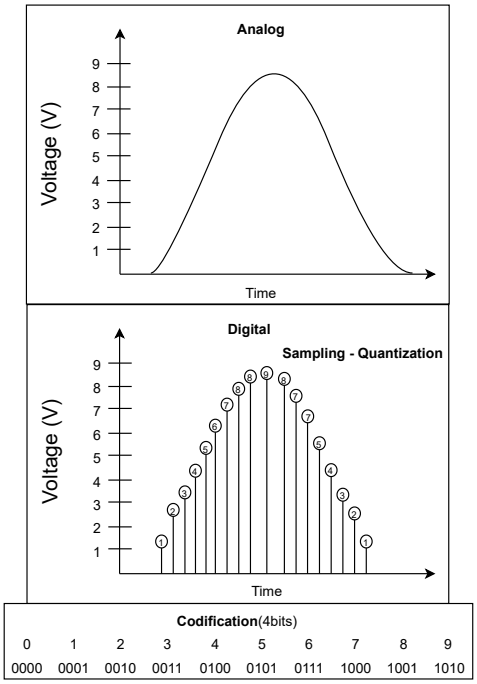

Figure 3.11: Analog to digital conversion example.

In addition to these parameters already mentioned there, are others such as the maximum bandwidth of the converter, a parameter that indicates up to which frequencies the attenuation will be less than $-3dB$. We also find the acquisition time, a parameter expressed in units of time and refers to how many units of time after sampling the signal are quantized.

In our case, the analog signals are of the order of nanoseconds, which, based on Nyquist, would imply selecting an ADC of the order of GSPS, in addition to having sufficient bit resolution to quantify the samples accurately and have a bandwidth higher than the $200MHz$, so that the Discriminator and Integrator signals are not attenuated. Using an ADC with the character-

istics mentioned above would work to obtain enough information to allow the application of the maximum breadth methodology, but the associated cost is high. Remember that the generation of analog signals depends on the load generator circuit, which makes the process controllable and reproducible in time. Considering this, a technique called sub-sampling can be applied. This technique will be described in section 3.3.4.

3.3.4 Sub-sampling

This technique consists of sampling a signal, which is fast for the acquisition system, repeatedly at different points in time. This technique allows the reconstruction of the original signal without the need for rapid sampling. Applying this technique depends on knowing, or being able to control, the moment of arrival of the signals to be processed. They must also have precise control and reading mechanisms. The ADC to implement this technique can be slower than that required by the Nyquist theorem, but it must guarantee a fast acquisition time that allows sampling at precise moments.

For the characterization of the ASIC, the charge generation process is controllable and repeatable, so it is possible to implement this technique with the appropriate elements.

In Fig 3.12 three graphs are shown in time, where the upper graph is the load trigger signal for the load generator circuit, the middle signal is a representation of one of the Chip outputs, and the graph below It is the response of the digital output of the Chip when the load greater than or equal to 1 activated pixel is received.

The sub-sampling process of the signal in the middle graph is graphically

expressed in Fig 3.13, wherein Fig 3.13(a) is shown at a certain point in time, Fig 3.13(b) at another, and so on until the different samples can reconstruct a significant part of the original signal (Fig 3.13(f)). Each of the samples can be an average of samples taken simultaneously to correct any noise that may exist.

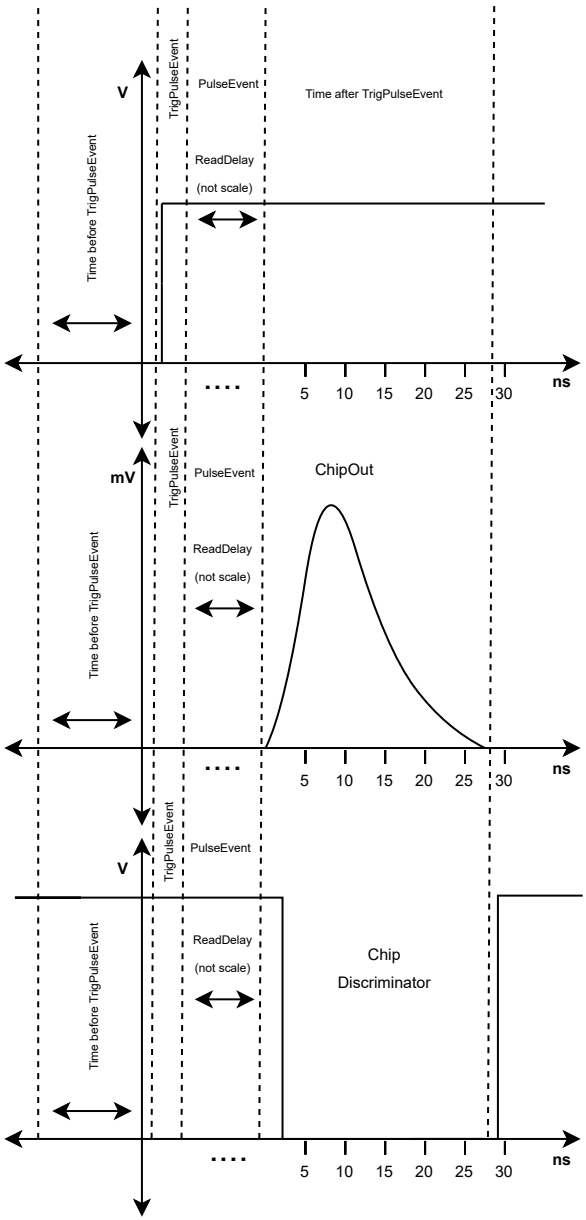

Figure 3.12: Succession of events in time

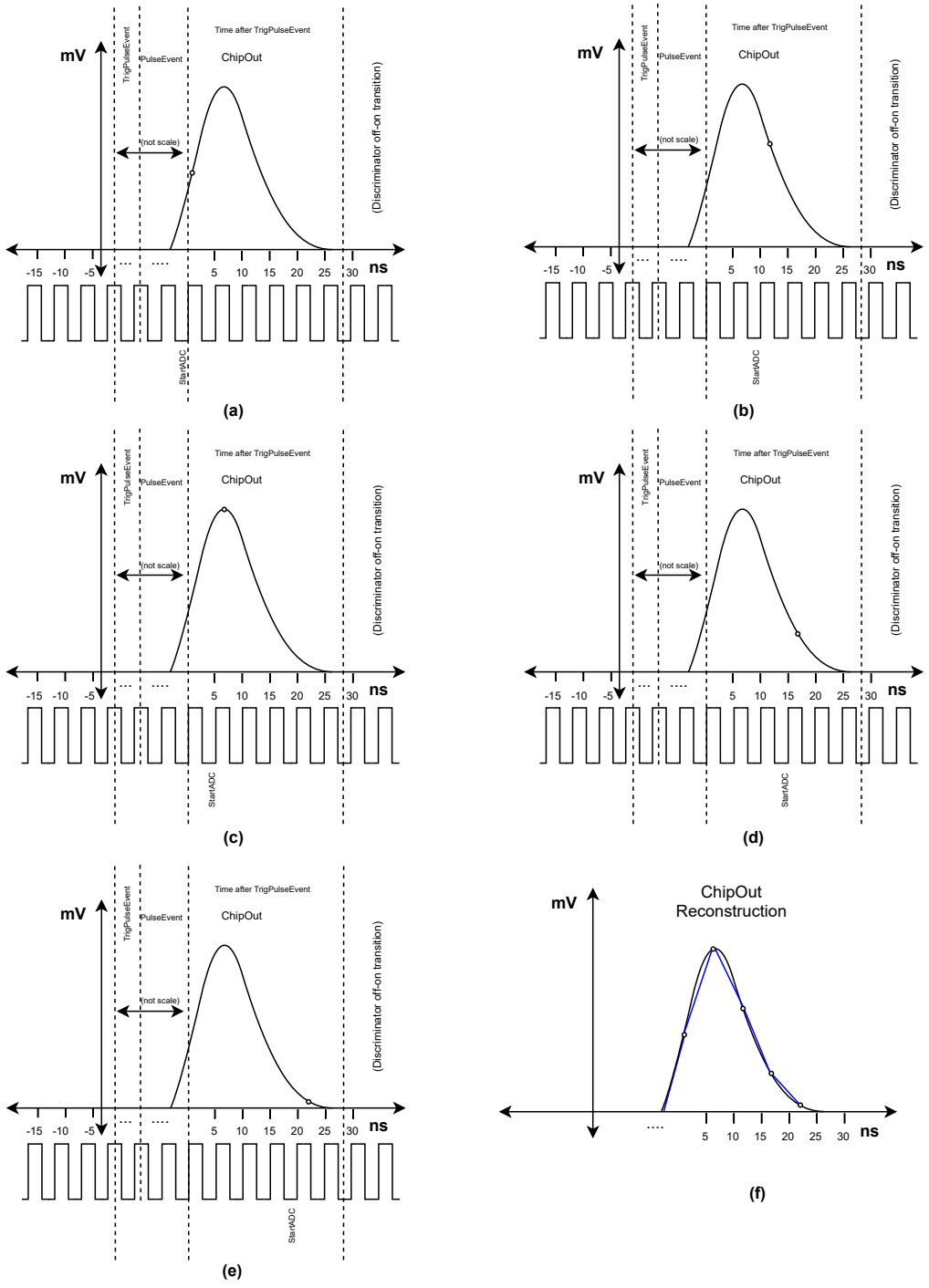

Figure 3.13: Sub-sampling methodology.

4

Implementation

To implement the methods described in the previous chapters, it is necessary to have a system that allows the control of events with nanosecond precision that provides flexibility and reconfigurations in some instances. Given the requirements, the use of an FPGA (field-programmable gate array) is proposed to implement the control mechanisms of the circuit characterization and verification process. The FPGA chosen is part of the Zynq-7000 family (Zybo Board).

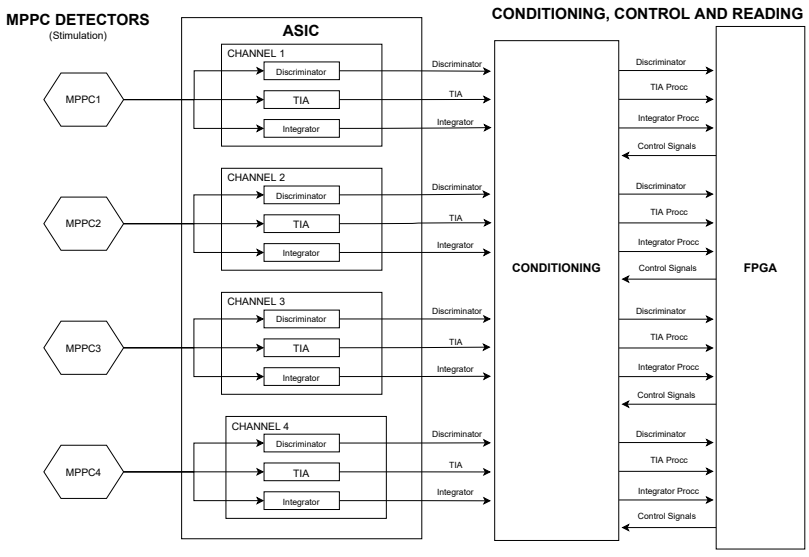

Figure 4.1: global view of the system.

A global view of the test system can be seen in Fig 4.1; it is possible to

see the MPPC detectors, the Chip and each of its channels, the outputs, a signal conditioning block, and finally, the FPGA. In the initial verification process, the MPPCs will be replaced by the load generator circuit of section 3.2. This circuit will be part of a PCB where other elements necessary for the test process will be soldered, the elaboration of this board and its specific components will be soldered. Will be presented in a later chapter.

The conditioning stage includes the analog to digital conversion of the analog signals of the Chip as well as the DAC that allows controlling the voltage V of the load generator circuits described in section 3.2, Fig 3.3.

It is also essential to consider that the Chip has 12 analog outputs, and each one delivers information. According to the requirements of Professor Abusleme and Renzo Barraza, it is not necessary to read all these signals in parallel, which allows only one ADC to be used for the entire system. However, a suitable multiplexer is required to achieve those mentioned above. The multiplexer must have a low input capacitance and a bandwidth large enough not to attenuate the chip signals. Reading the digital signals (discriminator) requires a digital circuit that will be implemented in the FPGA, which will detect the transition from high to low state and count how many times elapses will elapse until the transition from low to high state. The definition of the account of this circuit will be proportional to the FPGA clock speed. In this case, it will be 5ns, justified time if the data in Table 2.2 are analyzed.

In addition to the counter circuit, the FPGA must have other custom logic blocks, which allow, for example, to store information from the ADC quickly (on each clock edge) and be delivered to the user when requested. There

must also be logical blocks in charge of controlling the converters (ADC-DAC) to control their operation according to the mechanisms described in the datasheets of each component. Remember that the ASIC also has 4 DACs, one for each channel. The control of these blocks must also be considered in the custom blocks to be designed. In Fig 4.2, the conditioning stage and internal blocks of the FPGA can be seen in more detail. Note that the FPGA has two internal blocks, Custom logic, and Zynq Processor System. Zynq Processor System is the Xilinx manufacturer's designation for its SoC (System on Chip). In the words of the manufacturer: "Xilinx provides the Processing System IP Wrapper for the Zynq®-7000 to accelerate your design and its configuration for your embedded products. The Processing System IP is the software interface around the Zynq-7000 Processing System. The Zynq-7000 family consists of a system-on-chip (SoC) style integrated processing system (PS) and a Programmable Logic (PL) unit, providing an extensible and flexible SoC solution on a single die. The Processing System IP Wrapper acts as a logic connection between the PS and the PL while assisting you to integrate custom and embedded IPs with the processing system using the Vivado IP integrator."

Using this system, it is possible to interact with different peripherals of the ARM Cortex-A9 processor(UART, SPI, GPIOs) to facilitate the acquisition and control of custom logic through the AXI bus.

Specific components are :

- ADC: LTC2245 (Linear Technolgy)
- DAC: AD5344 (Analog devices)
- MUX: DG1207 (Maxim integrated)

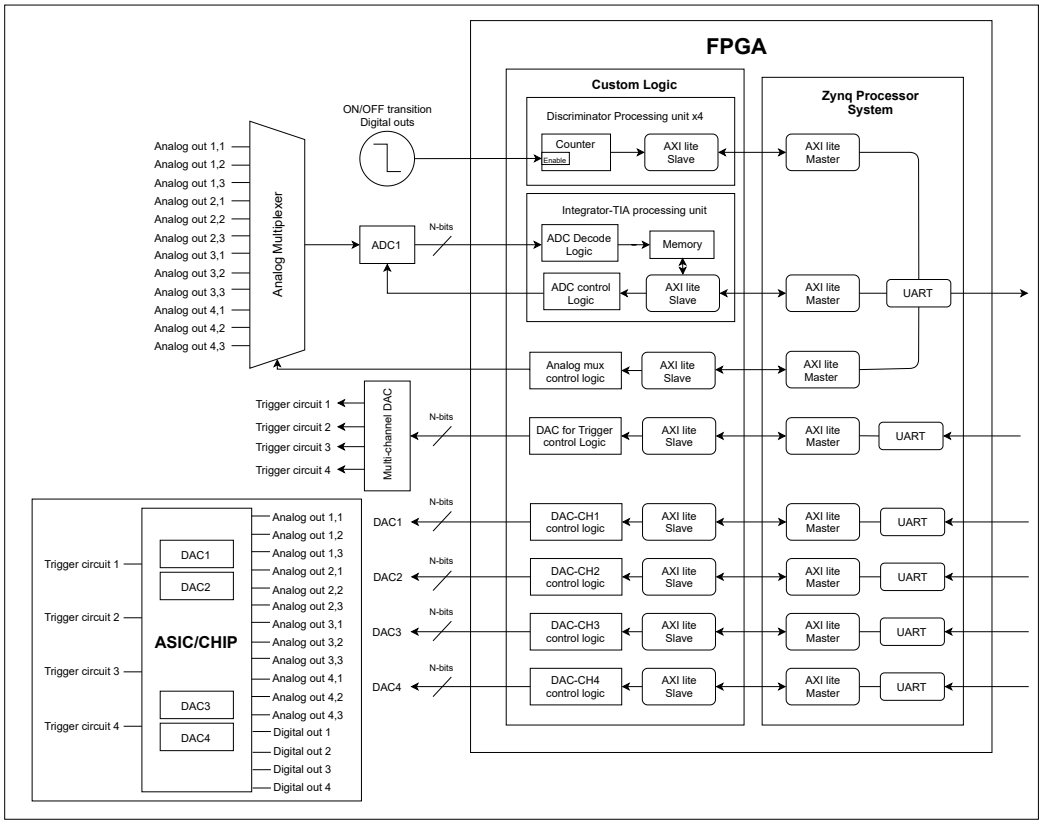

Figure 4.2: System implementation view.

5 Conclusions and future work

Based on the data provided by the chip designer in his Thesis (Altamirano, 2021), it is possible to use this information to devise a test scenario for the ASIC. The test environment must be adjusted to the physical requirements of the Chip for its correct functioning and operation. The work presented so far provides ideas and justifications for how it is planned to implement the integrated circuit characterization and validation environment. The justifications and requirements have been based in the great majority on the Thesis provided by the designer and works related to the verification of circuits with similar purposes.

5.1 Future work

As future work remains, the implementation of the digital blocks in charge of reading and controlling the elements of Fig 4.2 and the design and manufacture of a PCB where the ASIC and the other components necessary to carry out testing and characterization experiments will go.

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