EE6044 Advanced Analog IC Design – Homework 3

Question 1

1.

You have been tasked with designing a front-end preamplifier for the sensor interface of an ultra low-power wireless sensor node. An example of such a sensor is a piezoelectric device which could be used to measure industrial motor vibrations for fault detection. The specifications you have been given for this application are as follows:

Table 1.1. Front-end Preamplifier Specification

Parameter	Specification
A_v	> 50
f_u	$50MHz$
v_{out}	$> 600mVp-to-p$
$V_{OUT,Q}$	$0.6V$
V_{DD}	$1.2V$
C_L	$2pF$
$\overline{v}_n^{in}$	$\leq 250nV/\sqrt{Hz}$
I_{bias}	$4\mu A$

For simplicity, the architecture you must use is the Common Source Amplifier with Active Load, shown in Figure 1:

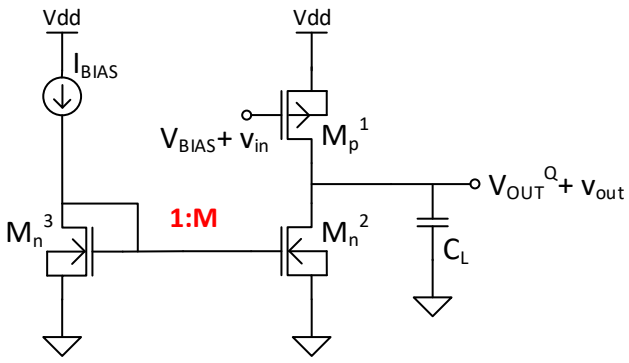

Figure 1: PMOS Input Common Source (CS) Amplifier with Active Load

a) Derive an expression for the small signal gain of the gain stage. **[5 marks]**

b) As a rule of thumb we usually set $f_T \geq 10 * f_u$. Derive an expression relating f_T, g_m/I_D and Area (WL). **[5 marks]**

c) From the CS circuit small signal model, derive an expression for the unity gain frequency f_U considering g_m/I_D of M1,the current of M1 $M * I_{bias}$, C_{dd}^1, C_{dd}^2, and C_L. **[5 marks]**

d) What is your initial estimate for g_m/I_D ratio for each transistor state why?. (Hint: low power operation of the gain stage is the design goal, balance this with the maximum V_{DSAT} that can be used for the load device M2.) **[5 marks]**

Question 2

The design is to be carried out on the Skywater 0.13μm process. In the following questions, assume the following: $V_{DD} = 1.2V$, ~~$L = 0.2\mu m$~~ $\gamma = 0.85$ for all transistors. For this question use python and the lookup functions to calculate your answers. Note that the g_m/I_D script assumes L & W in μm, all other quantities in the usual units. Remember $I_{bias} = 4\mu A$ and $V_{out}^Q = \frac{V_{DD}}{2} V$.

(a) Sweep the device length of M1 to see if the minimum gain spec of 50 can be achieved. (Hint as a simplification use the equation from 1(a) and set $g_{ds2} = 0.125 \times g_{ds1}$). Using the look_up ('GM_GDS') Produce a plot of gain versus L_1 to show the minimum length required to achieve the gain. Plot the gain for the estimated g_m/I_D from 1(a) and repeat the plot for four other g_m/I_D ratios. **[10 marks]**

(b) Setting the constraint $f_T \geq 10 * f_u$ use the look_up("GM_CGG") function to check that the L_1 and ${}^{g_m}/_{I_D}$ values from 2(a) satisfy this constraint. **[6 marks]**

(c) Take the expression for f_U from 1(c) and initially ignoring the parasitic capacitors C_{dd}^1 and C_{dd}^2 using the L_1 and ${}^{g_m}/_{I_D}$ values that satisfy 2(b) find the minimum $M * I_{Bias}$ where M is an integer that can achieve $f_U = 10MHz$. (Hint: solve the equation for M). Calculate the value of g_{m1}.

[8 marks]

(d) Using the ${}^{g_m}/_{I_D}$ values for M2 from 1(d) and the current from 2(c) find the values of L_2 and W_2 that achieve the requirement from 2(a) that $g_{ds2} = 0.125 \times g_{ds1}$. (Hint use the (lookup 'ID_W') to find W_2 and the lookup("GM_GDS") function with the ${}^{g_m}/_{I_D}$ to find L_2.

[6 marks]

Question 3

(a) From the value of γ given above, and the g_m values in 3(a), calculate the thermal spot noise current of each of the transistors. Refer this to the gate of the input transistor M_n^{M1} to obtain $\bar{v}_n^{in}$. Does this meet spec? **[9 marks]**

(b) Use the *lookupVGS* function to find the V_{GS}^{M1} and V_{GS}^{M2}. **[5 marks]**

(c) Using the equation from 1 (c) and the *lookup* function to calculate the C_{db} of M_n^{M2} and M_p^{M1}. (Cdd_M1 = PCH.look_up('CDD', VGS=Vgs_M1,) Along with the g_{m1} values obtained in Q2 (c), check that the requirement $f_U = 50MHz$ is still satisfied. **[7 marks]**

(d) If you are designing a current mirror active load would you use devices biased in weak inversion or strong inversion. Explain. **[4 marks]**

Question 4

Draw up your design in Cadence using the W and V_{BIAS} values calculated previously. Use the following analysis to validate the performance of your design:

(a) Perform DC Operating Point analysis to confirm I_D^{M1}, V_{out}^Q, $g_m I_D$, g_{ds} and C_{db} of all transistors. Confirm the headroom requirement by performing a DC sweep of the input v_{in}. **[7 marks]**

(b) Perform AC analysis to confirm the bandwidth of the circuit. **[8 marks]**

(c) Perform 'noise' analysis to confirm the thermal spot noise floor of the circuit. Plot the 'input noise' parameter from Direct Plot options. Ignore low frequency flicker noise effects. **[10 marks]**