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Logical-qubit operations in an error-detecting surface code

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Future fault-tolerant quantum computers will require storing and processing quantum data in logical qubits. Here we realize a suite of logical operations on a distance-2 surface code qubit built from seven physical qubits and stabilized using repeated error-detection cycles. Logical operations include initialization into arbitrary states, measurement in the cardinal bases of the Bloch sphere and a universal set of single-qubit gates. For each type of operation, we observe higher performance for fault-tolerant variants over non-fault-tolerant variants, and quantify the difference. In particular, we demonstrate process tomography of logical gates, using the notion of a logical Pauli transfer matrix. This integration of high-fidelity logical operations with a scalable scheme for repeated stabilization is a milestone on the road to quantum error correction with higher-distance superconducting surface codes.

Two key capabilities will distinguish an error-corrected quantum computer from present-day noisy intermediate-scale quantum (NISQ) processors[1]. First, it will initialize, transform and measure quantum information encoded in logical qubits rather than physical qubits, where a logical qubit is a highly entangled two-dimensional (2D) subspace in the larger Hilbert space of many more physical qubits. Second, it will use repetitive quantum parity checks to discretize, signal and (with the aid of a decoder) correct errors occurring in the constituent physical qubits without destroying the encoded information[2]. Provided the incidence of physical errors is below a code-specific threshold and the quantum circuits for logical operations and stabilization are fault tolerant, the logical error rate can be exponentially suppressed by increasing the distance (redundancy) of the quantum error correction (QEC) code employed[3]. So far, the exponential suppression for specific physical qubit errors (bit-flip or phase-flip) has been experimentally demonstrated[4–7] for repetition codes[8–10].

Leading experimental quantum platforms have taken key steps towards implementing QEC codes protecting logical qubits from general physical qubit errors. In particular, trapped-ion systems have demonstrated logical-level initialization, gates and measurements for single logical qubits in the Calderbank–Shor–Steane[11] and Bacon–Shor[12] codes. Most recently, entangling operations between two logical qubits have been demonstrated in the surface code using lattice surgery[13]. However, except for smaller-scale experiments using two ion species[14], trapped-ion experiments in QEC have so far been limited to a single round of stabilization.

In parallel, taking advantage of highly non-demolition measurements in circuit quantum electrodynamics[15], superconducting circuits have taken key strides in the repetitive stabilization of two-qubit entanglement[16,17] and logical qubits. Quantum memories based on 3D-cavity logical qubits in cat[18,19] and Gottesman–Kitaev–Preskill[20] codes have crossed the memory break-even point. Meanwhile, monolithic architectures have focused on logical qubit stabilization in a surface code realized with a 2D lattice of transmon qubits. Currently, the surface code[21] is the most attractive QEC code for solid-state implementation because of its practical nearest-neighbour-only connectivity requirement and high error threshold. Recent experiments[5,22] have demonstrated repetitive stabilization by post-selection in a surface code, which, due to its small size, is capable of quantum error detection but not correction. In particular, ref. [22] has demonstrated the preparation of logical cardinal states and logical measurement in two cardinal bases. In this Article, we go beyond previous work by demonstrating a complete suite of logical-qubit operations for this small (distance-2) surface code while preserving multi-round stabilization. Our logical operations include initialization anywhere on the logical Bloch sphere (with substantial improvement over previously reported fidelities), measurement in all cardinal bases and a universal set of single-qubit logical gates. For each type of operation, we quantify the increased performance of fault-tolerant variants over non-fault-tolerant ones. We use a logical Pauli transfer matrix to describe a logical gate, analogous to the procedure commonly used to describe gates on physical qubits[23]. Finally, we perform logical state stabilization by means of repeated error detection, where we compare the performance of two scalable, fault-tolerant stabilizer measurement schemes compatible with our quantum-hardware architecture[24].

The distance-2 surface code (Fig. 1a) uses four data qubits (D_1 to D_4) to encode one logical qubit, the 2D codespace of which is the even-parity (that is, eigenvalue +1) subspace of the stabilizer set:

$$\mathcal{S} = \{Z_{D1}Z_{D3}, X_{D1}X_{D2}X_{D3}X_{D4}, Z_{D2}Z_{D4}\}. \quad (1)$$

This codespace has logical Pauli operators

$$Z_L = Z_{D1}Z_{D2},\ Z_{D3}Z_{D4},\ Z_{D1}Z_{D4} \text{ and } Z_{D2}Z_{D3}, \quad (2)$$

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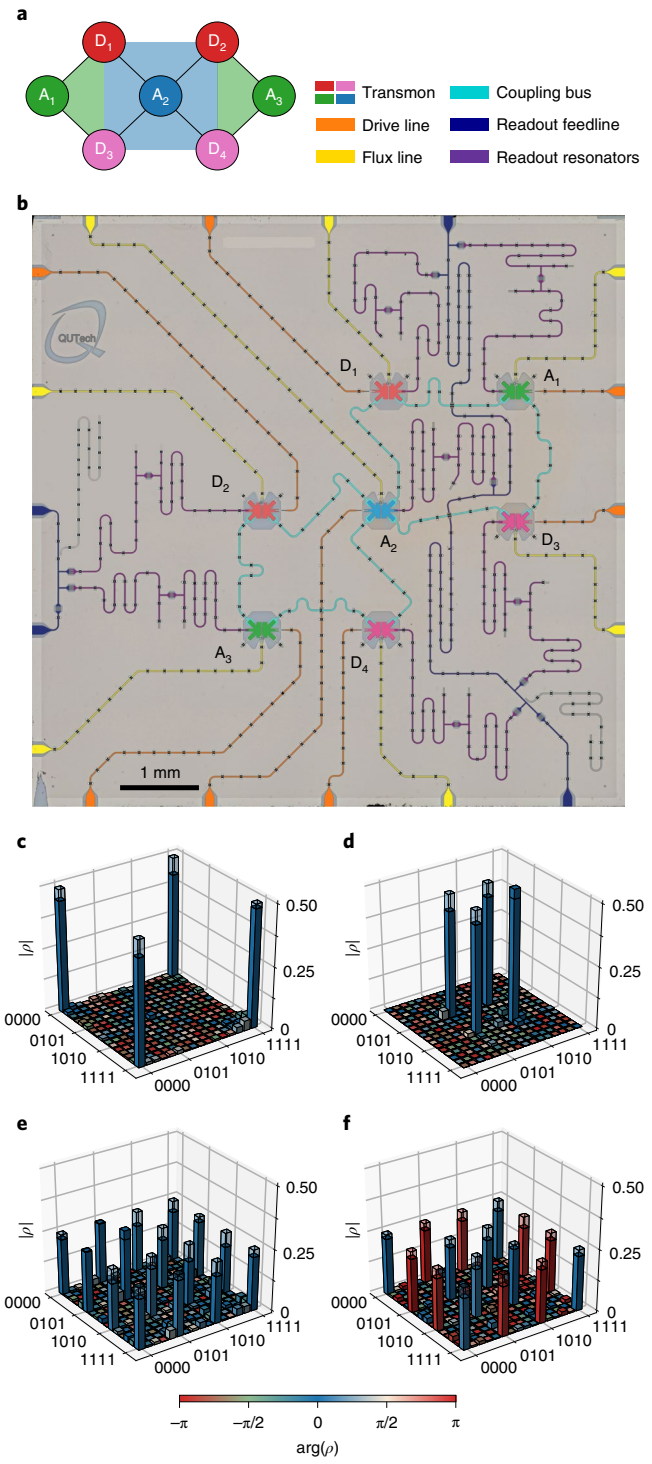

Fig. 1 | Surface-7 quantum processor and initialization of logical cardinal states. a, Distance-2 surface code. **b**, Optical image of the quantum hardware with added false colour to emphasize the different circuit elements. **c**–**f**, Estimated physical density matrices, ρ, after targeting the preparation of the logical cardinal states $|0_L\rangle$ (**c**), $|1_L\rangle$ (**d**), $|+_L\rangle$ (**e**) and $|-_L\rangle$ (**f**). Each state is measured after preparing the data qubits in $|0000\rangle$, $|1010\rangle$, $|++++\rangle$ and $|++--\rangle$, respectively. The ideal target state density matrix is shown in the shaded wireframe.

$$X_L = X_{D1}X_{D3} \text{ and } X_{D2}X_{D4}, \tag{3}$$

that anti-commute with each other and commute with $\mathcal{S}$, and the logical computational basis

$$|0_L\rangle = \frac{1}{\sqrt{2}}(|0000\rangle + |1111\rangle), \tag{4}$$

$$|1_L\rangle = \frac{1}{\sqrt{2}}(|0101\rangle + |1010\rangle). \tag{5}$$

Measuring the stabilizers using three ancilla qubits (A_1, A_2 and A_3 in Fig. 1a) allows detection of all physical errors that change the outcome of one or more stabilizers to $m=-1$. This list includes all errors on any one single qubit. However, no error syndrome is unique to a specific physical error. For example, a phase-flip in any one data qubit triggers the same syndrome: $m_{A_2}=-1$. Consequently, this code cannot be used to correct such errors. We thus perform state stabilization by post-selecting runs in which no error is detected by the stabilizer measurements in any cycle. In this error-detection context, an operation is fault tolerant if any single-fault produces a non-trivial syndrome and can therefore be post-selected out[25] (Supplementary Information).

Results

Stabilizer measurements. Achieving high performance in a code hinges on performing projective quantum parity (stabilizer) measurements with high assignment fidelity, meaning one can accurately discriminate parity, and low additional backaction such that the state of the qubits after the measurement is properly projected onto the parity subspace. We implement each of the stabilizers in $\mathcal{S}$ using a standard indirect-measurement scheme[26,27] with a dedicated ancilla. We benchmark the accuracy of each parity measurement by preparing the data qubits in a computational state and measuring the probability of ancilla outcome $m_A=-1$. As a fidelity metric, we calculate the average probability to correctly assign the parity $Z_{D1}Z_{D3}$, $Z_{D1}Z_{D2}Z_{D3}Z_{D4}$ and $Z_{D1}Z_{D3}$, finding 94.2%, 86.1% and 97.2%, respectively (Supplementary Fig. 2).

Logical-state initialization using stabilizer measurements. A practical means to quantify the backaction of stabilizer measurements is to use them to initialize logical states. As proposed in ref. [22], we can prepare arbitrary logical states by first initializing the data-qubit register in the product state

$$|\psi\rangle = (C_{\theta/2}|0\rangle + S_{\theta/2}|1\rangle)|0\rangle\left(C_{\theta/2}|0\rangle + S_{\theta/2}e^{i\phi}|1\rangle\right)|0\rangle \tag{6}$$

using single-qubit rotations R_y^θ on D_1 and R_ϕ^θ on D_3 acting on $|0000\rangle$ ($C_\alpha=\cos\alpha$ and $S_\alpha=\sin\alpha$). A follow-up round of stabilizer measurements ideally projects the four-qubit state onto the logical state

$$|\psi_L\rangle = \left(C_{\theta/2}^2|0_L\rangle + S_{\theta/2}^2e^{i\phi}|1_L\rangle\right)/\sqrt{C_{\theta/2}^4 + S_{\theta/2}^4} \tag{7}$$

with probability

$$P = \frac{1}{2}\left(C_{\theta/2}^4 + S_{\theta/2}^4\right). \tag{8}$$

We use this procedure to target initialization of the logical cardinal states $|0_L\rangle$, $|1_L\rangle$, $|+_L\rangle = (|0_L\rangle + |1_L\rangle)/\sqrt{2}$ and $|-_L\rangle = (|0_L\rangle - |1_L\rangle)/\sqrt{2}$. For the first two states, the procedure is fault tolerant according to the definition above. We characterize the produced states using full four-qubit state tomography including readout calibration and maximum-likelihood estimation (MLE; Fig. 1c–f). The fidelities F_{4Q} to the ideal four-qubit

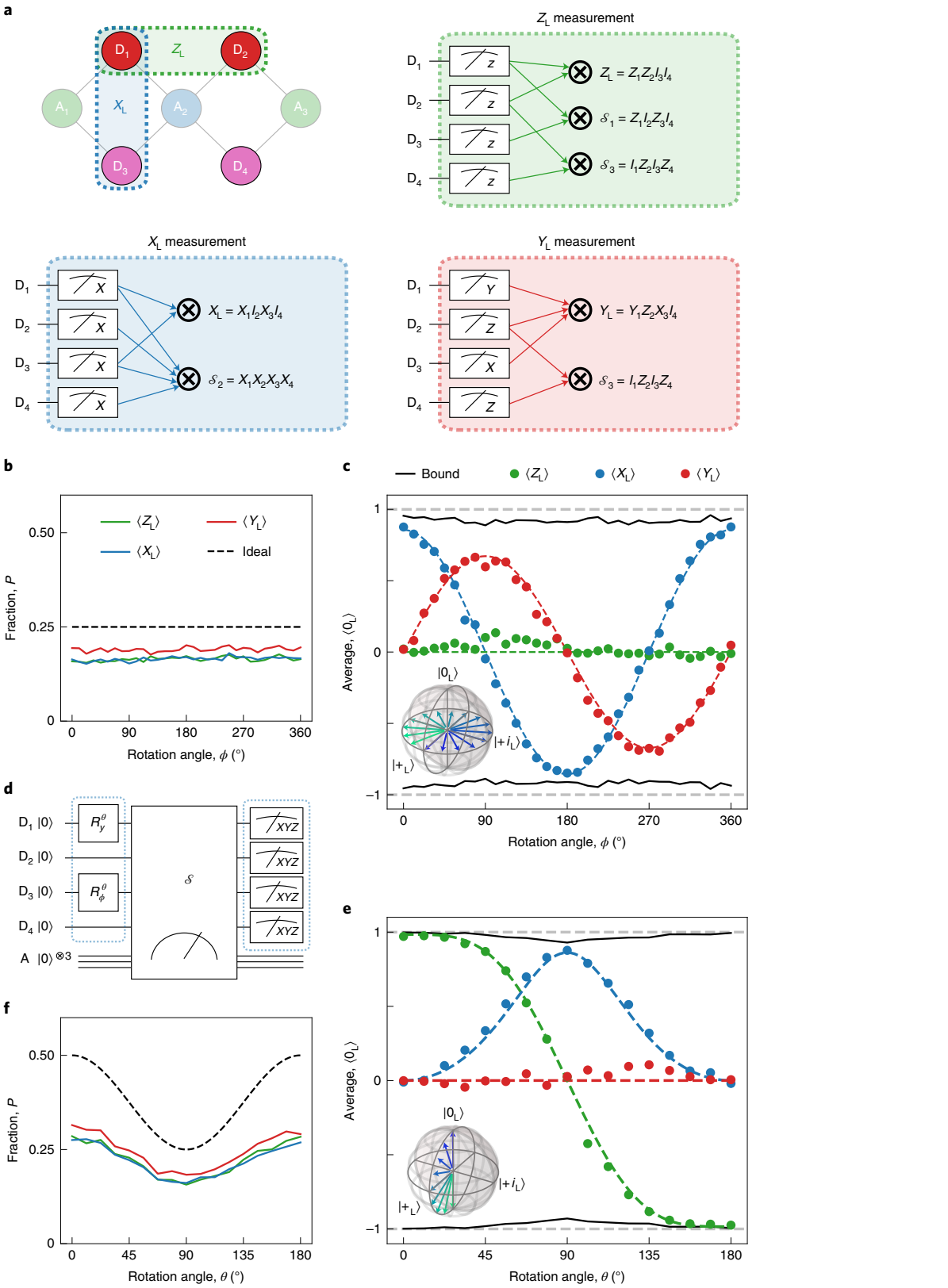

Fig. 2 | Arbitrary logical-state initialization and measurement in the logical cardinal bases. a, Assembly of the data-qubit measurements used to evaluate logical operators Z_L, X_L and Y_L with additional error detection. **d**, Initialization of logical states using the procedure described in equation (6). **c**,**e**, Z_L, X_L and Y_L logical measurement results as a function of gate angles ϕ (**c**) and θ (**e**). The coloured dashed curves show fits of the analytical predictions based on equations (9) and (11) to the data, the black curve denotes a bound based on the measured F_L of each state and the grey dashed lines denote the maximum and minimum expectation values. **b**,**f**, Total fraction P of post-selected data as a function of the input angle for each logical measurement. The dashed lines show the ideal fraction given by equation (8).

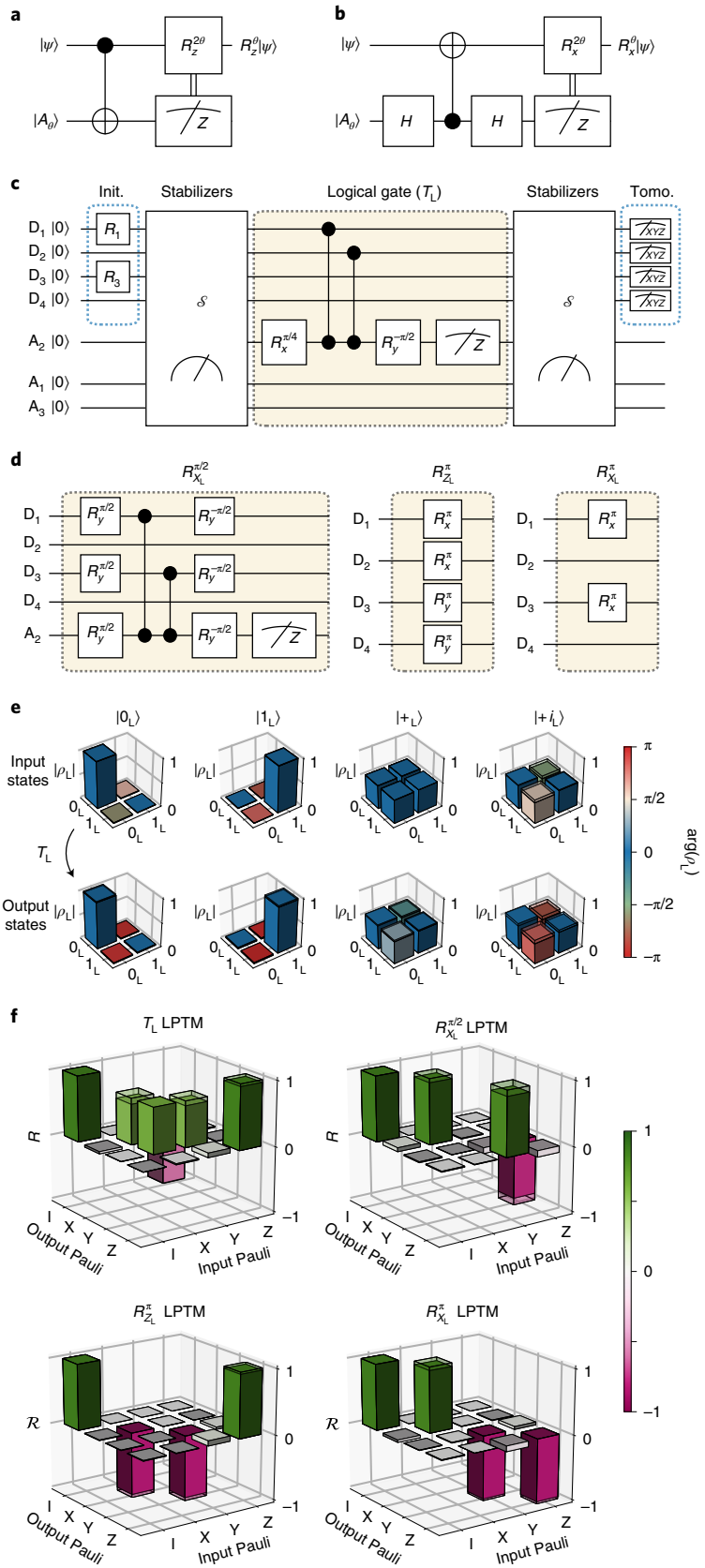

Fig. 3 | Logical gates and their characterization. a,**b**, General gate-by-measurement schemes realizing arbitrary rotations around the Z (**a**) and X (**b**) axes of the Bloch sphere. **c**, Process tomography experiment for the T_L gate. Input cardinal logical states are initialized using the method of Fig. 2. Output states are measured following a second round of stabilizer measurements. **d**, Logical $R_{X_L}^{\pi/2}$, $R_{Z_L}^{\pi}$ and $R_{X_L}^{\pi}$ gates compiled using our hardware-native gateset. **e**, Logical state tomography of input and output states of the T_L gate. These logical density matrices are obtained by performing four-qubit tomography of the data qubits and then projecting onto the codespace. **f**, Extracted (solid) and ideal (wireframe) logical Pauli transfer matrices, $\mathcal{R}$.

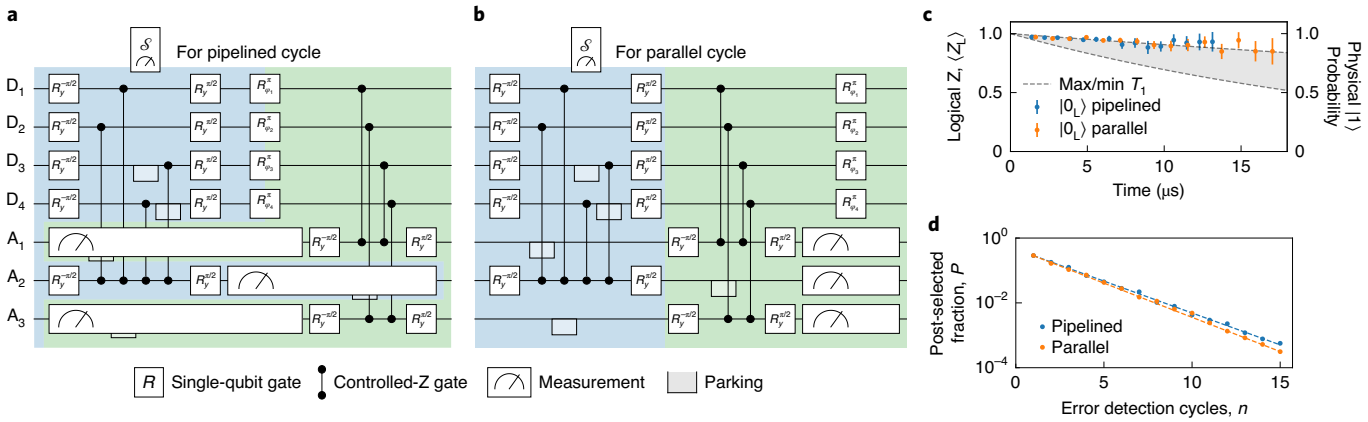

Fig. 4 | Repetitive error detection using pipelined and parallel stabilizer measurement schemes. a,b, Gate sequences used to implement the pipelined (**a**) and parallel (**b**) stabilizer measurement schemes. The gate duration is 20 ns for single-qubit gates, 60 ns for controlled-Z (CZ) gates and parking[16,24] and 540 ns for ancilla readout. The order of CZs in the $X_{D1}X_{D2}X_{D3}X_{D4}$ stabilizer (blue-shaded region) prevents the propagation of ancilla errors into logical qubit errors[25]. The total cycle duration for the pipelined (parallel) scheme is 840 ns (1,000 ns). **c**, Estimated Z_L expectation value $\langle Z_L\rangle$, measured for the $|0_L\rangle$ state, versus the duration of the experiment using the pipelined (blue) and the parallel (orange) schemes. We also plot the excited-state probability (right axis) set by the maximum and minimum physical qubit T_1. **d**, Post-selected fraction of data versus the number of error detection cycles n for the pipelined (blue) and parallel (orange) scheme.

target states are 90.0±0.3%, 92.9±0.2%, 77.3±0.5% and 77.1±0.5%, respectively. For each state, we can extract a logical fidelity F_L by further projecting the obtained four-qubit density matrix onto the codespace[22], finding 99.83±0.08%, 99.97±0.04%, 96.82±0.55% and 95.54±0.55%, respectively (Methods). This sharp increase from F_{4Q} to F_L demonstrates that the vast majority of errors introduced by the parity check are weight-1 and detectable. A simple modification makes the initialization of $|+_L\rangle$ ($|-_L\rangle$) also fault tolerant—initialize the data-qubit register in a different product state, namely $|++++\rangle$ ($|++--\rangle$), before performing the stabilizer measurements. With this modification, F_{4Q} increases to 85.4±0.3% (84.6±0.3%) and F_L to 99.78±0.09% (99.64±0.17%), matching the performance achieved when targeting $|0_L\rangle$ and $|1_L\rangle$.

Logical measurement of arbitrary states. A key feature of a code is the ability to measure logical operators. In the surface code, we can measure X_L (Z_L) fault tolerantly, albeit destructively, by simultaneously measuring all data qubits in the X (Z) basis to obtain a string of data-qubit outcomes (each +1 or −1). The value assigned to the logical operator is the computed product of data-qubit outcomes as prescribed by equations (3) and (2). Additionally, the outcome string is used to compute a value for the stabilizer(s) $X_{D1}X_{D2}X_{D3}X_{D4}$ ($Z_{D1}Z_{D3}$ and $Z_{D2}Z_{D4}$), enabling a final step of error detection (Fig. 2a). Measurement of $Y_L = +iX_LZ_L = Y_{D1}Z_{D2}X_{D3}$ is not fault tolerant. However, we lower the logical assignment error by also measuring D_4 in the Z basis to compute a value for $Z_{D2}Z_{D4}$ and thereby detect bit-flip errors in D_2 and D_4.

We demonstrate Z_L, X_L and Y_L measurements on logical states prepared on two orthogonal planes of the logical Bloch sphere. Setting $\theta=\pi/2$ and sweeping ϕ, we ideally prepare logical states on the equator (Fig. 2d):

$$|\psi_L\rangle = \left(|0_L\rangle + e^{i\phi}|1_L\rangle\right)/\sqrt{2}. \quad (9)$$

We measure the produced states in the Z_L, X_L and Y_L bases and obtain experimental averages $\langle Z_L\rangle$, $\langle X_L\rangle$ and $\langle Y_L\rangle$. As expected, we observe sinusoidal oscillations in $\langle X_L\rangle$ and $\langle Y_L\rangle$ and near-zero $\langle Z_L\rangle$. The reduced range of the $\langle Y_L\rangle$ oscillation evidences the non-fault-tolerant nature of the Y_L measurement. A second manifestation is the higher fraction P of post-selected data for Y_L (Fig. 2b). To quantify the logical assignment fidelity F_L^R with correction for initialization error, it is tempting to apply the formula

$$\frac{\langle O_L\rangle_{max} - \langle O_L\rangle_{min}}{2} = (2F_L^R - 1)(2F_L - 1),\ O \in \{X, Y\} \quad (10)$$

inspired by the standard method to quantify the readout fidelity of physical qubits from Rabi oscillations with limited initialization fidelity (described in the Supplementary Information). This method suggests $F_L^R = 95.8\%$ for X_L and 87.5% for Y_L. However, this method is not accurate for a logical qubit, because not all input states outside the codespace are rejected by the limited set of stabilizer checks computable from the data-qubit outcome string and, moreover, detectable initialization errors can become undetectable when compounded with data-qubit readout errors. An accurate method to extract F_L^R based on the measured 16×16 data-qubit assignment probability matrix (detailed in the Supplementary Information) gives $F_L^R = 98.7\%$ for X_L and 91.4% for Y_L.

Setting $\phi=0$ and sweeping θ, we then prepare logical states on the X_L–Z_L plane (Fig. 2e), ideally

$$|\psi_L\rangle = \left(C_{\theta/2}^2|0_L\rangle + S_{\theta/2}^2|1_L\rangle\right)/\sqrt{C_{\theta/2}^4 + S_{\theta/2}^4}. \quad (11)$$

Note that, due to the changing overlap of the initial product state with the codespace, fraction P is now a function of θ (equation (8)). The approximate extraction method based on the range of $\langle Z_L\rangle$ suggests $F_L^R = 99.4\%$, whereas the accurate method gives 99.8%. Note that, although both are fault tolerant, the Z_L measurement has higher fidelity than the X_L measurement as the former is only vulnerable to vertical double bit-flip errors, but the latter is vulnerable to both horizontal and diagonal double phase-flip errors.

Logical gates. Finally, we demonstrate a suite of gates enabling universal logical-qubit control (Fig. 3). Full control of the logical qubit requires a gateset comprising Clifford and non-Clifford logical gates. Some Clifford gates, like $R_{Z_L}^{\pi}$ and $R_{X_L}^{\pi}$ (where $R_{O_L}^{\theta} = e^{-i\theta O_L/2}$), can be implemented transversally and therefore fault tolerantly (Fig. 3d). We perform arbitrary rotations (generally non-fault tolerant)

Table 1 | Summary of logical initialization, measurement and gate operations and their performance

Logical operation		Characteristic	Logical fidelity metric	Value (%)
Initialization	$\|0_L\rangle$	FT	F_L	99.83
	$\|1_L\rangle$	FT		99.97
	$\|+_L\rangle$	Non-FT/FT		96.82/99.78
	$\|-_L\rangle$	Non-FT/FT		95.54/99.64
Measurement	Z_L	FT	F_L^R	99.8
	X_L	FT		98.7
	Y_L	Non-FT		91.4
Gate	$R^{\pi}_{X_L}$	FT	F_L^G	97.9
	$R^{\pi}_{Z_L}$	FT		98.1
	$R^{\pi/2}_{X_L}$	Non-FT		95.6
	T_L	Non-FT		97.3

Fault-tolerant operations are labelled 'FT' and non-fault-tolerant ones 'Non-FT'. Quoted F_L^R values are those extracted with the accurate method described in the Supplementary Information.

about the Z_L axis using the standard gate-by-measurement circuit[28] shown in Fig. 3a. In our case, the ancilla is physical (A_2), while the qubit transformed is our logical qubit. The rotation angle θ is set by the initial ancilla state $|A_\theta\rangle = (|0\rangle + e^{i\theta}|1\rangle)/\sqrt{2}$. Because we cannot do binary-controlled Z_L rotations, we simply post-select runs in which the measurement outcome is $m_{A2} = +1$. However, we note that these gates can be performed deterministicaly using 'repeat until success'[29]. Choosing $\theta = \pi/4$ implements the non-Clifford $T_L = R^{\pi/4}_{Z_L}$ gate. A similar circuit (Fig. 3b) can be used to perform arbitrary rotations around the X_L axis. We compile both circuits using our hardware-native gateset (Fig. 3c,d). To assess logical-gate performance, we perform logical process tomography using the procedure illustrated in Fig. 3e for T_L. First, we initialize into each of the six logical cardinal states $\{|0_L\rangle, |1_L\rangle, |+_L\rangle, |-_L\rangle, |+i_L\rangle, |-i_L\rangle\}$. We characterize each actual input state by four-qubit state tomography and project to the codespace to obtain a logical density matrix. Next, we similarly characterize each output state produced by the logical gate and a second round of stabilizer measurements to detect errors occurring in the gate (full data are provided in Supplementary Fig. 3). Using this over-complete set of input–output logical-state pairs, combined with MLE (Methods), we extract a logical Pauli transfer matrix (LPTM). The resulting LPTMs for the non-fault-tolerant T_L and $R^{\pi/2}_{X_L}$ gates as well as the fault-tolerant $R^{\pi}_{Z_L}$ and $R^{\pi}_{X_L}$ are shown in Fig. 3e. From the LPTMs, we extract average logical-gate fidelities F_L^G (equation (19)) of 97.3%, 95.6%, 97.9% and 98.1%, respectively.

Pipelined versus parallel stabilizer measurements. A scalable control scheme is fundamental to realize surface codes with large code distance. To this end, we now compare the performance of two schemes suitable for the quantum-hardware architecture proposed in ref. [24]. These schemes are scalable in the sense that their cycle duration remains independent of code distance. The pipelined scheme interleaves the coherent operations and ancilla readout steps associated with stabilizer measurements of type X and Z by performing the coherent operations of X (Z) type stabilizers during the readout of Z (X) type stabilizers (Fig. 4a). The parallel scheme performs all ancilla readouts simultaneously (Fig. 4b). The pipelined cycle scheme duration is shorter than the parallel scheme by 16%, which can potentially increase the performance of the code. This only occurs if the interleaved readout of ancillas does not result in increased measurement-induced dephasing between them. To compare their performance, we initialize and stabilize $|0_L\rangle$ for up to $n = 15$ cycles. We perform refocusing pulses ($R^{\pi}_{\varphi_i}$) on the data qubits to correct for coherent errors during the measurement of ancilla qubits. We also separately calibrate the equatorial rotation axis of this gate for each scheme to extract the best performance. At each n, we take data back to back for the two schemes to minimize the effect of parameter drift, repeating each experiment up to 256×10^3 times. Figure 4c shows the Z_L measurement outcome averaged over the post-selected runs. We extract the error-detection rate γ from the n-dependence of the fraction of post-selected data P (Fig. 4d) using the procedure described in the Methods. We observe that the error rate is slightly lower for the pipelined scheme ($\gamma_{pip} \approx 45\%$), most probably due to the shorter duration of the cycle. This superiority is consistent across different input logical states (Supplementary Fig. 4) with an average ratio $\gamma_{pip}/\gamma_{par}$ of 97%.

Discussion

We have demonstrated a suite of logical-level initialization, gate and measurement operations in a distance-2 superconducting surface code undergoing repetitive stabilizer measurements. For each type of logical operation we have quantified the increased performance of fault-tolerant variants over non-fault-tolerant variants. Table 1 summarizes all the results. We can initialize the logical qubit to any point on the logical Bloch sphere, with logical fidelity surpassing that shown in ref. [22]. In addition to characterizing initialized states using full four-qubit tomography, we also demonstrate logical measurements in all logical cardinal bases. Finally, we demonstrate a universal single-qubit set of logical gates by performing logical process tomography, using the concept of a logical-level Pauli transfer matrix. As expected, the fidelity of the fault-tolerant gates is higher than that of the non-fault-tolerant ones. However, one would expect a sharper difference given the typical error rates of the operations involved. We believe that this could be due to errors introduced by the stabilizer measurements, which might be dominant over the errors of the logical gate itself.

With a view towards implementing higher-distance surface codes using our quantum-hardware architecture[24], we compared the performance of two scalable stabilization schemes: pipelined and parallel measurement schemes. In this comparison, two main factors compete. On the one hand, the shorter cycle time favours pipelining. On the other hand, the pipelining introduces extra dephasing on ancilla qubits of one type during readout of the other. The performance of both schemes is comparable, but slightly higher for the pipelined scheme. From detailed density-matrix simulations, as discussed in the Supplementary Information, we further understand that conventional qubit errors such as energy relaxation, dephasing and readout assignment error alone do not fully account for the net error-detection rate observed in the experiment (Supplementary Fig. 10) and also not for the P reduction in Fig. 2b,f (Supplementary Fig. 11). We believe that the dominant error source is instead leakage to higher transmon states incurred during CZ gates. Our data (Supplementary Fig. 9) show that the error-detection scheme successfully post-selects leakage errors in both the ancilla and data qubits. Learning to identify these non-qubit errors and to correct them without post-selection is the subject of ongoing research[30–32] and an outstanding challenge in the quest for quantum fault tolerance with higher-distance superconducting surface codes[33], which so far have yet to be implemented with repeated error correction.

Online content

Any methods, additional references, Nature Research reporting summaries, source data, extended data, supplementary information, acknowledgements, peer review information; details of author contributions and competing interests; and statements of data and code availability are available at https://doi.org/10.1038/s41567-021-01423-9.

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Methods

Device. We used a superconducting circuit-QED processor (Fig. 1b) featuring the quantum-hardware architecture proposed in ref. [24]. In this arrangement, seven flux-tunable transmons are arranged in three frequency groups: a high-frequency group for D_1 and D_2, a middle-frequency group for A_1, A_2 and A_3, and a low-frequency group for D_3 and D_4. Similar to the device in ref. [22], each transmon is transversely coupled to its nearest neighbours using a coupling bus resonator dedicated to each pair. This most simple and minimal connectivity minimizes multi-qubit crosstalk. Also, every transmon has a dedicated flux line for two-qubit gating, and a dispersively coupled readout resonator with Purcell filter enabling frequency-multiplexed readout[17,34] using two feedlines. In contrast to ref. [22], every transmon has a dedicated microwave drive line for single-qubit gating, avoiding the need to drive any via a feedline and thus reducing driving crosstalk.

All transmons were flux-biased to their maximal frequency (that is, the flux sweetspot[35]), where the measured qubit relaxation (T_1) and dephasing (T_2) times lie in ranges of 27–102 µs and 55–117 µs, respectively. Detailed information on the implementation and performance of single- and two-qubit gates for this same device is available in ref. [36]. Device characteristics are also summarized in Supplementary Table 1.

The device was fabricated on a high-resistivity intrinsic Si<100> wafer that was first descummed using a UV-ozone cleaner and stripped of native oxides using buffered oxide etch solution (BOE 7:1). The wafer was subjected to hexamethyldisilazane vapour at 150 °C and sputtered with 200 nm of niobium titanium nitride (NbTiN). After dicing into smaller dies, a layer of hydrogen silsesquioxane (HSQ) was spun and baked at 300 °C to serve as an inorganic sacrificial mask for wet etching of NbTiN. This layer was removed after base-patterning steps. The quantum plane was defined using electron-beam lithography of a high-contrast, positive-tone resist spun on top of the NbTiN–HSQ stack. Post development, the exposed region was first dry-etched using a SF_6/O_2 mixture and then wet-etched to remove any residual metal. Dolan-bridge-style Al/AlO_x/Al Josephson junctions were then fabricated using standard double-angle electron-beam evaporation. Air bridges and crossovers were added using a two-step process. The first step involved patterning a galvanic contact using electron-beam resist (~6 µm thick) subjected to reflow. In the second step, the air bridges and crossovers were patterned with electron-beam-evaporated Al (450 nm thick). Finally, the device underwent dicing, resist liftoff and Al wirebonding to a printed circuit board.

State tomography. To perform state tomography on the prepared logical states, we measured the 4^4-1 expectation values of data-qubit Pauli observables, $p_i=\langle\sigma_i\rangle$, $\sigma_i\in\{I, X, Y, Z\}^{\otimes 4}$ (except $I^{\otimes 4}$). Interleaved with this measurement we also characterized the measurement positive operator-valued measure (POVM) used to correct for readout errors in p_i. These were then used to construct the density matrix

$$\rho=\sum_{i=0}^{4^4-1}\frac{p_i\sigma_i}{2^4} \tag{12}$$

with $p_0=1$, corresponding to $\sigma_0=I^{\otimes 4}$. Because of statistical uncertainty in the measurement, constructed state ρ might lack the physicality characteristic of a density matrix; that is, $\mathrm{Tr}(\rho)=1$ and $\rho\geq 0$. Specifically, ρ might not satisfy the latter constraint, while the former is automatically satisfied by $p_0=1$. To enforce these constraints, we used a maximum-likelihood method[23] to find the physical density matrix ρ_{ph} closest to the measured state, where closeness is defined in terms of best matching the measurement results. We thus minimized the cost function $\sum_{i=0}^{4^4-1}\left|p_i-\mathrm{Tr}(\rho_{\mathrm{ph}}\sigma_i)\right|^2$, subject to $\mathrm{Tr}(\rho_{\mathrm{ph}})=1$ and $\rho_{\mathrm{ph}}\geq 0$. We found the optimal $\rho_{\mathrm{ph}}^{\mathrm{opt}}$ using the convex-optimization package cvxpy via cvx-fit in Qiskit[37]. The fidelity to a target pure state, $|\psi\rangle$, was then computed as

$$F=\langle\psi|\,\rho_{\mathrm{ph}}^{\mathrm{opt}}\,|\psi\rangle. \tag{13}$$

One can further project ρ_{ph} onto the codespace to obtain a logical state ρ_{L} using

$$\rho_{\mathrm{L}}=\frac{1}{2}\sum_i\frac{\mathrm{Tr}(\rho_{\mathrm{ph}}\sigma_i^{\mathrm{L}})}{\mathrm{Tr}(\rho_{\mathrm{ph}}I_{\mathrm{L}})}\sigma_i^{\mathrm{L}}\quad,\quad\sigma_i^{\mathrm{L}}\in\{I_{\mathrm{L}},\,X_{\mathrm{L}},\,Y_{\mathrm{L}},\,Z_{\mathrm{L}}\} \tag{14}$$

where I_{L} is the projector onto the codespace. Here, we can compute the logical fidelity F_{L} using equation (13).

Process tomography in the codespace. A general single-qubit gate can be described[23] by a Pauli transfer matrix (PTM) $\mathcal{R}$ that maps an input state described by $p_i=\langle\sigma_i\rangle$, $\sigma_i\in\{I, X, Y, Z\}$, with $p_0=1$, to an output state p':

$$p_j'=\sum_i\mathcal{R}_{ij}p_i. \tag{15}$$

To construct $\mathcal{R}$ in the codespace, we used an over-complete set of input states, $\{|0_{\mathrm{L}}\rangle,\,|1_{\mathrm{L}}\rangle,\,|+_{\mathrm{L}}\rangle,\,|-_{\mathrm{L}}\rangle,\,|+i_{\mathrm{L}}\rangle,\,|-i_{\mathrm{L}}\rangle\}$, and their corresponding output states and performed linear inversion. The input and output logical states were characterized using state tomography of the data qubits to find the four-qubit state ρ, which was then projected to the codespace using

$$p_i^{\mathrm{L}}=\frac{\mathrm{Tr}(\rho\sigma_i^{\mathrm{L}})}{\mathrm{Tr}(\rho I_{\mathrm{L}})}\quad,\quad\sigma_i^{\mathrm{L}}\in\{I_{\mathrm{L}},\,X_{\mathrm{L}},\,Y_{\mathrm{L}},\,Z_{\mathrm{L}}\}. \tag{16}$$

We found that all the measured logical states already satisfy the constraints of a physical density matrix. This is likely to happen as one-qubit states that are not very pure usually lie within the Bloch sphere, even within the uncertainty in the measurement. The constructed LPTM, however, might not satisfy the constraints of a physical quantum channel, that is, trace preservation and complete positivity (TPCP). These are better expressed by switching from the PTM representation to the Choi representation. The Choi state $\rho^{\mathcal{R}}$ can be computed as

$$\rho^{\mathcal{R}}=\frac{1}{4}\sum_{i,j}\mathcal{R}_{ij}\,\sigma_j^T\otimes\sigma_i, \tag{17}$$

where the first tensor-product factor corresponds to an auxiliary subsystem. The TPCP constraints are $\mathrm{Tr}(\rho_{\mathrm{ph}}^{\mathcal{R}})=1$, $\rho_{\mathrm{ph}}^{\mathcal{R}}\geq 0$ and $\mathrm{Tr}_1(\rho_{\mathrm{ph}}^{\mathcal{R}})=1/2$, where Tr_1 is the partial trace over the auxiliary subsystem. In other words, $\rho_{\mathrm{ph}}^{\mathcal{R}}$ is a density matrix satisfying an extra constraint. We then found the optimal $\rho_{\mathrm{ph}}^{\mathcal{R},\,\mathrm{opt}}$ using the same convex-optimization methods as for state tomography and adding this extra constraint[23,38]. We computed the corresponding LPTM via

$$(\mathcal{R}_{\mathrm{ph}}^{\mathrm{opt}})_{ij}=\mathrm{Tr}(\rho_{\mathrm{ph}}^{\mathcal{R},\,\mathrm{opt}}\,\sigma_j^T\otimes\sigma_i) \tag{18}$$

and the average logical-gate fidelity using

$$F_{\mathrm{L}}^G=\frac{\mathrm{Tr}(\mathcal{R}_{\mathrm{ideal}}^{\dagger}\mathcal{R}_{\mathrm{ph}}^{\mathrm{opt}})+2}{6}, \tag{19}$$

where $\mathcal{R}_{\mathrm{ideal}}$ is the LPTM of the ideal target gate.

Extraction of the error-detection rate. The fraction of post-selected data P in the repetitive error-detection experiment (Fig. 4b) decays exponentially with the number of cycles n. This is consistent with a constant error-detection rate per cycle γ. We extracted this rate by fitting the function

$$P(n)=A(1-\gamma)^n. \tag{20}$$

Data availability

The data supporting the plots and claims within this paper are available online at http://github.com/DiCarloLab-Delft/Logical_Qubit_Operations_Data.

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Author contributions

J.F.M. performed the experiment and data analysis. M.B., N.H. and L.D. designed the device. N.M., C.Z. and A.B. fabricated the device. J.F.M. and H.A. calibrated the device. M.S.M. and W.V. designed the control electronics. B.M.V. performed the numerical simulations and F.B. implemented the MLE method. B.M.T. supervised the theory work. J.F.M. and L.D. wrote the manuscript with contributions from B.M.V., F.B. and B.M.T., and feedback from all co-authors. L.D. supervised the project.

Competing interests
The authors declare no competing interests.

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