Project report

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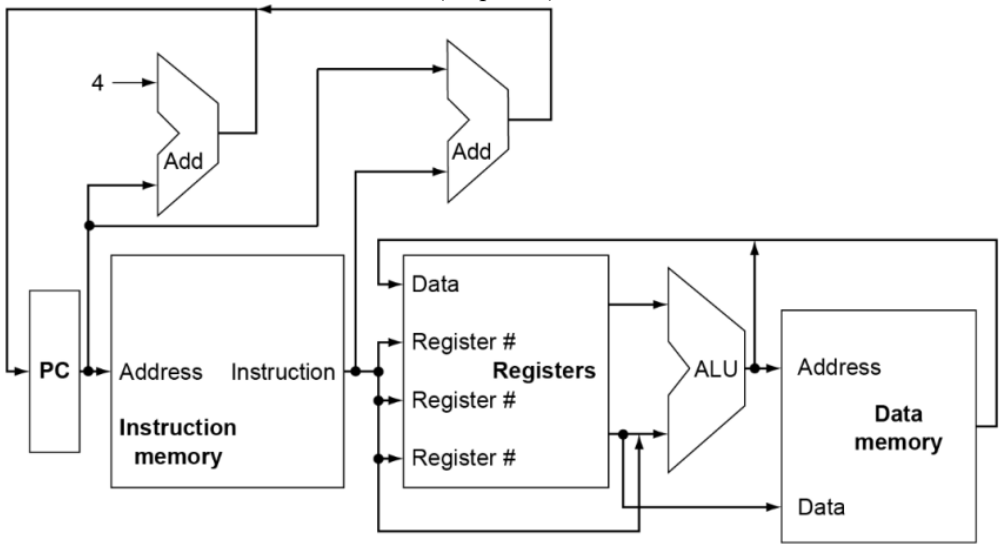
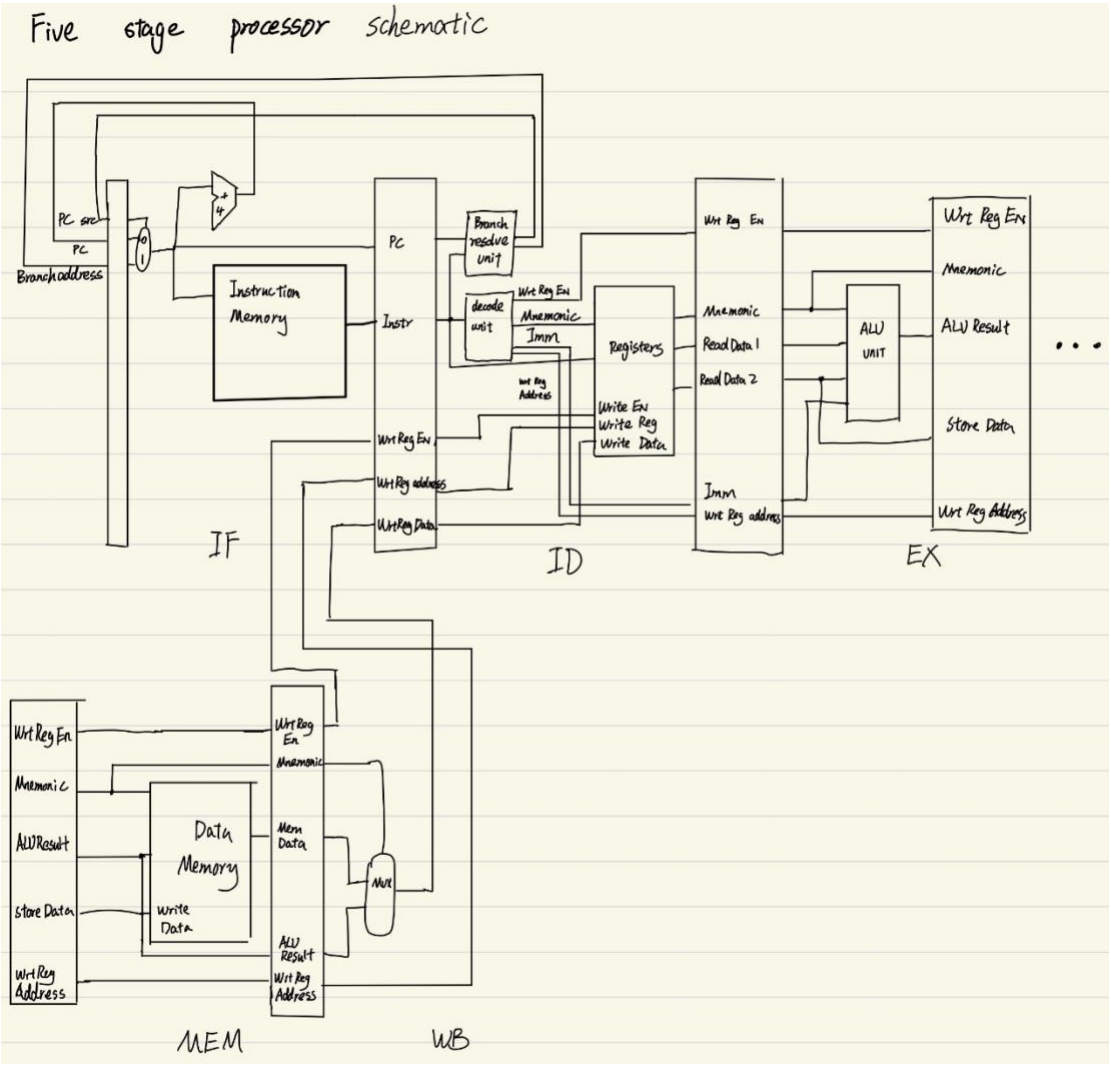
1) Draw the schematic for a single stage processor and fill in your code in the to run the simulator. (20 points)



2) Draw the schematic for a five stage pipelined processor and fill in your code to run the simulator. The processor should be able to take care of RAW and control hazards by stalling and forwarding.



(20 points)
3) Measure and report average CPI, Total execution cycles, and Instructions per cycle for both these cores by adding performance monitors to your code. (Submit code and print results to console or a file.) (5 points)

Single stage :

CPI: 1

Total execution cycles:
TC0: 9
TC1: 43
TC2: 8
TC3: 8
TC4: 38

Instructions per cycle:1

Five stage:

CPI:
TC0: 9/5 = 1.8
TC1: 43/39 = 1.1
TC2: 8/4 = 2
TC3: 8/5 = 1.6
TC4: 38/11 = 3.45

Total execution cycles:
TC0: 9
TC1: 43
TC2: 8
TC3: 8
TC4: 38

Instructions per cycle
TC0: 5/9 = 0.56
TC1: 39/43 = 0.91
TC2: 4/8 = 0.5
TC3: 5/8 = 0.625
TC4: 11/38 = 0.29

4) Compare the results from both the single stage and the five stage pipelined processor implementations and explain why one is better than the other. (5 points)

Single stage is better, because the pipelining in five stage program is not actually doing the work but adds to complexation and time of execution. Plus, single stage processor has better performance result and easier implementation, which doesn't need to handle hazard.

5) What optimizations or features can be added to improve performance? (Extra credit 1 point)
The current implementation doesn't support multi-thread. By adding multi-thread support, the performance result could improve drastically.