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COMPANY PROFILE

ROOMAN TECHNOLOGIES

- Rooman Technologies was started by a group of techies in the year 1999 in Bangalore, India, as a training center.
- They work with the government to help people learn new skills or improve existing ones.
- They offer many training and vocational courses for students and graduates.
- Teaching with the help of technology is their main goal.
- Their classrooms are well-designed and modern to help students learn and work together easily.

WADHWANI FOUNADTION

- Wadhwani Foundation started in 2001. It is a non-profit organization that works to create more jobs and help society.
- Their main goal is to speed up job creation and support economic development.
- They have trained over 300,000 government workers in new and emerging technologies.
- The foundation has helped test 400+ new ideas, supported 15+ startup projects, and completed 150+ training batches.
- Their work is helping improve job opportunities and development around the world.

TOOLS EXPOSED

- **EDA Playground – Online HDL Simulation & Verification Platform**

EDA Playground is a **cloud-based online platform** that allows users to write, simulate, and debug **Verilog, System Verilog, and VHDL** code without requiring any local installation of EDA tools. It integrates with industry-standard simulation tools to help engineers and students test their HDL designs quickly.

Introduction to Verilog HDL

- **Definition:**

  Verilog is a hardware description language (HDL) used to model, design, and simulate digital systems like processors, memory units, and control circuits. It allows precise description of how electronic circuits behave and interact.

- **Purpose of Verilog:**
  - To write human-readable code that represents logic circuits.
  - To perform functional verification through simulation before physical implementation.
  - To enable automated synthesis of digital designs into gate-level circuits.
  - To support design reuse and modular development in complex projects

Tasks Performed

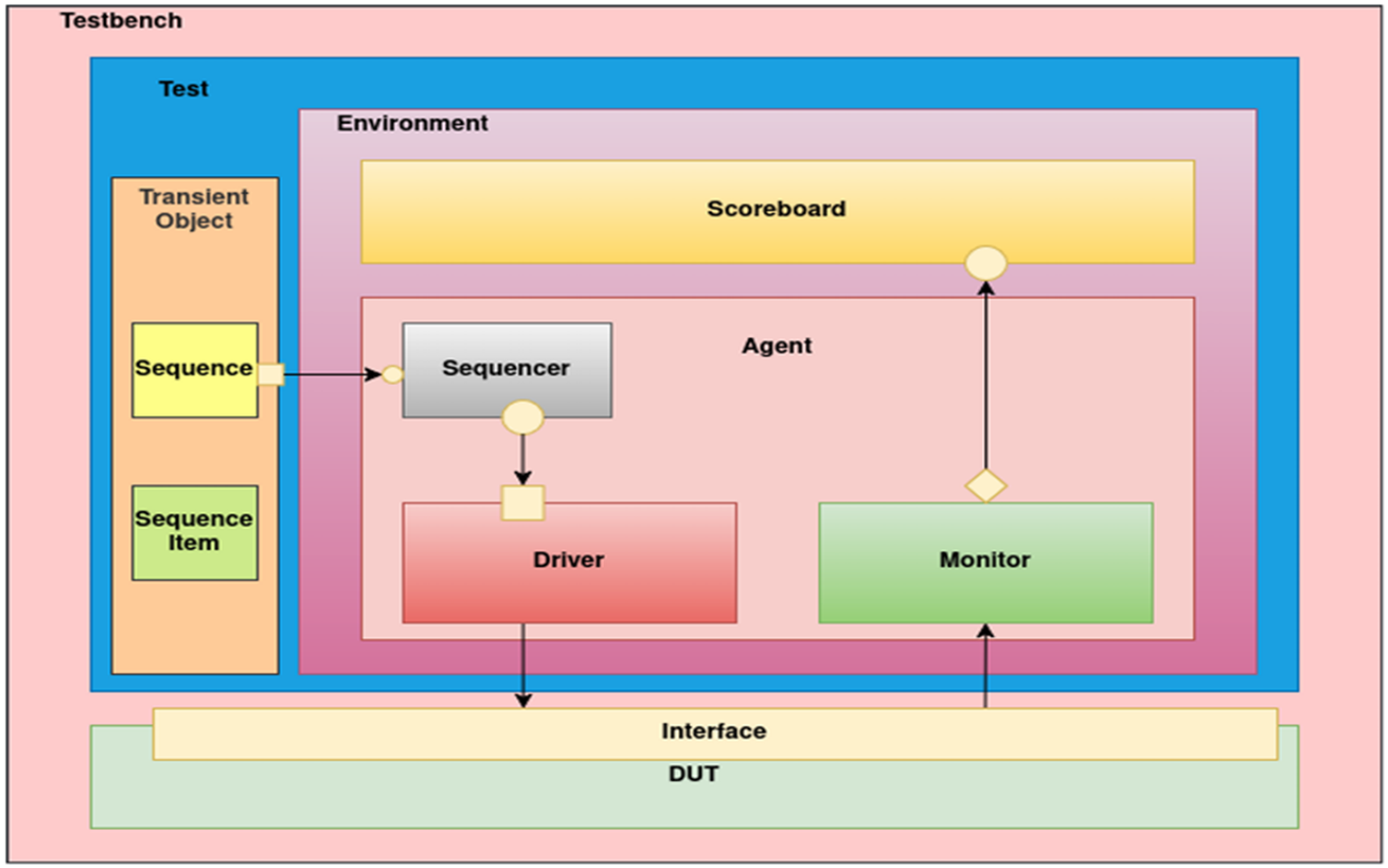
1. Design Implementation

Truth Table

A (Hex)	B (Hex)	Result (Hex)	Remark
3F800000	40000000	40400000	1.0 × 2.0 = 2.0
7F800000	3F800000	7F800000	∞ × 1.0 = ∞
00000000	3F800000	00000000	0 × 1.0 = 0
FF800000	3F800000	FF800000	-∞ × 1.0 = -∞
7FC00000	3F800000	7FC00000	NaN × 1.0 = NaN

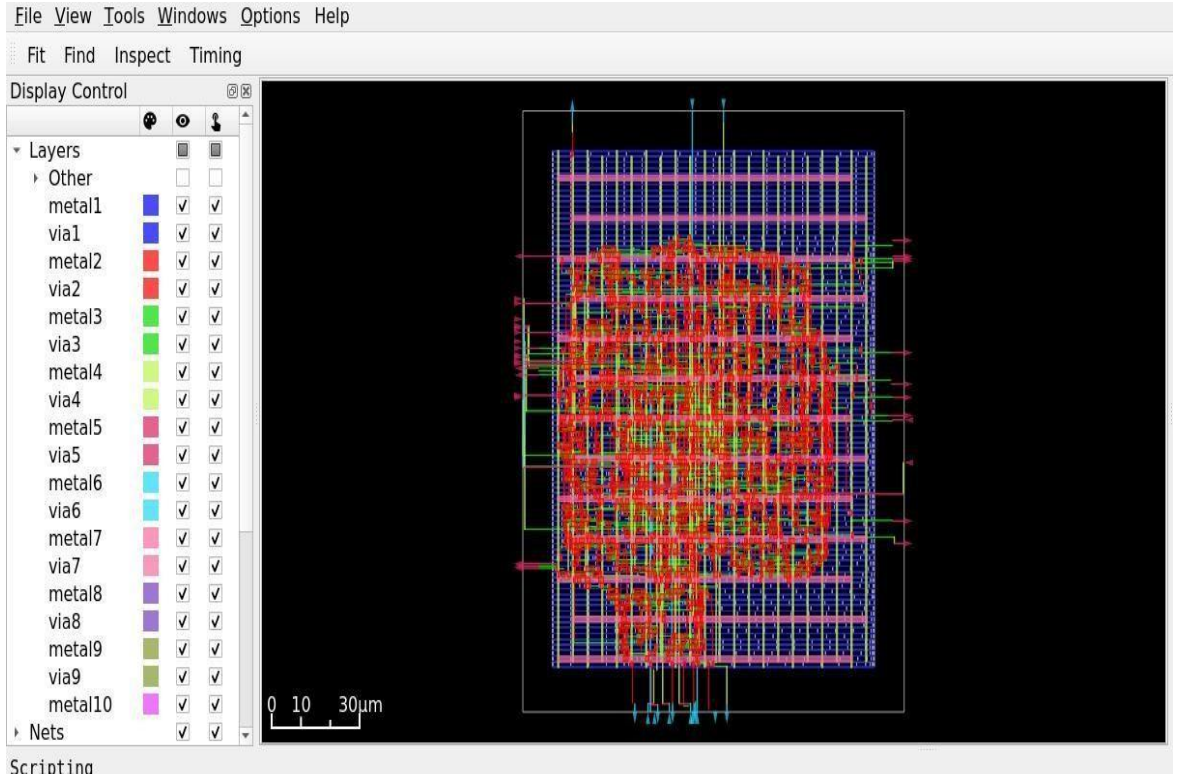
2. Functional Verification (UVM)

- Created a UVM testbench for verification of the comparator.
- Built key components: driver, monitor, sequencer, and scoreboard.
- Tested various input combinations including greater-than, less-than, and equal cases.



3. Generated GDS

- The 32-bit floating point multiplier was designed in Verilog using IEEE 754 standard for single-precision floating point. Performed floorplanning, placement, and global routing, followed by detailed routing.
- Applied Clock Tree Synthesis (CTS) to ensure proper clock signal distribution.
- Generated the final GDS-II layout, representing the physical implementation of the design.
- Extracted key metrics: design area, clock frequency, and total power consumption from the layout.



Reflection Notes

1. Learning and Growth:

Mastering UVM: Improved knowledge of UVM methodology, understanding how to build scalable and reusable testbenches. Learned the importance of coverage-driven verification and transaction-level modeling.

Physical Design Skills: Explored the complete ASIC flow using OpenROAD, from synthesis to GDS-II layout generation. Got hands-on experience with floorplanning, placement, clock tree synthesis, and routing.

2. Challenges Faced:

Timing Closure: Achieving a positive slack value while keeping the clock frequency high required several iterations of optimization.

Power Analysis: Balancing power consumption with performance and area constraints was a critical challenge

Conclusion

CONCLUSION

- Automation of the floating-point multiplier design enhances accuracy and reduces manual errors.
- The modular Verilog architecture ensures efficient implementation and easy debugging.
- Integration with OpenROAD provides a seamless path from RTL to GDS-II layout.

FUTURE SCOPE

•Integration with high-performance computing (HPC) processors

•Support for 64-bit double precision floating point operations

•Low-power optimization for portable and embedded devices