1.

```
tutorialspoint Online Verilog Compiler 🗹
                                                                              ∑ Terminal
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                                                                              &A = 0000
                                                                              \sim&A = 1111
     module operations;
                                                                              |A| = 0001
  6
                                                                              \sim |A| = 00000
         reg [3:0] A;
                                                                              ^A = 0001
  8
         output reg [3:0] out1_and, out2_nand, out3_or, out4_nor,
                                                                              \sim A = 0000
             out5_xor, out6_xnor;
                                                                              main.v:34: $finish called at 0 (1s)
 10
 11
         begin
              A = 4'b1101;
 13
              out1_and = \&A;
              out2_nand = \sim(&A);
 15
              out3_or = IA;
 16
              out4_nor = \sim |A;
              out5_xor = ^A;
 18
              out6_xnor =~^A;
 19
 20
 21
 22
              display (%A = %b", out1_and);
 23
              display ("-&A = %b", out2_nand);
              $display ("|A = %b", out3_or);
 24
 25
              display ("\sim |A = \%b", out4_nor);
              display ("^A = %b", out5_xor);
              display (\sim^A = b'', out6\_xnor);
 27
 28
 29
              $finish;
 30
 31
         end
```

2.

- a) 1'b0
- b) b) 1'bx

3.

- a) 1'bx
- b) 4'bxxxx
- c) 1'bx
- d) 12'b1010_1010_1x10
- e) 1'b1
- f) 1'b1

4.

a. 4'x11 is **illegal** as we can't represent an 8 bit constant in 4 bits. We require at least 5 bits to represent the above constant.

b. 'h3C is a legal declaration and will be represented in 32-bit binary as: **0000_0000_0000_0000_0000_0011_1100**

c. 12'HABC is legal declaration and will be represented in 12-bit binary as: **1010_1011_1100**

- d. 4'b111011 is legal declaration and the 6-bit number can be represented in 4 bits as: **1011**
- e. 4'b11?? Is legal and will be represented as: **4'b11zz**
- f. 8'b1100_1001 is legal and will be represented as: **1100_1001**