

Introduction to LICA

- Circuit means connection of various electronic component like R, L, C, transistors, diodes, MOSFETs, amps & oscillator called Circuits.
- All these ckt's integrated on a single IC called Integrated Ckts
- ICs also called silicon chip, computer chip, microchip.
- Generally, R, L, C, Diode and Transistor are placed on the PCB through soldering.
- But in an IC the active & passive components are fabricated together on single crystal of silicon.
- An IC is small chip that can function as an amp, oscillator, timer, microprocessor, or even computer Memory.
- An IC is a small wafer usually made of silicon, that can hold anywhere from 100s to millions of transistors, resistors, capacitors. These extremely small electronics can perform calculations & store data using either digital (or) analog technology.

Linear Integrated Ckts (LICs):

- LICs are also referred to as analog ICs due to the fact their i/p & o/p can take on a continuous range of values & the o/p are generally proportional to the i/p.
- IC's are also referred to as analog ICs due to the fact all the components in this ckt are fabricated on same ckt.
- Based on mode of operation ICs are classified as two types.
1) Linear IC 2) Digital IC.
- LICs are also referred to as analog ICs due to the fact their i/p & o/p can take on a continuous range of values & the o/p are generally proportional to i/p.

→ Difference b/w Linear and Digital ICs.

Linear ICs	Digital ICs
① Linear ICs (Linear Amplifiers)	② Digital ICs (Digital Amplifiers) and also called as non-linear ICs.
③ Linear ICs have linear output voltage and the output power is proportional to input power.	④ Digital ICs contains circuits whose input and output voltage are limited to two possible levels (low(0) or high(1)).
⑤ It is used in aircraft, space vehicles, radars, PLL, Oscilloscopes etc.	⑥ It is used in microprocessors, computers, clocks, digital watches, calculators etc.
⑦ It is commercially available in op-amps, voltage multipliers, voltage comparators, regulators, microwave flip flops, counters, registers etc.	⑧ It is commercially available in microprocessor chips, memory chips, A to D chips, D to A chips, logic gates, timers, regulators, microwave flip flops, counters, registers etc.
⑨ It consists of very less no. of transistors as compared to ICs.	⑩ It consists of more no. of transistors than LIs.

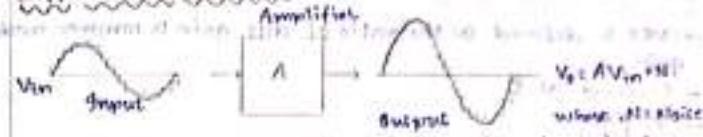
→ Advantages of ICs

- The entire physical size of IC is extremely small than that of discrete circ.
- The weight of an IC is very less as compared entire discrete circ.
- It's more reliable.
- Because of their smaller size it has lower power consumption.
- It can easily replace, but it can hardly repair, in case of failure.
- Because of an absence of parasitic capacitance effect it has increased operating speed.
- It is suitable for small signal operation.
- The reduction in power consumption is achieved due to extremely small size of IC.

→ Disadvantages of ICs:

- As IC is small in size it is unable to dissipate large amount of power. Increase in current may produce enough heat which may destroy the device.
- Inductors & transformers are needed connecting to extend to the semiconductor chip as it is not possible to fabricate on the semiconductor chip surface.

Differential Amplifiers



→ Note, in normal amplifier along with o/p noise is also there.

$$V_0 = A_d (V_1+ - V_1-) \quad \text{with noise: } V_0 = A_d \left(\frac{V_1+ + N_1}{2} - \frac{V_1- + N_1}{2} \right) = A_d V_{1m}$$

V_0 is proportional to V_{1m}

→ Diff. Amps are dual to amplifiers.

→ The o/p signal of a diff. amplifier proportional to the difference of the two i/p signals.

$$V_o = A_d V_{1m}$$

where, $V_{1m} = V_1+ - V_1-$
 A_d : proportionality constant
 $=$ differential gain of amplifier.

→ The above eqn shows an output expression for an ideal diff - amp.

→ But in case of practical diff. amp., the o/p signal depends on both differential signal & common mode signal.

→ The more practical equation of diff. Amp is given by

$$V_o = A_d V_{1d} + A_c V_c$$

where $V_{1d} = (V_1+ - V_1-)$ is differential signal
 $V_c = \frac{(V_1+ + V_1-)}{2}$ is Common mode Signal

A_d : Differential Gain

A_c : Common mode Gain

→ For a good practical diff - amp we require $A_d \gg A_c$.

→ So that o/p V_o depends only on V_{1d} & is independent on V_c.

→ Since the o/p of diff. amp. doesn't depend on common mode signal, so common mode signal is suppressed (Rejected).

→ The greatest advantage of diff. amp is that it suppresses the common mode signal, hence if there is any noise which is common to both signals get cancelled.

Common Mode Rejection Ratio (CMRR):

- CMRR is defined as the ratio of diff. gain to common mode gain.
- Denoted as 'f'.
- $f = \left| \frac{A_d}{A_c} \right|$
- It is mostly represented in decibel units.
- CMRR in dB = $20 \log \left(A_d/A_c \right)$.
- CMRR is figure of merit for diff-amp.
- Ideally, $CMRR = \infty$ i.e. $A_c = 0$. Common mode signal suppresses.
- Practically CMRR shall be as high as possible.

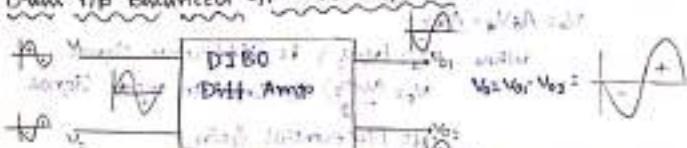
Characteristics of a Good Differential Amplifier:

- Differential gain ' A_d ' must be very high.
- Common mode gain ' A_c ' must be very low.
- CMRR must be very high.
- S/I impedance should be very high.
- O/p impedance should be very low.
- B.W should be very high.
- Characteristics of amplifier should not shift with temperature.
- Offset voltages and currents should be very low.

Types of Differential Amplifiers:

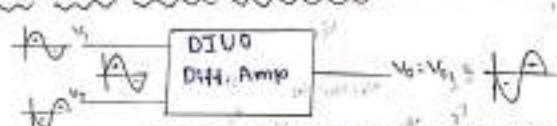
- DIBO - Dual I/p balanced o/p
- DIUD - Dual I/p unbalanced o/p
- SIBO - Single I/p balanced o/p
- SIUD - Single I/p unbalanced o/p

Dual I/p Balanced O/p Diff. Amplifier:



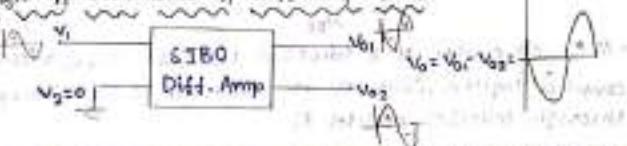
- The I/p 'V1' is applied as diff. signal by splitting it into 2 equal signals with oppo. phase angles V_1, V_2 . Hence V_1 can be $V_1 = V_1 - V_2$.
- The o/p is also taken as the difference of 2 I/p terminals. $V_d = V_{11} - V_{12}$.
- This configuration is also called as Fully differential configuration.

Dual I/p Unbalanced O/p diff. Amplifier:



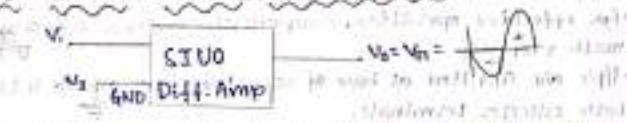
- The I/p 'V1' is applied as diff. signal by splitting it into 2 equal signals with opposite phase angles V_1, V_2 . Hence $V_1 = V_1 - V_2$.
- The o/p is taken at any of the two terminals. $V_d = V_{11} \text{ (or) } V_d = V_{12}$.
- The signal at other o/p is neglected.

Single I/p Balanced O/p diff. Amplifier:



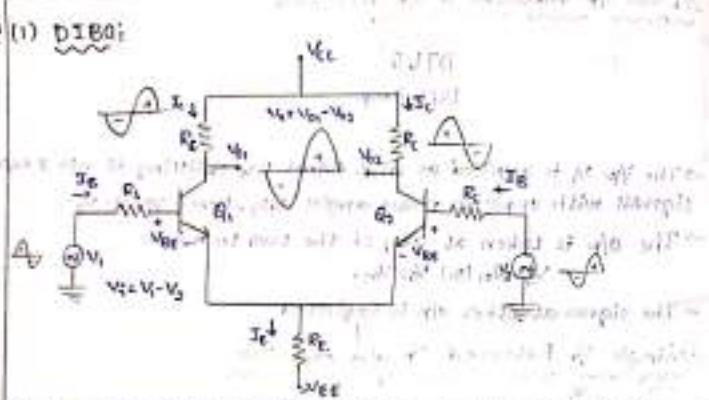
- The I/p 'V1' is applied to one of 2 I/p terminals while other is grounded. $V_1 = V_1$
- The o/p is taken as difference b/w 2 o/p terminals. $V_d = V_{11} - V_{12}$.

Single I/p Unbalanced O/p diff. Amplifier:



- The I/p 'V1' is applied to one of 2 I/p terminals while other is grounded. $V_1 = V_1$
- The o/p is taken at any one of 2 o/p terminals. $V_d = V_{11} \text{ or } V_d = V_{12}$.
- The signal at other o/p is neglected.

Ques 3 (1) DIBO:



→ Above circuit consists of 2 identical transistors Q₁, Q₂, with its emitters coupled together. Collector are connected to main supply V_{CC} through collector resistor R_C.

→ Magnitude of power supply V_{CC} & -V_{EE} will be same.

$$\therefore V_B = A_d (V_{B1} - V_{B2})$$

where A_d = differential gain.

V_{B1}, V_{B2} = ifp voltages.

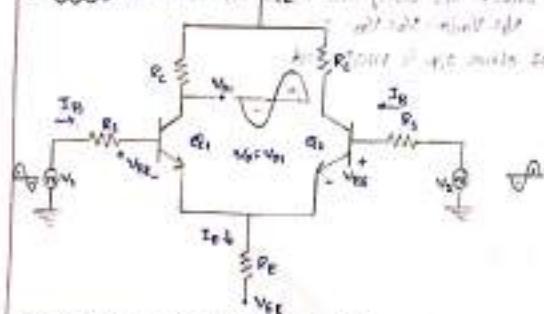
→ When V_{B1} = V_{B2} = 0 obviously the o/p will be zero i.e. diff. amp. suppresses common mode signals.

→ For effective operation, components on either side should be matched properly.

→ Ifps are applied at base of each transistor, and o/p is taken from both collector terminals.

→ There won't be any unnecessary dc content as dc contents in both o/p's gets cancelled each other.

2) DIUBO:



→ The ifp V_B is applied as differential signals by splitting it

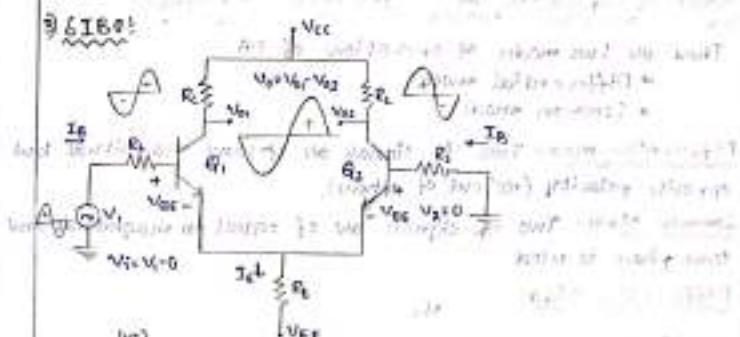
into 2 equal signals with opposite phase angles θ_1, θ_2 . Hence, $\theta_1 = \theta_2 = 90^\circ$.

→ The o/p is taken from any one of two pho nodes. $V_{BO} = V_{B1} + V_{B2}$

→ The signal at other o/p node is neglected.

→ Unbalanced o/p will contain unnecessary dc content.

3) SJUBO:



→ The ifp is applied to one of 2 pho terminals while other terminal is neglected. $V_{B1} = V_B$

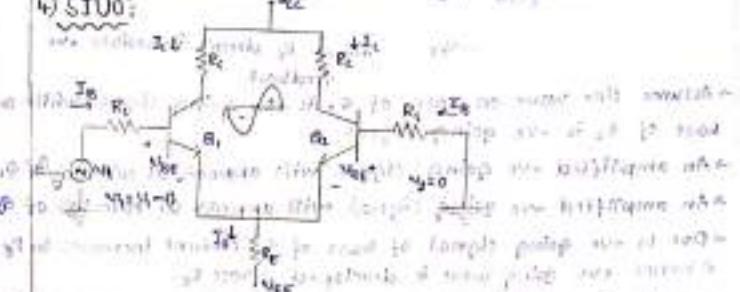
→ The o/p is taken from two o/p's.

$$\therefore V_{BO} = V_{B1} - V_{B2}$$

→ This will give us more amplifier version at o/p as it is combining effect of both transistors.

→ There won't be any unnecessary dc content in balanced o/p as dc contents in both o/p's get cancelled each other.

4) SJUBO:



→ When ifp V_B is applied to Q₁, it's amplified & inverted voltage gets generated at collector of Q₁.

→ At the same time, it's amplified & non-inverted 'V' gets generated at collector of Q₂.

→ Unbalanced op-amp contains unnecessary dc content as it is in the coupled amplifier. ∴ this configuration should follow by a level translator etc.

→ The effect of V_i is coupled to β_2 via common emitter resistor R_E .

Modes of Operation of Differential Amplifier

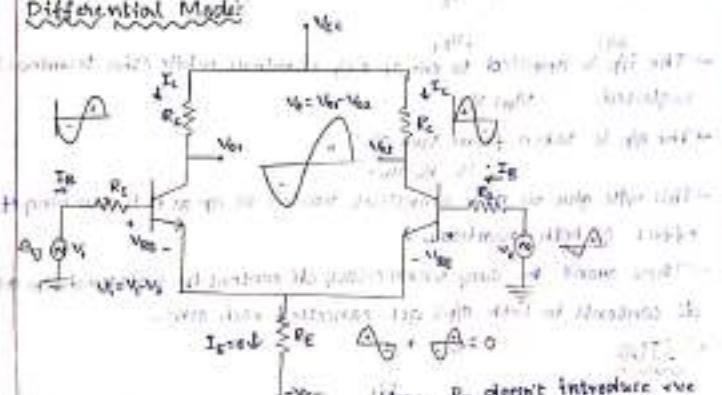
There are two modes of operations of DA

- * Differential mode
- * Common mode.

Differential mode: Two i/p signals one of same magnitude but opposite polarity (180° out of phase).

Common Mode: Two i/p signals one of equal in magnitude and same phase is used.

Differential Mode:



$$A_{differential} = \frac{V_{out}}{V_{in1}} = \frac{\beta_1}{\beta_2}$$

Hence R_E doesn't introduce any feedback.

→ Assume sine wave on base of Q_1 is the going signal while on base of Q_2 is -ve going signal.

→ An amplified -ve going signal will appear at collector of Q_1 .

→ An amplified +ve going signal will appear at collector of Q_2 .

→ Due to +ve going signal of base of Q_1 , current increases in R_E & hence +ve going wave is developed across R_E .

→ Due to -ve going signal of base of Q_2 , -ve going wave is developed across R_E because of emitted follower action of Q_2 .

→ So, signal voltages across R_E , due to effect of Q_1/Q_2 , are equal in magnitudes & 180° out of phase, due to matched transistors.

→ Hence the two signals cancel each other and there is no signal across R_E .

→ No AC signal flows through it.

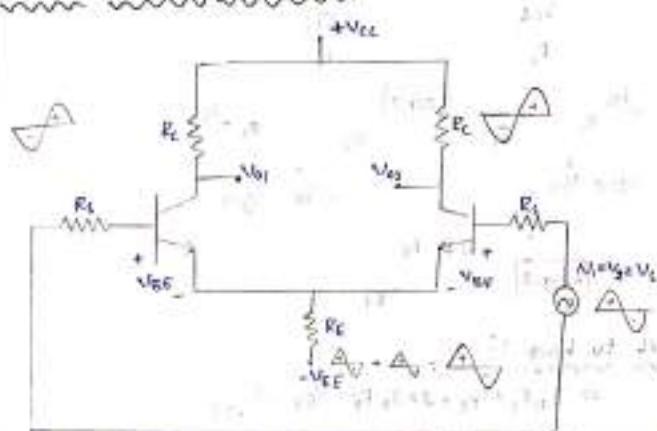
$$V_o = +10 - (-10) = 20$$

V_o is difference voltage in two signals.

→ Hence, the difference opo V_o is twice as the signal from either collector to ground.

$$\rightarrow A_d = V_o/V_{in1}$$

COMMON Mode Operation:



→ Two i/p signals one of equal in magnitude & same phase are used.

→ In phase signal develops inphase signal voltage across R_E .

→ Hence R_E carries a signal current & provides -ve feedback.

→ This -ve fb decreases A_d .

→ In signal voltages of equal magnitude will appear across 2 collectors of Q_1 & Q_2 .

→ $V_o = -10 - (-10) = 0$ negligibly small.

→ Ideally it should be zero.

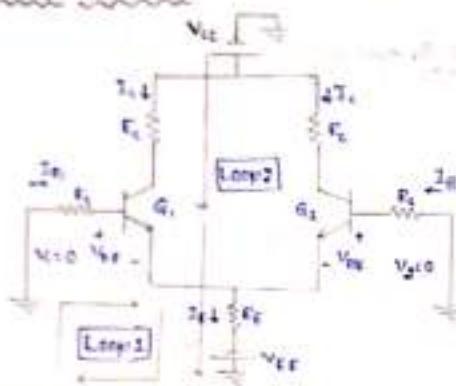
$$\rightarrow A_d = V_o/V_{in1}$$

$$\boxed{A_d = \frac{V_o}{V_{in1}}} = \boxed{\frac{V_o}{V_{in1}} = \frac{\beta_1}{\beta_2}}$$

DC analysis of a FET Differential Amplifier:

- To do the DC analysis we ground both the AC inputs.
- Apply KVL for Loop 1 as shown below. To get an eq. for the collector current I_C .
- Applying KVL for loop 2 as shown below; use the expression of I_C from loop 1, then we get an expression for V_{CE} .

DC eq. of BJTs:



KVL to Loop 1:

$$I_C R_1 + V_{BE} + 2 \cdot I_C R_E - V_{CE} = 0 \rightarrow (1)$$

W.K.T., $I_C = \beta I_B$

$$I_B = I_1 + I_2 \\ = (1/\beta) I_{CE}$$

$$\therefore I_C R_1 + V_{BE} + 2(1/\beta) I_{CE} R_E - V_{CE} = 0$$

$$\therefore I_C (R_1 + 2R_E + 2\beta R_E) = V_{CE} - V_{BE}$$

$$\therefore \frac{I_C}{\beta} (R_1 + 2R_E + 2\beta R_E) = V_{CE} - V_{BE}$$

$$\therefore I_C \left(\frac{R_1}{\beta} + 2R_E + 2\beta R_E \right) = V_{CE} - V_{BE} \quad (\because \beta \gg 1, V_{BE} \ll 1)$$

$$\therefore I_C \left(\frac{R_1}{\beta} + 2R_E \right) = V_{CE} - V_{BE}$$

$$\therefore \boxed{\frac{I_C (V_{CE} - V_{BE})}{(R_1/\beta + 2R_E)}} \rightarrow (2)$$

KVL to Loop 2:

$$-I_C R_1 + V_{CE} + 2 \cdot I_C R_E - V_{EE} = 0$$

From Eq.(1),

$$-I_C R_1 + I_C R_1 + V_{CE} - 2\beta I_C R_E = 0$$

$$\therefore V_{CE} = V_{EE} + V_{BE} - I_C R_E + I_C R_E$$

$$= V_{EE} + V_{BE} - I_C (R_E + R_E/\beta)$$

$$\therefore R_E \gg R_E/\beta, \text{ so, } R_E + R_E/\beta \approx R_E$$

$$\therefore V_{CE} = V_{EE} + V_{BE} - I_C R_E$$

→ Thus we get an expression for the operating point (I_C, V_{CE})

$$\therefore I_C = \frac{V_{CE} - V_{BE}}{(R_1/\beta + 2R_E)} \quad ; \quad V_{CE} = V_{EE} + V_{BE} - I_C R_E$$

AC Analysis of a Differential Amplifier:

→ To do the AC analysis we ground both DC inputs.

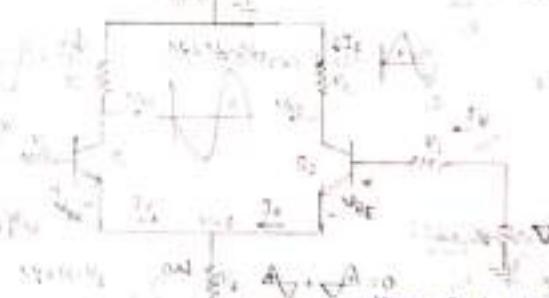
→ Differential amplifier has 2 AC gains

1) Differential gain (A_d)

2) Common mode gain (A_c)

→ We use small signal approx. h-parameter model for AC analysis.

→ We find Gain, i_{po} & ω_o impedances in the AC analysis.



Hence R_L doesn't introduce any loss.

→ The diff. eqn for differential amplifier is

$$V_{out} = A_d V_1 + A_c V_2$$

→ To find A_d , we set $V_2 = V_1/2$ and $V_1 = -V_2/2$, which results in $V_d = V_1 - V_2 = V_1$. At $V_2 = 0 [V_2 = \frac{V_1 + V_2}{2} = 0]$,

$$\therefore \text{Then, } V_{out} = A_d(V_1) + A_c(0).$$

$\Rightarrow V_{out} = A_{v2} V_2$

$$A_{v2} = \frac{V_{out}}{V_2}$$

- Since, V_1 & V_2 are 180° out of phase w.r.t. each other.
- This means that the current through resistor R_E is '0' as shown in fig.
- ∴ AC voltage at emitter nodes of both transistors is zero.
- Hence, both emitters are at virtual ground.
- Since the entire circuit is symmetric, we can use half circuit analysis to find V_{out}/V_2 .
- We use small signal approx. h-parameter model for the half circuit.

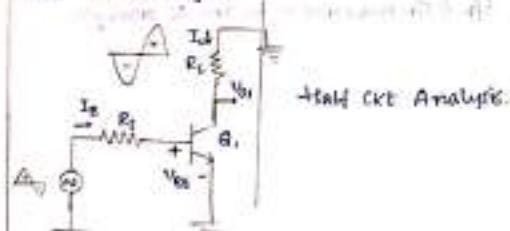
$$V_{out} = A_{v2} V_2 + A_{c2} V_c$$

$$V_{out} = A_{v2} \left[\frac{V_2}{2} - \left(-\frac{V_2}{2} \right) \right] + A_{c2} \left(\frac{V_2 - V_c}{2} \right)$$

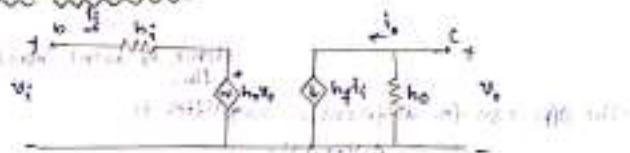
$$V_{out} = A_{v2} V_2$$

$$\therefore A_{v2} = \frac{V_{out}}{V_2}$$

- As the two transistors have the same characteristics then we can perform the AC analysis for only one half of the circuit hence called half circuit analysis.

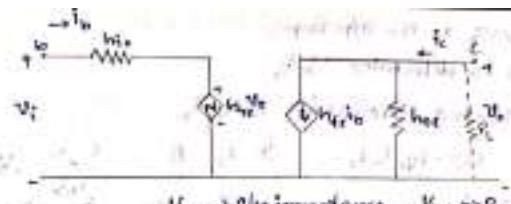


→ h-parameter model:

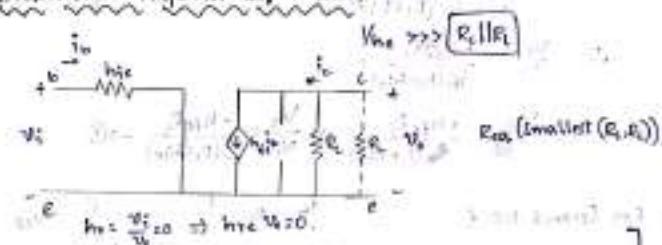


For CE Transistor,

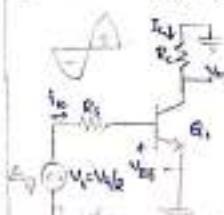
$$(h_{ie})_L = (3V_L)_L f_T$$



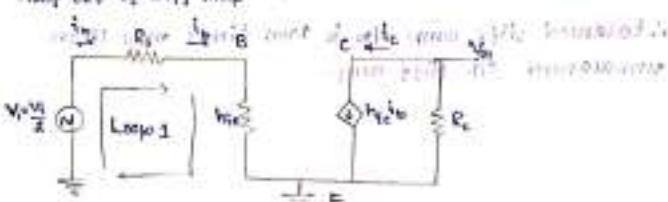
Approximate Hybrid Eq. Model:



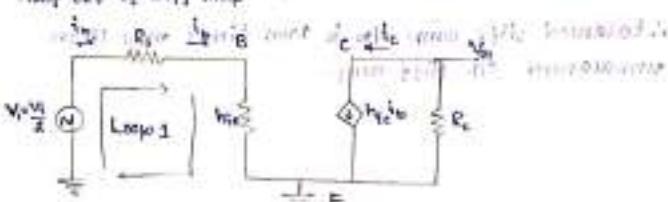
- The figure shows the circuit of the approx h parameter model for BJT.
- We replace the BJT with the approx model & find the gain V_{out}/V_1 .
- If we're using unbalanced configuration the op-amp will be V_1 and gain will be $A_{v1} = V_{out}/V_1$.
- If we're using balanced configuration the op-amp will be $V_{out} = V_1 - V_2$ & gain will be $A_{v2} = V_{out}/V_2$.



Half circuit of Diff amp



Approx. h-parameter model

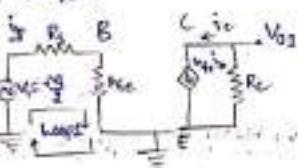


→ Applying KVL to the o/p loop.

→ Our aim is to determine V_{o1}/V_i

→ Current flowing through R_C is i_{fe}^2

$$V_{o1} = -h_{fe} i_{fe} R_C$$



→ KVL to loop 1,

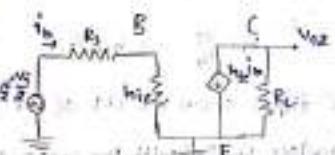
$$-V_i + i_B R_B + h_{fe} i_B R_C = 0$$

$$V_i = i_B (R_B + h_{fe} R_C)$$

$$\therefore \frac{V_{o1}}{V_i} = \frac{-h_{fe} R_C}{R_B + h_{fe} R_C}$$

$$\frac{V_{o1}}{V_i} = \frac{-h_{fe} R_C}{(R_B + h_{fe} R_C)} \Rightarrow \frac{V_{o1}}{V_i} = \frac{-h_{fe} R_C}{2(R_B + h_{fe} R_C)} \rightarrow (1)$$

→ For Second half,



$$\frac{V_{o2}}{V_i} = \frac{-h_{fe} i_B' R_C}{R_B + h_{fe}}$$

$$\frac{V_{o2}}{V_i} = \frac{-h_{fe} R_C}{R_B + h_{fe}}$$

$$\therefore \frac{V_{o2}}{V_i} = \frac{h_{fe} R_C}{2(R_B + h_{fe})} \rightarrow (2)$$

→ We can take o/p in 2 ways.

i) Unbalanced O/P:

$$\frac{V_{o1}}{V_i} = \frac{-h_{fe} R_C}{2(R_B + h_{fe})}$$

ii) For Balanced O/P:

$$\Delta V = \frac{V_{o1} - V_{o2}}{V_i} = \frac{V_{o1} - V_{o2}}{2V_i} = \frac{-h_{fe} R_C}{2(R_B + h_{fe})} - \frac{h_{fe} R_C}{2(R_B + h_{fe})} = \frac{-h_{fe} R_C}{R_B + h_{fe}}$$

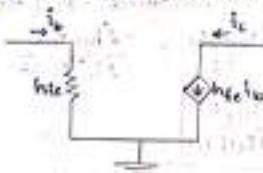
∴ Balanced diff amp o/p is two times more than unbalanced o/p diff amp.

→ AC Analysis of a 6180 Dif Amp

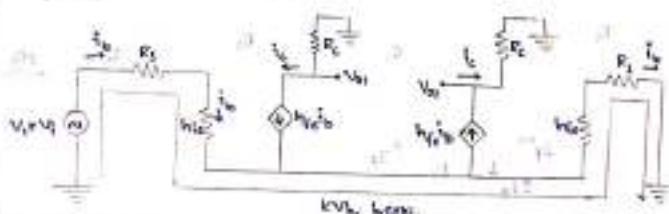
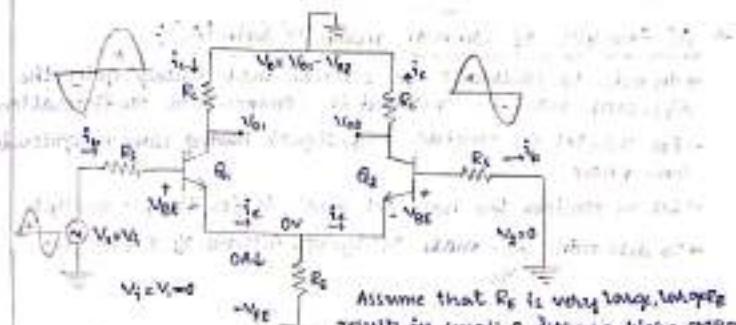
→ To do the AC analysis we ground both the DC ips & assume that R_E is very large, a large R_E results in a small AC & thus a higher CMRR.

→ We can't use half circuit analysis here, because the circuit is not symmetric.

→ We replace both BJTs with the approximate h-parameter model.



→ AC eq. diagram of 6180;



Apply KVL along the loop shown,

$$-V_i + h_{re} R_C + h_{oe} i_B + h_{re} R_E + i_E R_E = 0$$

$$\therefore V_{o1} = -i_B (R_C + R_E)$$

$$i_C = h_{oe} i_B$$

$$\therefore V_{o2} = -h_{oe} i_B R_E$$

Similarly,

$$V_{o1} = i_B R_C$$

$$\therefore V_{o2} = h_{oe} i_B R_E$$

Differential Gain for an unbalanced O/P Diff AMP

$$A_d = \frac{V_{o1}}{V_i} = -\frac{h_{fe} R_E}{2R_B(R_s+h_{fe})}$$

$$\therefore A_d = -\frac{h_{fe} R_E}{2(R_s+h_{fe})}$$

Differential Gain for a balanced O/P Diff Amp.

$$A_d = \frac{V_{o1}-V_{o2}}{V_i} = \frac{V_{o1}}{V_i} = -\frac{h_{fe} R_E}{2R_B(R_s+h_{fe})}$$

$$\therefore A_d = -\frac{h_{fe} R_E}{(R_s+h_{fe})}$$

The Diff. Gain of a balanced O/P Diff-Amp is double that of an unbalance O/P Diff-Amp.

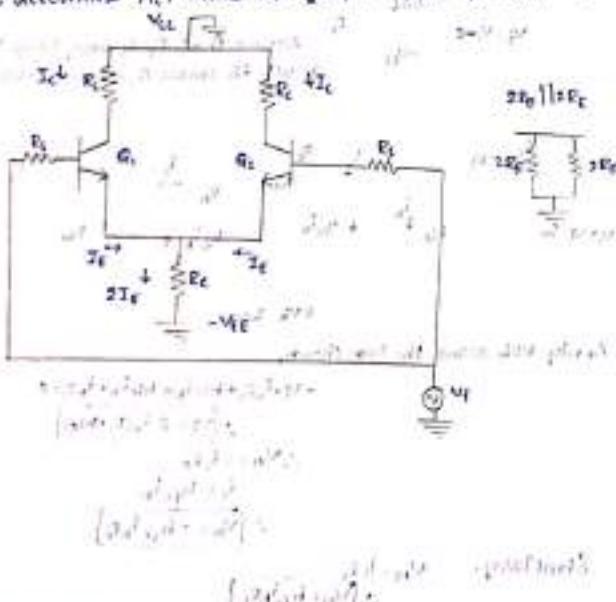
→ AC Analysis of Common mode 'V' Gain (A_v):

→ In order to calculate the common mode voltage gain, the diff. amp must be operated in Common mode configuration.

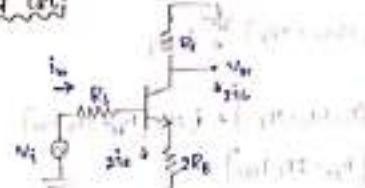
→ For this let us consider 2 signals having same magnitude & same phase.

→ Let us consider the half-circuit analysis for simple analysis.

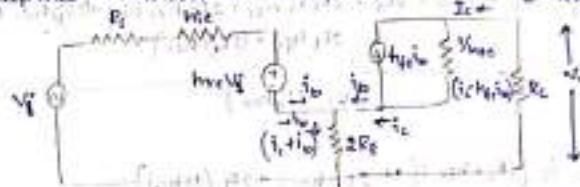
→ To determine A_v , make $V_1=V_2=V_i$. Assume $V_{o2}=0$ & $V_o=V_o$.



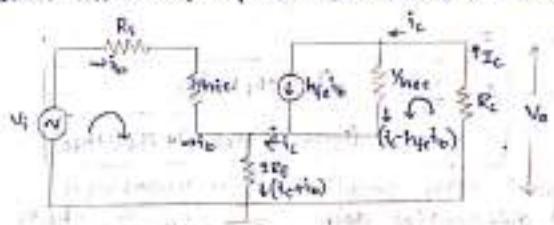
→ Half-Circuit



Replace transistors with h-parameter model [Exact h-parameter model]



→ Assume h_{ie} is very very small, the voltage is replaced by S.C.



$$V_o = -i_c R_L$$

$$A_v = \frac{V_o}{V_i}$$

Now,

$$V_i = R_b i_b + h_{ie} i_b + 2R_E (i_c + i_b) \quad (\text{KVL at } i_b)$$

$$V_i = i_b (R_b + h_{ie}) + 2R_E (i_c + i_b) \rightarrow 0.$$

Now,

$$i_c R_L + \frac{1}{h_{ce}} (i_c + h_{ie} i_b) + 2R_E (i_c + i_b) = 0 \quad (\text{KVL at the o/p})$$

$$i_c \left[R_L + \frac{1}{h_{ce}} + 2R_E \right] + i_b \left[2R_E - \frac{h_{ie}}{h_{ce}} \right] = 0.$$

$$i_c \left[R_L h_{ce} + 2R_E h_{ce} + 1 \right] + i_b \left[2R_E h_{ce} - h_{ie} \right] = 0.$$

$$\therefore i_b = \frac{i_c (R_L h_{ce} + 1 + 2R_E h_{ce})}{(h_{ie} - 2R_E h_{ce})}$$

→ $h_{ie} R_L \ll 1$, So, it is neglected.

$$\therefore i_b = \frac{i_c (1 + 2R_E h_{ce})}{(h_{ie} - 2R_E h_{ce})}$$

Sub 'i_b' in eq. ①.

$$V_1 = \frac{i_c (1 + 2R_E h_{fe}) (R_C + h_{ie} + 2R_E)}{h_{fe} - 2R_E h_{fe}} + i_L 2R_E$$

$$V_2 = \frac{i_c [(1 + 2R_E h_{fe}) (R_C + h_{ie} + 2R_E)] + i_L 2R_E [h_{fe} - 2R_E h_{fe}]}{h_{fe} - 2R_E h_{fe}}$$

$$= \frac{i_c [R_C + h_{ie} + 2R_E + 2R_E R_i h_{fe} + 2R_E h_{fe} h_{ie} + 2R_E^2 h_{fe}^2]}{2R_E h_{fe} - (2R_E^2 h_{fe})}$$

$$\therefore V_T = \frac{i_c [(R_C + h_{ie}) (1 + 2R_E h_{fe}) + 2R_E (1 + h_{ie})]}{h_{fe} - 2R_E h_{fe}}$$

$$\therefore A_{v2} = -i_L R_C$$

$$A_{v2} = \frac{V_2}{V_1} = \frac{-(h_{fe} - 2R_E h_{fe}) R_C}{(R_C + h_{ie})(h_{fe} - 2R_E h_{fe}) + 2R_E (1 + h_{ie})}$$

h_{ie} is very small value, so, it is neglected.

$$A_{v2} = \frac{V_2}{V_1} = \frac{-h_{fe} R_C}{(R_C + h_{ie}) + 2R_E (1 + h_{ie})}$$

Differential Gain :

$$A_{vd} = \frac{-h_{fe} R_C}{R_{thie}}$$

CMRR:

$$CMRR = \left| \frac{A_{vd}}{A_{v2}} \right| = \left| \frac{\frac{-h_{fe} R_C}{R_{thie}}}{\frac{-h_{fe} R_C}{(R_C + h_{ie}) + 2R_E (1 + h_{ie})}} \right|$$

$$\therefore CMRR = 1 + \frac{2R_E (1 + h_{ie})}{R_{thie}}$$

$CMRR \propto R_E$

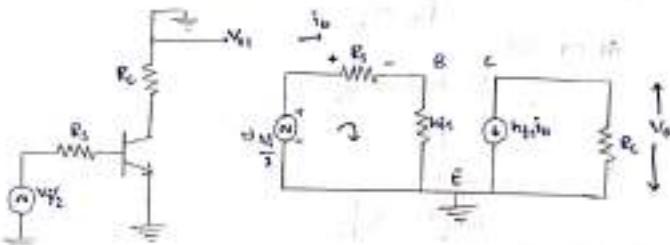
$\therefore CMRR$ is directly depends upon R_E .

$$\left[\text{and } h_{ie} \propto R_E \right]$$

(3) Input Resistance (i_{hp}) / Differential Input Impedance (R_i):
It is the equivalent resistance b/w one of the i/p terminals and the ground.

The i/p resistance is given by :

$$R_i = \frac{V_{11}}{I_B}$$



Applying KVL to i/p loop :

$$-V_{11} + i_B R_2 + h_{ie} i_B = 0$$

$$\therefore i_B = \frac{V_{11}}{2(R_2 + h_{ie})} \rightarrow 0$$

$$R_i = \frac{V_{11}}{I_B} = \frac{V_{11}}{\frac{V_{11}}{2(R_2 + h_{ie})}} = 2(R_2 + h_{ie})$$

$$R_i = R_{thie} \quad \boxed{\text{single transistor}}$$

For dual i/p circuit : Total i/p resistance ;

$$R_i = 2(R_{thie})$$

i/p resistance is completely independent of R_E whether it balanced or unbalanced.

(4) Output Resistance:

It is defined as equivalent resistance b/w one of the o/p terminal & the ground.

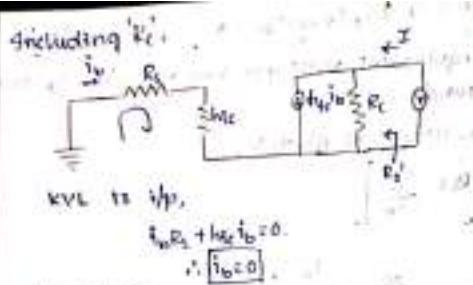
$$\text{i.e., } [R_o = R_C]$$

Inorder to find the o/p resistance, we have to make the i/p equal to zero, i.e., $V_1 = 0$ and add an external voltage source at the o/p side.

We how can find the o/p resistance in a way?

i) Including $R_C - R_o$

ii) Excluding $R_C - R_o$.



At o/p side,

$$I = h_{fe}i_b + \frac{V_o}{R_C}$$

$$I = \frac{V_o}{R_C}$$

$$\therefore \frac{V_o}{R_C} = R_L$$

$$\text{i.e., } R'_L = R_L$$



Composition:

Configuration	Circuit	A_d	R_i	R_o
DTBO		$\frac{-h_{fe}R_C}{R_{i\text{the}}}$	$\frac{1}{2(R_L+h_{fe})}$	R_C

DTVO		$\frac{-h_{fe}R_C}{2(R_L+h_{fe})}$	$2(E+V_{BE})$	R_C
STBO		$\frac{-h_{fe}R_C}{(R_L+h_{fe})}$	$R_{i\text{the}}$	R_C
STVO		$\frac{-h_{fe}R_C}{2(R_L+h_{fe})}$	$R_{i\text{the}}$	R_C

→ The -ve sign in diff. gain(A_d) represents that i/p & o/p are out of phase.

→ The common mode gain(A_c) is small for all configurations.

$$\text{i.e., } A_c = \frac{-h_{fe}R_C}{(R_L+h_{fe}) + 2R_E(1+h_{fe})}$$

Question

- i) Determine the o/p voltage of a diff. amplifier for the o/p voltage of 300mV & 240μA. The diff. gain of amplifier is 5000 if the value of CMRR is (1100×10^3) .

A) Given data.

$$V_1 = 200\text{mV}$$

$$V_2 = 240\text{mV}$$

$$A_d = 5000$$

$$\text{CMRR} = 100$$

$$V_o = A_d(V_1 - V_2)$$

$$V_o = V_1 - V_2 = 200\text{mV}$$

$$\text{CMRR} = \frac{A_d}{A_c}$$

$$A_c = \frac{5000}{100} = 50$$

$$V_o = \frac{V_1 + V_2}{2} = 220\text{mV}$$

$$V_o = 5000 \times 20\mu\text{A} + 50 \times 240\mu\text{A} = 10^4(30 \times 10^{-6} + 12 \times 10^{-6})$$

$$[V_o = 312\text{mV}]$$

- ii) CMRR = 10⁵.

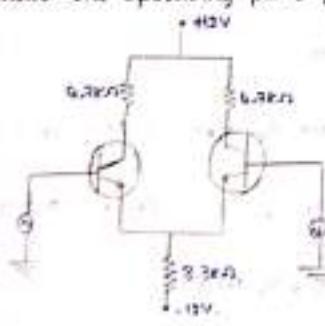
$$A_c = \frac{5000}{100} = \frac{5}{100} = \frac{1}{20} = 0.05.$$

$$V_o = A_d V_1 + A_c V_2$$

$$V_o = 5000 \times 20\mu\text{A} + 0.05 \times 240\mu\text{A}$$

$$[V_o = 300.0136\text{mV}]$$

- iii) Calculate the Operating point for ckt shown in fig.



$$R_C = 4.7\text{k}\Omega$$

$$R_E = 3.3\text{k}\Omega$$

$$V_{CC} = +15\text{V}, -V_{EE} = -15\text{V}, V_{BE} = 0.7\text{V}$$

Operating point (I_{CEQ}, V_{CEQ})

$$I_{CEQ} = I_C = \frac{V_{CC} - V_{BE}}{R_C} = \frac{15 - 0.7}{4.7 \times 10^3} = 1.912\text{mA}$$

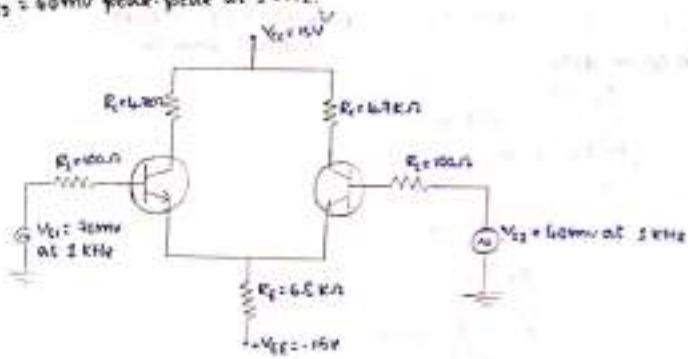
$$V_{CE} = V_{CC} - I_C R_C + V_{BE}$$

$$= 15 - (1.912 \times 10^{-3} \times 4.7 \times 10^3) + 0.7$$

$$V_{CE} = 4.65\text{V}$$

$$\therefore Q \text{ point is } (I_{CEQ}, V_{CEQ}) = (1.912\text{mA}, 4.65\text{V})$$

- 4) Fig shows DIRO diff. amplifier. Assuming Si transistors with $\beta = 2.8 \times 10^3$. Calculate (i) operating point values (ii) A_d (iii) A_c (iv) CMRR (v) o/p voltage V_o if $V_{in} = 70\text{mV}$ peak-to-peak at 3 kHz $V_{o2} = 60\text{mV}$ peak-to-peak at 3 kHz.



- A) i) Operating Point values (I_C, V_{CE})

$$I_{CQ} = \frac{V_{CEQ} V_{BEQ}}{(R_{E1} + R_{E2}) + R_C} = \frac{15 - 0.7}{(6.5 \times 10^3) + (2.8 \times 10^3)} = \frac{14.3}{14.3 \times 10^3}$$

$$I_{CQ} = 1.001\text{mA}$$

$$V_{CE} = V_{CC} - I_{CQ} R_C + V_{BE} = 15 - (1.001 \times 10^{-3} \times 6.5 \times 10^3) + 0.7$$

$$V_{CE} = 10.76\text{V}$$

$$\therefore Q \text{ point} = (1.001\text{mA}, 10.76\text{V}).$$

- ii) A_d :

$$A_d = \frac{h_{FE} R_C}{R_E + h_{FE}} = \frac{1000 \times 6.5 \times 10^3}{100 + 2.8 \times 10^3}$$

$$A_d = 12.216$$

- iii) A_c :

$$A_c = \frac{h_{FE} R_C}{(R_E + h_{FE})(h_{FE} + 1)} = \frac{4.7 \times 10^3 \times 10^3}{(100 + 2.8 \times 10^3) + 2.8 \times 10^3 (100)}$$

$$A_c = 0.3414$$

$$\text{iv) CMRR} = \left| \frac{A_d}{A_c} \right| = \frac{(R_E + h_{FE})(h_{FE} + 1)}{R_E + h_{FE}} = 494.65$$

$$\text{CMRR in dB} = 20 \log (494.65) = 63.62\text{dB}$$

(v) $V_o = A_d V_{d1} + A_u V_c$

$$V_{d1} \approx V_{d2} - V_{c2} = 30mV - 80mV = -50mV$$

$$V_c = \frac{V_{d1} + V_{d2}}{2} = \frac{-50 + 40}{2} = -5mV$$

$$V_o = (167.02) (-50mV) + (0.3424 \times 85mV)$$

$$V_o = 4.5615 + 15.777 \times 10^{-3}$$

$$\boxed{V_o = 4.5805V}$$

- ii) The common mode input to a certain diff. amp having $A_d = 10^4$, $A_u = 10^3$ is $4\sin(200\pi t)$. Determine V_o if CMRR is 60dB.
(common mode op-amp)

A) Given data.

$$A_d = 10^4$$

$$V_c = 4 \sin(200\pi t)$$

$$\text{CMRR} = 60 \text{ dB}$$

$$V_o = ?$$

$$20 \log \left| \frac{A_d}{A_u} \right| = 60$$

$$\frac{A_d}{A_u} = 10^3$$

$$A_u = \frac{10^4}{10^3} = 0.1 \text{ dB}$$

$$V_o = A_d V_{d1}$$

$$= 0.125 \times 4 \sin(200\pi t)$$

$$\boxed{V_o = 0.5 \sin(200\pi t) \text{ Volts}}$$

- iii) An Op-Amp has A_d of 100dB and CMRR of 95dB if $V_c = 2\text{mV}$, $V_{d1} = 4\text{mV}$ then V_d & V_o & diff. & common mode op-amp.

A) Given.

$$A_d = 100 \text{ dB}$$

$$\text{CMRR} = 95 \text{ dB}$$

$$20 \log A_d = 100$$

$$\boxed{A_d = 10^4}$$

$$\text{CMRR} = 20 \log \left| \frac{A_d}{A_u} \right| = 95$$

$$\log \left| \frac{A_d}{A_u} \right| = 4.95$$

$$\frac{A_d}{A_u} = 10^{4.95}$$

$$A_u = \frac{10^4}{10^{4.95}} = 0.127$$

$$V_d = (2-1.6)10^{-3} = 0.4 \text{ mV}$$

$$V_c = \frac{V_{d1} + V_{d2}}{2} = \frac{2+5.5}{2} = 1.8 \text{ mV}$$

$$V_{d1} = A_d V_{d2}$$

$$= 10^4 \times 0.4 \times 10^{-3}$$

$$V_{d1} = 4 \text{ mV}$$

$$V_c = A_u V_c$$

$$= 0.127 \times 1.8 \times 10^{-3}$$

$$\boxed{V_o = 0.3186 \text{ mV}}$$

→ DC Coupling:

→ Coupling is a way of interconnecting two ckt's.

→ There are different types of coupling depending upon types of device that are used to connect one ckt with the other. Namely (i) Direct Coupling.

(ii) RC coupling

(iii) Transformer Coupling.

→ DC coupling (also called conductive coupling) is the transfer of electrical energy by means of physical contact via a conductive medium, in contrast to inductive & capacitive coupling.

Why only DC Coupling?

DC-coupling is used by default in ckt's like IC op-amps. Since long coupling dev'ts like capacitors or inductors can't be fabricated on chips.

Advantages: i) Improved low freq. response.

ii) Reduced ckt cost.

iii) Min. offset errors.

iv) Monitoring of slowly varying signals is possible.

Applications: TV receivers, computers, regulator ckt's & op-amps.

→ Cascading Differential Amplifier:

Cascading: connecting (n) connecting n nof ckt's in series.

→ The series connection of diff. amplifiers called cascading, differential amplifier.

→ The main purpose of cascading the differential amplifier is to achieve high differential voltage gain and low common mode voltage gain. Hence cascading improves CMRR.

→ In order to improve the overall gain of ckt, cascading of different stages is used. Also, it provides perfect electrical and thermal

- α matching, compact in size and hence V_{out} is V_{in} .

How cascading improves gain?

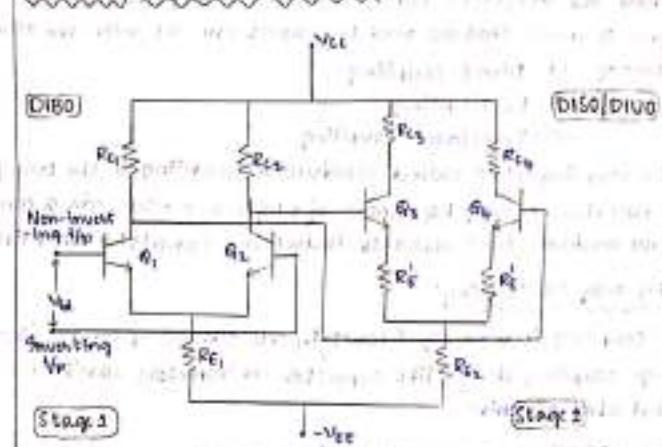
→ The overall h_{fe} impedance of cascaded DA is equal to h_{fe} impedance of first stage.

→ The overall h_{fe} impedance of cascaded DA is equal to h_{fe} impedance of last stage.

→ The overall voltage gain of the cascaded circuit is the product of gains of individual voltage gains.

$$\text{I.e., } A_d(\text{overall}) = A_{d1} \cdot A_{d2} \cdot A_{d3} \dots$$

Cascade differential amplifier is:



→ Stage 1 is BIBO diff. amplifier while Stage 2 is DIOS/DIUD differential amplifier.

→ The transistors Q_1, Q_2 should be identical in Stage 1. Q_3, Q_4 should be identical in Stage 2.

→ In Stage 2 a pair of swamping resistors are used to improve the h_{fe} impedance of diff. amplifier i.e.

→ Swamping resistors also increase the linearity ranges of diff. amplifier & reduces the effect of temp. on the transistor parameters.

→ The main requirement for the successful operation of such cascaded circuit is perfect matching of transistors & resistor values.

→ Hence, choose transistors, say, such as CA3086 or LM3146 for perfect matching transistors.

→ Fundamentals of Inverting and Non-Inverting h_{fe} Terminal

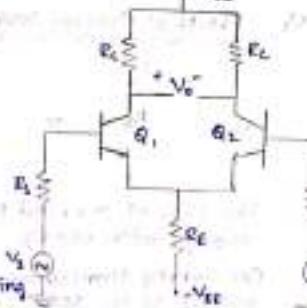
→ In differential amplifier the h_{fe} voltage V_b is given by

$$V_b = A_{d1}(V_1 - V_2) = (V_{d1} - V_{d2})$$

When $V_1 = 0$, $V_b = A_{d1}V_2$, V_2 applied.

& when $V_1 = 0$, $V_b = A_{d2}V_1$, V_1 applied.

$$V_b = A_{d2}(V_1 - V_2) = (V_{d1} - V_{d2})$$



→ Methods of Improving CMRR

→ As we know that higher the CMRR, better is the performance of DA.

→ To improve the CMRR, the A_c must be reduced to '0' and R_f tends to infinity (because of $-V_{CE}$ f/b of R_f).

Effect of R_f :

→ Practically R_f can't be selected very high due to certain limitations such as:

i) Reduced I_{CQ} causes distortion in the op-amp response.

ii) Large R_f needs higher biasing voltages to set the Q-point, which increases wastage of power.

iii) Large R_f occupies large area on chip.

→ Hence practically instead of increasing R_f various methods are used which provide increased R_f without limitation.

→ As M.K.T,
$$\text{CMRR} = \left(\frac{A_d}{A_c} \right) = 1 + \frac{2R_f(\text{ih}_{\text{fe}})}{R_f + \text{ih}_{\text{fe}}}$$

→ From h-parameter analysis of DA, A_c is

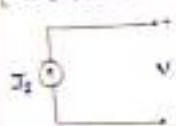
$$A_c = \frac{-\text{ih}_{\text{fe}} R_f}{(R_f + \text{ih}_{\text{fe}}) + 2R_f(\text{ih}_{\text{fe}})}$$

→ Different methods for the improving CMRR:

- DA with constant current source.
- Constant current bias using Zener diode.
- Current Mirror Ckt.

→ Constant Current Bias:

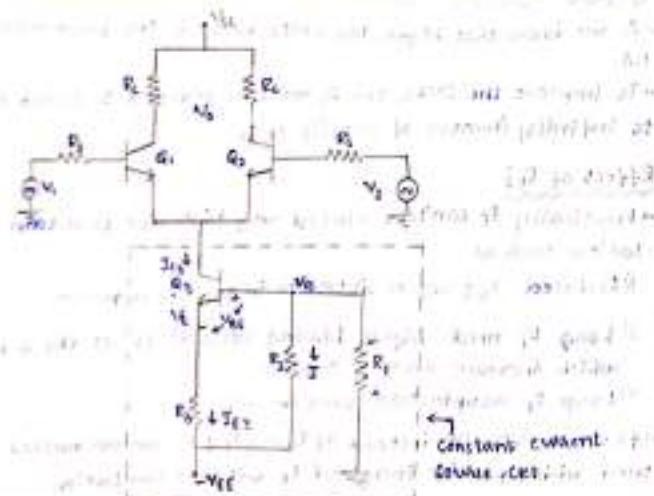
Ideal Current Source



Supplies constant current to load.

Can supply any amount of voltage of the load.

→ Constant current source gives very high impedance (R_{eff}):



→ Let current through R_3 be J_{E3} .

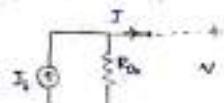
→ While current through R_3 is J .

→ Neglect base current of Q_2 i.e., $J_{B2} = 0$.

∴ Current through R_3 is J .

Our aim is to maintain J_{E3} as constant.

Practical Current Source



The current supplied to the load changes with voltage.

Can supply limited amount of voltage to the load.

$$I_{E3} = \frac{V_B - (-V_{BE})}{R_3} = \frac{V_B + V_{BE}}{R_3}$$

where $V_{BE} = V_B - V_E$ Now to determine V_E , apply KVL

$$V_E = V_B - V_{BE}$$

$$V_E = -J R_1$$

$$\text{base voltage } V_E = -\frac{V_{BE} R_1}{R_1 + R_2}$$

$$I_{E3} = \frac{V_B - V_E + V_{BE}}{R_3}$$

$$= \frac{-V_{BE} R_1 - V_{BE} + V_{BE}}{R_3} = \frac{V_{BE} \left[1 - \frac{R_1}{R_1 + R_2} \right] + V_{BE}}{R_3}$$

$$I_{E3} = \frac{V_{BE} \left[\frac{R_2}{R_1 + R_2} \right] + V_{BE}}{R_3}$$

Here $I_{E3} \approx I_{E2}$.

∴ V_{BE} , R_1 , R_2 , R_3 and V_B are constants, so current I_{E3} is almost constant.

→ Because two halves of the DA are symmetric each has half of the current I_{E3} .

$$\therefore I_{E3} = J_E + I_{E2}$$

Drawback:

→ But in practice V_{BE} isn't constant, it changes w.r.t. temp.

→ Temp. Compensation: Constant current Source (using two diodes)

→ In previous ckt, V_{BE} is not constant but changes w.r.t. temperature approximately at the rate of 2-5 mV/°C.

→ This intrinsic may change I_{E3} (I_{E2}), there is a necessity to provide thermal compensation.

→ From junction of emitters of Q_1 & Q_2 , such a thermal compensation is provided by replacing R_3 by diodes D_1 & D_2 .

→ As the temp. increases, the current i.e., the current I_{E2} , at the same time the diode con current also increases.

→ Due to increase current I_{E2} , the base current of Q_3 i.e., this compensates further increase in I_{E3} .

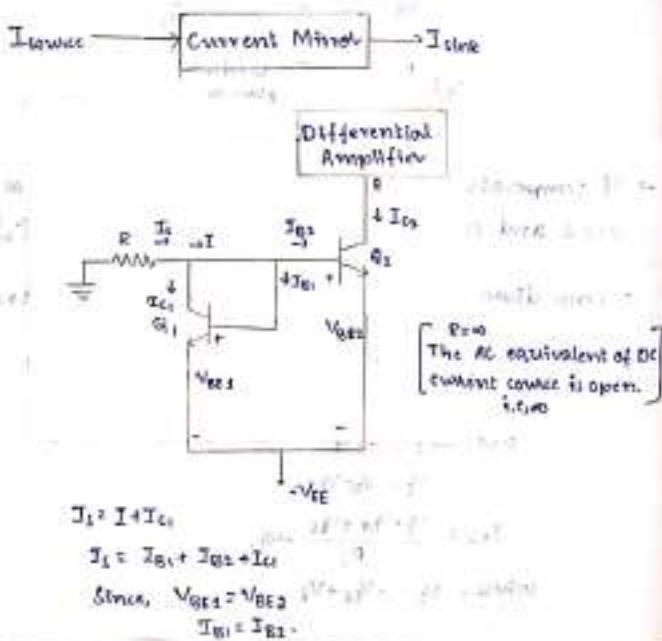
→ Transistor and diodes are of same material, then they have same temp. coefficient.

$$I_{EB} = \frac{-V_F + V_Z - V_{BE} + V_E}{R_3} = \frac{V_Z - V_{BE}}{R_3}$$

If V_2 & V_{BE} has same temp. coefficient then $I_C3(T_E)$ remains constant w.r.t. variations in temperature.

→ Current Mirrorth

- The current mirror in which output current is forced to equal to input current is called Current Mirror Ckt i.e., $I_{C2} = I_S$.
 - In a current mirror the opamp current is a mirror image of the current.
 - From fig. Once the current I_S is set up, the current I_{C2} is established automatically to be approximately equal to I_S . The current mirror is the special case of constant current bias, it can be used to setup constant currents in differential amplifier stages.
 - The current mirror bias requires few components than the constant current bias circuits.



$\therefore I_C \approx I_{E_3}$.

$$\Rightarrow I_6 = I_{B1} + I_{B2} + I_{C1} = 2I_{B2} + I_{C1}$$

$$T_{t2} = \frac{T_{t1}}{\mu} + T_{t3} \quad \text{with } [T_t, \mu T_R] = 0$$

$$J_5 = J_{6,2} \left(1 + \frac{2}{\beta} \right)$$

$$\frac{I_{C2}}{I_b} = \frac{1}{1 + (\beta/\mu)} \approx 3 \quad (\text{if } \beta \gg \mu)$$

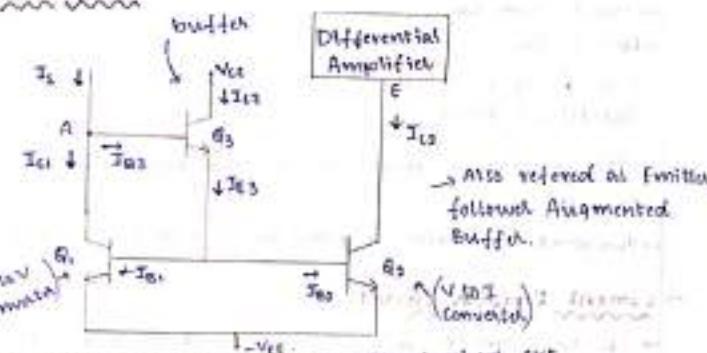
卷之三

- The above ckt shows a simple current mirror.
 - ' I_C ' is a source current which is a constant.
 - θ_1 & θ_2 are matched transistors.
 - This ckt forces ' I_C ' to be equal to ' I_S '.
 - As long as ' I_S ' is constant, ' I_C ' remains constant.
 - The ckt may not work properly because ' β ' is very small.

→ Improved Current Mirror Ckt:

From the previous ckt, if ' B ' is small then I_3 can't be equal to I_2 i.e., $I_2 \neq I_3$. In that case, modified Current Mirror ckt is used.

Cet diagramme



- The above circuit is an improved current mirror circuit.
 - The circuit works efficiently even for moderate value of P .
 - KCL at point A. (adv. for improved)

卷之三十一

Jea E. B. Jeat Tsi

$$J_{\text{eff}} = (t + \mu) J_{\text{eff}},$$

$$I_{B3} = \frac{I_{C3}}{1+\beta}$$

$$I_3 = I_{C1} + \frac{I_{C3}}{1+\beta}$$

$$I_{B3} = I_{B1} + I_{B2}$$

Since $V_{BE1} = V_{BE2}$, $I_{B1} = I_{B2}$ & $I_{C1} = I_{C2}$

$$I_{B3} = I_{B1} + I_{B2}$$

$$I_3 = I_{C1} + \frac{I_{C3}}{1+\beta}, \quad \left(I_B = \frac{I_3}{\beta} \right)$$

$$I_3 = I_{C1} + \frac{2I_{C3}}{1+\beta}$$

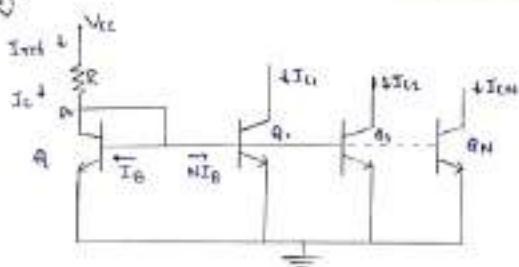
$$I_3 = I_{C1} \left[1 + \frac{2}{\beta(1+\beta)} \right]$$

$$\frac{I_{C1}}{I_3} = \frac{1}{1 + \frac{2}{\beta(1+\beta)}} \approx 1$$

$$I_{C1} \approx I_3$$

- Various adv. of Current Mirror Ckt are:
- It provides very high emitter resistance ' R_E '.
- It requires less components than constant current bias.
- Simple to design.
- Easy to fabricate.
- If properly matched transistors collector current thermal stability is achieved.
- Therefore, current mirror ckt is commonly most used in op-amp ckt.
- Improved frequency response due to base current compensation.
- Current Repeater Circuit:
- The basic current mirror can be used to source current to more than one load. Such a ckt is called Current Repeater.
- If all the transistors are identical, then current $I_C = I_{C1} = I_{C2} = \dots = I_{CN} = I_{ref}$ which is identically equal to ' I_{ref} '.

Ckt:



Applying KCL at node 'a':

$$I_{ref} = I_C + I_B + N I_B$$

$$I_{ref} = I_C + \frac{I_C}{\beta} + N \frac{I_C}{\beta}$$

$$= I_C \left[1 + \frac{(N+1)}{\beta} \right]$$

$$I_{ref} = I_C \left[\frac{R + N + 1}{R} \right]$$

$$I_C = I_{ref} \left[\frac{R}{R + N + 1} \right]$$

$$I_C = \frac{I_{ref}}{1 + (N+1)}$$

($\because \beta$ is large)

$$I_C \approx I_{ref}$$

$$I_C = I_{C1} = I_{C2} = I_{C3} = \dots = I_{CN} = I_{ref}$$

UNIT-2

→ Integrated Circuits:

- An IC is a miniature low cost electronic ckt consisting of active and passive components fabricated together on a single crystal of silicon.
- The active components are transistors and diode & passive components are resistors and capacitors.

→ Advantages of ICs:

- Miniaturization and hence increased equipment density.
- Cost reduction.
- Increased system reliability due to the elimination of soldered joints.
- Improved functional performance.
- Matched devices.
- Increased operating speeds.
- Reduction in power consumption.

→ ~~etc~~

→ Classification of IC's:

- ICs can be classified into
 - Analog - Linear.
 - Digital - Digital.
 - Mixed Signal (both analog & digital on the same chip).

→ Digital IC:

- Digital ICs can contain millions of logic gates, flipflops, multiplexers, and other cks in a few square millimeters.
- The small size of these cks allow high speed, low power dissipation, and reduced manufacturing costs.

→ These Digital ICs, typically microprocessors, DSPs and micro controllers work using binary mathematics process "one" and "zero" signals.

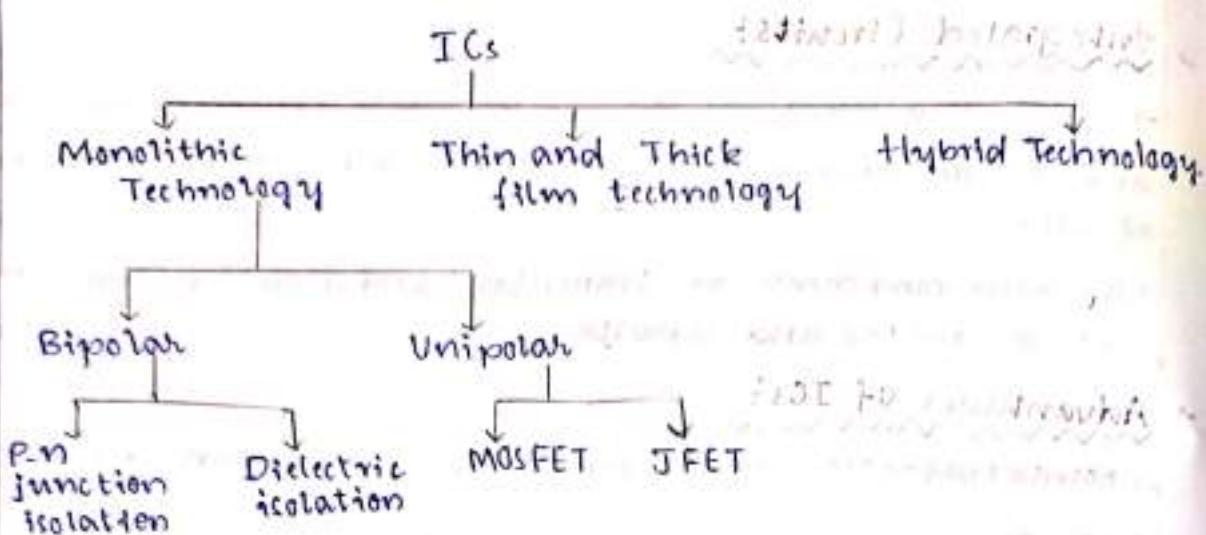
→ Analog IC:

→ Analog ICs, such as sensors, power management cks, and OP-Amp, work by processing continuous signal.

→ They perform functions like amplification, active filtering, demodulation, mixing.

Classification of ICs:

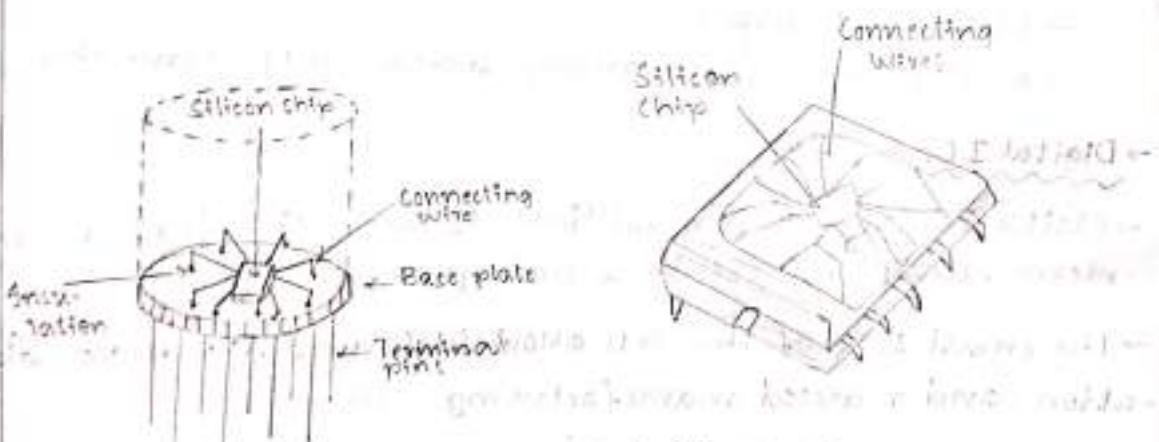
Based on various technologies



Monolithic ICs:-

In this all active as well as passive components along with interconnectors are integrated on single crystal.

Monolithic is originated from Greek word means "single stone" or "One Stone". Thus this word is appropriate as the components are integrated on single piece of silicon crystal. The various process involved in the fabrication of different devices are carried out in a single plane. Hence this is also referred as Planar Technology.



(a) Can-type enclosure (b) Plastic Package

Most Monolithic ICs are further classified based on active devices used. They are bipolar ICs & unipolar ICs.

Based on isolation Bipolar < P-n junction isolation
dielectric isolation.

Based on type of FET < MOSFET.
JFET.

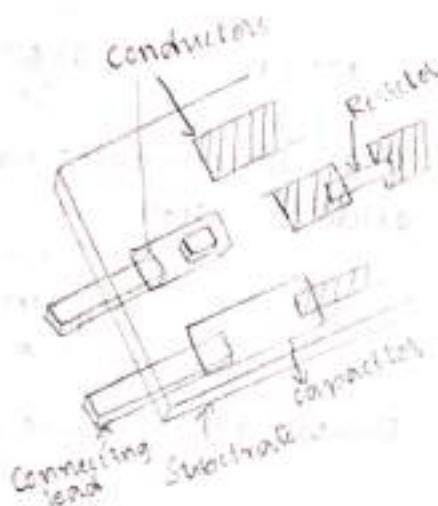
Key Point: The monolithic ICs are preferred for the applications in which identical electronic ckt's are required in large number.

The monolithic ICs provide lowest per unit cost by highest reliability. But due to the power limitations, monolithic ICs are preferred only in low power applications!

Thick and Thin Film Technology:

In thin-film ICs glass or a ceramic surface is used to deposit films of conducting material. Here, resistors and conductors are fabricated by controlling the width and the thickness of the films and by using different materials.

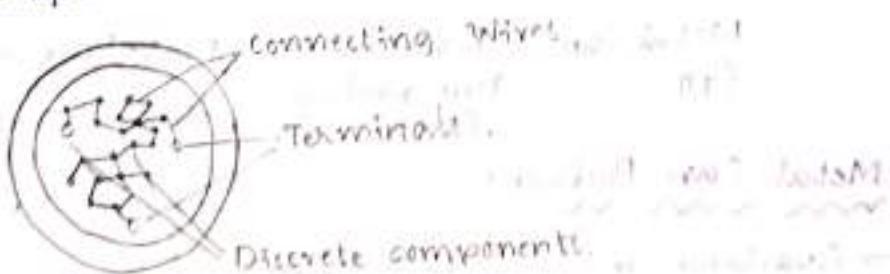
These CKTs are also referred to Printed thin-film CKTs. Screens are actually made of stainless steel wire mesh & the inks or pastes which have conductive, resistive or dielectric properties. After printing these CKTs are kept in high temp furnace.



Key point: ICs fabricated by thin or thick films technology usually have better component tolerances and they provide better high-freq. performance than monolithic ICs.

Hybrid Technology:

Hybrid ICs are constructed by interconnecting a no. of ^(a) multichip individual chips.



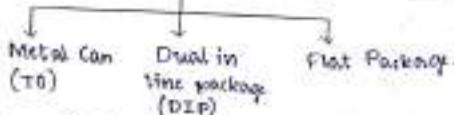
Hybrid or Multichip IC.

The hybrid or multichip CKTs also have better performance than monolithic CKTs. However it is expensive. But it is economical for smaller quantity.

IC family Proprietary	Monolithic IC	Thick-Thin film	Hybrid IC
Substrate	Silicon	Glass, Ceramic	(i) Glass, Ceramic (ii) Silicon.
Structure	Active & Passive devices along with interconnects on single chip.	Active & Passive devices on an insulating substrate along with interconnection.	(i) Passive devices & interconnections on one insulating substrate with active devices wire bonded. (ii) Active devices on a single chip while passive devices along with interconnections on thick-thin film.
Active devices	(i) BJT (ii) MOSFET	MOSFET	(i) BJT (ii) MOSFET
Passive devices	(i) Diffused resistors, oxide capacitors. (ii) MBS resistors, oxide capacitors.	Metal film resistor, oxide capacitor.	(i) Metal film resistor, cement resistor, oxide capacitor. (ii) Metal film resistor, oxide capacitor.
Application	Linear and Digital IC	Digital IC	Linear and Digital IC
Advantage	High reliability	Better high freq. performance	Better Performance

→ IC Package Types:

IC Package

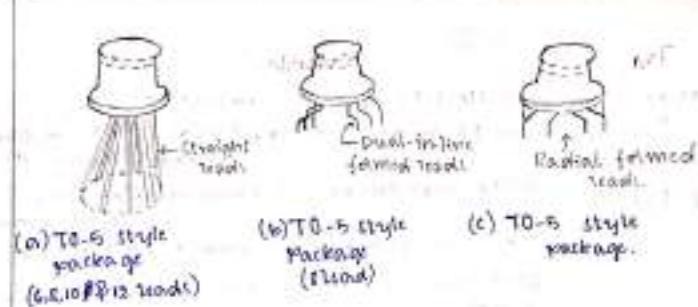


Metal Can Packages:

→ Available in 3, 5, 8, 10 & 12 pins.

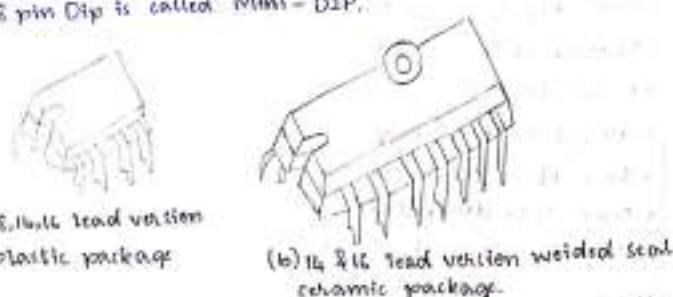
→ Also called Transistor pack.

→ Plane is effective for heat dissipation, hence used in Power amplifiers.



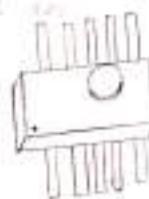
Dual-in-Line Package:

- Popular for commercial applications.
- Chip mounted inside a plastic or ceramic case.
- Easy to handle & mount, widely used.
- Available with 15, 16, 18, 20, 40 pins etc.
- 8 pin Dip is called Mini-DIP.



Flat Pack:

For cases where space is critical, the flat pack gives a compact package. In this type, chip is enclosed in a rectangular ceramic case. The terminals are taken out through sides and ends, available with 8, 10, 14, or 16 pins.



Type	Criteria:
1. Metal Can Package	(i) Heat Dissipation is important. (ii) For high power applications like Power Amps, Voltage regulators etc.
2. DIP	(i) For experimental or bread boarding purposes only 12 pins are required. (ii) Bending/bending of leads is not required. (iii) Suitable for printed circuit boards as lead spacing is more.
3. Flat Pack	(i) More reliability is required. (ii) Light in weight. (iii) Suitable for airborne applications.

If all 3 packages are suitable for the application then the various factors influence the choice of the IC package.

Factors affecting selection of IC package:

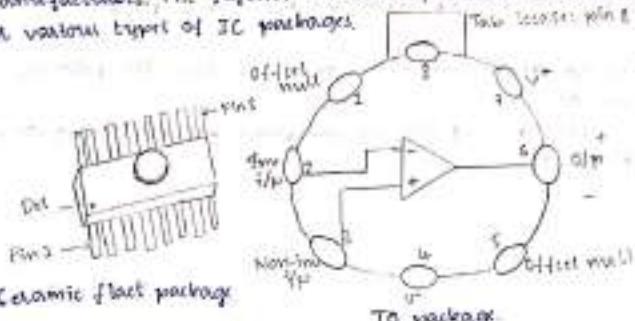
- Relative cost.
- Reliability.
- Weight of the package.
- Ease of IC fabrication.
- Power to be dissipated.
- Need of external heat sink.

Note:

Level of Integration	No of active devices per chip
SSI	Less than 100
MSI	100 - 10,000
LSI	1000 - 1,00,000
VLSI	Over 100,000
ULSI	Over 1 million.

Pin Identification:

The pin identification methods are different as per the manufacturers. The figures shows the pin identification used for various types of IC packages.



(a) 14 lead version flat pack

(b) Metal can package

Temperature Ranges:

There are three different temp. grades based on which the op-amp ICs are classified. These temp. ranges are:

- Military temperature range: -55°C to $+125^{\circ}\text{C}$ (0°C to $+85^{\circ}\text{C}$).
- Industrial temp. range: -40°C to $+85^{\circ}\text{C}$ (0°C to $+85^{\circ}\text{C}$).
- Commercial temp. range: 0°C to 70°C (0°C to 70°C).

Individual data sheet of each IC include the various IC parameters and the temp. conditions under which the parameters are determined. The military grade devices are always superior and with very precisely controlled parameters. The commercial grade ICs have the worst tolerance & hence are the cheapest.

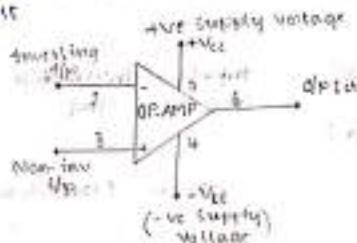
Op-Amp Symbol and Terminals:

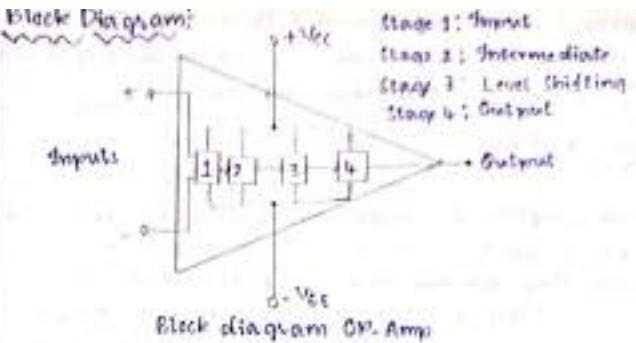
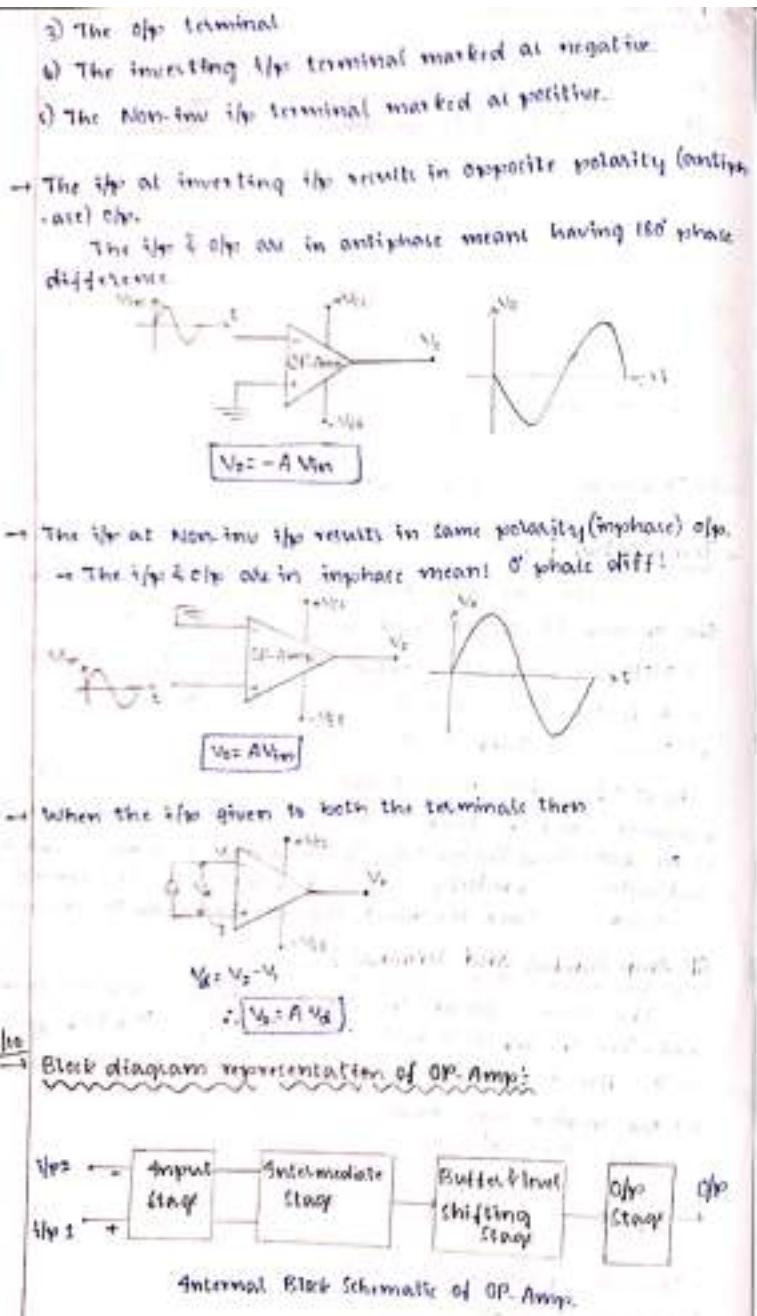
The symbol for an op-amp along with its various terminals. The op-amp is indicated basically by a triangle which points in the direction of signal flow.

All the op-amps have atleast following 7 terminals:

i) The +ve supply voltage terminal V_{CC} (+V).

ii) The -ve supply voltage terminal $-V_{EE}$ (-V).





→ An OP-Amp is a opamp multi stage direct coupled high gain AC feedback amplifier.
 → They're available as ICs.
 → They amplify both AC & DC signals.
 → They can perform mathematical operations like Addition, Sub., Mult., Div.

→ Applications:

- Active filters.
- Oscillators.
- Comparators.
- Voltage Regulators.
- Pulse Generators.

→ Input Stages:

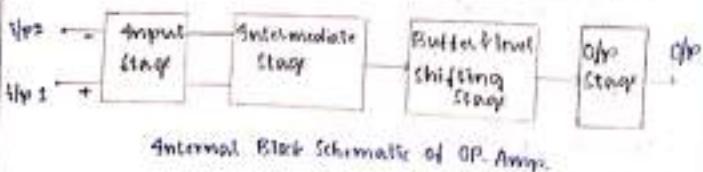
The i/p stage requires high input impedance to avoid loading on the sources. It requires 2 i/p terminals. It also requires low output impedance. All such requirements are achieved by using the DIBO in the i/p stage. The function of diff. Amp is to amplify the difference b/w the two i/p signals. The diff. amplifier has high output impedance. This stage provides most of the voltage gain of the amplifier.

→ **Requirement:** High voltage difference b/w the two inputs & high input impedance.

→ **Intermediate Stage:** Small voltage gain & low output current.

The o/p of the i/p stage drives the next stage which is an intermediate stage. This is another diff. amplifier DIBO. It single ended o/p. The over-all gain requirement of op-amp is very high. The i/p stage alone can't provide such a high gain. The main function of the intermediate stage is to provide an

→ Block diagram representation of OP-Amp:



additional voltage gain required practically intermediate stage isn't a single amplifier but the chain of cascaded amplifiers called Multistage amplifier.

(Requirement: V_{out} has voltage gain. Direct coupling without coupling capacitor.)

④ Level Shifting Stage:

All the stages are directly coupled to each other. As the previous amplifier d.c. signals pass the coupling capacitors don't need tocouple the stages. Hence the d.c. quiescent voltage level of previous stage gets applied at the A_1 to the next stage. Hence stage by voltage dc level remains well above ground potential. Such a high d.c. voltage level may drive the transistors into saturation. This further may cause distortion in the o/p due to clipping. Thus we must limit the maximum o/p voltage swing without any distortion. Hence before the o/p stage, it is necessary to bring such a high d.c. voltage level to zero volts w.r.t. ground.

The level shifter stage brings the d.c. level down to ground potential, when no signal is applied at the A_1 terminals. Then the signal is given to the last stage which is the o/p stage.

The buffer is normally an emitter follower whose input impedance is very high. This prevents loading of the high gain stage.

⑤ Output Stage:

The basic requirements of an o/p stage are low o/p impedance & large o/p voltage swing and high current sourcing & sinking capability.

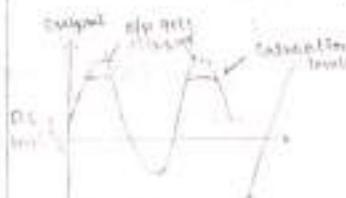
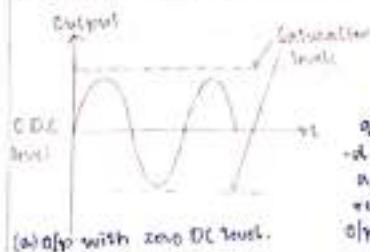
The "Push-Pull complementary amplifier" meets all these requirements & hence used as an o/p stage. This stage increases the o/p voltage swing and keeps the voltage swing symmetric about ground. The stage takes the current supplying capability of the OP Amp.

→ Level Shifting Stage in OP-Amp:

At coupling capacitor stage used to couple the amplifiers in the intermediate stage. The d.c. biasing voltage flows through through the amplifier chain. This finally appears as a significant d.c. component at the o/p along with a.c. o/p.

Following are the effects due to such d.c. component at the o/p:
① The o/p gets distorted.

② It limits the maximum o/p voltage swing.



The main purpose of the level shifting stage is to shift the o/p quiescent d.c. level towards the ground with minimum change in the a.c. signal. This also satisfies the requirement of ensuring that its o/p should have quiescent voltage level of 0V for zero tip signal.

Level Shifting Circuit:

① Simplest level shifting circuit:



It is the simplest type of level shifter circuit.

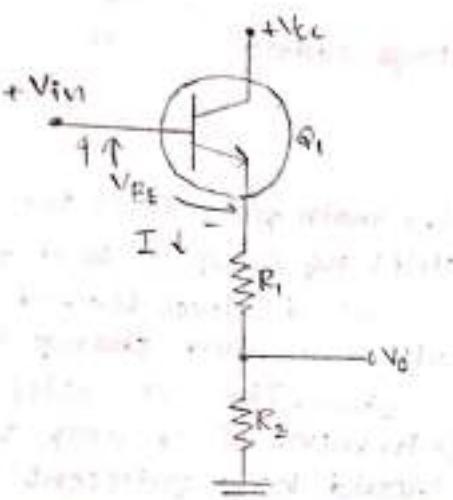
It is basically an emitter follower circuit. In this circuit, the amount of shift obtained is equal to V_{BE} , which is almost 0.7V. So V_{in} is the increased level signal and V_{o} is the o/p with reduced level.

$$V_{in} - V_{BE} - V_0 = 0$$

$$\boxed{V_0 = V_{in} - V_{BE}}$$

Keypoint: The -ve sign indicates the downward shift in the level.

2) Typical level shifting CKT:



But generally a shift of 0.7 V isn't sufficient. Hence the CKT is modified with the help of two resistances R_1 & R_2 .

This is an emitter follower (cf) stage which also acts as a buffer to isolate high gain stages from the o/p stage.

To find the level shift, consider current I flowing through the emitter of the transistor.

Apply KVH to B-E loop.

$$+V_{in} - V_{BE} - I(R_1 + R_2) = 0$$

$$I = \frac{V_{in} - V_{BE}}{R_1 + R_2}$$

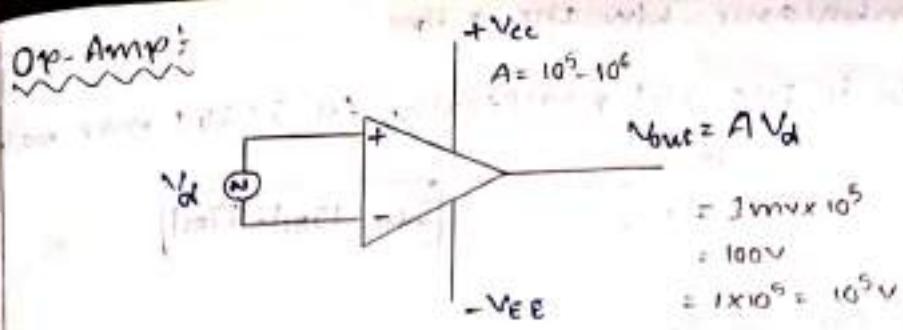
Here,

$$V_0 = IR_2$$

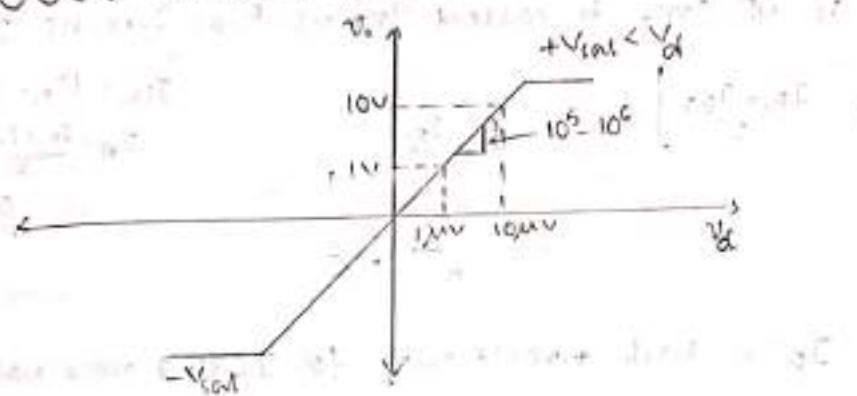
$$\boxed{V_0 = \frac{(V_{in} - V_{BE})R_2}{R_1 + R_2}}$$

Drawbacks:

- i) It's AC gain starts decreasing as R_2 decreased to improve the net d.c. level shift.
- ii) It's o/p impedance is also relatively high (as $R_2 \uparrow$) because of insertion of resistance at the o/p.



Voltage Transfer Curve of Op-Amp:



Parameters of Op-Amp:

They're categorised as of two types.

1) DC characteristics

- g/p bias current.
- g/p offset current.
- g/p offset voltage.
- O/p offset voltage.
- Thermal drift.
- CVRR

2) AC characteristics

- Slew Rate.
- Freq. Response.
- CMRR.

→ Input Offset Current (I_{ios}):

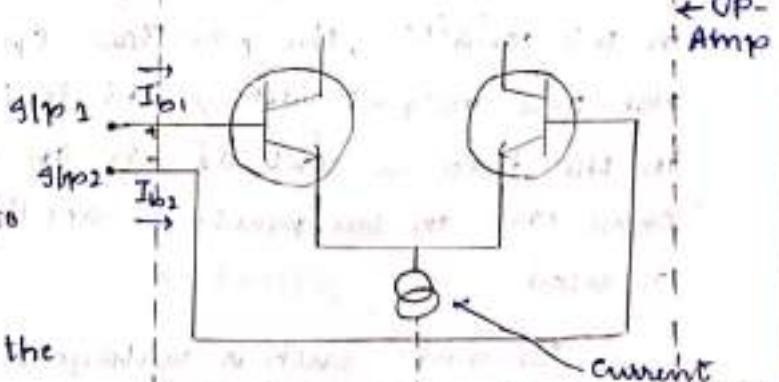
The algebraic difference b/w the currents flowing into the 2 i/p terminals of Op-Amp is called Input Offset Current. (I_{ios}).

Denoted as ' I_{ios} '.

$$I_{ios} = |I_{B1}| - |I_{B2}|$$

I_{B1} : Current flowing into the non-inv i/p.

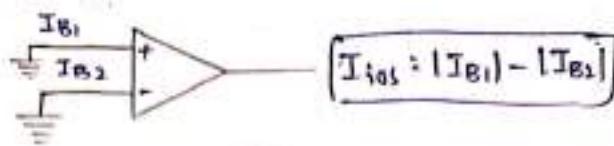
I_{B2} : Current flowing into the inv i/p.



Even though both the transistors are identical it isn't possible to have I_{B1} & I_{B2} exactly equal to each other because of the

internal imbalance b/w the 2 i/p's.

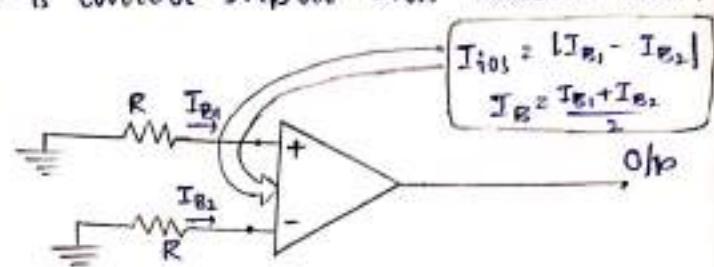
Ideally I_{ios} is zero, but practically for IC741 max value is 200nA.



Soln: Input Bias Current (I_B):

The average of two currents flowing into the i/p terminals of OP-Amp is called Input Bias Current (I_B).

$$I_B = \frac{I_{B1} + I_{B2}}{2}$$



Ideally $I_B = 0$, but practically for IC741 max value is 500nA.

Note: Both I_B and I_{ios} are temperature dependent.

Eg: If the base currents for the emitter coupled transistors of diff. Amps are 18mA & 22mA, determine.
(i) i/p bias current (ii) i/p offset current.

A) Given, $I_{B1} = 18\text{mA}$; $I_{B2} = 22\text{mA}$.

$$(i) I_B = \frac{I_{B1} + I_{B2}}{2} = \frac{18+22}{2} = 20\text{mA}.$$

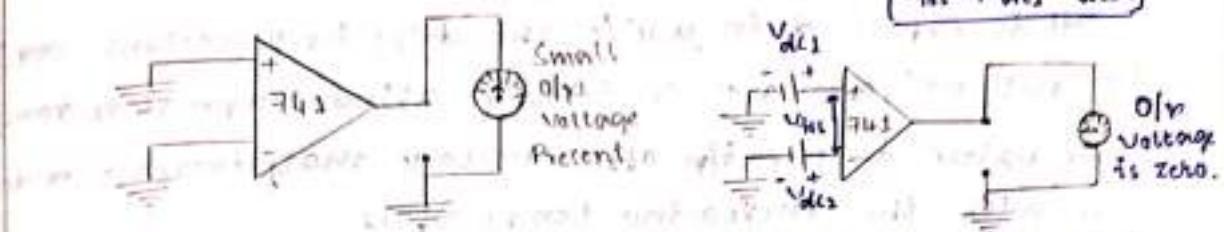
$$(ii) I_{ios} = |I_{B1} - I_{B2}| = |18-22| = 4\text{mA}.$$

Input Offset Voltage:

Whenever both the i/p terminals of the op-amp are grounded, ideally the o/p voltage should be zero. However in this condition, the practical op-amp shows a small non-zero output voltage. This is due to mismatching present in the internal ckt of an op-amp. Such a voltage can cause error in the practical application, for which Op-Amp is used.

To make such a voltage zero, it is necessary to apply small difference voltage b/w the two i/p terminals of an op-amp. This voltage is called Input Offset Voltage.

The differential voltage that must be applied b/w the two i/p terminals of an op-amp, to make the o/p voltage zero is called input offset voltage and denoted as V_{ios} .



The V_{ios} can be +ve or -ve hence absolute value of the V_{ios} is mentioned in the data sheet.

Smaller the V_{ios} , better the matching of the i/p terminals.
Ideally V_{ios} is zero but practically for IC741 max value is 6mV.

Output Offset Voltage (V_{oos}):

The o/p offset voltage is the d.c voltage present at the o/p terminals when both the i/p terminals are grounded. Both i/p offset voltage ' V_{ios} ' and i/p bias current contribute to generate o/p offset voltage.

Thermal Drift:

The op-amp parameters i/p offset voltage ' V_{ios} ', i/p bias current ' I_B ' and i/p offset current ' I_{ios} ' are not constants but vary with the factors:

i) Temperature (ii) Supply voltage changes and (iii) Time.

The effect of change in temperature on the parameters is most severe. Let us discuss the effect of change in temperature on these parameters.

Effect on Input Offset Voltage:

The effect of change in temperature on the i/p offset voltage is defined by a factor called thermal voltage drift. It is also called as i/p offset voltage drift.

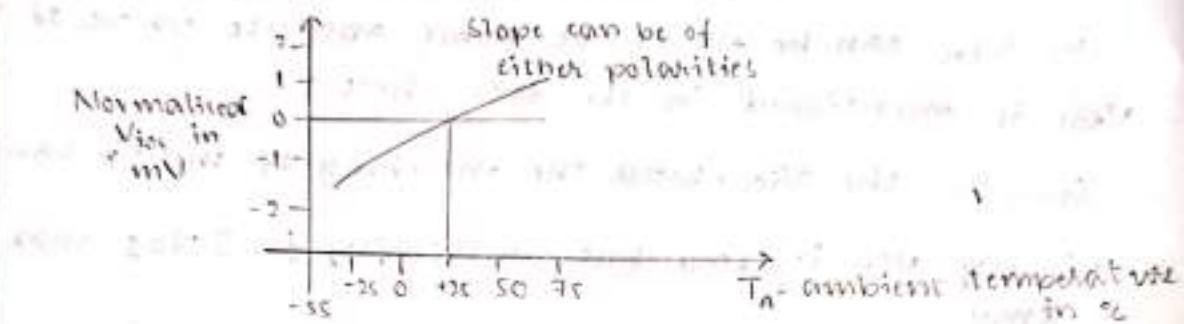
The thermal voltage drift is defined as average rate of change of i/p offset voltage per unit change in temperature.

Mathematically it is given by,

$$\text{I/p offset voltage drift} = \frac{\Delta V_{ios}}{\Delta T}$$

ΔV_{ios} - change in i/p offset voltage.
 ΔT - change in temperature.

It is expressed in $\mu\text{V}/^\circ\text{C}$. The drift isn't constant and it is not uniform over specified operating temperature range. The value of the i/p offset voltage may increase or decrease with the increasing temperature.



The graph of normalized values of i/p offset voltage versus temperature for MC1741 op-amp.

At room temperature, $V_{ios} = 0$ as per graph.

→ Effect on I/p Offset and Bias Currents:

Similar to the i/p offset voltage, i/p bias current & i/p offset current aren't constants but vary with temperature. The effect of temperature on i/p bias current is defined by a factor called "Input bias Current Drift". While effect on i/p offset current is defined by a factor called "Input Offset Current Drift".

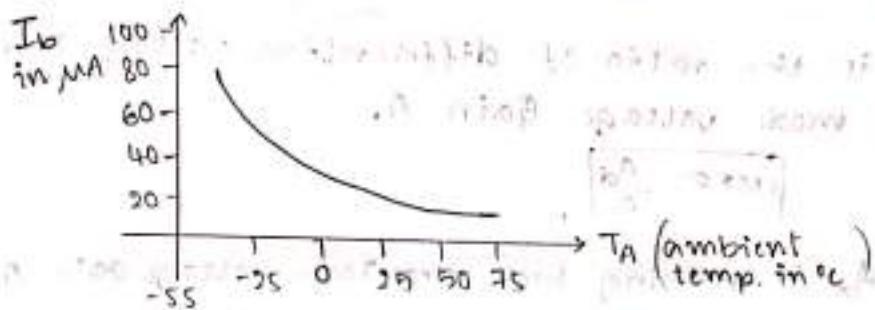
The average rate of change of i/p bias current per unit change in temperature is called I/p Bias Current Drift.

The average rate of i/p offset current per unit change in temperature is called I/p offset Current Drift.

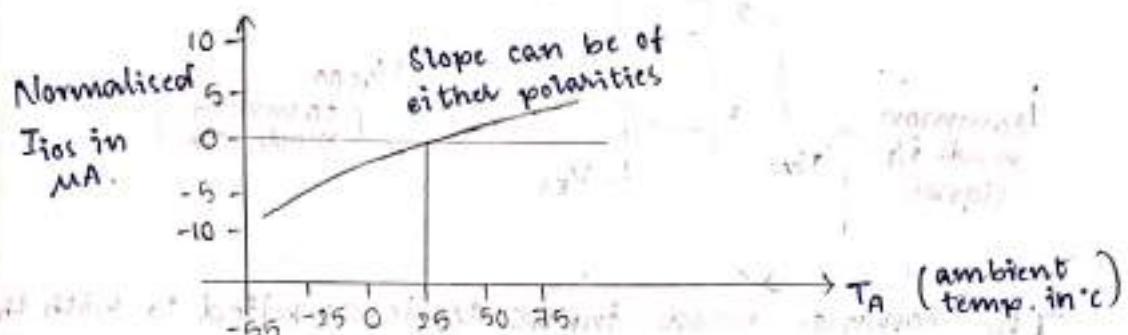
Mathematically,

$$\text{Thermal drift in i/p bias Current} = \frac{\Delta I_{B(i/p)}}{\Delta T}$$

$$\text{Thermal drift in i/p offset Current} = \frac{\Delta I_{ios}}{\Delta T}$$



Input bias current drift.



Op-amp Offset current drift.

→ Differential Input Resistance:

It is also called input resistance of op-amp.

It is the equivalent resistance measured at either the inverting or non-inverting input terminal with the other input terminal grounded. It is denoted as "R_i".

Ideally it should be infinite while for op-amp IC 741 it is of the order of $2M\Omega$, for FET input op-amp it can be as high as few 'G Ω ' ($10^2\text{-}10^3\Omega$).

→ Input Capacitance:

It is the equivalent capacitance measured at either the inverting or non-inverting input terminal with the other input terminal grounded. It is denoted as 'C_i'.

For op-amp 741C, it is 1-4 pF.

→ Open Loop Voltage Gain:

It is the ratio of o/p voltage to the differential i/p voltage, when op-amp is in open loop configuration, without any feedback. It is also called Large Signal Voltage Gain.

Denoted as A_{OL}.

$$A_{OL} = \frac{V_o}{V_d}$$

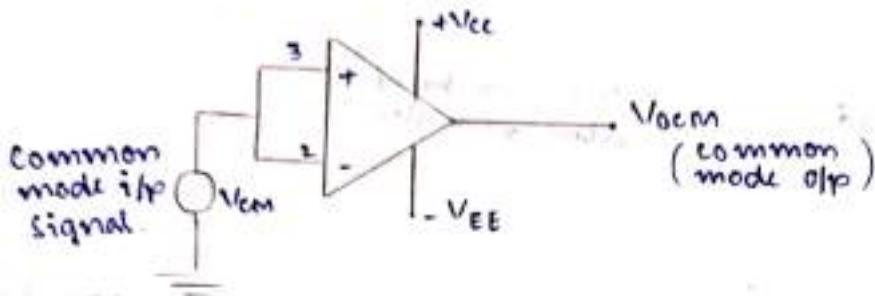
For op-amp IC 741C it is typically 2,00,000.

→ CMRR:

It is the ratio of differential voltage gain A_d to common mode voltage gain A_c .

$$CMRR = \frac{A_d}{A_c}$$

Now A_d is nothing but open loop voltage gain A_{OL} and A_c is measured by using the circuit as shown.



The common mode input V_c is applied to both the i/p terminals of op-amp. Then the output V_{oc} is measured.

Then A_c as
$$A_c = \frac{V_{oc}}{V_c}$$
.

→ Slew Rate: It is the maximum rate of change of output voltage with time.

Units (specified in V/msec).

$$\text{Slew rate } S = \frac{dV_o}{dt} \Big|_{\text{max}}$$

It indicates how fast output changes if i/p is also changing. It is specified by operating op-amp in unity gain condition. Thus if i/p is instantly changing like a square wave then for unity gain, o/p also must change instantly. But practically it can't change instantly. The slew rate indicates how fast the o/p can change.

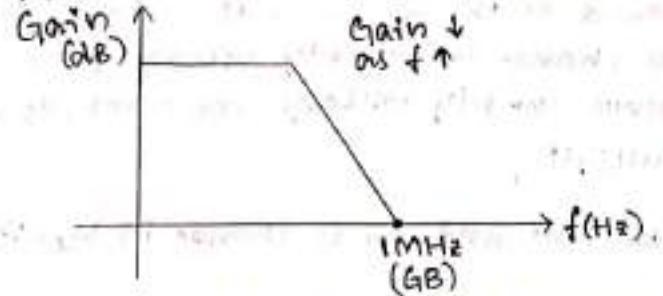
The slew rate is caused due to limited charging rate of the compensating capacitor and current limiting and saturation of the internal stages of an op-amp, when a high frequency large amplitude signal is applied. The internal capacitor voltage cannot change instantaneously. It is given by

$$\frac{dV_o}{dt} = \frac{1}{C}$$

For large charging rate, the capacitor should be small or charging current should be large.

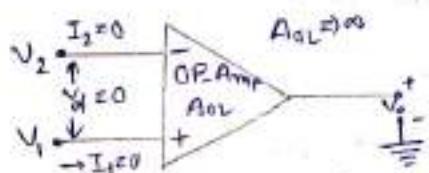
Hence, the slew rate for the op-amp whose maximum internal capacitor charging current is known can be as
$$S = I_{max}/C$$
.

→ Gain Bandwidth Product:



It is the B.W. of Op-Amp when voltage gain is unity(1). It is denoted as GB. The gain is generally expressed in dB. Thus unity gain has dB value $20\log 1 = 0$ dB. So on the graph of gain in dB against frequency, the GB can be shown as above. It is about 1MHz for IC741. The GB is also called "Unity Gain Bandwidth" (UGB) or "Closed loop Bandwidth".

→ Ideal OP-Amp characteristics:



Ideal OP-Amp.

- An ideal op-amp draws no current from both the inputs i.e., $I_1=I_2=0$ & input impedance is ' ∞ '.
- Gain = ∞ , $V_d = V_1 - V_2 = 0$.
- O/p impedance is zero.
- a) Infinite Voltage Gain: ($A_{OL}=\infty$):
It is differential open loop gain. It is infinite for an ideal Op-Amp.

- b) Infinite Input Impedance ($R_{in}=\infty$): (It ensures that no current can flow into an ideal Op-amp).
- c) Zero Output Impedance ($R_o=0$): (ensures that o/p voltage remains same irrespective of load).
- d) Zero Offset Voltage ($V_{o1}=0$): (ensures zero o/p for zero i/p).

- e) Infinite Bandwidth.

- f) Infinite CMRR ($\beta=\infty$): (ensures that $A_v=0$).

- g) Infinite Slew rate ($S=\infty$): (ensures that o/p changes simultaneously with the changes in i/p).

$$S = \frac{dV_o}{dt} \Big|_{\text{maximum}}$$

- h) No effect of temperature.

i) Power Supply Rejection Ratio : (PSRR \neq 0)

It is defined as the ratio of the change in V_{IO} offset voltage due to the change in supply voltage producing it, keeping other power supply voltage constant. It is also called Power Supply Sensitivity.

If V_{EE} is constant and due to change in V_{CC} , there is a change in V_{IO} .

$$PSRR = \frac{\Delta V_{IO}}{\Delta V_{CC}} \mid V_{EE} \text{ constant}$$

If V_{CC} fixed and V_{EE} changes then

$$PSRR = \frac{\Delta V_{IO}}{\Delta V_{EE}} \mid V_{CC} \text{ constant}$$

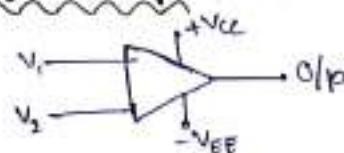
Ideally PSRR = 0.

Expressed in mV/V or MV/V.

→ Large Signal Voltage Gain:

$$\uparrow \text{Voltage Gain} = \frac{V_o}{V_{in}} \rightarrow (\text{large}).$$

→ O/P Voltage Swing:



→ The OP-Amp O/p voltage swing is decided by the supply voltages. It never exceeds the limits $+V_{CC}$ & $-V_{EE}$.

Ideal Characteristics of OP-Amp:

Characteristics	Symbol	Values
Open Loop Voltage Gain	A_{OL}	∞
Input Impedance	R_{in}	∞
Output Impedance	R_o	0
Offset Voltage	V_{os}	0
Bandwidth	B.W	∞
CMRR	P	∞
Skew Rate	S	∞
Power Supply Rejection Ratio	PSRR	0

Voltage Transfer Curve of OP-Amp:

The graph of o/p voltage V_o plotted against the differential i/p voltage V_d ; assuming gain constant Voltage transfer curve or characteristics of op-amp.

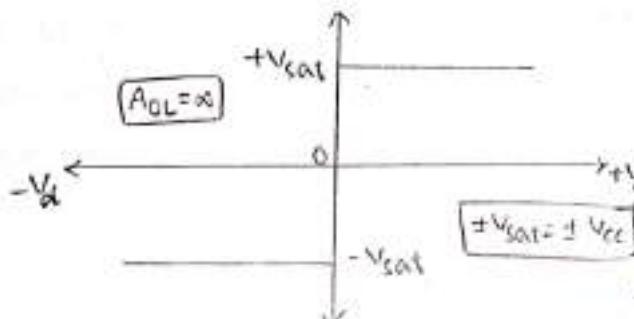
Ideal Voltage Transfer Curve:

Ideally open loop gain of op-amp is ∞ .

$$A_{OL} = \frac{V_o}{V_d} = \infty$$

$$V_d = \frac{V_o}{\infty} = 0$$

$$V_o = A_{OL} V_d$$



Thus for zero i/p, the o/p of op-amp is always at saturation level $\pm V_{sat}$, due to infinite gain. Thus voltage transfer curve for ideal op-amp is a vertical line as shown.

Thus ideally range of i/p for ideal Voltage Transfer Curve, linear operation of op-amp is zero.

Practical Voltage Transfer Curve:

Practically A_{OL} is finite for the op-amp. For op-amp IC741, it is 2×10^5 .

$$V_o = A_{OL} \cdot V_d$$

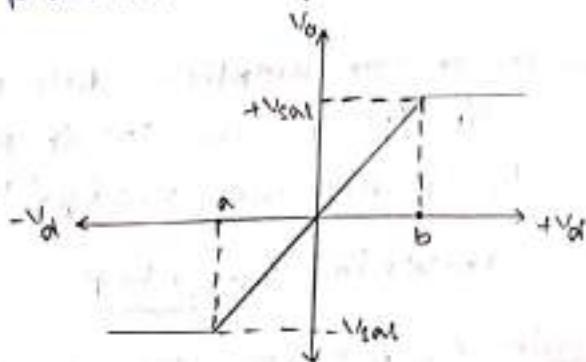
$$\pm V_{sat} = 2 \times 10^5 V_d$$

The saturation voltages are almost $\pm 15V$.

$$V_d = \frac{\pm 15}{2 \times 10^5} = \pm 75 \mu V$$

Here practically till V_d is between $-75 \mu V$ & $+75 \mu V$, the o/p will vary linearly with i/p. But once V_d exceeds $\pm 75 \mu V$, the o/p is saturated.

The practical voltage transfer curve is shown below.



a-b is i/p range for linear operation which is very small.

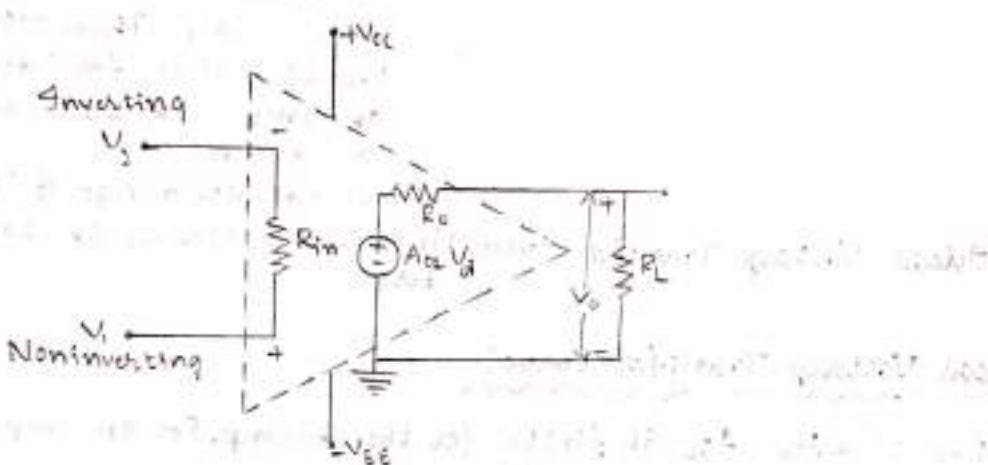
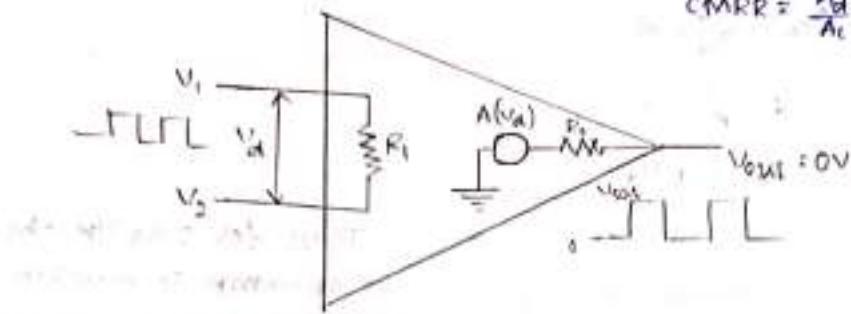
Thus,

- i) If V_d is greater than corresponding to b , the op-amp attains $+V_{sat}$.
- ii) If V_d is less than corresponding to a , the op-amp attains $-V_{sat}$.
- iii) Thus range $a-b$ is i/p range for which op-amp varies linearly with the i/p. But as A_{OL} is very high, practically this range is very small.

→ OP-Amp Equivalent Circuit

$$\text{Slew rate} = \infty \quad [V/\mu\text{s}]$$

$$\text{CMRR} = \frac{A_d}{A_c} = \infty$$



Eq. Ckt of an OP-Amp.

$$V_o = A_{OL} V_d = A_{OL} (V_1 - V_2)$$

Where

A_{OL} = Large signal open loop voltage gain.

V_d = Difference voltage $V_1 - V_2$.

V_1 = Non-inv. i/p voltage w.r.t. ground.

V_2 = Inv. i/p voltage w.r.t. ground.

R_i = i/p resistance of op-amp.

R_o = o/p resistance of op-amp.

$$V_o \propto V_d$$

It is to be noted that the op-amp amplifies difference voltage V_d and not the individual i/p voltages. Thus the o/p polarity gets decided by the polarity of difference voltages V_d .

Voltage "A_{OL}V_d" is Thevenin's eq. voltage source.

R_o = Thevenin's eq. resistance looking back into the o/p terminals.

→ AC Characteristics

→ Transient Response Rise Time

When the o/p of the OP-Amp is suddenly changing like pulse type, then the rise time of the response depends on the cut-off frequency f_H of the op-amp. Such a rise time is called cut-off frequency limited rise time or transient rise time.

$$t_r \propto \frac{1}{f_H}$$

$$t_r = \frac{0.35}{f_H}$$

t_r - Rise time; f_H - Cut-off frequency.

Eg: The open loop gain of a certain op-amp falls to 0dB at a freq. of 10 MHz. Find the transient response rise time, if it is used as unity gain amplifier.

A) For Unity Gain amplifier, $UGB = f_H = 10\text{MHz}$ (Given).

$$\therefore t_r = \frac{0.35}{f_H} = \frac{0.35}{10 \times 10^6}$$

$$[t_r = 35\text{nsec}]$$

→ AC Characteristics of OP-Amp

The important AC characteristics of OP-Amp are

- 1) Slew Rate
- 2) Frequency Response.
- 3) Transient Response, Rise time

→ Slew Rate:

→ Slew rate indicates the ability of OP-Amp with which it can change its o/p according to the changes in input.

→ i.e., how fast OP-Amp can able to respond.

→ The max rate of change of o/p response of the OP-Amp w.r.t. time

$$S = \left. \frac{dV_o}{dt} \right|_{\max} \quad (\text{Practical value is } 0.5 \text{ V/msec}).$$

→ Let $V_s = V_m \sin \omega t$ be the i/p to the OP-Amp. Let the OP-Amp is connected as unity gain amp.

$$\therefore V_o = V_s = V_m \sin \omega t.$$

We have

$$S = \left. \frac{dV_o}{dt} \right|_{\max}$$

$$= V_m \cdot \omega \cdot \cos \omega t \Big|_{\max} = V_m \cdot \omega$$

$$\therefore S = 2\pi f V_m$$

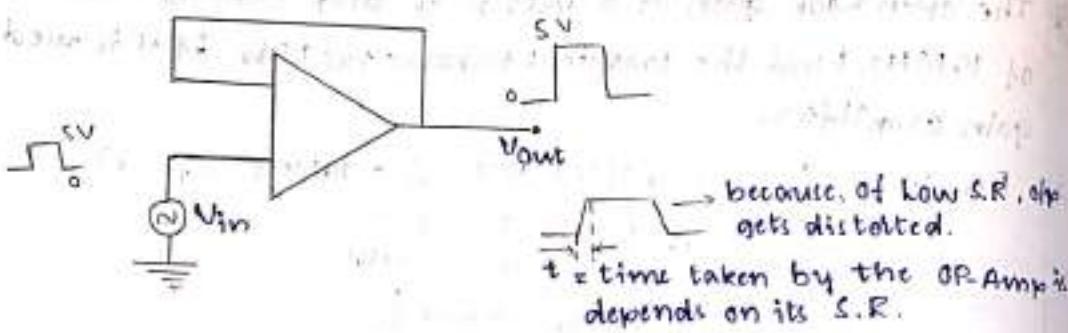
→ The speed of OP-Amp is limited by the charging/discharging time of the largest capacitor present in the OP-Amp.
(Present at intermediate stage to enhance stability of OP-Amp).

The charging current of the capacitance is given by

$$I = C \cdot \frac{dV_o}{dt} \Rightarrow \frac{dV_o}{dt} = I/C$$

$$\text{Slow rate, } S = \frac{dV_o}{dt} \Big|_{\text{max}} = \frac{I_{\text{max}}}{C}$$

$$\therefore S = \frac{I_{\text{max}}}{C}$$



2) Frequency Response of OP-amp:

→ Frequency response of an amplifier is the plot b/w voltage gain and frequency.

→ For an ideal OP-Amp B.W is ' ∞ '.

→ But practically gain falls at high frequencies.

→ This is due to the presence of Compensation Capacitance (or) Parasitic Capacitance.

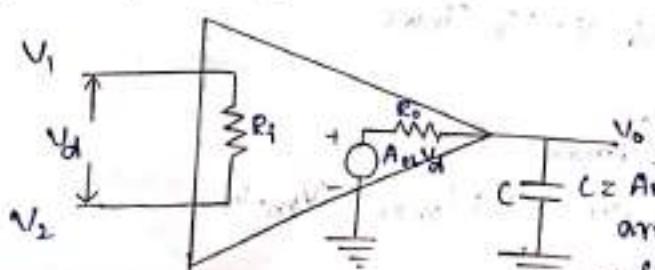
Two conductors separated by insulator on substrate produces capacitance effect called Parasitic Capacitance.

Obtaining the frequency Response:

→ To obtain the frequency response consider the high frequency model of the OP-Amp with capacitance at the o/p.

→ Let $-jX_C$ be the capacitive reactance due to capacitor 'C' from the fig. using voltage divider rule.

$$-jX_C = \frac{1}{j\omega C}$$



C = An internal capacitive effect are represented by this capacitor.

High frequency model of OP-Amp:

$$V_o = \frac{A_{OL} V_d \times \frac{1}{j\omega C}}{R_o + \frac{1}{j\omega C}}$$

$$\frac{V_o}{V_d} = A_v(f) = \frac{A_{OL}}{1 + j\omega R_o C}$$

$$A_v(f) = \frac{A_{OL}}{1 + j\omega f/f_H}$$

$$\boxed{A_v(f) = \frac{A_{OL}}{1 + j\omega f/f_H}}$$

$$\text{where } f_H = \frac{1}{2\pi R_o C}$$

Being Biased Being complex in nature, the gain can be expressed in polar form as follows

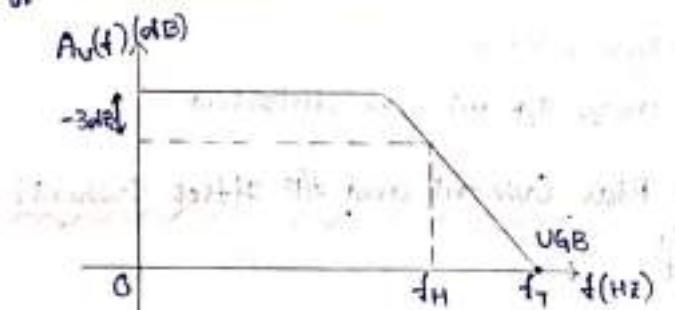
$$|A_v(f)| = \frac{A_{OL}}{\sqrt{1 + (f/f_H)^2}}, \quad \phi(f) = \tan^{-1}(f/f_H)$$

A_{OL} = Gain of OP-amp at '0 Hz'.

f = Operating frequency (Hz).

f_H = break frequency of the OP-Amp Ckt.

V_d = Differential Voltage.



1. At $f = f_H$ gain falls by '3dB'.

f_H is called cut-off frequency
also called corner frequency.

2. For $f < f_H$ - Gain is almost constant.

$f > f_H$ - Gain falls at the rate of 20 dB/dec.

F_T is also called Gain bandwidth Product.

F_T is the 1MHz freq. at 0dB gain i.e., $A=1$

$$\therefore F_T \approx A v f_H$$

3. At $f = F_T$ gain becomes 0dB is called "Unity Gain Frequency".

Eg:1 An OP-Amp operates as a unity gain buffer with 3V (Peak to peak) square wave i/p. If op-amp is ideal with slew rate 0.5 V/Msec, find the maximum freq. of operation.

A) Given ckt is unity Gain,

Peak to peak = 3V of square wave.

$$\therefore V_m = \frac{V_{P-P}}{2} = \frac{3}{2} = 1.5 \text{ V.}$$

From Slew Rate,

$$f_m = \frac{s}{2\pi V_m} = \frac{(0.5)}{\frac{2\pi \times 1.5}{10^6}} \\ = 53.051 \text{ KHz.}$$

This is maximum frequency of operation.

Eg:2 For a typical op-amp, $I_{CQ} = 15 \text{ mA}$ and $C = 35 \text{ pF}$. The peak value of i/p is 12V. Determine slew rate & maximum possible frequency of i/p voltage that can be applied to get undistorted o/p.

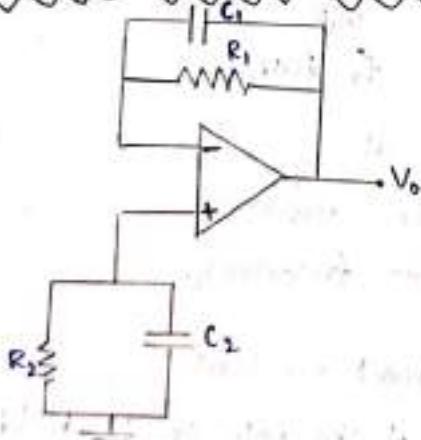
A) $I_{max} = I_{CQ} = 15 \text{ mA}$, $C = 35 \text{ pF}$, $V_m = 12 \text{ V}$.

$$\therefore s = \frac{I_{max}}{C} \\ = \frac{15 \times 10^{-6}}{35 \times 10^{-12}} = 0.4285 \times 10^6 \text{ V/sec} = 0.4285 \text{ V/Musec.}$$

$$\text{and } f_m = \frac{s}{2\pi V_m} = \frac{0.4285 \times 10^6}{2\pi \times 12} \\ = 5.684 \text{ KHz.}$$

Upto this frequency, o/p will be distorted.

→ Measurement of I/P Bias Current and I/P offset Current;



i) I/P bias current defined as the average of the two DC currents entering into two terminals of OP-Amp.

$$I_B = \frac{I_{B1} + I_{B2}}{2}.$$

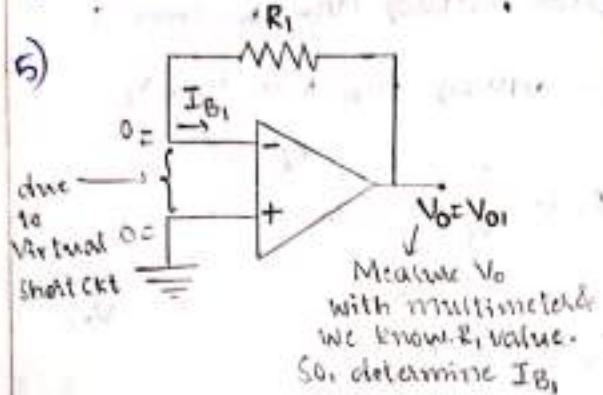
ii) I/P offset current is defined as algebraic difference of two currents.

$$I_{ios} = |I_{B1}| - |I_{B2}|.$$

3) For obtaining $I_B = I_{ios}$ we need to determine I_{B1}, I_{B2} .

4) Now to determine I_{B1} we connect Non-inv node directly to ground.

5)

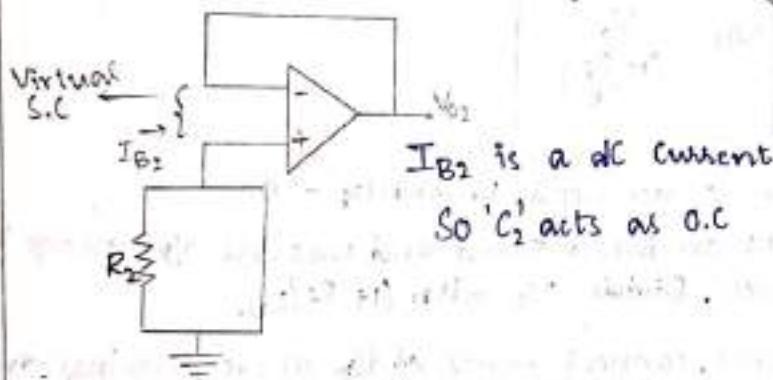


Since the bias current is a DC current. So, 'C' acts as O.C.

∴ The relation b/w R_1, I_{B1}, V_o

$$I_{B1} = \frac{V_{o1} - 0}{R_1} = \frac{V_{o1}}{R_1}.$$

6) To measure I_{B2} , connect inverting i/p node directly to o/p i.e., to create a S.C across R_{if2} .



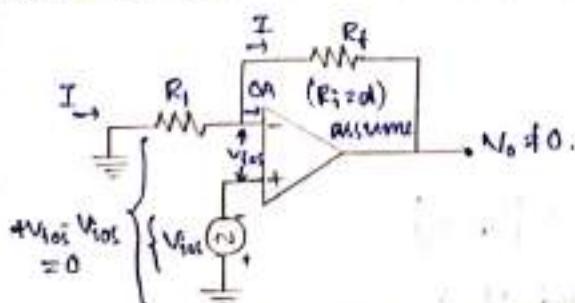
$$I_{B2} = \frac{0 - V_{o2}}{R_2} = -\frac{V_{o2}}{R_2}.$$

7) Once you know I_{B1}, I_{B2} we can calculate.

$$\begin{aligned} I_B &= \frac{I_{B1} + I_{B2}}{2} \\ I_{ios} &= |I_{B1}| - |I_{B2}| \end{aligned}$$

→ Measurement of I_{IP} offset Voltage:

i) I_{IP} offset voltage is defined as the amount of voltage must be applied at i/p in order to make o/p is 'zero'.



2) We need to find out how much voltage must be applied at i/p to make o/p voltage at 'zero'.

3) Practically there is some o/p voltage means o/p offset voltage present because o/p nodes aren't at equal voltages.

4) If two i/p voltages are equal, therefore theoretically o/p voltages 'zero'.

5) If we know V_{ios} , it is required to apply same amount voltage in opposite direction, hence total voltage (V_{ios}) becomes '0'.

6) We need to find difference voltage b/w V_A & V_B .

To find

current through R_1 is

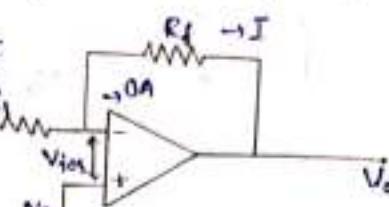
$$I = \frac{0 - V_{ios}}{R_1} \text{ or } I = \frac{-V_{ios}}{R_1}$$

current through R_f is

$$I = \frac{V_{ios} - V_o}{R_f}$$

$$-\frac{V_{ios}}{R_1} = \frac{V_{ios} - V_o}{R_f} \Rightarrow V_o = V_{ios} \left(1 + \frac{R_f}{R_1}\right)$$

$$\therefore \boxed{V_{ios} = \frac{V_o}{\left(1 + \frac{R_f}{R_1}\right)}}$$

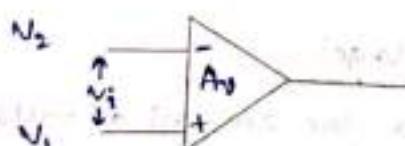


7) For Eq., $V_{ios} = 3\text{mV}$ \therefore We need to apply -3mV .

Connect above ckt on Bread Board and measure o/p voltage V_o using multimeter. Divide V_o with $(1 + R_f/R_1)$.

8) If we get $V_{ios} = 5\text{mV}$, connect -5mV at i/p of $-ve$ terminal. In that way we can cancel offset voltage.

→ Concept of Virtual Ground (or) Virtual Ground Ckt in OP-Amp;



i) $V_i = V_1 - V_2$; $A_v = \frac{V_o}{V_i}$; If Op-amp is ideal, $A_v \approx \infty$.

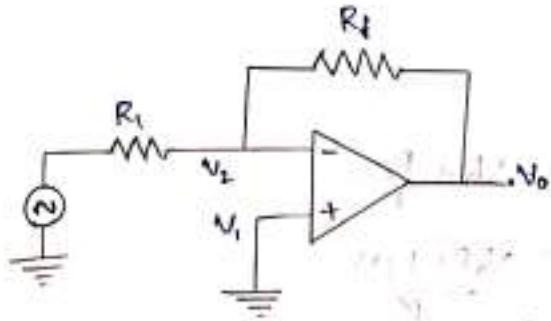
$$A_v \approx \infty \approx \frac{V_o}{V_i}$$

$$\Rightarrow V_i \approx \frac{V_o}{A_v} \approx 0$$

$$\Rightarrow V_1 - V_2 \approx 0 \Rightarrow \boxed{V_1 \approx V_2}$$

3) If V_1 is at physical ground $V_1 = 0$

Then $V_i \approx 0$ (even V_2 not connected to ground).



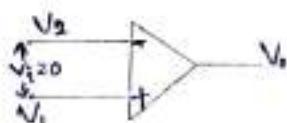
If V_i is at ground, V_2 should be at 0V.

V_i is at Physical Ground, $V_i = 0$.
 Then V_2 is at virtual Ground, $V_2 = 0$ as $V_i = V_2$ ($V_i \neq 0$).

3) Because of $A_{v\infty} = \infty$

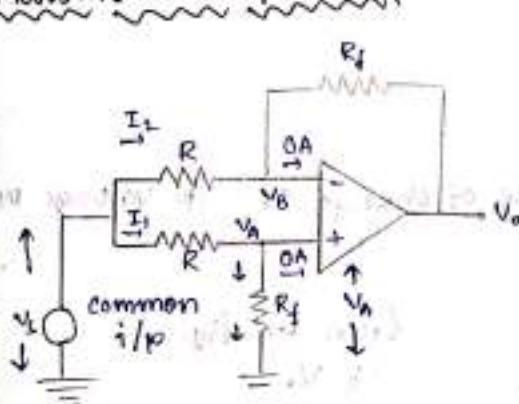
$$V_i = 0 \Rightarrow V_2 = V_1$$

There is no physical wire b/w V_2 & V_i , but still $V_2 = 0$. This is called Virtual Short Ckt.



$V_2 = 0$ (for only short ckt, Voltage $\neq 0$).

→ Measurement of CMRR:



$$\text{1) CMRR} = \frac{A_d}{A_c}$$

V_s = Common mode signal.

2) Common mode Gain is multimeter
 $A_c = \frac{V_o}{V_s}$ (Practically)
 (Theoretically)

3) Differential Gain is

$$A_d = \frac{V_o}{V_i} = \frac{V_o}{(V_A - V_B)} \quad \begin{cases} \text{It can} \\ \text{be calculated} \\ \text{theoretically} \end{cases}$$

4) To find A_d theoretically

According to current directions R & Rf in series. By using voltage divider rule

$$V_A = \frac{V_s \times R_f}{R + R_f}$$

5) For obtaining V_B assume I_2 flowing through R & Rf.

I_2 is written as

$$I_2 = \frac{V_s - V_B}{R}$$

$$I_2 = \frac{V_B - V_o}{R_f}$$

$$\therefore \frac{V_s - V_B}{R} = \frac{V_B - V_o}{R_f}$$

$$\frac{R_f}{R} (V_S - V_B) = V_B - V_o$$

$$\frac{R_f}{R} V_S - \frac{R_f}{R} V_B = V_B - V_o$$

$$\frac{R_f(V_S - V_B)}{R} + V_B \left(1 + \frac{R_f}{R}\right) = V_o + \frac{R_f V_S}{R}$$

$$V_B \left(\frac{R_f+R}{R}\right) = V_o + \frac{R_f V_S}{R}$$

$$V_B = \frac{V_o R}{R_f+R} + \frac{R_f V_S}{R_f+R}$$

Calculate

$$V_A - V_B$$

$$V_A - V_B = \frac{V_S R_f}{R+R_f} - \frac{V_o R}{R_f+R} - \frac{V_S R_f}{R_f+R}$$

$$A_d = \frac{V_o}{V_A - V_B} = \frac{V_o}{-V_o R} = -\frac{R_f+R}{R}$$

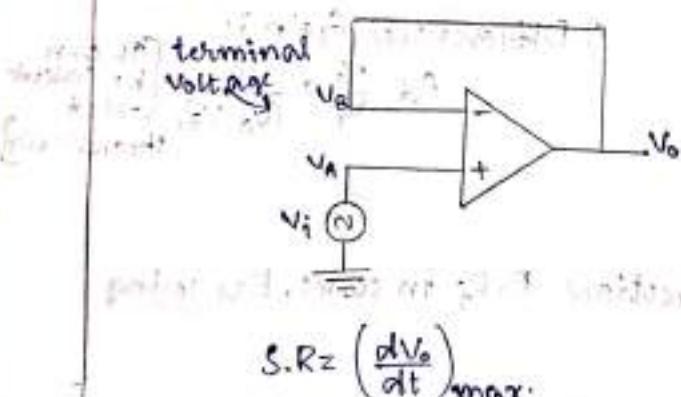
$$A_d = -\frac{(1+R_f)}{R}$$

$\therefore CMRR = \frac{A_d}{A_c} \xrightarrow{\text{Calculated theoretically using } \frac{1+R_f}{R}}$

$A_c \rightarrow$ take ' V_o ' value using multimeter, ' V_S ' open terminal voltage.

→ Measurement of Slew Rate;

→ Slew rate is a maximum rate of change of op-amp voltage w.r.t. time.



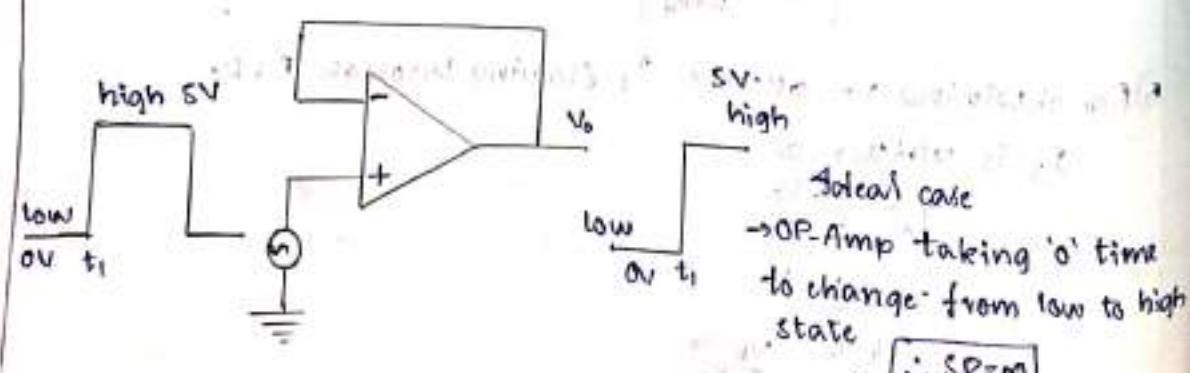
from the fig.

$$V_B = V_o$$

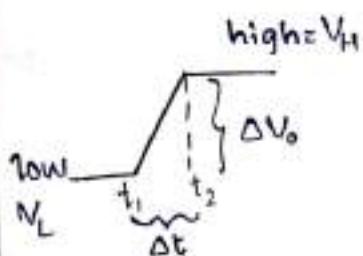
$$V_A = V_B = (\text{one to virtual S.C.})$$

$$V_i = V_B$$

$$\therefore V_o = V_i \quad \text{and} \quad \frac{V_o}{V_i} = 1 \quad (\text{Unity Gain Amplifier})$$



because of S.R op-amp get distorted
 S.R = high
 t_z time taken by the op-amp is depends on its S.R.
 due to parasitic capacitance



$$\begin{aligned}
 S.R &= \left(\frac{dV_o}{dt} \right)_{\max} \\
 &= \left(\frac{\Delta V_o}{\Delta t} \right)_{\max} = \frac{V_H - V_L}{t_2 - t_1}
 \end{aligned}$$

In this way we can measure S.R

→ For example take $V_i = V_m \sin 2\pi f t$

For Unity Gain amp, $V_o = V_i = V_m \sin 2\pi f t$

$$\frac{dV_o}{dt} = \frac{d}{dt} (V_m \sin 2\pi f t) = V_m 2\pi f \cos 2\pi f t$$

$$\left(\frac{dV_o}{dt} \right)_{\max} = (V_m 2\pi f \cos 2\pi f t)_{\max} \quad (\because \cos(2\pi f t) \text{ max value is } 1)$$

$$S.R = 2\pi f V_m$$

Unit 3

Part - I :- Linear application of Op-Amp

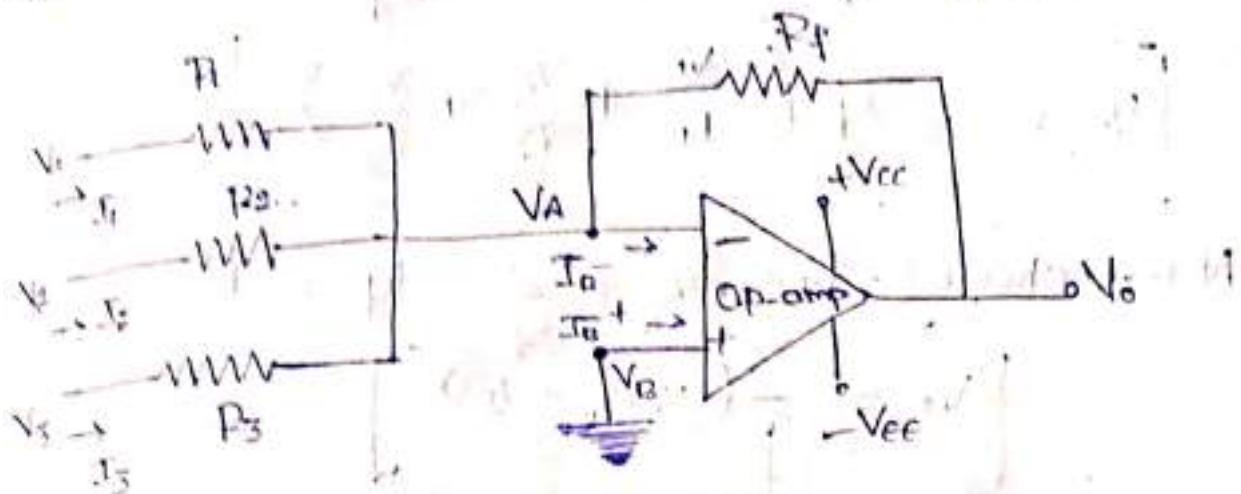
- * Open and closed loop Configuration
- * Inverting and non-inverting amplifiers
- * Summer (S) adder, Subtraction of differential amplifier.
- * Ideal and practical integrator
- * Ideal and practical differentiator
- * Instrumentation amplifier
- * V to I and I to V Converter

Summer (S) Summing Amplifier :-

- A Summer (S) adder is a circuit which is used to add several input signals.
- As the input impedance of the Op-Amp is very high, therefore more number of input signals can be applied to the Op-Amp.
- There are two types of Summing Amplifier.
 1. Inverting Summing amplifier.
 2. Non-inverting Summing Amplifier.

Inverting Summing Amplifier :-

The figure shows Inverting Summing Amplifier with three inputs. Signals V_1, V_2, V_3 are applied to three Resistors R_1, R_2, R_3 .



Analytic :-

from the figure $V_A = 0$

According virtual ground concept

$$V_A = V_B = 0$$

Now

$$I_1 = \frac{V_1 - V_A}{R_1} = V_1 / R_1$$

$$I_2 = \frac{V_2 - V_A}{R_2} = V_2 / R_2$$

$$I_3 = \frac{V_3 - V_A}{R_3} = V_3 / R_3$$

$$I_f = \frac{V_A - V_o}{R_f} = -V_o / R_f$$

Apply KVL at node 'A'

$$I_1 + I_2 + I_3 = I_f + I_B^-$$

$$\frac{V_1}{R_1} + \frac{V_2}{R_2} + \frac{V_3}{R_3} = -\frac{V_o}{R_f} + 0 \quad (I_B^- = 0)$$

$$V_o = -R_f \left(\frac{V_1}{R_1} + \frac{V_2}{R_2} + \frac{V_3}{R_3} \right)$$

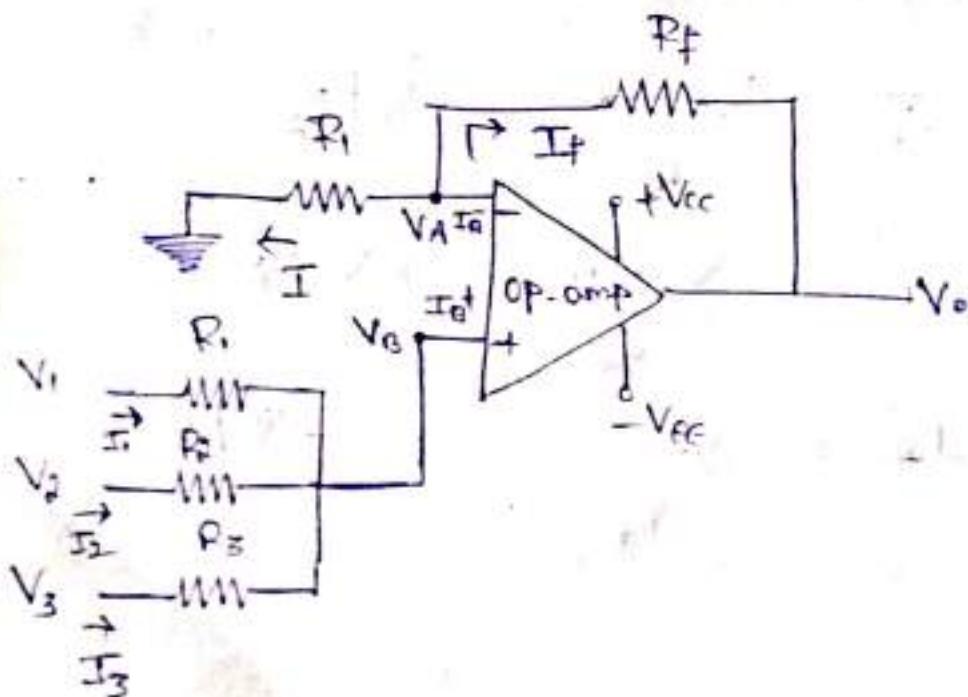
Now, choose $R_1 = R_2 = R_3 = R_f = R$

$$V_o = -(V_1 + V_2 + V_3)$$

indicates inverting amplifier

Non-inverting Summing Amplifier :-

The figure shows non-inverting summing amplifier with three input signals V_1, V_2, V_3 are applied to the resistors R_1, R_2, R_3 .



Analysis :- According to virtual ground process
 $\Rightarrow V_A = V_B$

from the figure

$$I_1 = \frac{V_1 - V_B}{R_1} = \frac{V_1 - V_A}{R_1}$$

$$I_2 = \frac{V_2 - V_B}{R_2} = \frac{V_2 - V_A}{R_2}$$

$$I_3 = \frac{V_3 - V_B}{R_3} = \frac{V_3 - V_A}{R_3}$$

Apply KCL at node B

$$I_1 + I_2 + I_3 = I_B^+$$

$$\frac{V_1 - V_A}{R_1} + \frac{V_2 - V_A}{R_2} + \frac{V_3 - V_A}{R_3} = 0 \quad (I_B^+ = 0)$$

$$\frac{V_1}{R_1} - \frac{V_A}{R_1} + \frac{V_2}{R_2} - \frac{V_A}{R_2} + \frac{V_3}{R_3} - \frac{V_A}{R_3} = 0$$

$$\frac{V_1}{R_1} + \frac{V_2}{R_2} + \frac{V_3}{R_3} = \frac{V_A}{R_1} + \frac{V_A}{R_2} + \frac{V_A}{R_3}$$

$$V_B = V_A = \frac{V_1/R_1 + V_2/R_2 + V_3/R_3}{(1/R_1 + 1/R_2 + 1/R_3)}$$

from the figure

$$I_F = \frac{V_A - V_o}{R_F} = \frac{V_B - V_o}{R_F}$$

$$I = \frac{V_A}{R_1} = \frac{V_B}{R_1}$$

Apply KCL at node A

$$I + I_B + I_f = 0$$

$$I = -I_f$$

$$I = -\left(\frac{V_B - V_o}{R_f}\right)$$

$$I = -\frac{V_B}{R_f} + \frac{V_o}{R_f}$$

$$\frac{V_B}{R_1} = -\frac{V_B}{R_f} + \frac{V_o}{R_f}$$

$$V_B \left(\frac{1}{R_1} + \frac{1}{R_f} \right) = \frac{V_o}{R_f}$$

$$V_o = R_f \left(\frac{1}{R_1} + \frac{1}{R_f} \right) V_B$$

$$V_o = R_f \left[\frac{1}{R_1} + \frac{1}{R_f} \right] \left[\frac{V_1/R_1 + V_2/R_2 + V_3/R_3}{1/R_1 + 1/R_2 + 1/R_3} \right]$$

Choose $R_1 = R_2 = R_3 = R_f = R$

$$V_o = \frac{R \left(\frac{1}{R} + \frac{1}{R} \right) \left[\frac{V_1}{R} + \frac{V_2}{R} + \frac{V_3}{R} \right]}{1/R + 1/R + 1/R}$$

$$V_o = \frac{2}{3} (V_1 + V_2 + V_3)$$

Case 2 :- $R_1 = R_2 = R_3 = R$, $R_f = 2R$

$$V_o = \frac{1}{2R} \left[\frac{1}{R} + \frac{1}{2R} \right] \left[\frac{V_1/R + V_2/R + V_3/R}{1/R + 1/R + 1/R} \right]$$

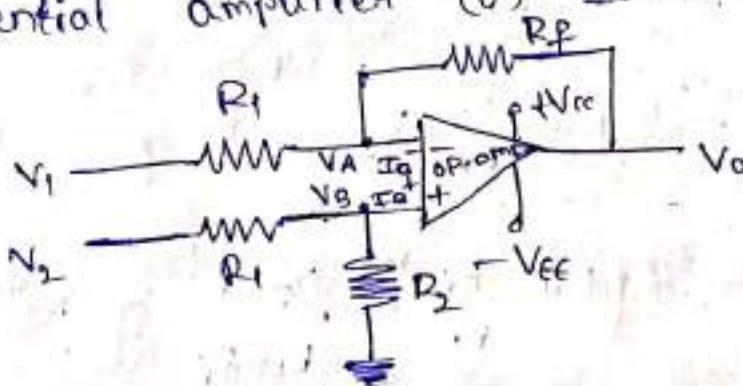
$$= \frac{1}{2R} \left[\frac{2+1}{2R} \right] \frac{(V_1 + V_2 + V_3)/R}{3/R}$$

$$= \beta \times (V_1 + V_2 + V_3) \frac{1}{R} \times \frac{R}{3}$$

$$\boxed{V_o = V_1 + V_2 + V_3}$$

Subtractor / Difference amplifier :-

Subtractor is a device (SI) circuit which is used to produce the difference b/w the input signal. The figure shows basic differential amplifier (SI) Subtractor.



Analysis :-

according to Virtual ground Concept

$$\boxed{V_A = V_B}$$

How the response of the differential amplifier can be obtained by using Super position theorem.

Case 1 :- V_1 is active and V_2 is grounded
then the subtractor becomes inverting amplifier.

$$\text{Now, inverting amplifier } V_{o1} = -\frac{R_f}{R_i} V_1$$

$$= -\frac{R_f}{R_i} V_1 \rightarrow ①$$

Case 2 :- V_1 is grounded and V_2 is active,
then the subtractor becomes non-inverting amplifier.

Now, Non-inverting Amplifier

$$V_{o2} = \left(1 + \frac{R_f}{R_i}\right) V_2$$

$$= \left(1 + \frac{R_f}{R_i}\right) V_B$$

$$= \left(1 + \frac{R_f}{R_i}\right) \frac{V_B R_2}{R_1 + R_2} \rightarrow ②$$

$$V_o = V_{o1} + V_{o2}$$

$$= -\frac{R_f}{R_i} V_1 + \left(1 + \frac{R_f}{R_i}\right) \frac{V_B R_2}{R_1 + R_2}$$

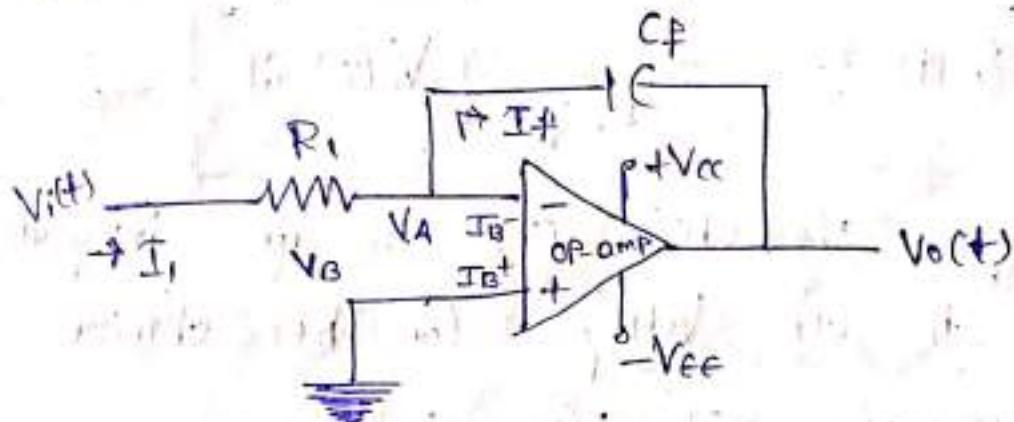
$$= -\frac{R_f}{R_i} V_1 + \left(1 + \frac{R_f}{R_i}\right) \frac{V_B R_2}{R_1 + R_2}$$

$$V_o = -\frac{R_2}{R_1} V_i + \left(\frac{R_2 + R_f}{R_1} \right) \frac{V_2 - V_o}{R_2 + R_f}$$

$$= -\frac{R_2}{R_1} V_i + V_2 \frac{R_f}{R_1}$$

$$V_o = \frac{R_f}{R_1} (V_2 - V_1)$$

Ideal Integrator :- In integrator CKT which produces time integral of input signal at the output. The figure shows an ideal OP-AMP Integrator.



Analysis :-

From the figure $V_B = 0$

according to virtual ground concept

$$V_A = V_B = 0 \quad (\because V_B = 0)$$

From the figure

$$I_1 = \frac{V_i(t) - V_A}{R_1}$$

$$V = \frac{1}{C} \int i dt$$

$$I = C \frac{dv}{dt}$$

$$I_f = C_f \cdot \frac{d(V_A - V_o(t))}{dt}$$

$$T_f = -C_f \frac{dV_i(t)}{dt}$$

Apply KCL at node A

$$I_i = I_f + I_n$$

$$[I_f = I_i] \Rightarrow (I_n = 0)$$

$$\frac{V_o(t)}{R_i} = -C_f \int \frac{dV_i(t)}{dt}$$

$$\frac{dV_o(t)}{dt} = -\frac{1}{R_i C_f} V_i(t)$$

$$V_o(t) = -\frac{1}{R_i C_f} \int V_i(t) dt \rightarrow ①$$

from eq ① the above circuit is an integrator
because the o/p Voltage can be obtained
by integration of i/p Voltage.

frequency response of the ideal integrator :-

→ frequency response is graph drawn
between frequency vs gain in db.

→ In Order to draw the frequency
response let us consider a eqn ①

$$① \Rightarrow V_o(t) = -\frac{1}{R_i C_f} \int V_i(t) dt$$

apply Laplace transform on b & c

$$V_o(s) = -\frac{1}{R_1 C_f} \cdot V_i(s) \cdot \frac{1}{s}$$

$$\Rightarrow V(j\omega) = -\frac{1}{j\omega R_1 C_f} V_i(j\omega)$$

Now, $A = \frac{V_o(j\omega)}{V_i(j\omega)} = -\frac{1}{j\omega R_1 C_f} \quad (\because \omega = 2\pi f)$

$$|A| = \left| \frac{V_o(j\omega)}{V_i(j\omega)} \right| = \left| \frac{-1}{j\omega R_1 C_f} \right| \quad \begin{cases} \therefore |a| = a \\ |ib| = b \end{cases}$$

$$|A| = \left| \frac{1}{j\omega R_1 C_f} \right|, |A| \text{ in dB} = 20 \log \frac{1}{j\omega R_1 C_f}$$

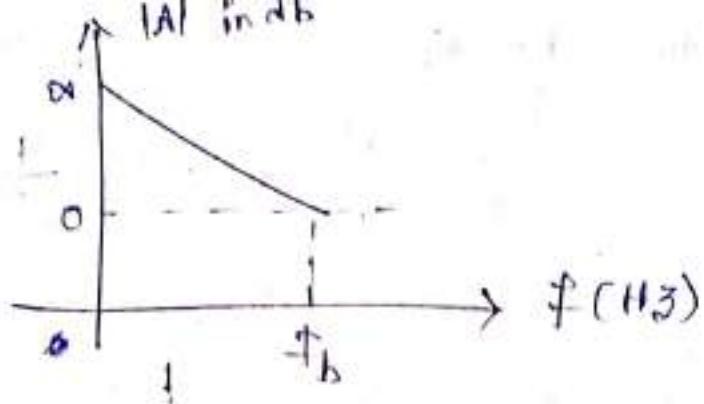
put $\omega = 0 \Rightarrow |A| = \infty, |A| \text{ in dB} = \infty$

at $\omega = \omega_b \Rightarrow |A| \text{ in dB} = 0$

$$\Rightarrow 20 \log \frac{1}{j\omega_b R_1 C_f} = 0$$

$$\frac{1}{j\omega_b R_1 C_f} = 10^0 = 1$$

$$\boxed{\omega_b = \frac{1}{j\omega R_1 C_f}} \rightarrow \text{Cut off frequency}$$



Drawbacks of ideal integrator :-

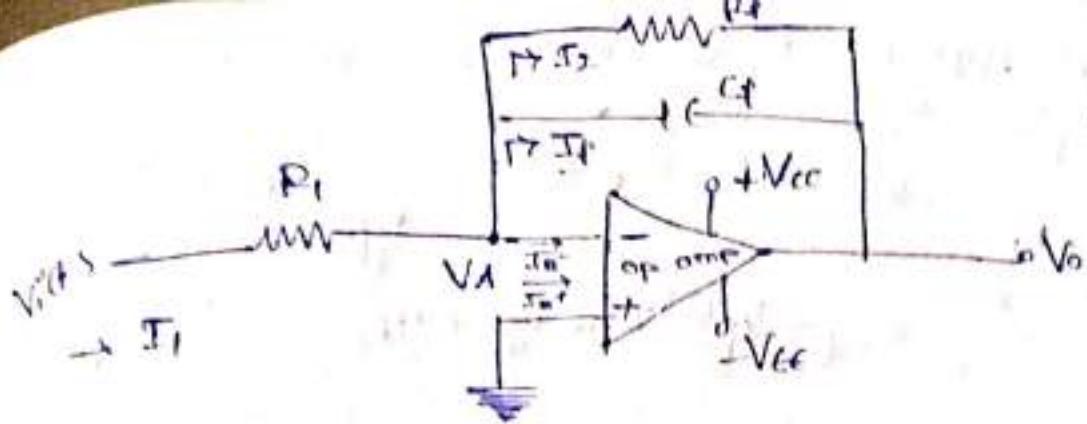
→ When the input signal is zero (81) at low frequency (81) low value then the feed back capacitor (C_f) acts as 0. Open circuit . then the integrator becomes open loop OP-amp . hence the gain is '0' .

* This problem can be avoided in practical integrator by shunting the resistor (R_f) in parallel with C_f .

practical integrator :-

→ The practical integrator can be obtained by placing a feed back Resistor (R_f) in shunt with C_f .

→ Here the parallel combination C_f and R_f decouples some power. Hence the practical integrator is also called as lossy integrator .



Analysis :-

from the figure $V_B = 0$

according to virtual ground concept

$$V_A = V_B = 0$$

from the figure,

$$I_1 = \frac{V_i(t) - V_A}{R_1} = \frac{V_i(t)}{R_1}$$

$$I_f = C_f \frac{d(V_A - V_o(t))}{dt}$$

$$= -C_f \frac{dV_o(t)}{dt}$$

$$I_g = \frac{V_A - V_o}{R_g} = -\frac{V_o}{R_g}$$

Apply KVL at node A

$$\Rightarrow I_1 = I_B + I_f + I_g$$

$$I_1 = I_f + I_g \quad (\because I_B = 0)$$

$$\frac{V_i(t)}{R_1} = -C_f \frac{dV_o(t)}{dt} - \frac{V_o(t)}{R_g}$$

Apply Laplace transform

$$\frac{V_i(s)}{R_1} = -C_F s V_o(s) - \frac{1}{R_F} V_o(s)$$
$$= -V_o(s) (s C_F + 1/R_F)$$

$$V_o(s) = \frac{-V_i(s)}{R_1 (s C_F + 1/R_F)}$$

\therefore The value R_F must be high.

frequency response of practical amplifier :-

→ frequency response is the graph drawn b/w frequency V_o gain in db.

→ In order to draw the frequency response

let us consider $V_o(s) = -V_i(s)$

$$\frac{R_1 (s C_F + 1/R_F)}{-(R_F/R_1) V_i(s)}$$
$$= \frac{-(R_F/R_1)}{(1 + s C_F R_F)} V_i(s)$$

Now,

$$A = \frac{V_o(s)}{V_i(s)} = \frac{-(R_F/R_1)}{1 + s C_F R_F}$$

$$\text{put } s = j\omega$$

$$A = \frac{V_o(j\omega)}{V_i(j\omega)} = \frac{- (P_f | R_1)}{1 + j(\frac{f}{f_a} + P_f)} \quad (\because \omega = 2\pi f)$$

Consider $f_a = \frac{1}{2\pi P_f C_f}$

$$\Rightarrow A = \frac{V_o(j\omega)}{V_i(j\omega)} = \frac{- (P_f | R_1)}{1 + j(\frac{f}{f_a})}$$

$$|A| = \left| \frac{V_o(j\omega)}{V_i(j\omega)} \right| = \left| \frac{- (P_f | R_1)}{1 + j(\frac{f}{f_a})} \right|$$

$$|A| = \left| \frac{V_o(j\omega)}{V_i(j\omega)} \right| = \frac{|P_f | R_1}{\sqrt{1 + \left(\frac{f}{f_a} \right)^2}}$$

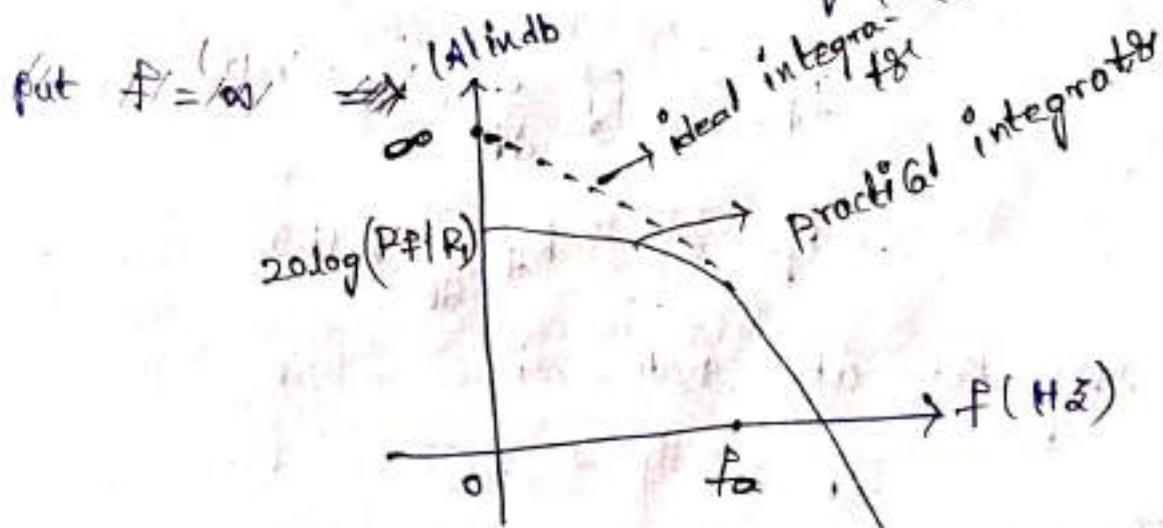
$$|A| \text{ in dB} = 20 \log \left(\frac{|P_f | R_1}{\sqrt{1 + \left(\frac{f}{f_a} \right)^2}} \right)$$

if put $f = 0 \Rightarrow |A| \text{ in dB} = 20 \log \left(\frac{P_f}{R_1} \right)$

put $f = f_a \Rightarrow |A| \text{ in dB} = 20 \log \left(\frac{P_f / R_1}{\sqrt{2}} \right)$

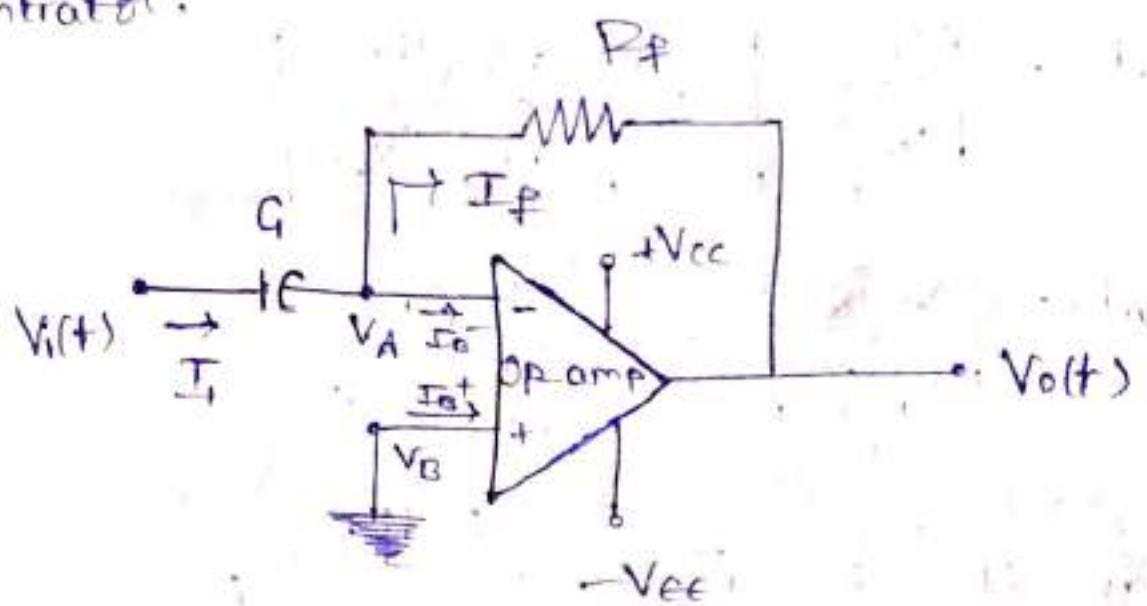
$$= 20 \log \left(\frac{1}{\sqrt{2}} \right) + 20 \log \left(\frac{P_f}{R_1} \right)$$

$$= -3 \text{ dB} + 20 \log \left(\frac{P_f}{R_1} \right)$$



ideal Differentiator :-

- * Differentiator is the ckt which produces time integral of the ifp signal at the op of the Op-amp.
- * The figure shows an ideal Op-Amp differentiator.



Analysis :-

from the figure $V_B = 0$

according to Virtual ground Concept

$$V_A = V_B = 0 \quad (\because V_B = 0)$$

from the figure

$$I_1 = C \frac{d}{dt} (V_i(t) - V_A) = C \frac{d V_i(t)}{dt}$$

$$I_F = \frac{V_A - V_o(t)}{R_F} = \frac{-V_o(t)}{R_F}$$

Apply KCL at node A,

$$I_1 = I_F + I_B$$

$$C \frac{d V_i(t)}{dt} = \frac{-V_o(t)}{R_F}$$

$$-V_o(t) = C R_F \frac{d V_i(t)}{dt}$$

$$V_o(t) = -C R_F \frac{d V_i(t)}{dt}$$

→ ①

from Eq ①, the above ckt is an
differentiator because the op voltage can
be obtained by differentiating the ip.

frequency response of the ideal differentiator

* frequency response is the graph drawn b/w frequency and gain.

→ In Order to draw the frequency response

Let us consider the Eq ① $\Rightarrow V_o(t) = -R_f G \frac{dV_i}{dt}$

$$\Rightarrow V_o(s) = -R_f G s V_i(s)$$

$$A = \frac{V_o(s)}{V_i(s)} = -R_f G s$$

$$A = \frac{V_o(j\omega)}{V_i(j\omega)} = -R_f G j\omega = -R_f C_1 j^2 \pi f$$

Consider 0 frequency $f_0 = \frac{1}{2\pi R_f C_1}$

$$\Rightarrow A = \frac{V_o(j\omega)}{V_i(j\omega)} = -j(f/f_0)$$

$$|A| = \left| \frac{V_o(j\omega)}{V_i(j\omega)} \right| = \left| (f/f_0) \right|$$

$$|A| \text{ in dB} = 20 \log (f/f_0)$$

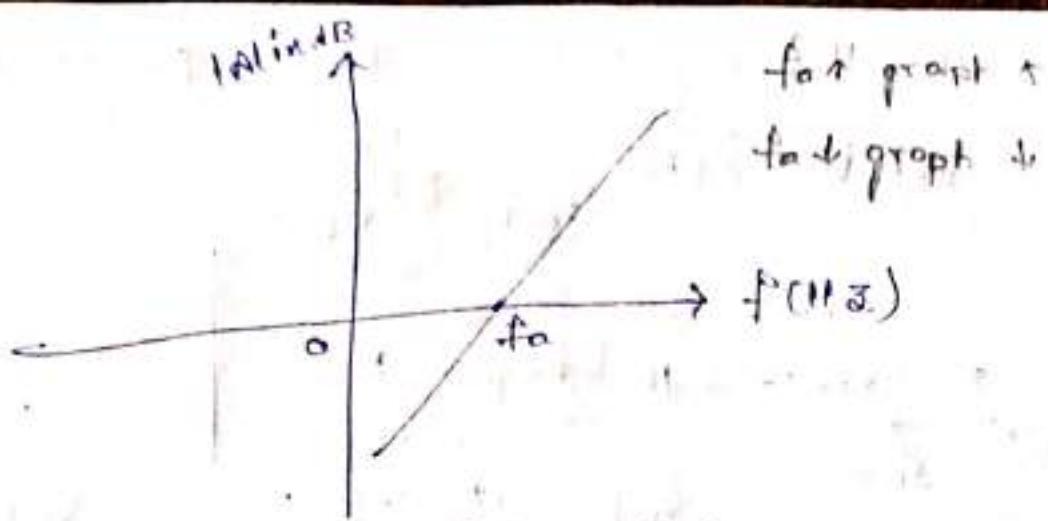
$$\text{put } f=f_0 \Rightarrow |A| \text{ in dB} = 20 \log(1) = 0 \text{ dB}$$

$$f=2f_0 \Rightarrow |A| \text{ in dB} = 20 \log(2) = 6.02 \text{ dB}$$

$$f=3f_0 \Rightarrow |A| \text{ in dB} = 20 \log(3) = 9.54 \text{ dB}$$

$$f=f_0/2 \Rightarrow |A| \text{ in dB} = 20 \log(\frac{1}{2}) = -6.2 \text{ dB}$$

$$f=f_0/3 \Rightarrow |A| \text{ in dB} = 20 \log(\frac{1}{3}) = -9.5 \text{ dB}$$



Limitation of ideal differentiator :-

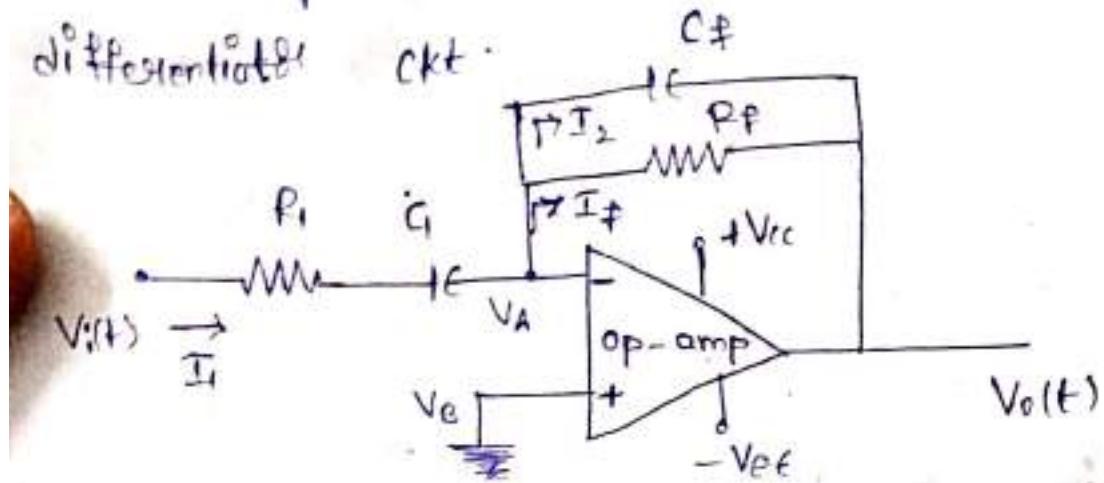
→ The differentiator Ckt's are more sensitive to noise, Noise Signals with small amplitudes will have large derivatives at the output. So to avoid the noise signals entering into the differentiator place resistor R_f in series with G .

→ In order to limit the high frequency gain of the differentiator place a capacitor C_f in H with R_f .

practical differentiator :-

===== The (draw) limitations of the ideal differentiator are eliminated in practical differentiator by placing Resistor R_i in series with G , the capacitor R_f in shunt with C_f .

→ The figure shows the practical differentiator ckt.



from the figure $V_B = 0$

According to Virtual Ground Concept,

$$V_A = V_B = 0$$

From the figure

$$I_1 = \frac{V_i(t) - V_A}{R_1 + 1/\text{sc}_f} = \frac{V_i(t)}{R_1 + 1/\text{sc}_f}$$

$$I_f = \frac{V_A - V_o(t)}{R_f} = -\frac{V_o(t)}{R_f}$$

$$I_o = V_A - C_f \frac{dV_o(t)}{dt}$$

Apply KCL at node 'A'

$$I_1 = I_B^- + I_f + I_o$$

$$\Rightarrow I_1 = I_f + I_o \quad (\because I_B^- = 0)$$

$$\Rightarrow \frac{V_i(t)}{R_1 + 1/\text{sc}_f} = -\frac{V_o(t)}{R_f} - C_f \frac{dV_o(t)}{dt}$$

$$\rightarrow \frac{V_i(s)}{R_1 + sC_1} = \frac{V_o(s)}{R_f} - C_F s V_o(s)$$

$$= \left(\frac{1}{R_f} + sC_F \right) V_o(s)$$

$$\frac{V_i(s) sG_F}{(1 + sG_F R_1)} = - \frac{(1 + sC_F R_f)}{R_f} V_o(s)$$

$$V_o(s) = \frac{-sC_F R_f}{(1 + sC_F R_f)(1 + sG_F R_1)} V_i(s)$$

frequency response of the practical differentiator:-

* Frequency response is the graph drawn b/w frequency and gain.

* In Order to draw the frequency response set up Consider the Eq ①

$$\Rightarrow V_o(s) = \frac{-sC_F R_f}{(1 + sC_F R_f)(1 + sG_F R_1)} V_i(s)$$

$$A = \frac{V_o(s)}{V_i(s)} = \frac{-sC_F R_f}{(1 + sC_F R_f)(1 + sG_F R_1)}$$

$$\text{put } s = j\omega \text{ and } \omega = 2\pi f$$

$$\frac{V_o(j\omega)}{V_i(j\omega)} = \frac{-j^2\pi f C_f R_f}{(1+j^2\pi f C_f R_f)(1+j^2\pi f C_1 R_1)}$$

put $C_f R_f = C_1 R_1$

$$A = \frac{V_o(j\omega)}{V_i(j\omega)} = \frac{-j^2\pi f R_f C_1}{(1+j^2\pi f C_1 R_1)(1+j^2\pi f C_1 R_1)}$$

$$= \frac{-j^2\pi^2 R_f C_1}{(1+j^2\pi f C_1 R_1)^2}$$

$$f_0 = \frac{1}{2\pi R_1 C_1} \quad \& \quad f_b = \frac{1}{2\pi R_f C_1}$$

$$A = \frac{V_o(j\omega)}{V_i(j\omega)} = \frac{-f/f_b}{(1+j(f/f_b))^2}$$

$$|A| = \frac{f}{f_b} \cdot \frac{1}{(\sqrt{1+(f/f_b)^2})^2}$$

$$|A| \text{ in db} = 20 \log \left(\frac{f/f_b}{(1+(f/f_b)^2)^{1/2}} \right)$$

$$\text{Put } f=f_a \Rightarrow |A| \text{ in db} = 20 \log \frac{(f_a/f_b)}{(1+(f_a/f_b)^2)^{1/2}}$$

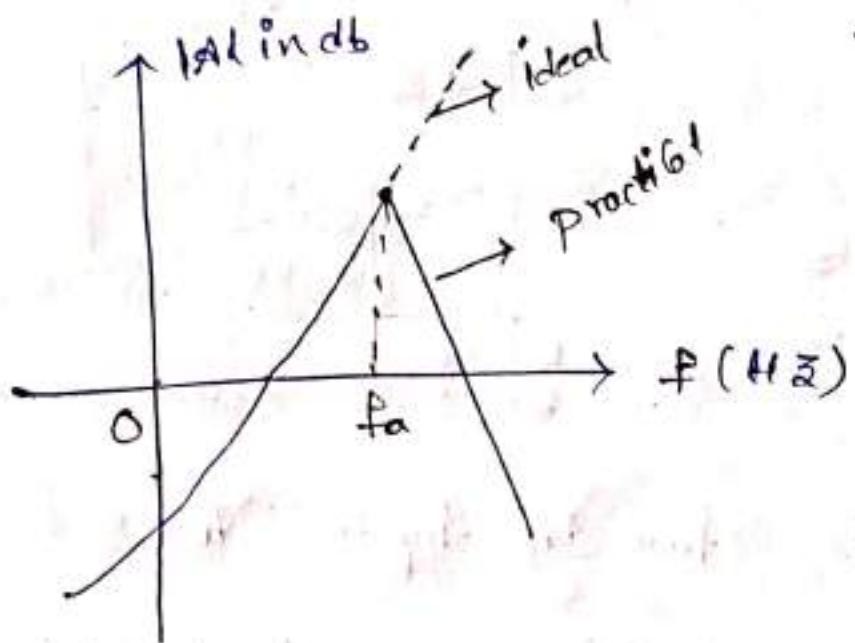
$$= 20 \log \frac{(f_a/f_b)}{\sqrt{2}}$$

$$= 20 \log 1/2 + 20 \log (f_a/f_b)$$

$$= -6.02 \text{ db} + 20 \log (f_a/f_b)$$

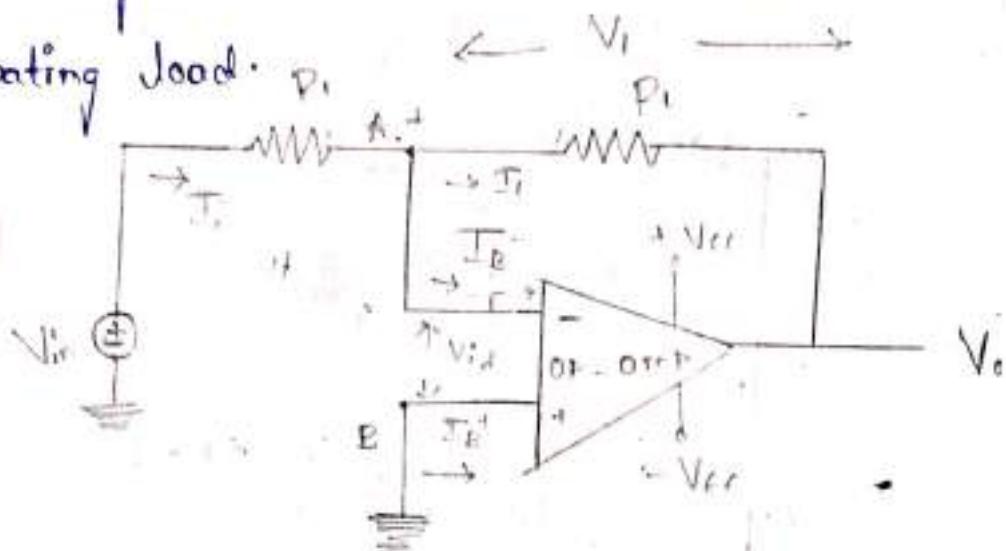
$$f = f_a \Rightarrow |A| \text{ in db} = -13.04 \text{db} + 20 \log\left(\frac{B \cdot f_a}{f_b}\right)$$

$$f = f_{a1/2} \Rightarrow |A| \text{ in db} = -1.93 \text{db} + 20 \log\left(f_a / 2f_b\right)$$



V to I Converter with floating load :-

The figure shows V to I Converter with floating load.



Analysis :- from the figure $V_B = 0$ (\because non-inverting input $i_{IP} = 0$)

According to Virtual ground Concept

$$V_A = V_B = 0$$

Apply KCL at Node 'A'

$$I_i = I_L + I_B^-$$

ideal op-amp
 $R_i = \infty$

$$I_i = I_L \quad (\because I_B^- = 0)$$

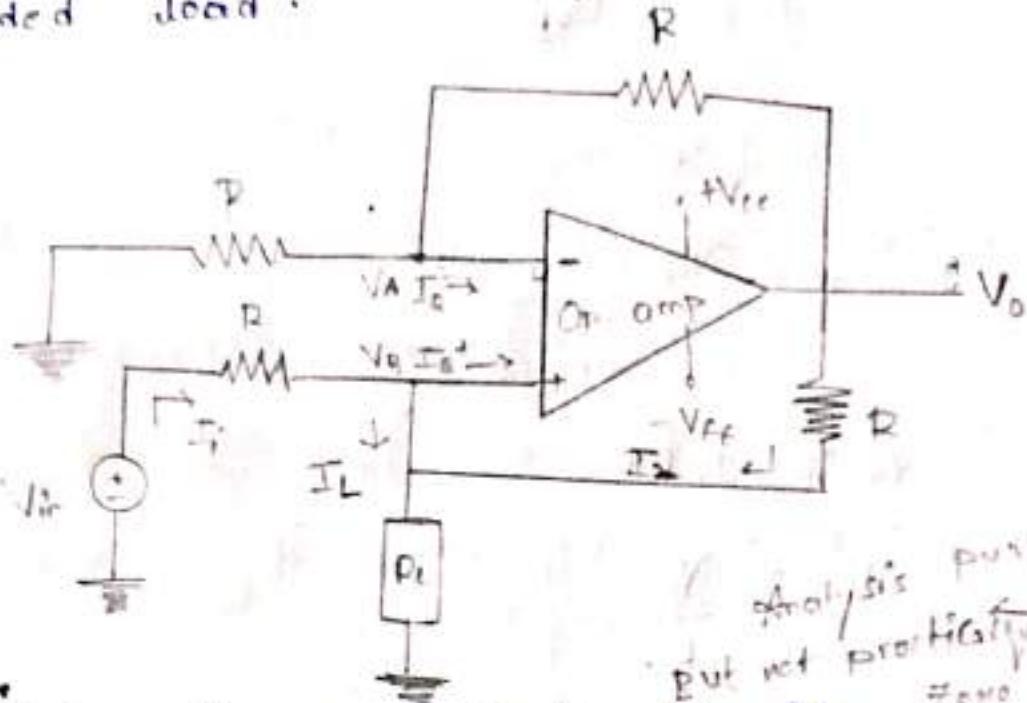
$$\frac{V_{in}}{R_i} = I_L$$

$$V_{in} = R_i I_L$$

$$I_L = \frac{V_{in}}{R_i}$$

$$I_L \propto V_{in}$$

V to I Converter with grounded load :-
The figure shows V to I Converter with grounded load.



Analysis :- from the figure $V_A = V_B$

apply KCL at Node 'B' $I_1 + I_2 = I_L + I_B$

$I_1 + I_2 = I_L \quad (\because I_B = 0)$

$$\frac{V_{in} - V_B}{R} + \frac{V_o - V_B}{R} = \frac{V_B}{R_L} I_L$$

$$\frac{V_{in} + V_o - V_B - V_B}{R} = I_L$$

$$\frac{V_{in} + V_o - 2V_B}{R} = I_L$$

$$\Delta V_B = V_{in} + V_o - R I_L$$

$$V_B = \frac{V_{in} + V_o - R I_L}{2}$$

Voltage expression for Non-inverting input terminal is given as below

$$V_o = \left(1 + \frac{R_f}{R_i}\right) V_i$$

$$= \left(1 + \frac{R}{R_i}\right) V_B$$

$$= 2 V_B$$

$$V_o = 2 \left(V_{in} + V_B - I_L R \right)$$

$$V_{in} = I_L R$$

$$I_L = \frac{V_{in}}{R}$$

I to V Converter :-

→ The Current to Voltage Converters are also called as Transresistance Amplifiers.

(Do it own)

Instrumentation Amplifiers :-

- Instrumentation Amplifiers Are used in monitoring and (Controlling) of physical parameters like :- measurement Temperature, Humidity , light Intensity , flow Control Etc. in Industries .
- For Example :- Sugar Factory requires measurement of sugar levels and temperature of juice .
- Also o Dairy plant requires precise measurement of temperature and humidity . These measurements helps the Industries in producing the quality product .
- The Measurement of physical quantities in generally carried out with the help of a device Called as Transducer .
- Transducer is a device which converts one form of energy into another form .
Ex :- Thermo Couple , $\frac{V+e}{e+m}$ Microphone , etc .
- But Most of the op's of the transducers are very low in the order of

millivolts & microvolts.

→ These voltages are not sufficient to drive the next level systems. So, we may use using Instrumentation Amplifiers.

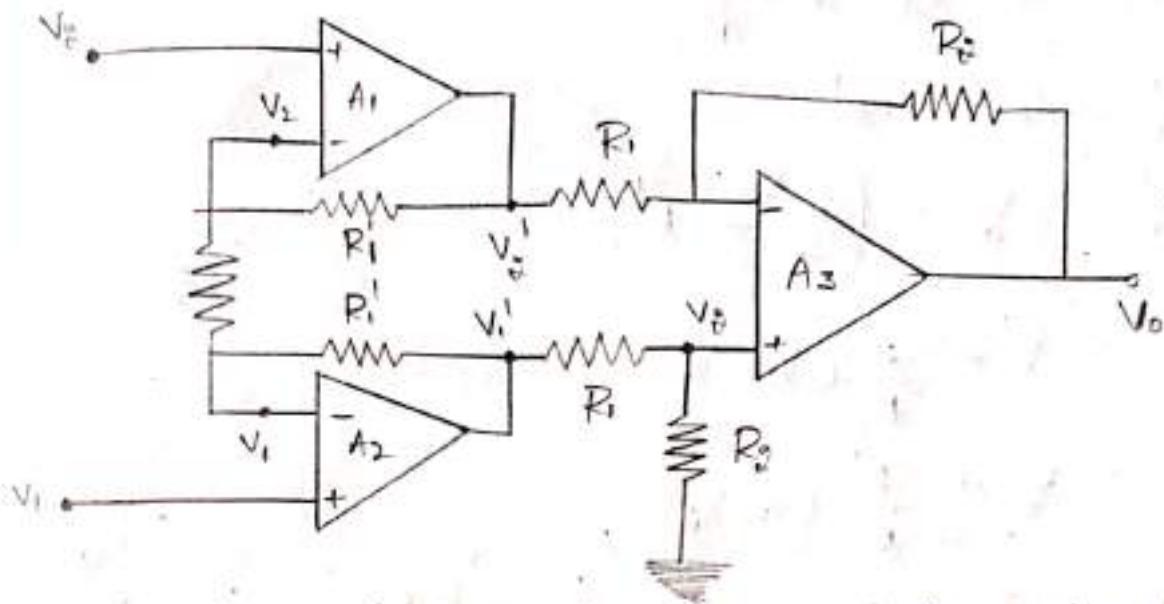
→ The Major function of instrumentation amplifiers is to precise amplification of low level o/p of the Transducers.

Features of Instrumentation Amplifiers :-

- * High CMRR
- * High gain
- * High input impedance
- * High Bandwidth
- * Low output impedance
- * High slew rate
- * Low PSRR
- * Low offset voltages, and Currents
- * Low thermal drift. (change in op-amp parameters w.r.t temperature - Thermal drift)

Three Op-amp Instrumentation Amplifiers :-

→ The figure shows 3 - Op amp instrumentation amplifier with gains A_1 , A_2 , & A_3 which uses non-inverting configuration of Op-amp.



→ Here A_1 & A_2 are Voltage followers where as A_3 is called differential amplifier.

Analysis :-

$$\text{from the figure } V_g' = V_2 + IR'$$

$$V_1' = V_1 - IR'$$

$$\text{and also } V_3 = \frac{V_1' \times R_2}{R_1 + R_2}$$

$(V_g' - V_1') > (V_2 - V_1)$ because the amplified

version of V_1 & V_2 .

Case 1 :- When $V_1 = V_2$. The net current flowing in the resistance 'IR' is zero. Then $V_g' = V_2$ & $V_1' = V_1$. Then the differential amplifier (A_3) produces zero o/p voltage.

i.e., $V_o = 0$.

Case 2 :- when $V_1 \neq V_2$ the current follows
in resistor R' so $I = \frac{V_1 - V_2}{R'}$

\Rightarrow (Now the o/p Voltage)

$$V'_1 = V_2 + IR'$$

$$V'_2 = V_2 + \left(\frac{V_1 - V_2}{R} \right) R'$$

$$V'_1 = V_1 - \frac{R'}{R} (V_1 - V_2)$$

$$V'_2 = V_2 + \frac{R'}{R} (V_1 - V_2)$$

\rightarrow Now the o/p Voltage $V_o = -\frac{R_2}{R_1} V_1 + \left(1 + \frac{R_2}{R_1} \right) V_2$

$$V_o = -\frac{R_2}{R_1} V'_1 + \left(1 + \frac{R_2}{R_1} \right) V'_2$$

$$= -\frac{R_2}{R_1} V'_1 + \left(1 + \frac{R_2}{R_1} \right) \frac{V'_1 \times R_2}{R_1 + R_2}$$

$$= -\frac{R_2}{R_1} \left(V_2 + \frac{R'}{R} (V_1 - V_2) \right) + \left(1 + \frac{R_2}{R_1} \right) \frac{V'_1 \times R_2}{R_1 + R_2}$$

$$= -\frac{R_2}{R_1} \left(V_2 + \frac{R'}{R} (V_1 - V_2) \right) + \left(1 + \frac{R_2}{R_1} \right) \frac{R_2}{R_1 + R_2} \left[V_1 - \frac{R'}{R} (V_1 - V_2) \right]$$

$$= -\frac{R_2}{R_1} \left(V_2 + \frac{R'}{R} (V_1 - V_2) - \left(V_1 - \frac{R'}{R} (V_1 - V_2) \right) \right] \quad \left(\frac{R_2 + R_1}{R_1 + R_2} \right)$$

$$= -\frac{R_2}{R_1} \left[V_2 + \frac{R'}{R} (V_1 - V_1') - V_1 + \frac{R'}{R} (V_1 - V_2) \right]$$

$$= -\frac{R_2}{R_1} \left(\frac{\partial R'}{R} (V_1 - V_2) - (V_1 - V_2) \right)$$

$$= -\frac{R_2}{R_1} (V_1 - V_2) \left(\frac{\partial R'}{R} - 1 \right)$$

$$\boxed{V_o = \frac{R_2}{R_1} \left(\frac{\partial R'}{R} + 1 \right) (V_1 - V_2)}$$

Instrumentation amplifier using Transducer bridge :-

Answer in Text book (write)

Part - 2 :- Non linear application of Op-amp

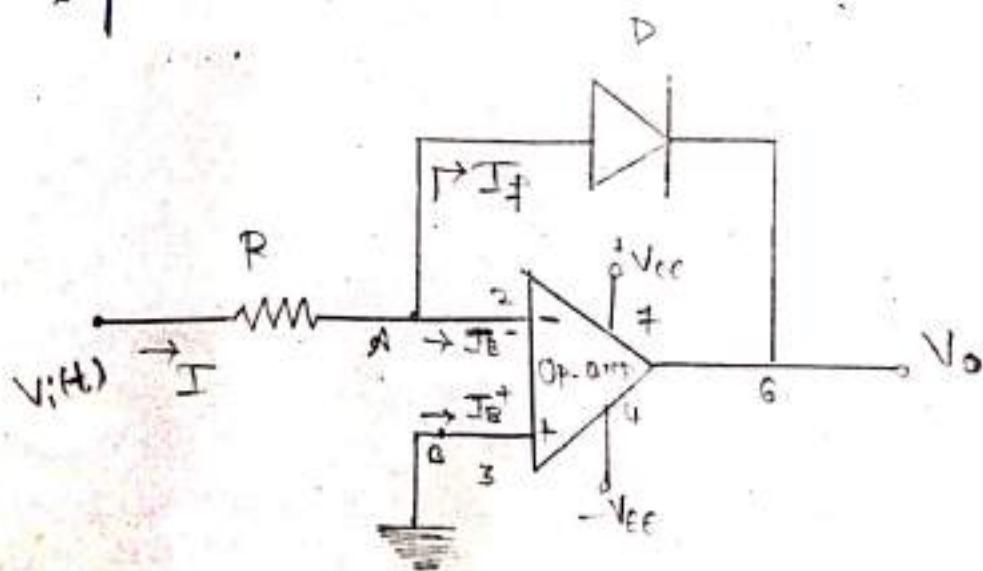
Topics :-

- * Comparators
- * Log (8) logarithmic Amplifiers
- * Anti log (8) anti-logarithmic amplifiers
- * precision rectifiers
- * Multi Vibrators
- * Schmitt Trigger.

Log (8) logarithmic Amplifier :-

→ A ckt in which whose o/p Voltage is logarithmic of i/p Voltage is called logarithmic amplifiers.

→ The fig shows Simple logarithmic Amplifier using diode (D)



Analysis is from the fig $V_A = 0$

According to Virtual ground Concept

$$V_A = V_B = 0$$

also

$$I = \frac{V_i(t) - V_A}{R}$$

$$I = \frac{V_i(t)}{R}$$

$$I_F = I_0 \left(e^{\frac{V_i(t)}{V_T}} - 1 \right)$$

Apply KCL at node 'A'

$$I = I_B^- + I_F$$

$$I = I_F \quad (\because I_B^- = 0)$$

$$\frac{V_i(t)}{R} = I_0 \left(e^{\frac{V_i(t)}{V_T}} - 1 \right) \quad V/V_T$$

$$\frac{V_i(t)}{R} = I_0 \left(e^{\frac{V_i(t)}{V_T}} \right) \quad (\because 1 < e^x)$$

$$e^{\frac{V_i(t)}{V_T}} = \frac{V_i(t)}{I_0 \cdot R}$$

Taking 'ln' on Both Sides

$$\ln \left(e^{\frac{V_i(t)}{V_T}} \right) = \ln \left(\frac{V_i(t)}{I_0 \cdot R} \right)$$

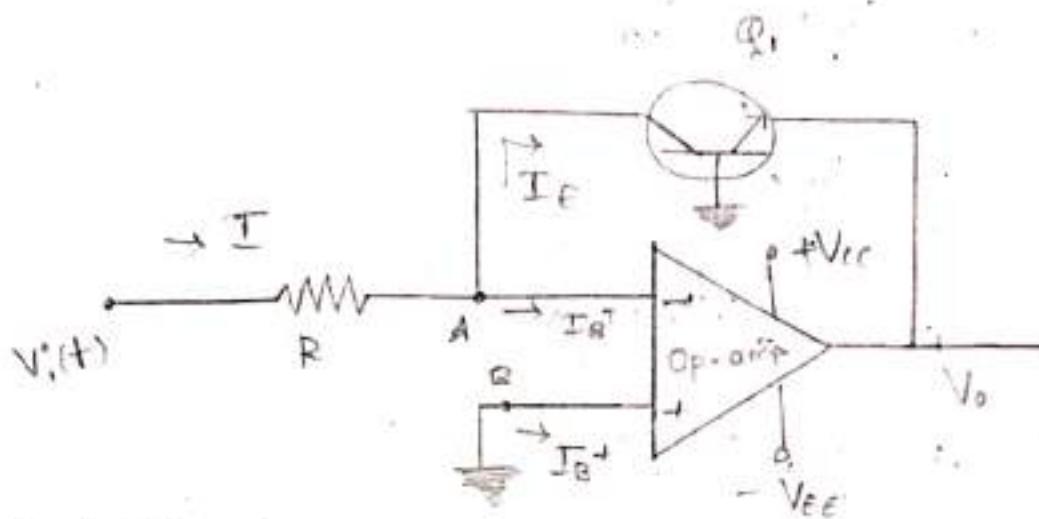
$$\frac{V_i(t)}{V_T} = \ln \left(\frac{V_i(t)}{I_0 \cdot R} \right)$$

$$\boxed{V_o = V_T \cdot \ln \left(\frac{V_i(t)}{I_0 \cdot R} \right)}$$

\therefore The o/p Voltage is logarithmic of i/p Voltage.

Logarithmic Amplifier using Transistor

→ The fig shows logarithmic amplifier using Transistor.



Analysis :-

from the fig. $V_B = 0$

According to Virtual ground Concept

$$V_A = V_B = 0$$

$$\text{also } I = \frac{V_i(t) - V_A}{R}$$

$$I = \frac{V_i(t)}{R}$$

$$I_E = I_s (e^{\frac{V_T}{V_{BE}} - 1})$$

Apply kcl at node 'A'

$$I = I_B^- + I_E$$

$$I = I_E \quad (\because I_B^- = 0)$$

$$\frac{V_i(t)}{R} = T_c \left(e^{\frac{V_o W \cdot V_T}{T_c}} \right)$$

$$\frac{V_i(t)}{R} = T_c \left(e^{\frac{V_o W \cdot V_T}{T_c}} \right) \quad (\because T_c = e^{\frac{V_o W \cdot V_T}{T_c}})$$

$$e^{\frac{V_o W \cdot V_T}{T_c}} = \frac{V_i(t)}{T_c \cdot R}$$

Taking \ln on both sides

$$\ln \left(e^{\frac{V_o W \cdot V_T}{T_c}} \right) = \ln \left(\frac{V_i(t)}{T_c \cdot R} \right)$$

$$\frac{V_o}{W \cdot V_T} = \ln \left(\frac{V_i(t)}{T_c \cdot R} \right)$$

$$V_o = W \cdot V_T \ln \left(\frac{V_i(t)}{T_c \cdot R} \right)$$

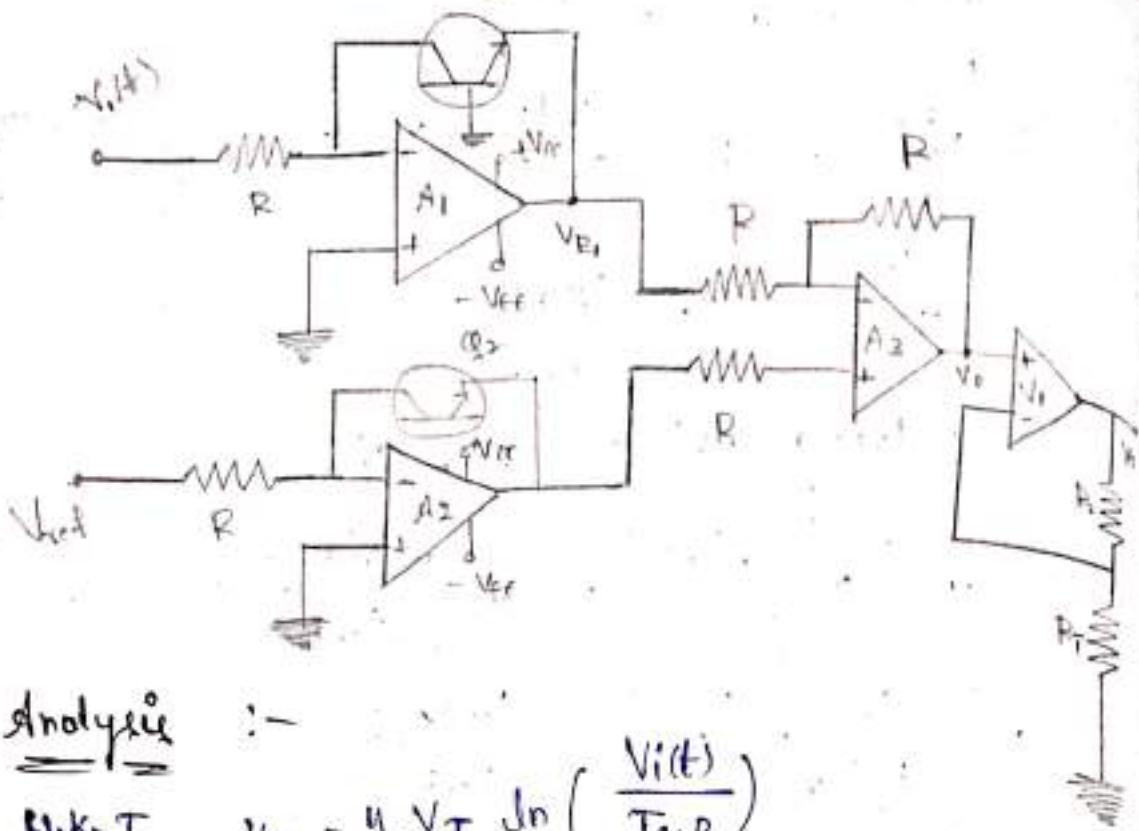
\therefore The o/p Voltage is logarithmic of i/p

Voltage.

Temperature Compensated Logarithmic amplifier:-

→ The fig shows temperature Compensated amplifier, which is constructed by using two log amplifiers, one differential amplifier of one Voltage follower.

→ If one logarithmic is applied to $V_i(t)$ of another logarithmic amplifier is applied to reference Voltage (V_{ref}).



Analysis :-

$$N \cdot k \cdot T \quad V_{o1} = \eta \cdot V_T \ln \left(\frac{V_i(t)}{I_S \cdot R} \right)$$

$$V_{o2} = \eta \cdot V_T \ln \left(\frac{V_{ref}}{I_S \cdot R} \right)$$

$$V_o = V_{o1} - V_{o2}$$

$$V_o = \eta \cdot V_T \ln \left(\frac{V_i(t)}{I_S \cdot R} \right) - \eta \cdot V_T \ln \left(\frac{V_{ref}}{I_S \cdot R} \right)$$

$$= \eta \cdot V_T \ln \left(\frac{V_i(t)}{I_S \cdot R} \times \frac{I_S \cdot R}{V_{ref}} \right)$$

$$= \eta \cdot V_T \ln \left(\frac{V_i(t)}{V_{ref}} \right)$$

$$V_{Comp} = \left(1 + \frac{R_2}{R_1} \right) V_o$$

$$V_{Comp} = \left(1 + \frac{R_2}{R_1} \right) \cdot \eta \cdot V_T \ln \left(\frac{V_i(t)}{V_{ref}} \right)$$

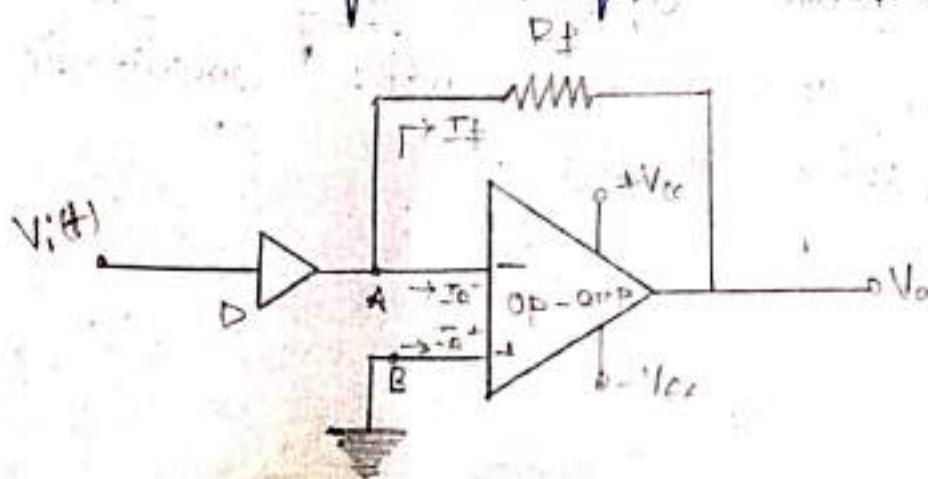
Thermistor (8) Sensor

- Here R_T is the thermistor resistance.
- whose resistance changes w.r.t. changes in temperature.
- Here the value of R_T is selected in such a way that, this will cancel the change in the value of V_T when temperature changes.

Anti-log (d) anti- logarithmic Amplifier :-

- A ckt in which whose o/p voltage is exponential of i/p voltage is called anti-exponential logarithmic amplifier.

- The fig shows basic anti-logarithmic amplifier using inverting Op-Amp.



Analysis :-

from the fig $V_B = 0$

According to Virtual ground Concept

$$V_A = V_B = 0$$

from the fig $I = I_0 (e^{\frac{V_A - V_T}{V_{TH} \cdot V_T}})$

$$I_P = \frac{V_A - V_o(t)}{R} = \frac{-V_o(t)}{R}$$

apply kcl at node 'A'

$$I = I + I_B$$

$$I = I_B \left[\because I_B = 0 \right]$$

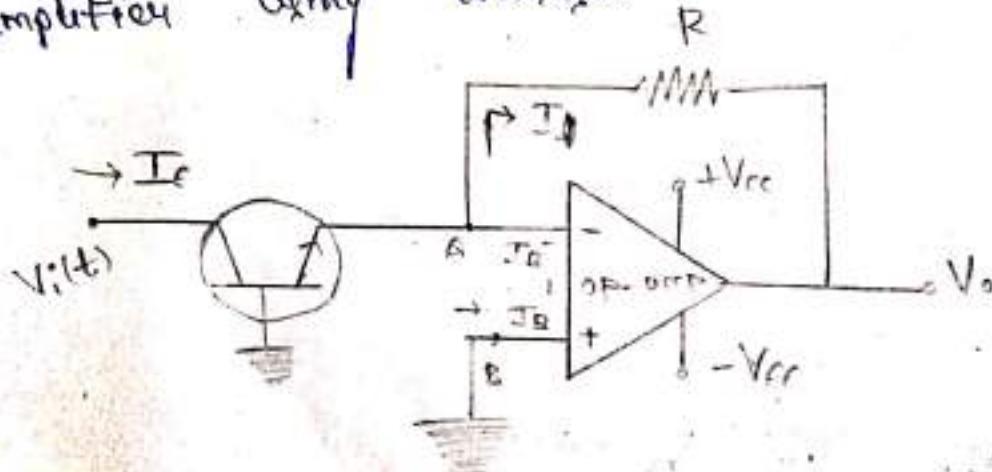
$$I_0 (e^{\frac{V_A - V_T}{V_{TH} \cdot V_T}}) = -\frac{V_o(t)}{R}$$

$$\boxed{V_o(t) = -I_0 R \cdot e^{\frac{V_i(t) - V_T}{V_{TH} \cdot V_T}}}$$

from the above expression the o/p is exponential of the i/p voltage hence it is

Called as anti-log

Anti-logarithmic amplifier using transistor:
→ The figure shows the anti-logarithmic amplifier using transistor.



Continuation

(Continued)
According to Virtual ground Concept

$$V_A = V_B = 0$$

also

$$I_e = I_s (e^{\frac{V_A - V_T}{N_v}} - 1)$$

$$f \cdot I = \frac{V_A - V_o(t)}{R}$$

$$I = -\frac{V_o(t)}{R}$$

Apply KCL at node 'A'

$$I = I_B + I_E$$

$$I = I_E \quad (\because I_B = 0)$$

$$-\frac{V_o(t)}{R} = I_E (e^{V_i(t)} | V_o, V_T)$$

$$V_o(t) = -I_E \cdot R (e^{V_i(t)} | V_o, V_T)$$

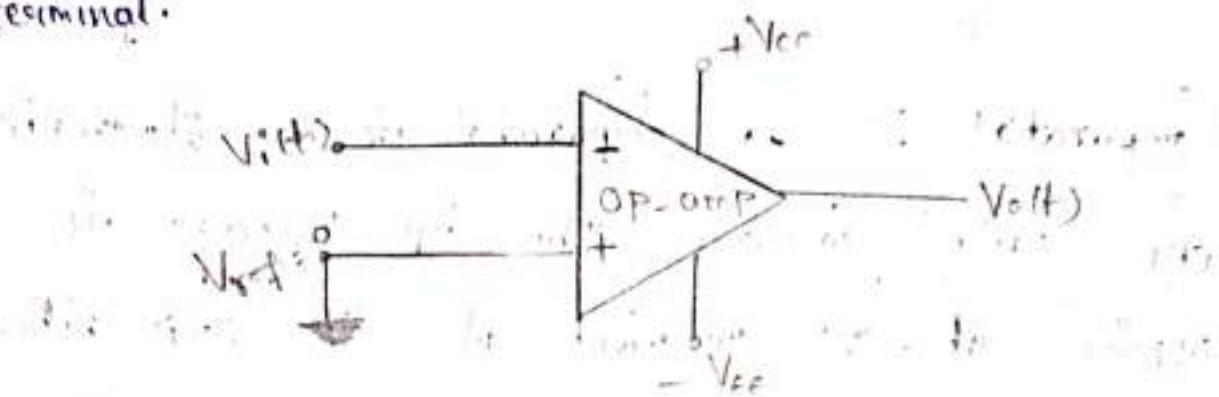
Comparat^{or} :- A Comparat^{or} is an electronic ckt which compares the ip Voltage is applied at one terminal of Op-amp with the reference Voltage is applied at another terminal of op-amp & produces an op Voltage high (H) low depending upon the ip Voltage.

- The only one application in which Open loop Configuration of Op-amp is used is Comparat^{or}.
- There are 2-types of Comparat^{or}

1. Inverting Comparat^{or}
2. Non-Inverting "

Inverting Comparator :-

→ The fig shows inverting Comparator in which the input signal is applied to inverting terminal whereas the reference voltages are applied to non-inverting terminal.



Operation :-

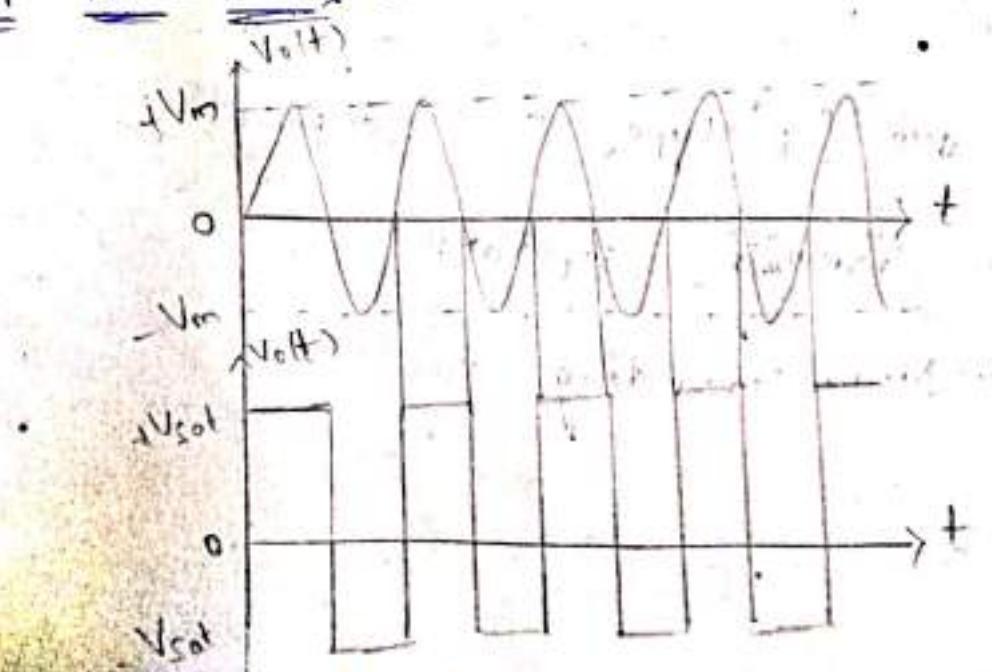
Case (i) :- When $V_i(t) > V_{ref}$ then the op-amp

voltage will be $V_o(t) = -V_{sat}$

Case (ii) :- When $V_i(t) < V_{ref}$ then the op-amp

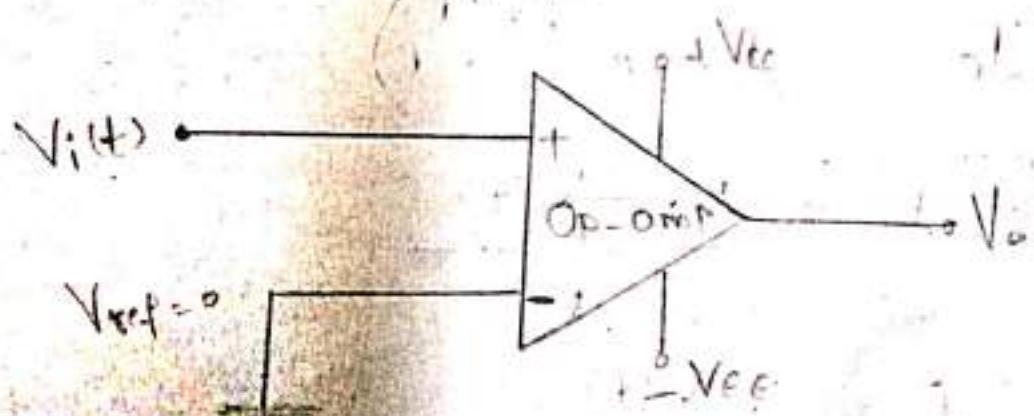
voltage will be $V_o(t) = V_{sat}$

Op-amp Wave-forms :-



2. Non-inverting Comparator :-

→ The fig shows the non-inverting Comparator in which the input signal is applied to the non-inverting terminal whereas the V_{ref} is applied to inverting terminal.

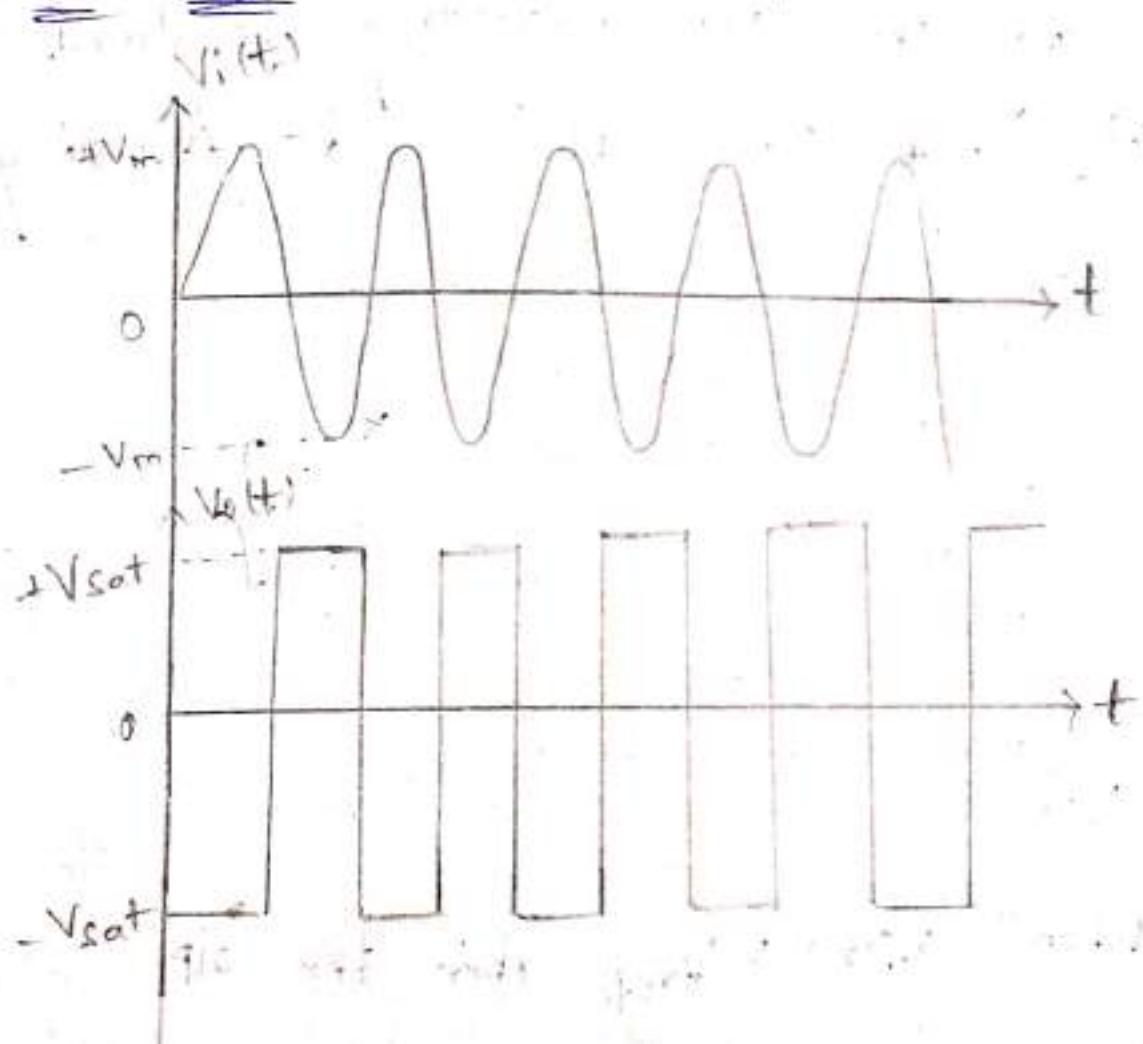


Operation :-

Case i :- When $V_i(t) > V_{ref}$ then the op
Voltage will be $V_o = +V_{sat}$

Case ii :- When the $V_i(t) < V_{ref}$ then the op
Voltage will be $V_o = -V_{sat}$

bip. voltage :- (Non-inverting)



Applications of Comparator

→ Some of the following applications are

1. Zero Crossing detector
2. Time marker generator
3. Window detector
4. Level detector

1. Zero Crossing detector :- (Inverting & Non-Inverting)

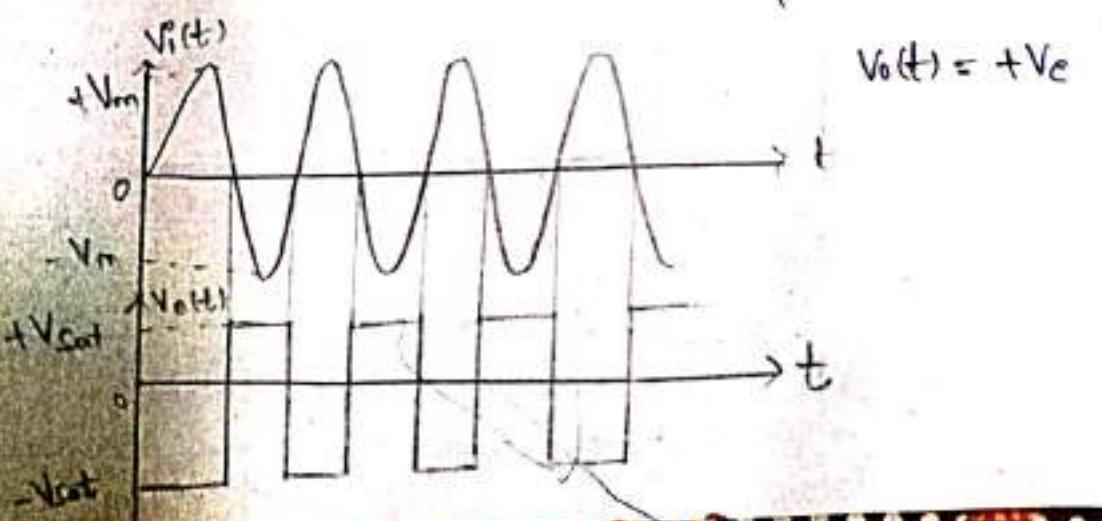
The basic Comparator can be used as Zero-Crossing detector.

→ In Zero Crossing detector, whenever the o/p Voltage crosses zero Volts then the o/p Voltage will change from one level to another level.

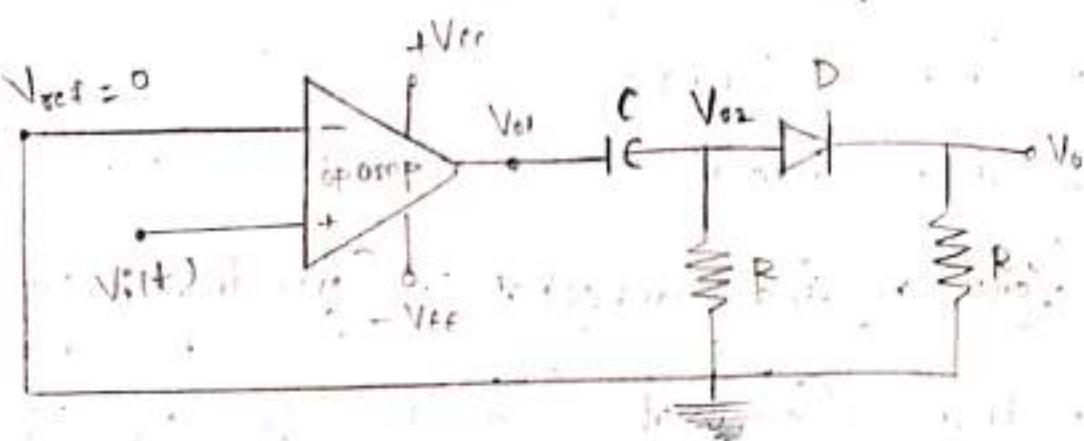
→ The figure shows the inverting Op-amp.

(i) $V_i(t) > V_{ref}$
 $V_o(t) = -V_e$

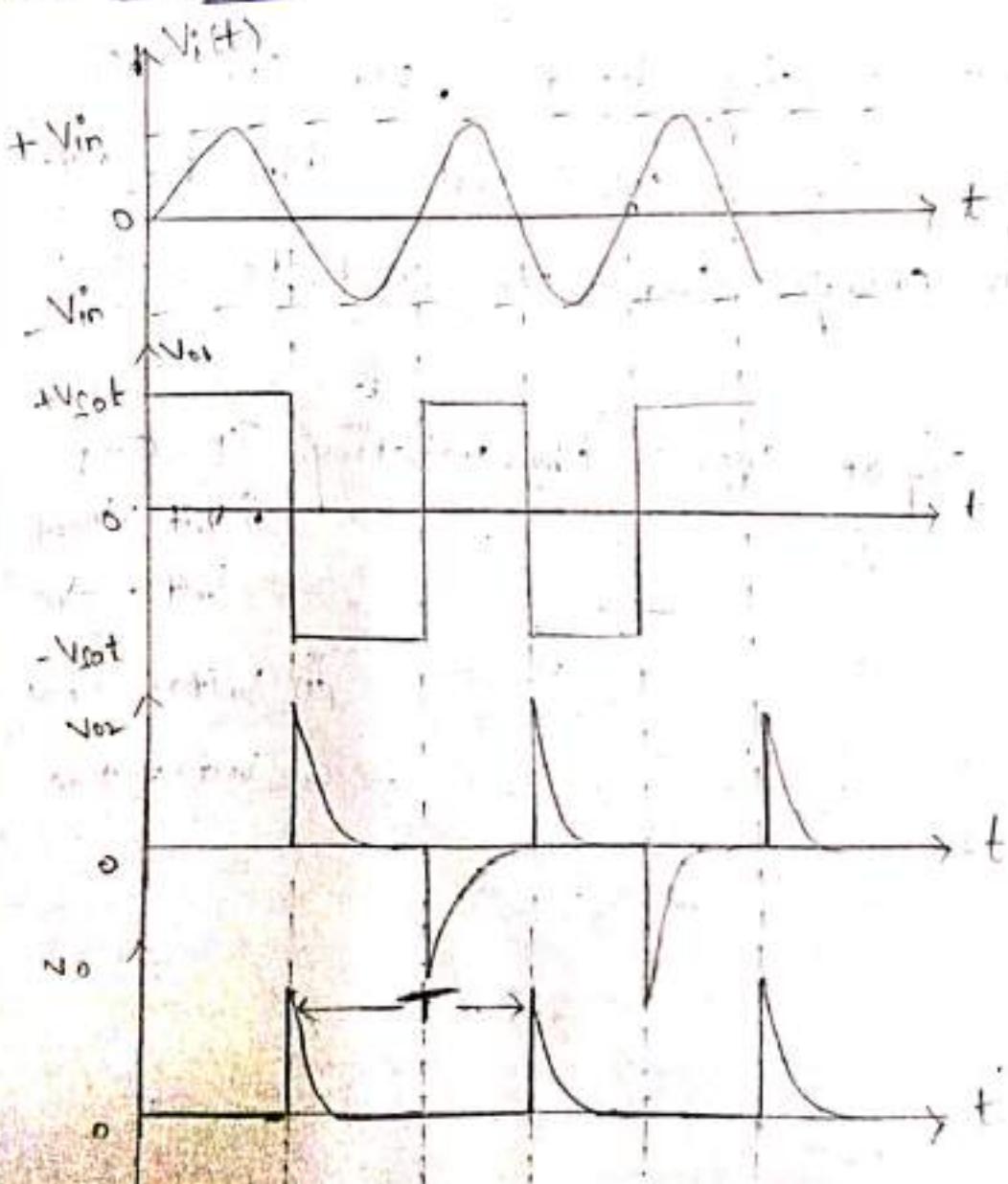
(ii) $V_i(t) < V_{ref}$
 $V_o(t) = +V_e$



Time Market generation :- The fig shows ckt diagram for time market generation. It can be obtained by connecting the RC differentiated ckt at the o/p of Zero crossing detector.



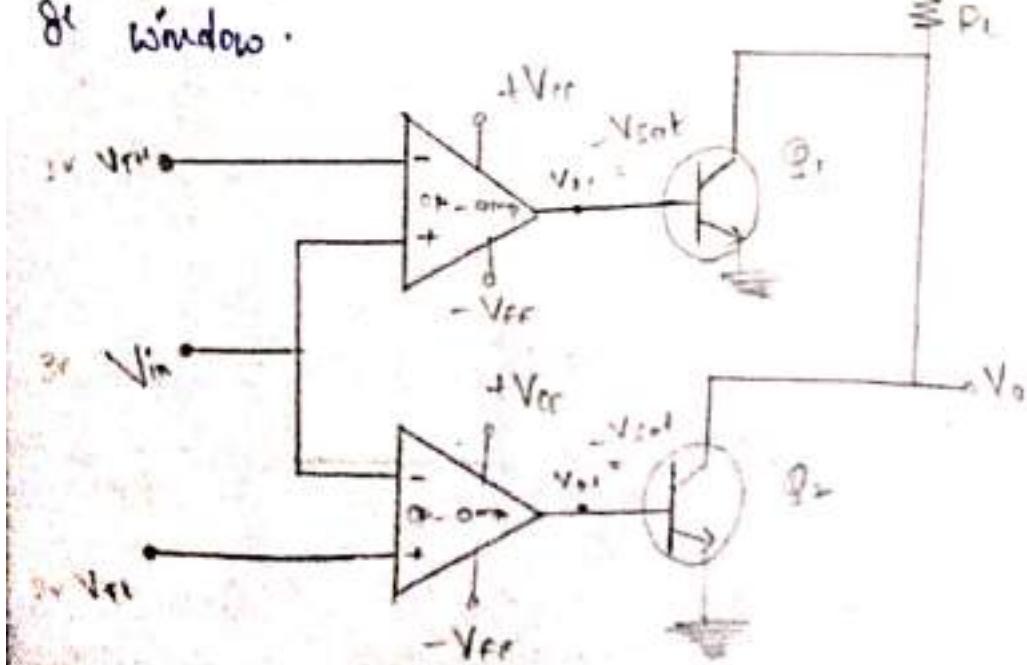
OLP wave form :-



Operation :- From the ckt the o/p V_o will be Square wave with magnitudes +V_{sat} and -V_{sat} as it is a Zero Crossing detector and also when it is applied to a differentiable ckt the o/p will be a waveform containing +ve and -ve spikes. The Diode D will filter -ve spikes and the o/p will have +ve spikes which are separated by time interval of 't'.

Window Detector :-

The fig shows window detector when a unknown Voltage falls within a Specified Voltage window.



Operation :-

Case(i) :- When input voltage is b/w

V_{RL} and V_{TH} then the both transistors are
in off.

$$\therefore V_o = +V_{cc}$$

Case(ii) :- when input Voltage $V_{in} > V_{TH}$ then
 $\varnothing_1 = \text{off}$, $\varnothing_2 = \text{on}$, then

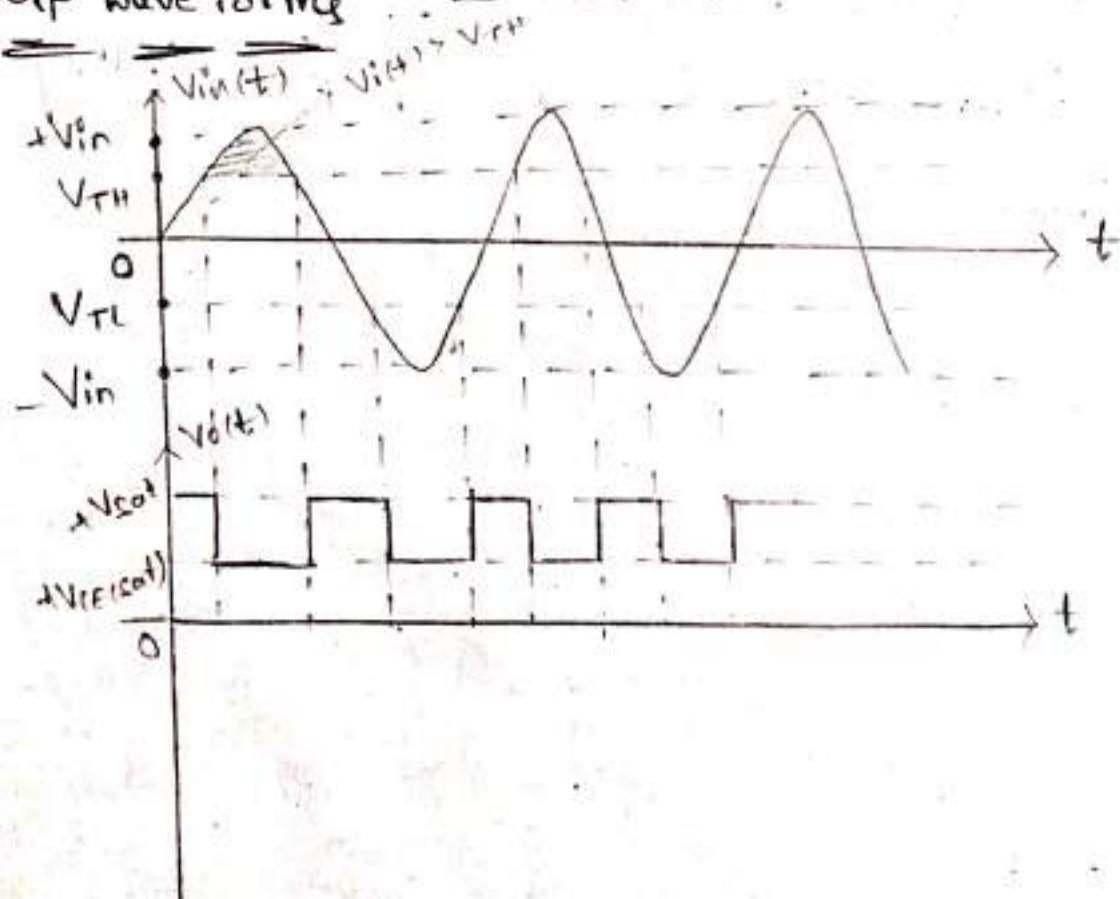
$$\therefore V_o = V_{ce(\text{sat})}$$

Case(iii) :- When input Voltage $V_{in} > V_{TH}$ then

$\varnothing_1 = \text{on}$, $\varnothing_2 = \text{off}$, then

$$\therefore V_o = V_{ce(\text{sat})}$$

O/p waveforms :-



Multi Vibrators :-

→ Multi Vibrators are regenerated ckt's which are mainly used in timing applications.

Based on their Operational characteristics, they are divided into three types.

1. A Stable Multi Vibrator

2. Mono Stable "

3. Bi Stable "

→ A stable Multivibrator are also called as free running oscillators. It has two quasi stable states and zero stable states.

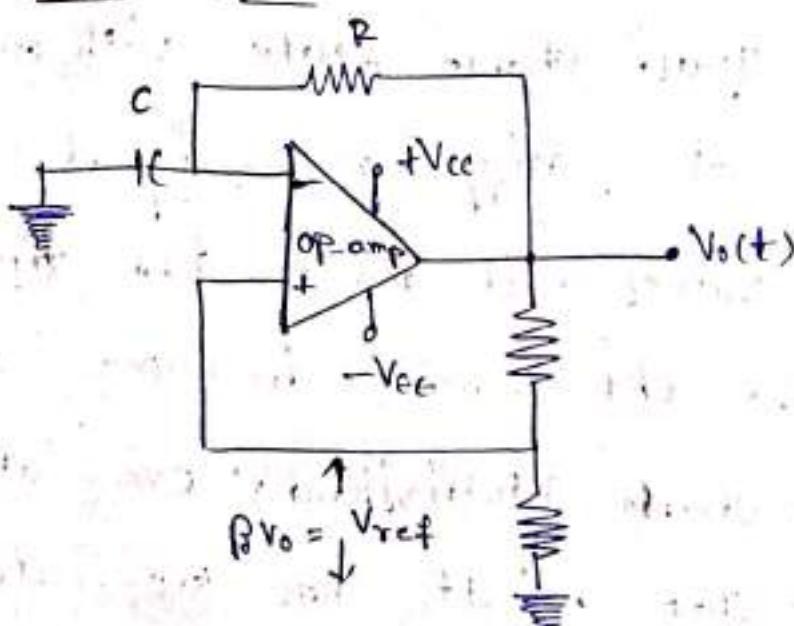
It toggles b/w one quasi stable to another quasi stable state with out any influence of triggering signal. The Component values will decide the time for which the ckt remains in one state.

→ Mono stable Multivibrators are also called as one-shot. It has one stable state and one quasi stable state. To change the state of a machine from quasi to stable state by applying

triggering signal. A suitable timing network determines time delay from quasi-stable state to stable state.

→ Bistable MultiVibrators are also called as flip flop. It has two stable states and zero quasi stable states. It requires an external triggering to change the state of the stable from one stable state to another stable state and vice versa.

Astable MultiVibrator :- (Square Wave generator)



Operation :-

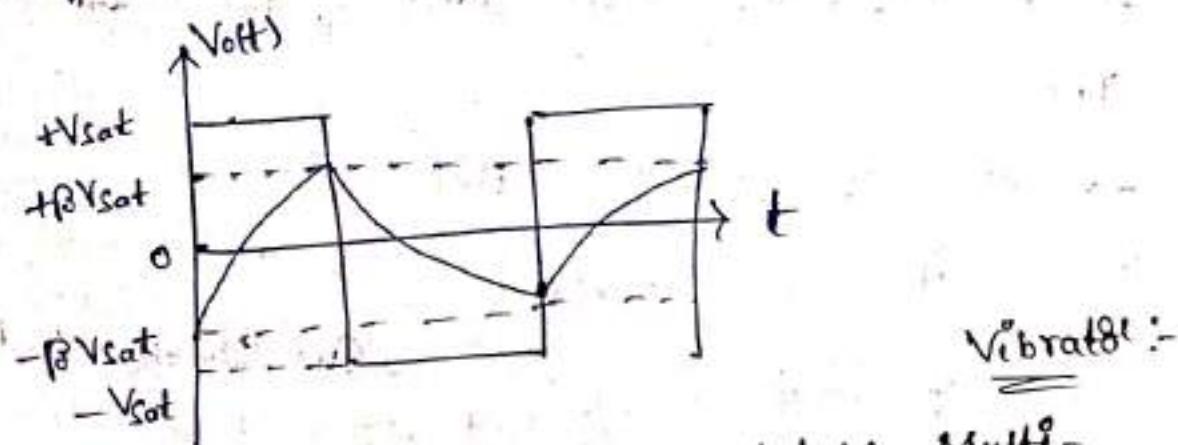
To understand the operation initially

- (i) Initially the op-amp of Op-Amp is at $+V_{sat}$. Now the Capacitor charging towards

$+V_{sat}$ for the resistor 'R' and also a fraction of o/p Voltage ($+BV_{sat}$) is fed to the non-inverting terminal. after sometime $t=t_1$, the voltage of the Capacitor is greater than $+BV_{sat}$ then the o/p Voltage changes from $+V_{sat}$ to $-V_{sat}$.

(ii) When $V(t) = -V_{sat}$, the Capacitor 'C' trying to discharge towards $-V_{sat}$ if also fraction of o/p Voltage ($-BV_{sat}$) is fed to the non-inverting i/p of Op-Amp. after some time at $t=t_1$, the voltage of the Capacitor is just less than $-BV_{sat}$ then o/p Voltage changes from $-V_{sat}$ to $+V_{sat}$

→ This process will be continue to generate the Square wave.



Expression for o/p Voltage of Astable Multi-

$$V_o = V_f + (V_i - V_f) \cdot e^{-\frac{t}{RC}}$$

Here $V_i = -BV_{sat}$ $V_f = +V_{sat}$ ($\because \tau = RC$)

at $t = T_1 \Rightarrow V_o = V_c = +\beta V_{sat}$

$$\Rightarrow +\beta V_{sat} = V_{sat} + (-\beta V_{sat} - V_{sat}) e^{-T_1/R_C}$$

$$\frac{\beta V_{sat}}{V_{sat}} = V_{sat} (1 - \beta - 1) \cdot e^{-T_1/R_C}$$

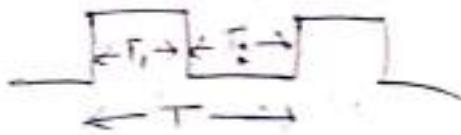
$$\therefore T = R_C \ln \left(\frac{1 + \beta}{1 - \beta} \right)$$

If $T = 2T_1$

$$= 2R_C \ln \left(\frac{1 + \beta}{1 - \beta} \right)$$

$$= 2R_C \ln \left(\frac{1 + \frac{R_2}{R_1 + R_2}}{1 - \frac{R_2}{R_1 + R_2}} \right)$$

$$T = 2R_C \ln \left(\frac{R_1 + 2R_2}{R_1} \right)$$



$$\text{if } \beta = \frac{R_2}{R_1 + R_2}$$

Monostable Multivibrator using Op-Amp :-

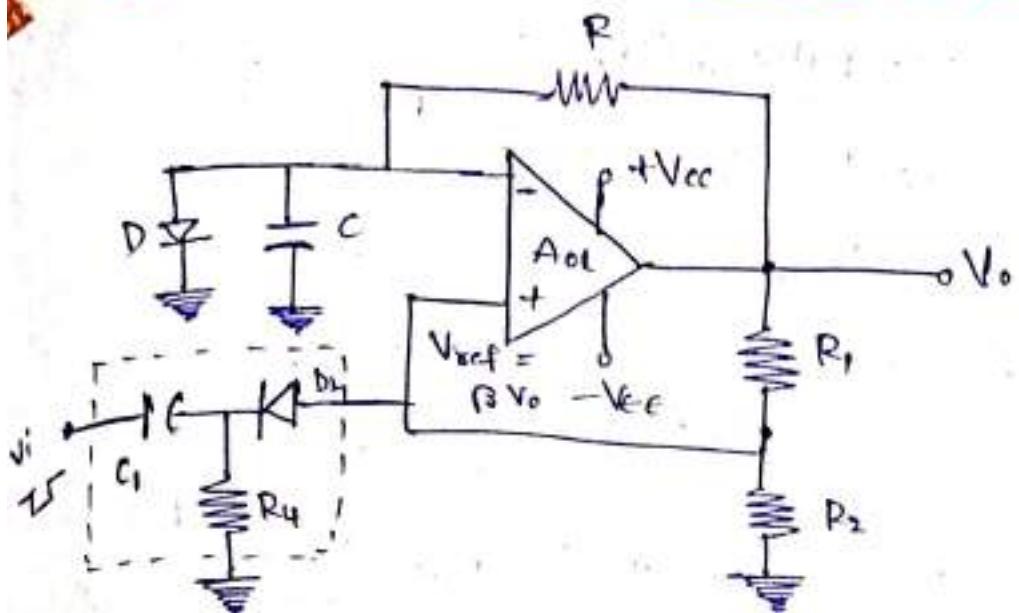
→ The fig shows monostable multivibrator using op-amp.

→ If for one stable state of one quasi stable state.

→ Let us assume that

$$\begin{aligned} &\text{if } V_o = +V_{sat} \\ &\text{if } V_{ref} = +\beta V_{sat} \end{aligned} \quad \left. \begin{array}{l} \text{One Stable State} \\ \text{Quasi Stable State} \end{array} \right\}$$

$$\begin{aligned} &\text{if } V_o = -V_{sat} \\ &\text{if } V_{ref} = -\beta V_{sat} \end{aligned} \quad \left. \begin{array}{l} \text{Quasi Stable State} \\ \text{One Stable State} \end{array} \right\}$$



Operation :-

→ Initially the monostable multivibrator is in the stable state.
 (write own)

Expression for pulse width :-

$$V_o = V_f + (V_i - V_f) \cdot e^{-t/RC} \quad \rightarrow \textcircled{1}$$

$$V_f = -V_{sat}$$

$$V_i = V_D(8) 0.7V$$

$$\text{at } t=T \Rightarrow V_o = V_c = -\beta V_{sat}$$

$$\textcircled{1} \Rightarrow -\beta V_{sat} = -V_{sat} + (V_D + V_{sat}) \cdot e^{-T/RC}$$

Then Simply we get

$$T = RC \ln \left(\frac{1 + V_D / V_{sat}}{1 - \beta} \right) \rightarrow \textcircled{1}$$

$$\text{if } R_1 = R_2 \Rightarrow \beta = \frac{R_2}{R_1 + R_2} = \frac{R}{R+R} = 0.5$$

$$V_D = 0.7V$$

$$\pm V_{sat} = \pm 15V \Rightarrow \frac{V_D}{V_{sat}} = \frac{0.7}{0.5} \ll 1$$

put Eq \textcircled{2} in Eq \textcircled{1}

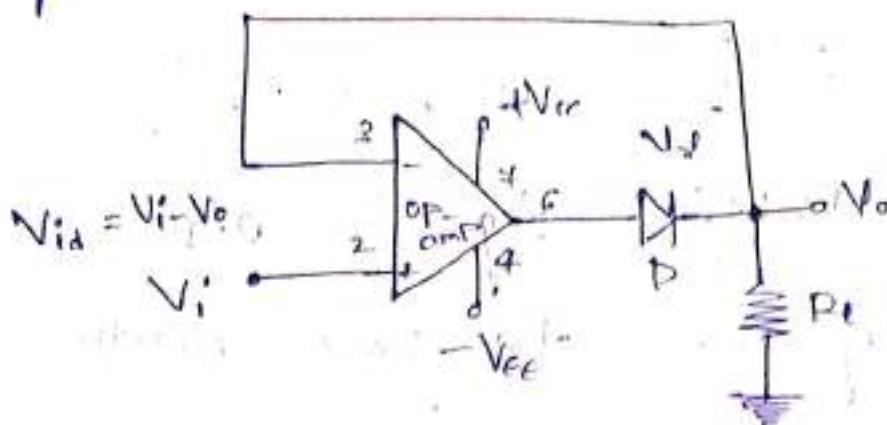
$$T = RC \ln \left(\frac{1}{1-0.5} \right)$$

$$T \approx 0.693 RC$$

Op-amp using diodes (rectification)

→ The major limitation of Ordinary diode
is that they can't rectify the voltages
below 0.7V (Cut in volt).

→ A ckt acts like ideal diode can be design by placing the diode 'D' in the feed back loop of Op-Amp as shown in figure.



Analyse :-

from the above fig

$$V_{oA} = V_{id} \cdot A_{ol}$$

$$V_{oA} = (V_i - V_o) \cdot A_{ol}$$

$$V_d + V_o = V_i A_{ol} - A_{ol} V_o$$

$$V_o(1 + A_{ol}) = V_i A_{ol} - V_d$$

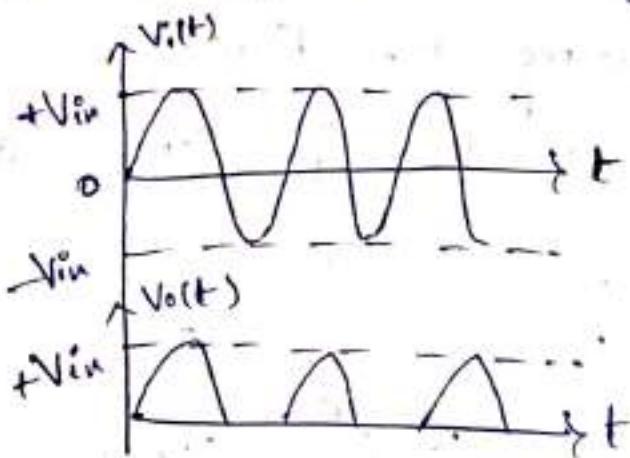
$$V_o = \frac{V_i A_{ol}}{1 + A_{ol}} - \frac{V_d}{1 + A_{ol}}$$

$$= \frac{V_i A_{ol}}{A_{ol}} - \frac{V_d}{A_{ol}}$$

$$V_o = V_i - \frac{V_d}{A_{ol}}$$

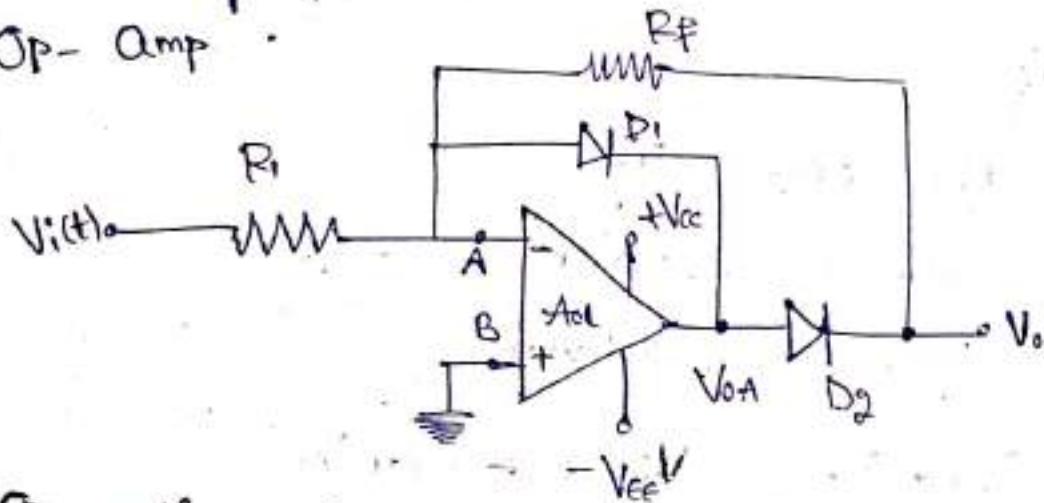
from the above expression, the cut-in-voltage of diode is divided by gain A_{ol} . hence,

the effect of V_{in} will be eliminated.



Half wave Rectifier using Op-amp :-

→ The fig shows half wave rectifier using Op-amp.



Operation :-

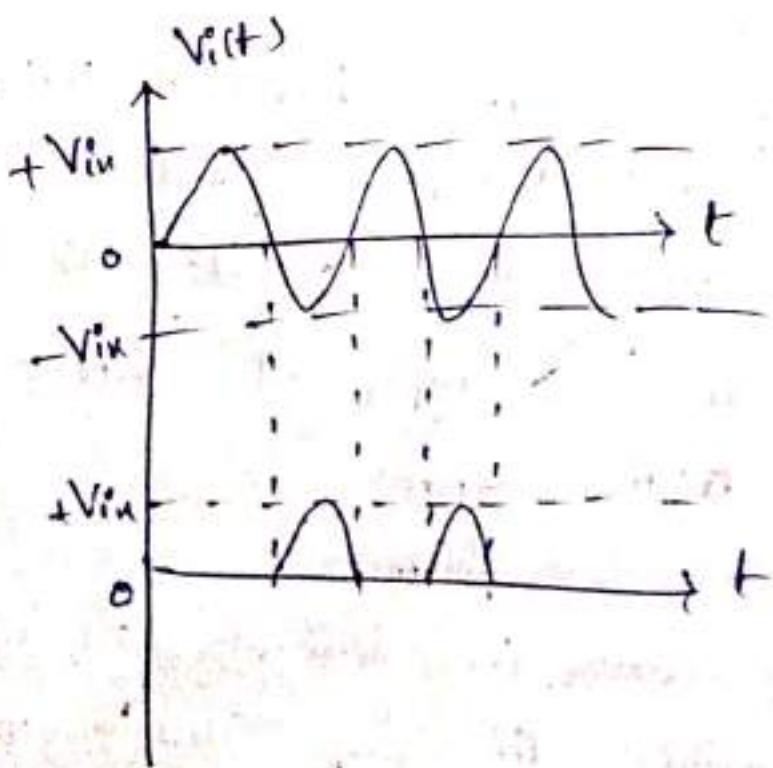
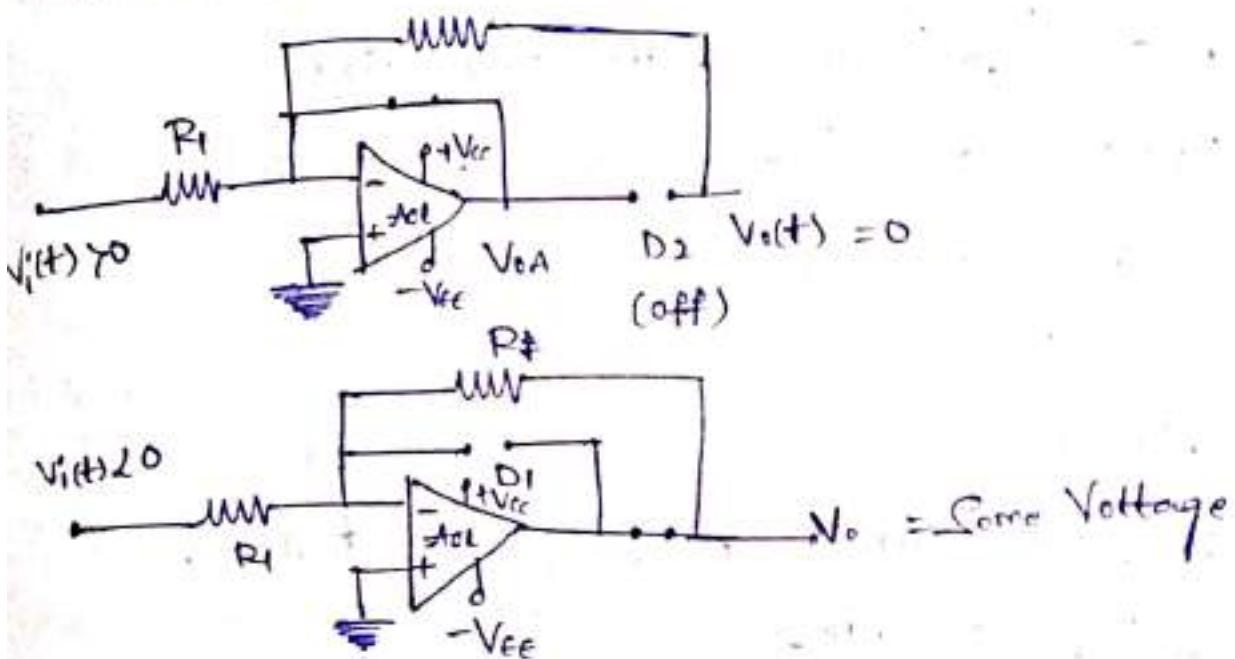
→ The half wave rectifier using OP-amp
is operated in two cases.

→ Case 1 :- $V_i(t) > 0$ & Case 2 :- $V_i(t) < 0$

Case 1 When $V_i(t) > 0$, the Diode D₁ is F.B
& Diode D₂ is R.B. BeCoz V_{OA} is -ve. Then
the op Voltage $V_o(t) = 0$

Case 2 :- when $V_i(t) < 0$, the Diode D_1 is P-B i.e., off, & Diode D_2 is F-B bcoz V_{OA} is +ve. Then the o/p voltage is present.

→ The fig shows Equivalent diagrams for Case 1 & Case 2.

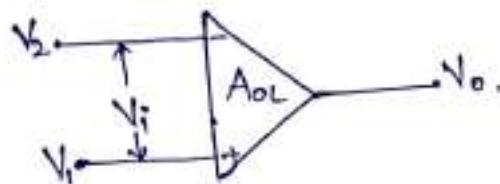


30/07/19
Tuesday.

3. Linear & Non-linear Applications of Op-Amps

open loop configurations of op-amp:

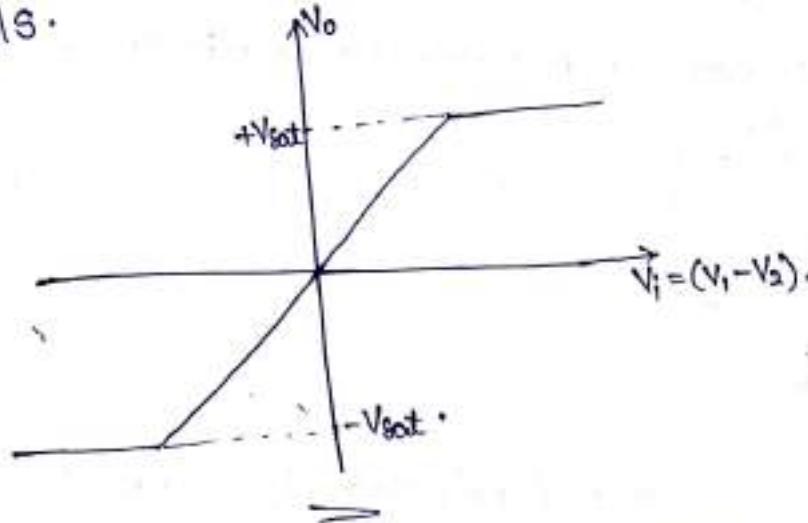
open loop Differential Amplifier (Difference Amplifier) :-



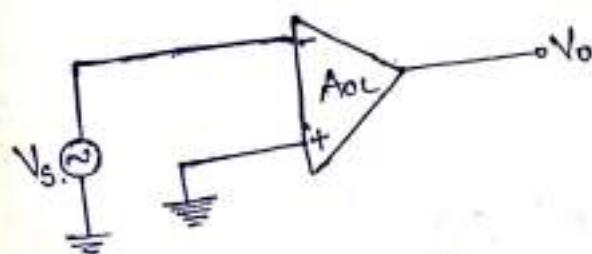
In the above circuit,

$$V_0 = A_{OL} (V_1 - V_2)$$

Op-Amp amplifies the difference between the two input signals.



Op-Amp has an open loop Inverting Amplifier :-



From the above circuit

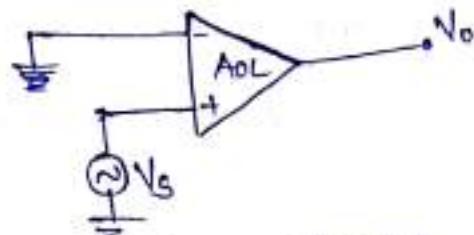
$$V_0 = A_{OL} (0 - V_s)$$

$$\therefore V_0 = -A_{OL} \cdot V_s$$

\therefore Input and output signals are 180° out of phase.

Hence this amplifier is called inverting Amplifier.

Open Loop - Non-inverting Amplifier:



From the above figure

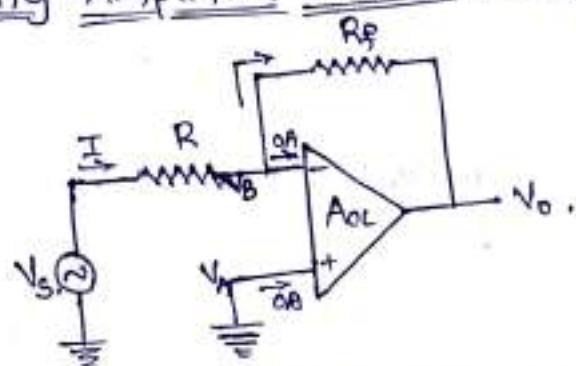
$$V_o = A_{OL} (V_s - 0)$$

$$V_o = A_{OL} \cdot V_s.$$

∴ There is no phase shift between input & output signals.
Hence this amplifier is called non-inverting amplifier.

Closed Loop Configuration of Op-Amp:-

Inverting Amplifier (Closed Loop Inverting Amplifier) :-



The above circuit is inverting Amplifier because the input signal will connect to the inverting terminal of the op-Amp.

From the circuit

$$V_A = 0$$

because of the virtual short circuit

$$V_A = V_B$$

$$\therefore V_B = 0$$

current I through R is

$$I = \frac{V_s - V_B}{R} = \frac{V_s}{R}$$

current I through R_f is

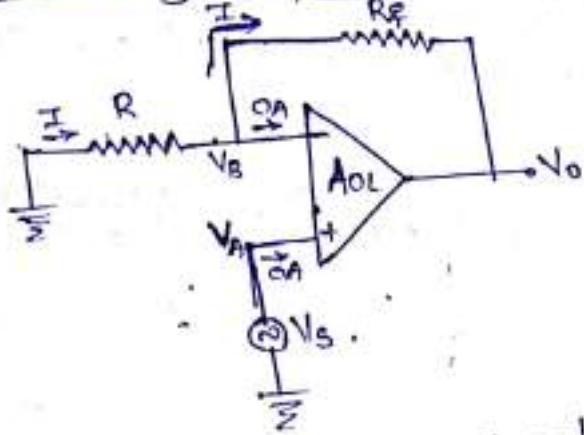
$$I = \frac{V_B - V_o}{R_f} = -\frac{V_o}{R_f}$$

$$\therefore \frac{V_s}{R} = \frac{V_o}{R_f}$$

$$\therefore \boxed{\frac{V_o}{V_s} = -\frac{R_f}{R}}$$

since voltage gain is negative, input and output signals will be out of phase.

Non-Inverting Amplifier :



In the above circuit, signal is applied to the non-inverting terminal. Hence this amplifier is called non-inverting amplifier.

From the circuit

$$V_A = V_s$$

Because of the virtual short circuit

$$V_A = V_B$$

$$\therefore V_B = V_s$$

current I through R is

$$I = \frac{0 - V_B}{R} = -\frac{V_B}{R} = -\frac{V_s}{R}$$

current I through R_f is

$$I = \frac{V_B - V_o}{R_f} = \frac{V_s - V_o}{R_f}$$

$$\therefore \frac{V_s - V_o}{R_f} = -\frac{V_s}{R}$$

$$V_s - V_o = -\frac{R_f}{R} V_s$$

$$V_s \left(1 + \frac{R_f}{R}\right) = V_o$$

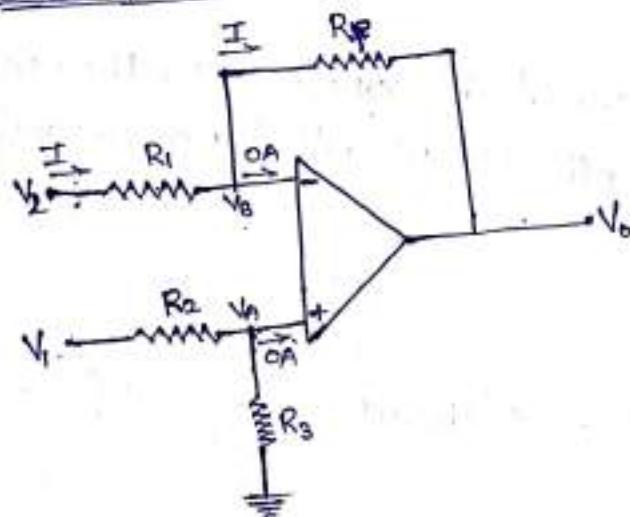
$$\boxed{\frac{V_o}{V_s} = \left(1 + \frac{R_f}{R}\right)}$$

Since the voltage gain is positive, there is no phase shift between the input & output signals.
Hence this amplifier is called as Non-inverting Amplifier.

3/10/19
Wednesday.

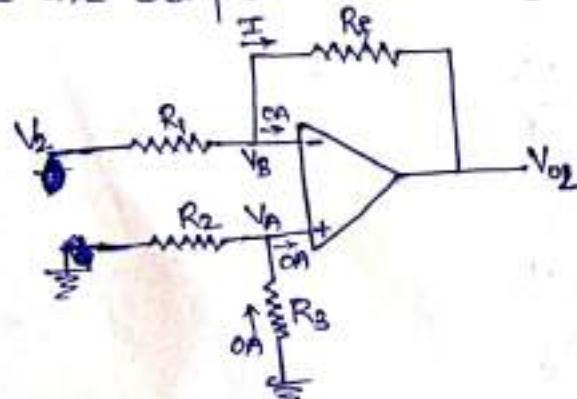
Differential Amplifier (or) Difference Amplifier (or) Subtractor (or)

Scaled Subtractor:



since OP-Amp is a linear device, we can use superposition to find V_o .

Let V_{o2} be the output when only signal V_2 is present.



$$I = \frac{V_2 - V_B}{R_1} ; \quad (\text{current } I \text{ through } R_1)$$

$$I = \frac{V_B - V_{02}}{R_F} ; \quad (\text{current } I \text{ through } R_F)$$

$$\therefore \frac{V_2 - V_B}{R_1} = \frac{V_B - V_{02}}{R_F}$$

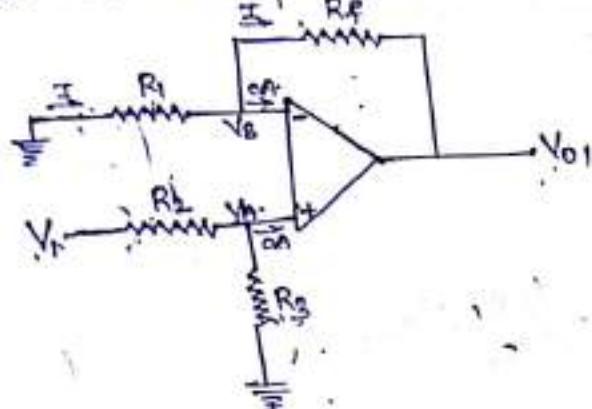
But $V_A = 0$; But $V_B = V_A$; $V_B = 0$.

$$\frac{V_2}{R_1} = \frac{-V_{02}}{R_F}$$

$$\Rightarrow \frac{V_{02}}{V_2} = -\frac{R_F}{R_1}$$

$$\boxed{V_{02} = -\frac{R_F}{R_1} \cdot V_2}.$$

Let V_{01} be the output when only signal V_1 is present.



R_2, R_3 carry the same current.

$$\therefore V_A = \frac{V_1 \cdot R_3}{R_2 + R_3}$$

$$\text{But } V_A = V_B ; \quad V_B = \frac{V_1 \cdot R_3}{R_2 + R_3}$$

current I through R_1

$$I = \frac{0 - V_B}{R_1} = -\frac{V_B}{R_1}$$

Current I through R_F

$$I = \frac{V_B - V_{01}}{R_F}$$

$$\therefore -\frac{V_B}{R_1} = \frac{V_B - V_{O1}}{R_F}$$

$$\Rightarrow \frac{V_{O1}}{R_F} = V_B \left(\frac{1}{R_F} + \frac{1}{R_1} \right)$$

$$V_{O1} = V_B \left(1 + \frac{R_F}{R_1} \right)$$

$$V_{O1} = \left(\frac{V_1 \cdot R_3}{R_2 + R_3} \right) \left(1 + \frac{R_F}{R_1} \right)$$

$$V_{O1} = \frac{V_1 \cdot R_3}{R_2 + R_3} \cdot \left(\frac{R_1 + R_F}{R_1} \right)$$

when both V_1 & V_2 are present.

$$V_o = V_{O1} + V_{O2} \quad (\text{According to superposition})$$

$$V_o = \frac{V_1 \cdot R_3}{R_2 + R_3} \left(\frac{R_1 + R_F}{R_1} \right) - \frac{R_F}{R_1} \cdot V_2$$

$$\text{If } R_F = R_3, R_1 = R_2.$$

$$V_o = \frac{V_1 \cdot R_F}{R_F + R_1} \left(\frac{R_1 + R_F}{R_1} \right) - \frac{R_F}{R_1} \cdot V_2.$$

$$V_o = \frac{V_1 \cdot R_F}{R_1} - \frac{V_2 \cdot R_F}{R_1}$$

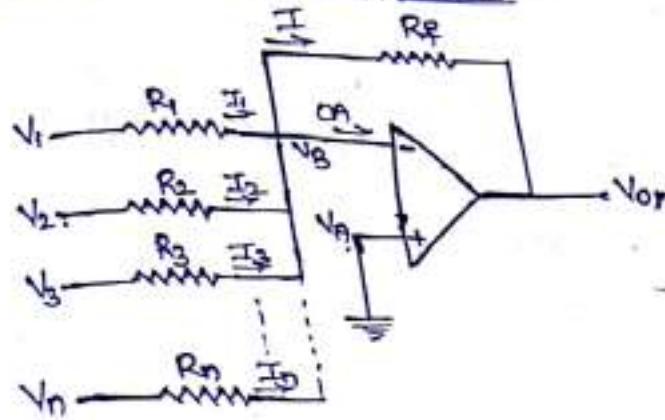
$$V_o = \frac{R_F}{R_1} (V_1 - V_2)$$

$\therefore V_o$ is proportional to the difference of the two input voltages.
Hence the circuit is called scaled differentiator or
Differential ^{Amplifier} (or) scaled subtractor.

$$\text{If } R_F = R_1$$

$$V_o = V_1 - V_2$$

Op-Amp as a Summing Amplifier (or) Adder (or) Summer (or)
 Inverting Summing Amplifier:



In the above figure -

$$\text{current } I = I_1 + I_2 + I_3 + \dots + I_n \rightarrow \textcircled{1}$$

$$V_A = 0; \text{ But } V_B = V_A;$$

$$\therefore V_B = 0$$

$$I_1 = \frac{V_1 - V_B}{R_1} = \frac{V_1}{R_1}$$

$$I_2 = \frac{V_2 - V_B}{R_2} = \frac{V_2}{R_2}$$

$$I_n = \frac{V_n - V_B}{R_n} = \frac{V_n}{R_n}$$

current through R_f is

$$I = \frac{V_B - V_o}{R_f} = \frac{-V_o}{R_f}$$

$$\textcircled{1} \Rightarrow \frac{-V_o}{R_f} = \frac{V_1}{R_1} + \frac{V_2}{R_2} + \frac{V_3}{R_3} + \dots + \frac{V_n}{R_n}$$

$$V_o = -\frac{R_f}{R_1} V_1 - \frac{R_f}{R_2} V_2 - \frac{R_f}{R_3} V_3 - \dots - \frac{R_f}{R_n} V_n.$$

$$\text{If } R_1 = R_2 = R_3 = \dots = R_n = R,$$

$$V_o = -\frac{R_f}{R} V_1 - \frac{R_f}{R} V_2 - \frac{R_f}{R} V_3 - \dots - \frac{R_f}{R} V_n$$

$$\therefore V_o = -R_f (V_1 + V_2 + V_3 + \dots + V_n)$$

\therefore The output is inverted & scaled sum of the inputs.

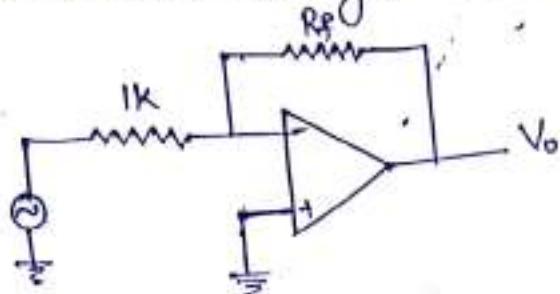
If $R_f = R$ then

$$V_o = -(V_1 + V_2 + V_3 + \dots + V_n)$$

01/08/19
Thursday.

1. Determine the feedback resistance in the following OP-Amp circuits and the gain is 60.

(i)



A. Given Gain = 60.

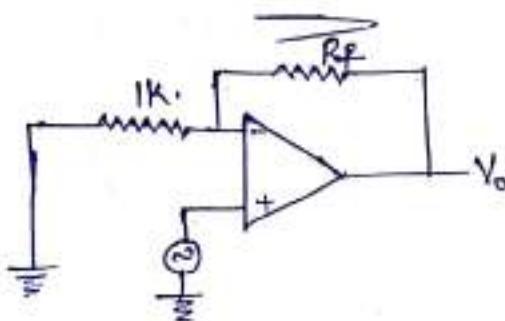
$$R = 1K$$

$$\therefore A_v = -\frac{R_f}{R} \Rightarrow |A_v| = \left| \frac{R_f}{R} \right|$$

$$60 = \frac{R_f}{1K}$$

$$\Rightarrow R_f = 60K$$

(ii)



A. $A_v = 60$

$$A_v = 1 + \frac{R_f}{R}$$

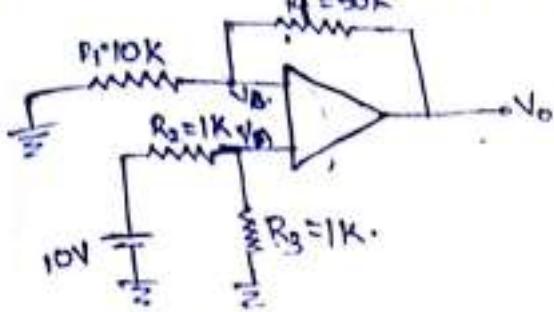
$$60 = 1 + \frac{R_f}{1K}$$

$$59 = \frac{R_f}{1K}$$

$$R_f = 59K$$



(i) Find V_o in the following circuit.



Given $R_1 = 10\text{K}$, $R_2 = 1\text{k}$, $R_3 = 1\text{k}$, $R_f = 50\text{K}$.

$$\text{w.r.t. } V_o = \frac{V_B \cdot R_3}{R_2 + R_3} \left(\frac{R_1 + R_f}{R_1} \right)$$

$$V_o = \frac{10 \times 1\text{k}}{1\text{k} + 1\text{k}} \left(\frac{10\text{k} + 50\text{k}}{10\text{k}} \right)$$

$$= 5(6)$$

$$V_o = 30\text{V}$$

(ii)

$$V_B = \frac{10 \times 1\text{k}}{1\text{k} + 1\text{k}} = 5\text{V}$$

$$\therefore V_B = V_A ; V_B = 5\text{V}$$

$$I = \frac{0 - V_B}{10\text{k}} \doteq \frac{V_B - V_o}{50\text{k}}$$

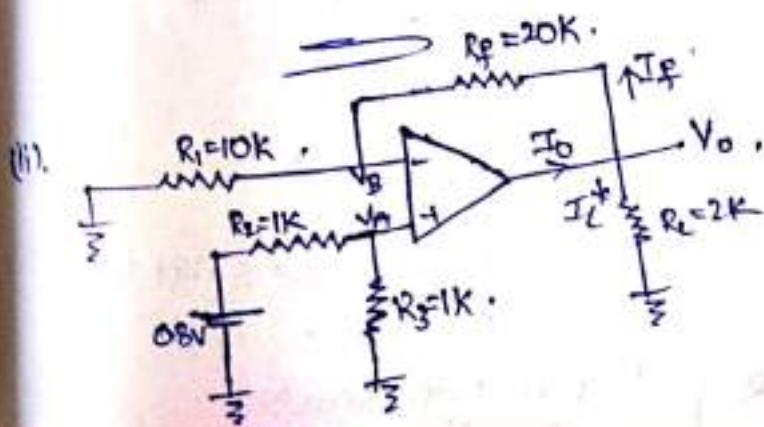
$$-\frac{V_B}{10\text{k}} = \frac{V_B - V_o}{50\text{k}}$$

$$-\frac{5}{10\text{k}} = \frac{5 - V_o}{50\text{k}}$$

$$\frac{2}{50\text{k}} = 5 - V_o$$

$$V_o = 30\text{V}$$

Determine I_f , I_L ?



$$V_A = \frac{0.8 \times 1K}{1K + 1K} = \frac{0.8K}{2K} = 0.4V$$

$$V_B = V_A \therefore V_B = 0.4V$$

$$I = \frac{0 - V_B}{10K} = \frac{-0.4}{10K}$$

$$I = \frac{V_B - V_o}{20K} = \frac{0.4 - V_o}{20K}$$

$$\frac{-0.4}{10K} = \frac{0.4 - V_o}{20K}$$

$$\frac{-0.4 \times 20}{10K} = 0.4 - V_o$$

$$V_o = 1.2V$$

$$I_f = -I$$

$$= -\left(\frac{0 - V_B}{10K}\right)$$

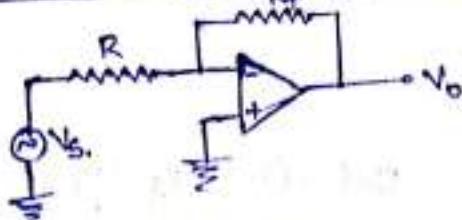
$$I_f = \frac{0.4}{10K} = \frac{0.4}{10K} = 0.04mA$$

$$I_L = \frac{V_o}{R_L} = \frac{1.2}{2K} = 0.6mA$$

$$I_o = I_L + I_f \\ = (0.04 + 0.6)mA \\ = 0.64mA$$

Comparison between Inverting & Non-inverting Amplifier

Inverting

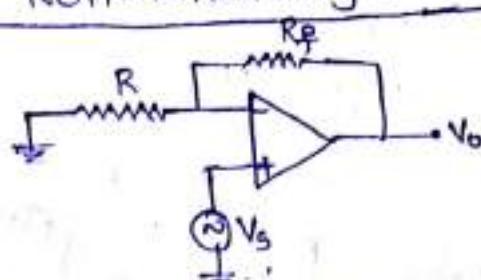


2) Gain $\frac{V_o}{V_s} = -\frac{R_f}{R}$

3) 180° phase shift between Input & Output.

4) Input impedance $R_i = \frac{V_s}{I} = R$

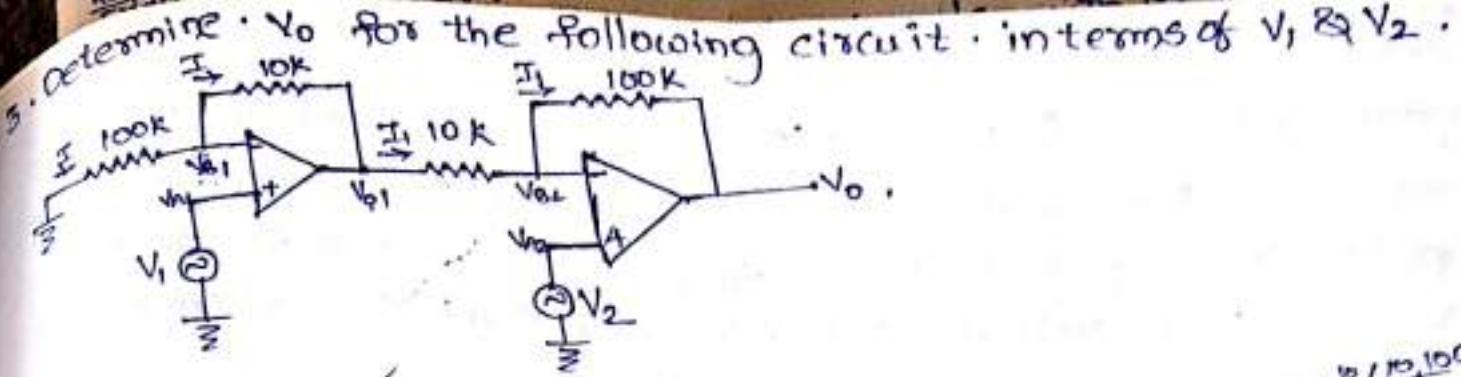
Non-Inverting



2) Gain $\frac{V_o}{V_s} = (1 + \frac{R_f}{R})$

3) There is no phase shift between Input & Output.

4) Input impedance $R_i = \frac{V_s}{I} = \infty$



$$I = \frac{0 - V_{B1}}{100K} = -\frac{V_{B1}}{100K}$$

$$I = \frac{V_{B1} - V_{o1}}{10K}$$

$$\therefore -\frac{V_{B1}}{100K} = \frac{V_{B1} - V_{o1}}{10K}$$

$$\frac{V_{o1}}{10K} = \frac{V_{B1}}{10K} + \frac{V_{B1}}{100K}$$

$$\frac{V_{o1}}{10K} = \frac{V_{B1} + 10V_{B1}}{100K}$$

$$V_{o1} = \frac{11V_{B1}}{10}$$

$$(V_{A1} = V_{B1}) \quad V_{A1} = V_1$$

$$V_{o1} = \frac{11V_1}{10}$$

$$I_1 = \frac{V_{o1} - V_{B2}}{10K}$$

$$(V_{A2} = V_{B2}) \quad V_B$$

$$V_{A2} = V_2$$

$$\therefore V_{B2} = V_2$$

$$= \frac{\frac{11V_1}{10} - V_2}{10K}$$

$$= \frac{11V_1 - 10V_2}{100K}$$

$$I_1 = \frac{V_{B2} - V_o}{100K} = \frac{V_2 - V_o}{100K}$$

$$\frac{11V_1 - 10V_2}{100K} = \frac{V_2 - V_o}{100K}$$

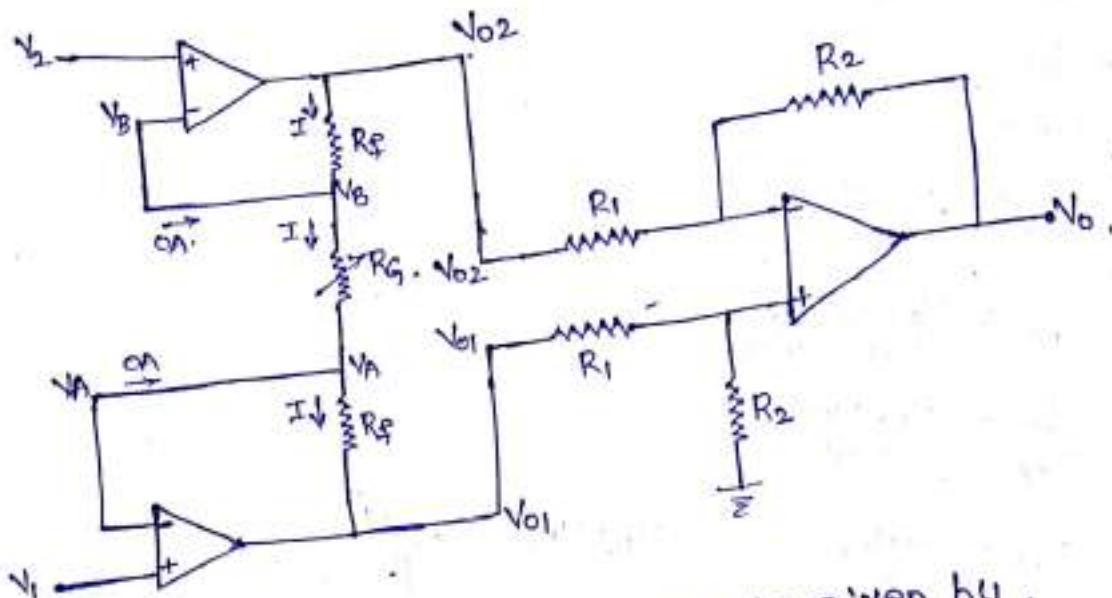
$$11V_1 - 10V_2 = V_2 - V_o$$

$$V_o = 11V_2 - 11V_1$$

$$\boxed{V_o = 11(V_2 - V_1)}$$

30/8/19
Tuesday

Instrumentation Amplifier: (8) 3-opamp Instrumentation Amplifier
Instrumentation amplifiers are used to measure very sensitive signals coming from Transducers. These signals are of very low level voltage signals which need to be amplified with high accuracy and high gain.



The output voltage of the second stage is given by.

$$V_O = \frac{R_2}{R_1} (V_{O1} - V_{O2})$$

Because of virtual short circuit

$$V_A = V_B, V_1 = V_2$$

From the circuit

$$I = \frac{V_{O2} - V_{O1}}{R_F + R_G + R_F} = \frac{V_{O2} - V_{O1}}{R_G + 2R_F}$$

$$I = \frac{V_B - V_A}{R_G} = \frac{V_2 - V_1}{R_G}$$

$$\therefore \frac{V_{O2} - V_{O1}}{2R_F + R_G} = \frac{V_2 - V_1}{R_G}$$

$$\Rightarrow V_{O2} - V_{O1} = \left(\frac{2R_F + R_G}{R_G} \right) (V_2 - V_1)$$

$$V_{O2} - V_{O1} = \left(\frac{2R_F + R_G}{R_G} \right) (V_2 - V_1)$$

$$V_{O1} - V_{O2} = \frac{2R_F + R_G}{R_G} (V_1 - V_2)$$

$$V_o = \frac{R_2}{R_1} \left(1 + \frac{2R_F}{R_G} \right) (V_1 - V_2)$$

If $R_1 = R_2$

$$V_o = \left(1 + \frac{2R_F}{R_G} \right) (V_1 - V_2)$$

Advantages :-

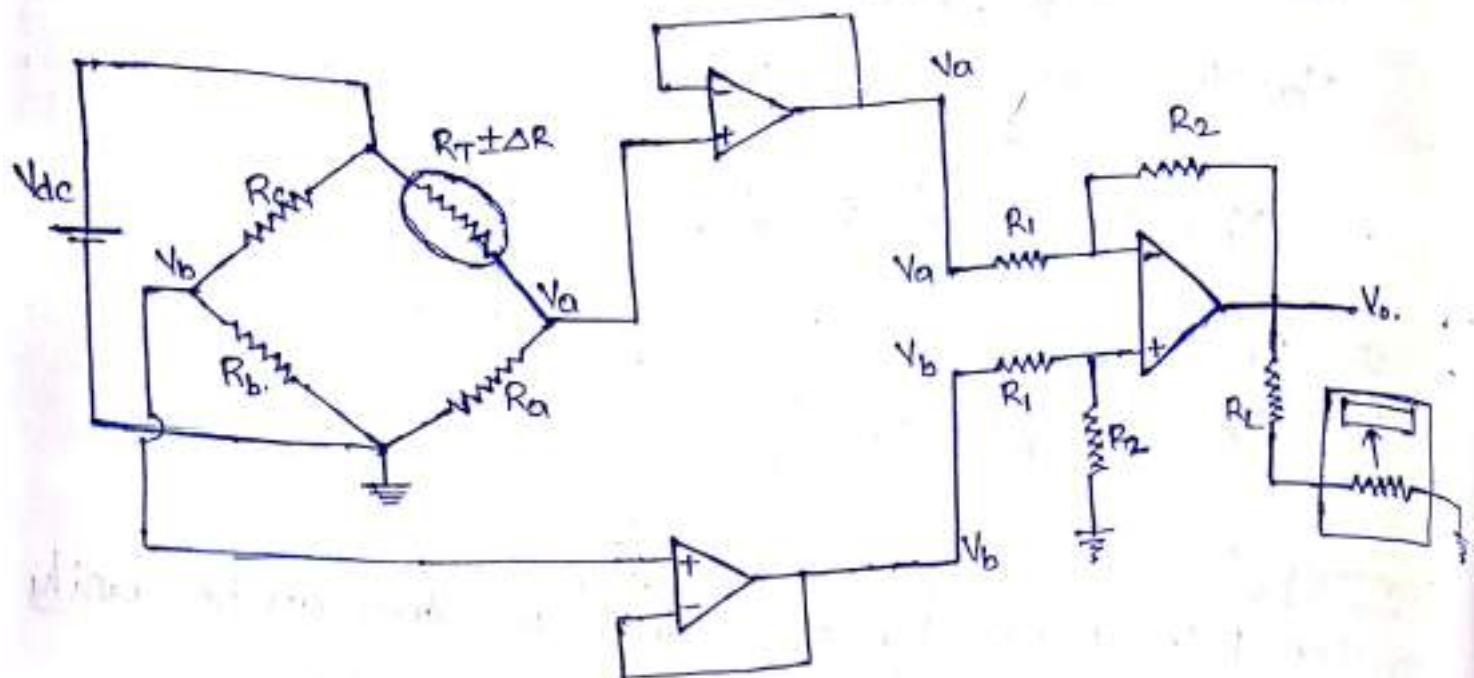
- * with the help of variable resistance R_G gain can be easily adjusted.
- * since gain depends upon the ratio of resistors, accuracy will be more.
- * Both input signals V_1, V_2 are connected to non-inverting terminals of op-Amp which provide high input impedance. ∴ the smallest signals can be picked up by the amplifier.
- * the input to the second stage is coming from the output of op-Amp from the first stage. ∵ the opamp output impedance is very low.
- * the opamp output impedance is very low.
- ∴ the first stage will not load the second stage.
- ∴ First stage will not load the second stage, common mode gain since op-Amps are used in both the stages, common mode gain signals are suppressed.

Alia
Wednesday.

Transducer bridge Instrumentation Amplifier:

The below figure shows a Transducer bridge instrumentation Amplifier.

Let the bridge is balanced at reference temperature.



Let \$R_T\$ be the resistance of the thermistor at the reference temperature.

At the bridge is

∴ At reference temperature

$$V_a = V_b$$

From the figure

$$V_a = \frac{V_{dc} \cdot R_a}{R_a + R_T}$$

$$V_b = \frac{V_{dc} \cdot R_b}{R_b + R_c}$$

$$\therefore \frac{V_{dc} \cdot R_a}{R_a + R_T} = \frac{V_{dc} \cdot R_b}{R_b + R_c}$$

$$\frac{R_a + R_T}{R_a} = \frac{R_b + R_c}{R_b}$$

$$1 + \frac{R_T}{R_a} = 1 + \frac{R_c}{R_b}$$

$$\boxed{\frac{R_T}{R_a} = \frac{R_c}{R_b}}$$

when temperature changes R_T changes by $\pm \Delta R$

$$V_a = \frac{V_{dc} \cdot R_a}{R_a + R_T + \Delta R}$$

$$V_b = \frac{V_{dc} \cdot R_b}{R_b + R_c}$$

output voltage V_o of the differential amplifier is given

by $V_o = \frac{R_2}{R_1} (V_b - V_a)$

$$V_o = \frac{R_2}{R_1} \left[\frac{V_{dc} \cdot R_b}{R_b + R_c} - \frac{V_{dc} \cdot R_a}{R_a + R_T + \Delta R} \right]$$

Let $R_a = R_b = R_c = R_T = R$

$$V_o = \frac{R_2}{R_1} \left[\frac{V_{dc} \cdot R}{2R} - \frac{V_{dc} \cdot R}{2R \pm \Delta R} \right]$$

$$V_o = V_{dc} \cdot \frac{R_2}{R_1} \left[\frac{1}{2} - \frac{1}{2R \pm \Delta R} \right]$$

$$V_o = V_{dc} \cdot \frac{R_2}{R_1} \left(\frac{2R \pm \Delta R - 2R}{2(2R \pm \Delta R)} \right)$$

$$V_o = V_{dc} \cdot \frac{R_2}{R_1} \left(\frac{\pm \Delta R}{2(2R)} \right) \quad (\because \Delta R \ll 2R)$$

$$V_o = V_{dc} \cdot \frac{R_2}{R_1} \left(\frac{\pm \Delta R}{4R} \right)$$

$$\therefore V_o \propto \Delta R$$

ΔR depends upon change in temperature ΔT .

$\therefore V_o$ is proportional to change in temperature. Hence the above circuit can be used to calibrate a temperature measuring device.



Op-Amp as an integrator:

Ideal Integrator:

The above figure represents an ideal integrator.

$$V_A = 0 \text{ &}$$

$$V_B = V_A \Rightarrow V_B = 0$$

current through the resistor

$$i = \frac{V_i - V_B}{R} = \frac{V_i - 0}{R} = \frac{V_i}{R} \rightarrow ①$$

current through the capacitor

$$i = C \cdot \frac{dV_C}{dt}$$

$$i = C \cdot \frac{d}{dt} (V_B - V_o) \rightarrow ②$$

$$\text{from } ① \text{ & } ② \Rightarrow \frac{V_i}{R} = C \cdot \frac{d}{dt} (V_B - V_o)$$

$$\frac{V_i}{R} = -C \cdot \frac{d}{dt} V_o$$

$$\frac{dV_o}{dt} = -\frac{1}{RC} V_i$$

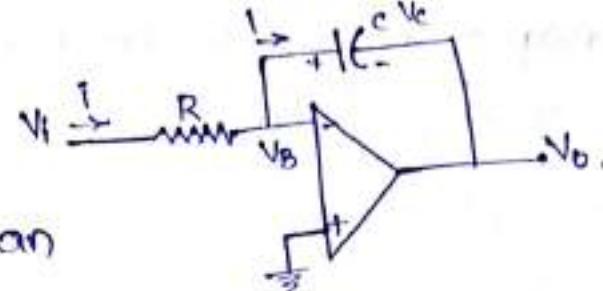
Integrating on both sides.

$$\int \frac{dV_o}{dt} \cdot dt = - \int \frac{1}{RC} V_i dt$$

$$V_o = -\frac{1}{RC} \int V_i dt$$

If integration period is from t_1 to t_2 , the above becomes

$$V_o = -\frac{1}{RC} \int_{t_1}^{t_2} V_i dt + V_o(t_1)$$



Frequency response of an ideal integrator :-

$$V_o(t) = -\frac{1}{RC} \int v_i(t) dt.$$

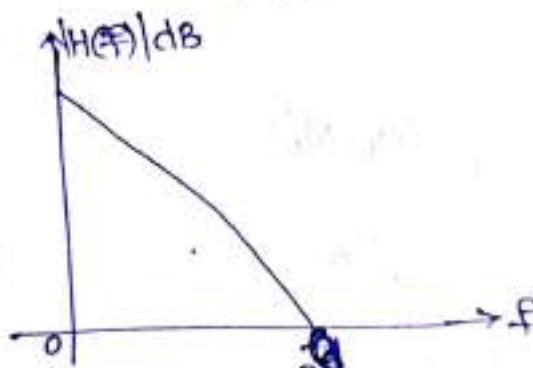
Apply Laplace transform of both sides

$$V_o(s) = -\frac{1}{RC} \cdot \frac{1}{s} V_i(s)$$

$$\frac{V_o(s)}{V_i(s)} = \frac{-1}{SRC}$$

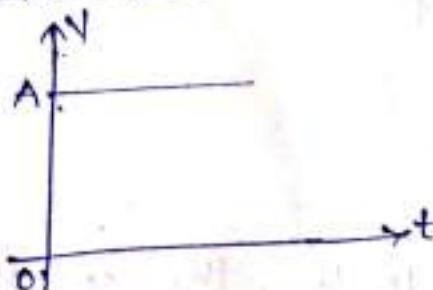
$$\Rightarrow H = \frac{V_o(j\omega)}{V_i(j\omega)} = \frac{-1}{j\omega RC} \\ = \frac{1}{j2\pi f RC}$$

$$|H(f)| = \frac{1}{2\pi f RC}.$$



Integrator output for various types of input signals :-

Step Input :-



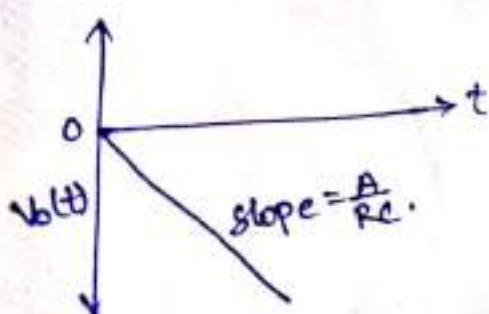
$$v_i(t) = A u(t)$$

$$\text{Assume } V_o(0) = 0$$

$$V_o(t) = -\frac{1}{RC} \int_0^t A u(t) dt$$

$$= -\frac{A}{RC} \int_0^t u(t) dt$$

$$= -\frac{A}{RC} (t - 0)$$



$$V_o(t) = -\frac{A}{R} \cdot t$$

ii) Square Wave input :

$$v_i(t) = A \quad ; 0 < t < T/2$$

$$v_i(t) = -A \quad ; \frac{T}{2} < t < T$$

$$\begin{aligned} v_o(t) &= \frac{-1}{RC} \int v_o(t) dt + v_o(0) \\ &= \frac{-1}{RC} \int_0^T v_o(t) dt + 0 \\ &= \frac{-1}{RC} \left[\int_0^{T/2} v_o(t) dt + \int_{T/2}^T v_o(t) dt \right] \\ &= \frac{-1}{RC} \int_0^{T/2} A dt + \left(\frac{-1}{RC} \int_{T/2}^T -A dt + v_o(T/2) \right) \\ &= \frac{A}{RC} \left[\frac{T}{2} - 0 \right] + \frac{A}{RC} \left[t - T/2 \right] = 0 \end{aligned}$$

$$v_i(t) = A, \quad 0 < t < T/2$$

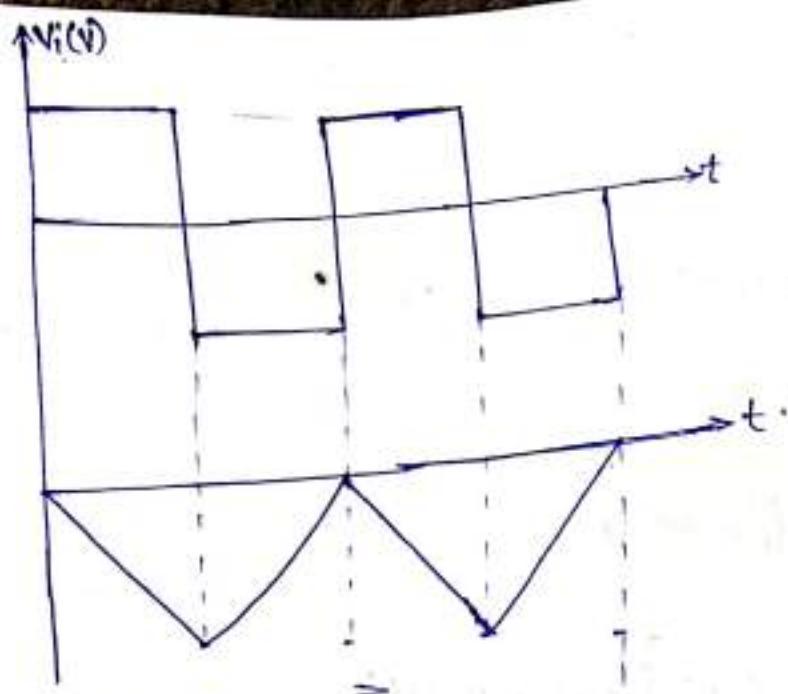
$$v_o(t) = \frac{-1}{RC} \int_0^t A dt = -\frac{A}{RC} t$$

$$\text{at } t = T/2 \Rightarrow v_o(T/2) = -\frac{A}{RC} \cdot \frac{T}{2}$$

$$v_i(t) = -A \quad \text{if } T/2 < t < T$$

$$\begin{aligned} v_o(t) &= \frac{-1}{RC} \int_{T/2}^t -A dt + v_o(T/2) \\ &= \frac{A}{RC} \left(t - \frac{T}{2} \right) - \frac{A}{RC} \left(\frac{T}{2} \right) \end{aligned}$$

$$v_o(t) = \frac{A}{RC} \cdot \left(t - \frac{T}{2} \right)$$



Sinusoidal Input:

$$\text{Let } V_i(t) = A \sin \omega_m t.$$

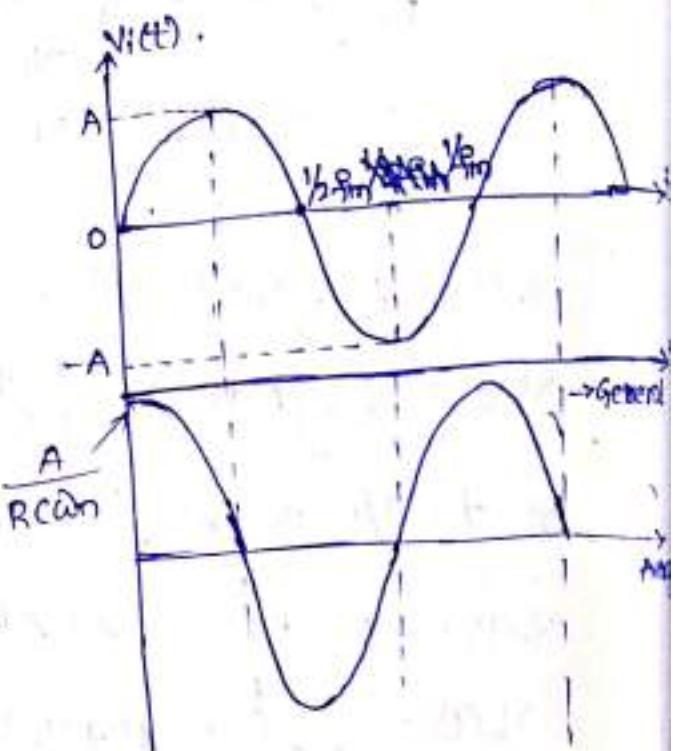
$$V_o(t) = -\frac{1}{RC} \int_{0}^t V_i(t) dt + V_0(t)$$

$$= -\frac{1}{RC} \int_{0}^t A \sin \omega_m t dt + 0$$

$$= -\frac{A}{RC} \left[\frac{-\cos \omega_m t}{\omega_m} \right]_0^t$$

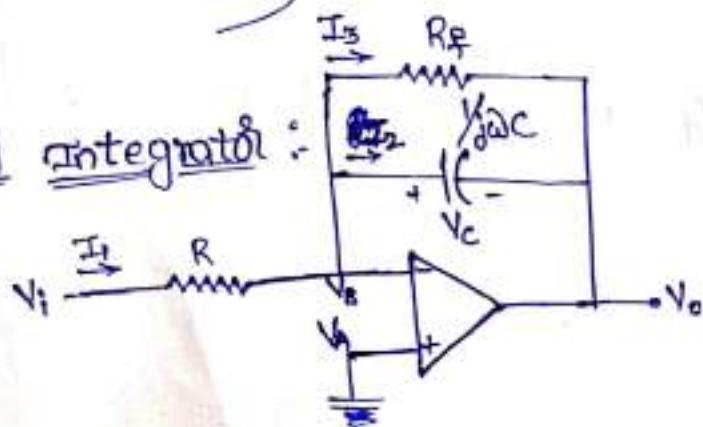
$$= +A \frac{(\cos \omega_m t - 1)}{\omega_m R C}$$

$$= \frac{A \cos \omega_m t}{\omega_m R C} - \frac{A}{\omega_m R C}.$$



09/09/19
Monday.

Practical Integrator:



In ideal integrator the feedback part consists of a capacitor. For low frequencies impedance of the capacitor is very high. Because of this, capacitor can acts as an open circuit and the output of op-amp may saturate to $+V_{sat}$ or $-V_{sat}$. To avoid this a resistor R_f is added in parallel to the capacitor as shown in the above figure. It is called as practical integrator.

From the above figure

$$V_A = 0; V_B = V_A = 0$$

$$I_1 = I_2 + I_3$$

$$I_1 = \frac{V_i - V_B}{R} = \frac{V_i}{R}$$

$$I_2 = \frac{V_C}{1/SC} = SC V_C = SC(V_B - V_o)$$

$$I_2 = -SC V_o$$

$$I_3 = \frac{V_B - V_o}{R_f} = -\frac{V_o}{R_f}$$

$$\therefore I_1 = I_2 + I_3$$

$$\frac{V_i}{R} = -SC V_o - \frac{V_o}{R_f}$$

$$\frac{V_i}{R} = -V_o \left(\frac{1}{R_f} + SC \right)$$

$$V_i = -V_o \left(\frac{R}{R_f} + SCR \right)$$

$$A = \frac{V_o}{V_i} = \frac{\frac{1}{R} + \frac{1}{R_f}}{\frac{R}{R_f} + SCR}$$

If $\frac{R}{R_f} \ll SCR$ then

$$A \approx \frac{-1}{SCR} \Rightarrow \frac{V_o}{V_i} = \frac{-1}{SCR}$$

$$V_o(s) = \frac{-1}{SCR} \cdot V_i(s)$$

$$\boxed{V_o(t) = -\frac{1}{RC} \int V_i(t) dt}$$

Frequency Response of practical Integrator :-

$$\frac{V_o}{V_i} = \frac{-1}{R + SCR}$$

Multiply numerator & denominator with $\frac{R_f}{R}$.

$$A = \frac{V_o}{V_i} = \frac{(-R_f/R)}{1 + SCR_f} = \frac{-R_f/R}{1 + j\omega R_f C}$$

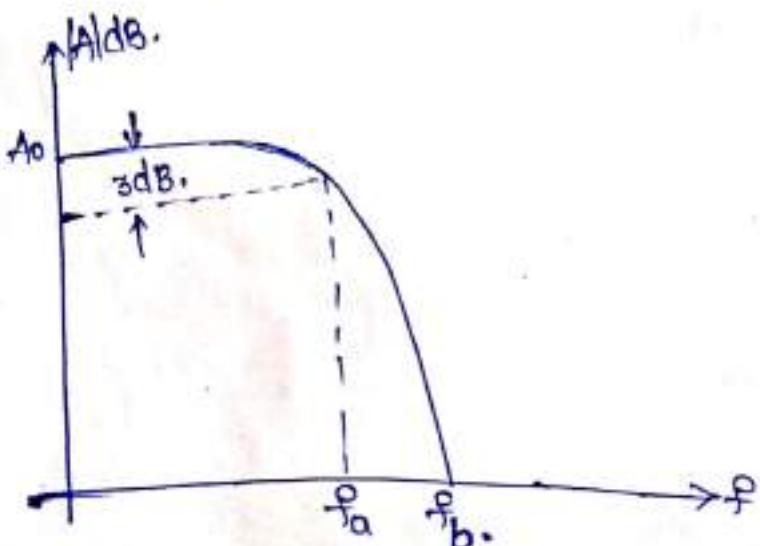
$$\text{Let } -\frac{R_f}{R} = A_0, \quad \checkmark$$

$$A = \frac{A_0}{1 + j\omega R_f C}$$

$$A = \frac{A_0}{1 + j \left(\frac{\omega}{f_a}\right)}$$

$$f_a = \frac{1}{2\pi R_f C}$$

$$|A| = \frac{A_0}{\sqrt{1 + \left(\frac{\omega}{f_a}\right)^2}} ; \quad \text{at } \omega = f_a, |A| = \frac{A_0}{\sqrt{2}}$$



At $f = f_b$

$$|A| = 1$$

f_b is called unity gain frequency.

$$f_b = \frac{A_0}{\sqrt{1 + \left(\frac{f_b}{f_a}\right)^2}} \quad \text{but } f_b \gg f_a \\ \left(\frac{f_b}{f_a}\right) \gg 1$$

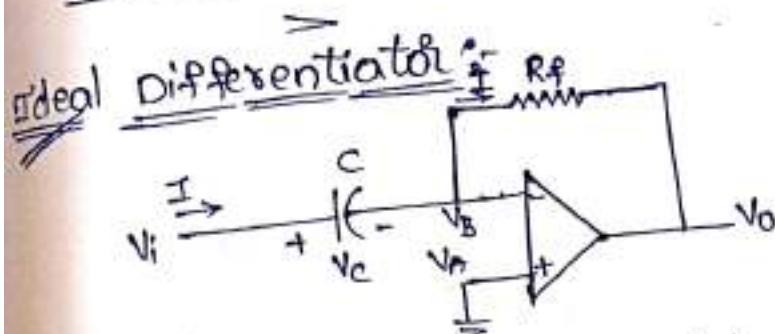
$$f_b = \frac{A_0}{\sqrt{\left(\frac{R_f}{R}\right)^2}}$$

$$f_b = A_0 \cdot f_a$$

$$f_b = -\frac{R_f}{R} \cdot f_a$$

$$f_b = -\frac{R_f}{R} \cdot \frac{1}{2\pi R_f C}$$

$$\boxed{f_b = \frac{1}{2\pi R C}}$$



The above figure shows an ideal differentiator.
From the above figure

$$V_A = 0$$

$$\therefore V_A = V_B = 0$$

capacitor current

$$I = C \frac{dV_C}{dt} = C \frac{d(V_i - V_B)}{dt} = C \frac{dV_i}{dt}$$

$$I = \frac{V_B - V_o}{R_f} = -\frac{V_o}{R_f}$$

$$\therefore \frac{-V_o}{R_F} = C \cdot \frac{dV_i}{dt}$$

$$\Rightarrow V_o = -R_F C \cdot \frac{dV_i}{dt}$$

The above circuit acts as a differentiator.
Frequency Response of an Ideal Differentiator:

$$V_o(t) = -R_F C \cdot \frac{dV_i(t)}{dt}$$

$$V_o(s) = -R_F C s V_i(s)$$

$$\frac{V_o(s)}{V_i(s)} = A = -s R_F C$$

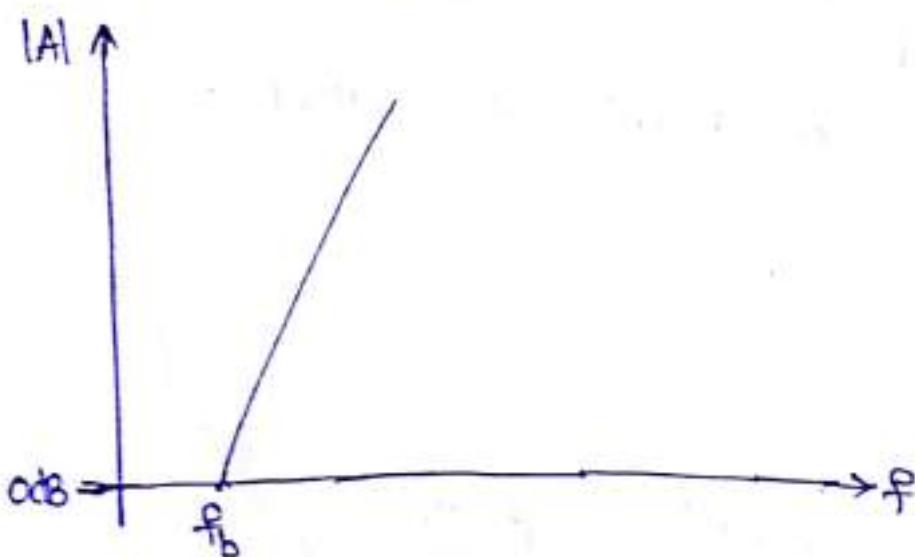
$$A = -j\omega R_F C$$

$$= -j2\pi f R_F C$$

$$A = -j \left(\frac{\omega}{f_b} \right)$$

$$\text{where } f_b = \frac{1}{2\pi R_F C}$$

$$|A| = \left(\frac{\omega}{f_b} \right)$$



1/09/19
Wednesday
Differentiator output for various types of inputs:

Step Input:

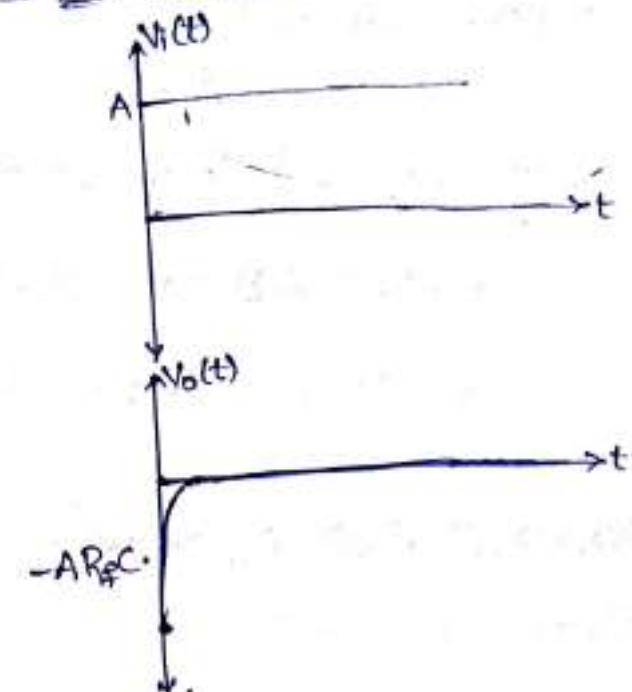
$$V_i(t) = A u(t)$$

$$V_o(t) = -R_f C \cdot \frac{dV_i(t)}{dt}$$

$$= -R_f C \cdot \frac{d}{dt}(A u(t))$$

$$= -A R_f C \frac{du(t)}{dt}$$

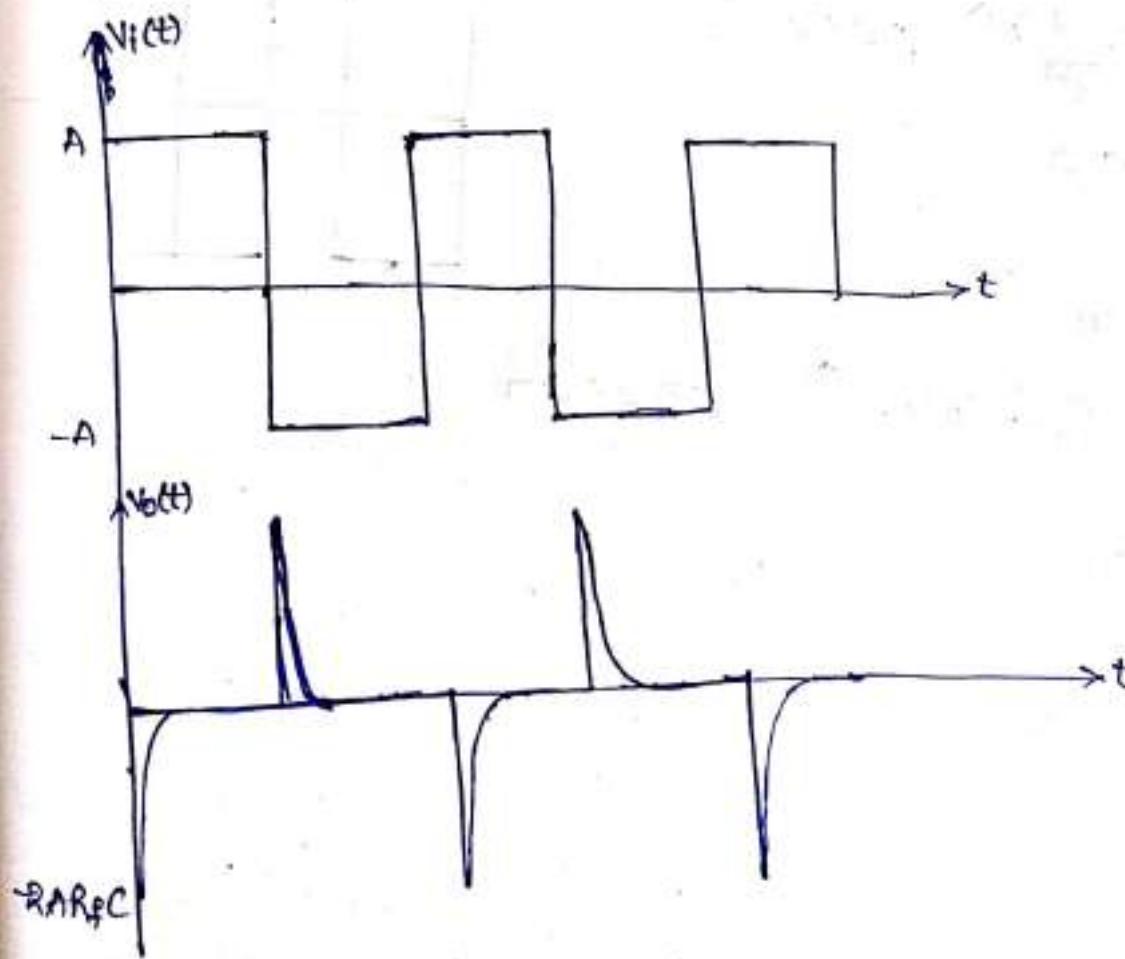
$$= -A R_f C \delta(t)$$



i) Square Wave Input:

$$V_i(t) = A, 0 < t < T/2$$

$$= -A, T/2 < t < T$$



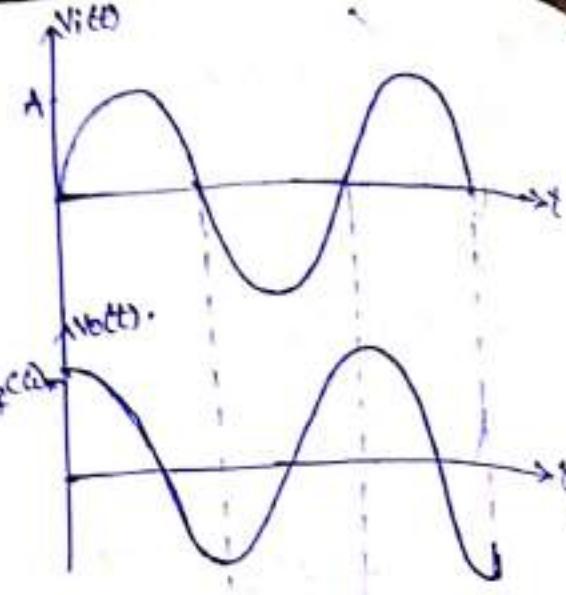
Sinusoidal Input:

$$V_i(t) = A \sin \omega_m t \\ = A \sin \omega_m \pi f_m t$$

$$V_o(t) = -R_f C \cdot \frac{d}{dt} (A \sin \omega_m \pi f_m t)$$

$$= -R_f C A \omega_m \pi f_m \cos \omega_m \pi f_m t \cdot -A R_f C \omega_m$$

$$= -A R_f C \omega_m \cos \omega_m \pi f_m t$$



Rectangular Waveform:

Triangular Input:

$$V_i(t) = At \quad , 0 < t < T/2$$

$$= -A(t-T), \quad T/2 < t < T$$

$$V_o(t) = -R_f C \cdot \frac{dV_i(t)}{dt}$$

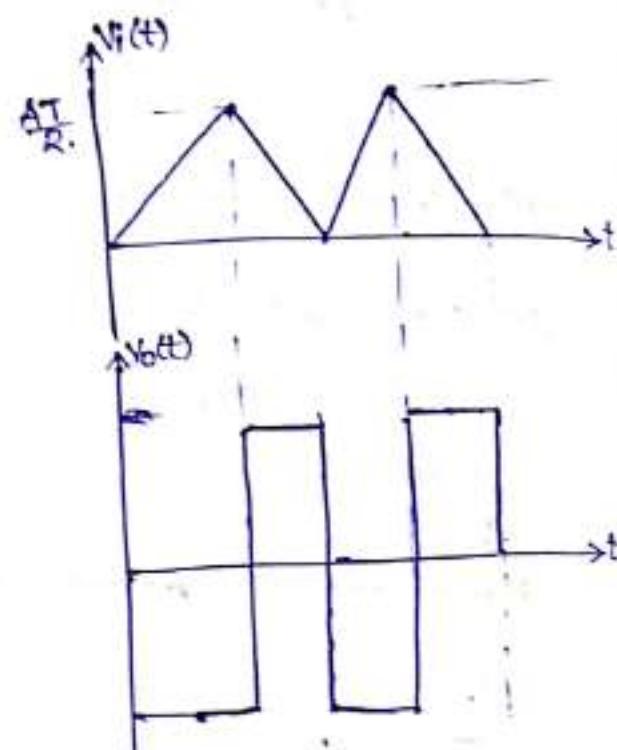
$$= -R_f C \cdot \frac{d(At)}{dt}, \quad 0 < t < T/2$$

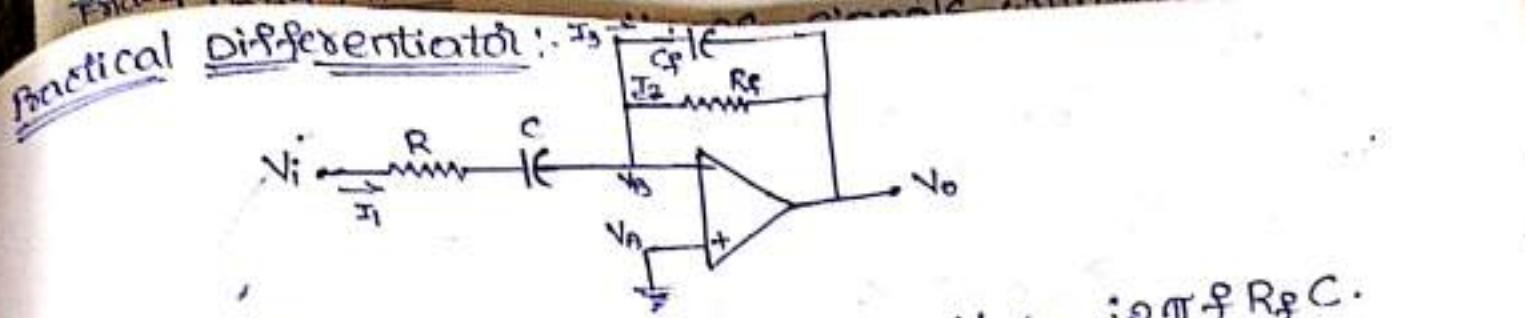
$$= -R_f C A$$

$$V_o(t) = -R_f C \cdot \frac{d}{dt} V_i(t)$$

$$= -R_f C \frac{d}{dt} (-A(t-T)) \quad , \quad T/2 < t < T$$

$$= R_f C A$$





An ideal differentiator, the gain is $\frac{V_o}{V_i} = -j2\pi f R_f C$. As f increases gain will also increase. At high frequencies the op-amp may saturate.

Also at high frequencies system catches noise which will be amplified.

To reduce noise amplification at high frequencies and bring stability to the gain, we add a resistor in series to the input capacitance and a capacitor in parallel to the feedback resistance.

$$V_A = 0$$

$\Rightarrow V_A = V_B = 0$. (virtual short circuit).

$$I_1 = \frac{V_i - V_B}{R + \frac{1}{SC}} = \frac{V_i}{R + \frac{1}{SC}}$$

$$I_2 = \frac{V_B - V_o}{R_f} = -\frac{V_o}{R_f}$$

~~$$I_3 = \frac{V_B - V_o}{\frac{1}{SC_f}} = -\frac{V_o}{\frac{1}{SC_f}} = -V_o SC_f$$~~

$$\therefore I_1 = I_2 + I_3$$

$$\frac{V_i}{R + \frac{1}{SC}} = -\frac{V_o}{R_f} - V_o SC_f$$

$$\frac{V_i}{(R + \frac{1}{SC})} = -V_o \left(\frac{1}{R_f} + SC_f \right)$$

$$\frac{V_o}{V_i} = \frac{-1}{(R + \frac{1}{SC}) (\frac{1}{R_f} + SC_f)}$$

$$\frac{V_o}{V_i} = \frac{-1}{\left(\frac{SCR+1}{SC}\right) \left(\frac{1+SC_f R_f}{R_f}\right)}$$

$$\frac{V_o}{V_i} = \frac{-SCR_f}{(1+SCR)(1+SC_f R_f)}$$

let $RC = R_f C_f$

$$\frac{V_o}{V_i} = \frac{-S R_f C}{(1+SCR)^2}$$

$$\frac{V_o}{V_i} = \frac{-j\omega R_f C}{(1+j\omega RC)^2} = \frac{-j\omega f R_f C}{(1+j\omega f RC)^2}$$

At low frequencies $1 \gg |j\omega f RC|$

$$\therefore \frac{V_o}{V_i} = -j\omega f R_f C = -S R_f C.$$

$$V_o = -S R_f C V_i$$

$$V_o(t) = -R_f C \cdot \frac{d(V_i)}{dt}$$

∴ At low frequencies the circuit behaves as a differentiator

$$\frac{V_o}{V_i} = \frac{-j\omega f R_f C}{(1+j\omega f RC)^2}$$

$$= \frac{-j \left(\frac{\omega}{f_b} \right)}{\left(1 + j \left(\frac{\omega}{f_a} \right) \right)^2}$$

$$f_b = \frac{1}{2\pi R_f C} ; \quad f_a = \frac{1}{2\pi R C}.$$

At high frequencies $\left(\frac{f}{f_a}\right) \gg 1$

$$\frac{V_o}{V_i} = \frac{-j\left(\frac{R}{R_b}\right)}{\left(j\left(\frac{R}{R_a}\right)\right)}$$

$$\frac{V_o}{V_i} = \frac{j\left(\frac{R}{R_b}\right)}{j\left(\frac{R}{R_a}\right)}$$

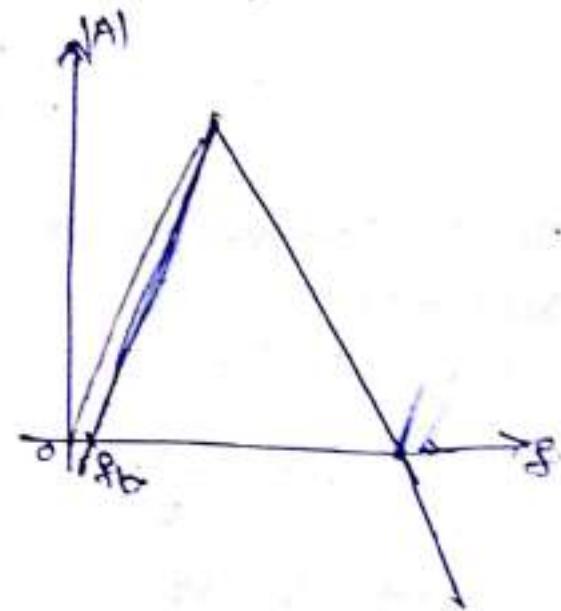
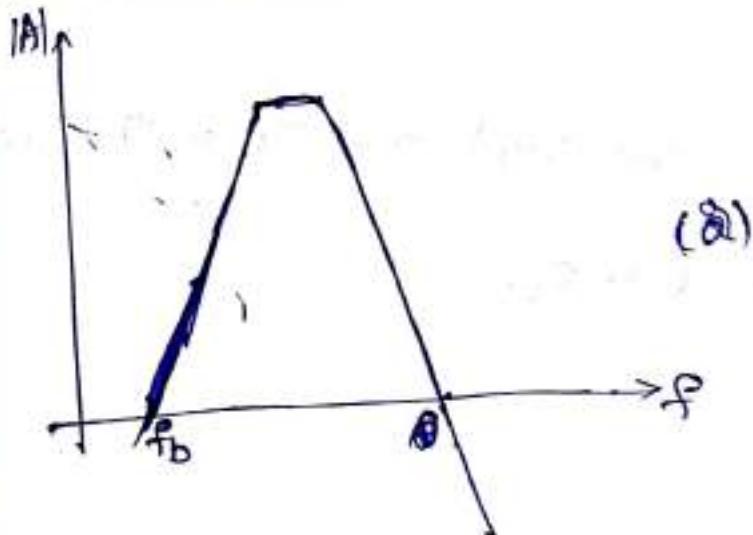
$$\frac{V_o}{V_i} = j\left(\frac{R}{R_b}\right) \times \left(\frac{R_a}{R}\right)$$

$$\frac{V_o}{V_i} = j \cdot \frac{R_a}{R_b} \cdot \frac{1}{j} = j k \frac{1}{f}$$

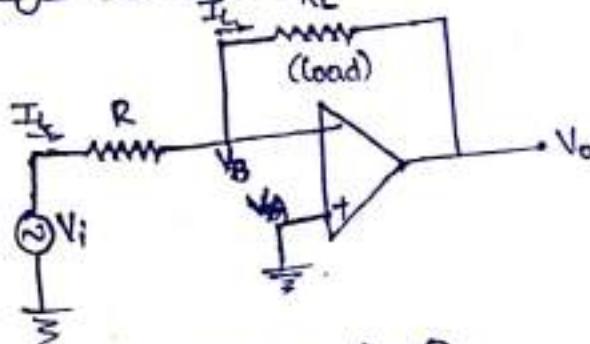
$$k = \text{constant} = \frac{R_a}{R_b}$$

At high frequencies gain decreases with frequency.

Frequency Response:



Voltage to current converter (with floating load)



$$V_B = 0 \Rightarrow V_A = 0$$

$$I_L = \frac{V_i - V_B}{R} = \frac{V_i}{R}$$

The above circuit $V_B = 0$

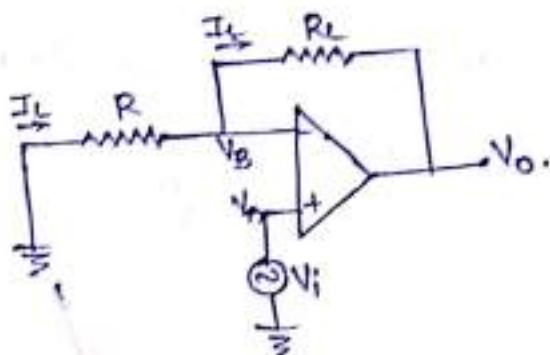
$$\Rightarrow V_A = 0$$

Load R_L is connected in the feedback path.
Load current is I_L . The same current passes through:

$$\therefore I_L = \frac{V_i - V_A}{R} = \frac{V_i}{R}$$

$$I_L \propto V_i$$

\therefore The given circuit is converted voltage into current.



In the above circuit R_L is the load and I_L is the load current.

Current I_L flows through R & R_L .

$$\therefore I_L = \frac{0 - V_B}{R}$$

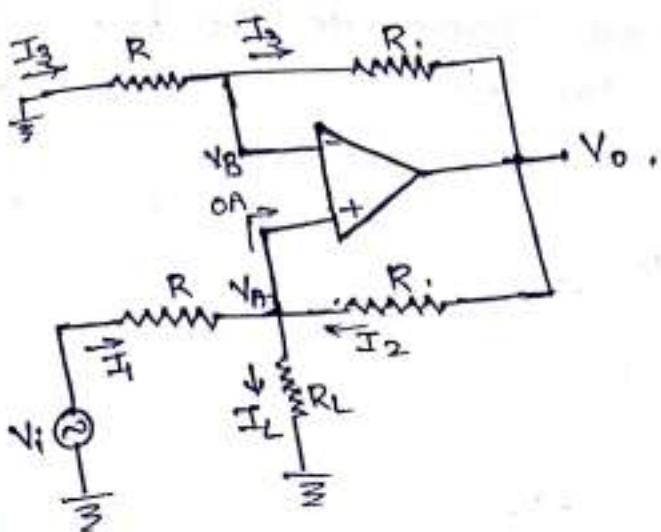
$$\text{But } V_A = V_i$$

$$\Rightarrow V_B = V_i$$

$$I_L = \frac{-V_i}{R}$$

$$I_L \propto V_i$$





By writing KCL at node A.

$$I_1 + I_2 = I_L$$

$$\frac{V_i - V_A}{R} + \frac{V_o - V_A}{R} = \frac{V_A}{R_L} I_L$$

$$\frac{V_i + V_o - 2V_A}{R} = \frac{V_A}{R_L} I_L$$

$$\frac{V_i + V_o - RV_A}{R} = I_L$$

$$\boxed{V_i + V_o - 2V_A = I_L \cdot R} \rightarrow ①$$

By writing KCL at node B.

$$I_3 = \frac{O - V_B}{R} = -\frac{V_B}{R} = -\frac{V_A}{R}$$

$$I_3 = \frac{V_B - V_o}{R} = \frac{V_A - V_o}{R}$$

$$-\frac{V_A}{R} = \frac{V_A - V_o}{R}$$

$$V_o = 2V_A$$

Substitute in equ ①.

$$① \Rightarrow V_i + V_o - 2V_A = I_L R$$

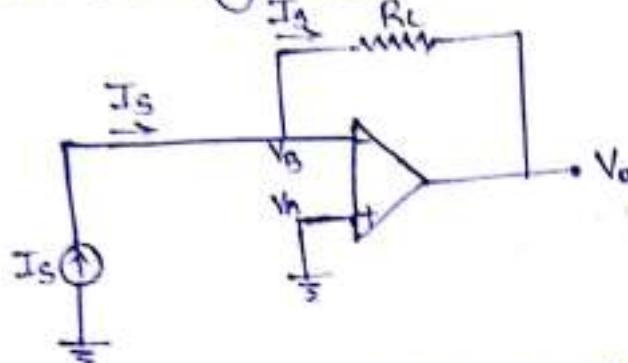
$$V_i + 2V_A - 2V_A = I_L R$$

$$I_L = \frac{V_i}{R}$$

$$I_L \propto V_i$$

\therefore The load current I_A is proportional to the input voltage hence this circuit converts the voltage to current.

Current to Voltage converter:



The above circuit current I_S passes through feedback resistor R_L .

$$I_S = \frac{V_B - V_{B^-}}{R_L}$$

$$\text{But } V_A = 0 \Rightarrow V_B = 0$$

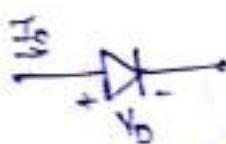
$$I_S = -\frac{V_O}{R_L} \Rightarrow V_O = -I_S R_L$$

$$V_O \propto I_S$$

\therefore The above circuit acts a current to voltage converter.

Unit-II Part-2

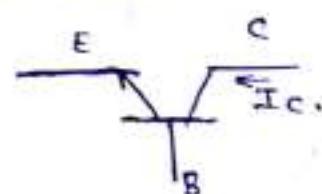
Non-linear Applications of Op-Amps:



$$I = I_0 (e^{\frac{V_B}{V_T}} - 1)$$

$$I_0 = I_0 (e^{\frac{V_B}{V_T}} - 1)$$

$$I_0 = I_0 \cdot e^{\frac{V_B}{V_T}}$$



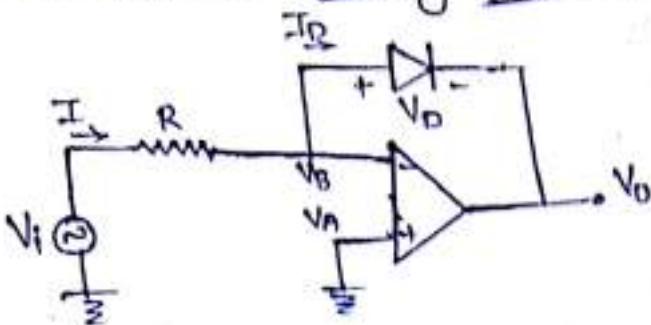
$$I_C \approx \alpha I_E$$

$$I_C \approx \alpha I_S e^{\frac{V_{BE}}{V_T}}$$

$$\alpha \approx 1$$

$$I_C \approx I_S \cdot e^{\frac{V_{BE}}{V_T}}$$

Logarithmic Amplifier using Diode w.r.t. Amp:



The above figure shows a logarithmic amplifier.

$$V_A = 0 \Rightarrow V_B = 0$$

The current I through R is given by

$$I = \frac{V_i - V_B}{R} = \frac{V_i}{R}$$

The relationship between diode current I_D and diode voltage V_0 is given by

$$I_D = I_0 e^{\frac{V_0}{mV_T}}$$

$$\text{But } V_0 = V_B - V_0$$

$$\Rightarrow V_0 = -V_0$$

$$\text{and } I = I_D$$

$$\therefore \frac{V_i}{R} = I_0 e^{-\frac{V_0}{mV_T}}$$

$$e^{-\frac{V_0}{mV_T}} = \frac{V_i}{I_0 R}$$

$$\frac{1}{e^{\frac{V_0}{mV_T}}} = \frac{V_i}{I_0 R}$$

$$e^{\frac{V_0}{mV_T}} = \frac{I_0 R}{V_i}$$

Apply loge on both sides i.e. (\ln)

$$\ln e^{\frac{V_0}{mV_T}} = \ln \frac{I_0 R}{V_i}$$

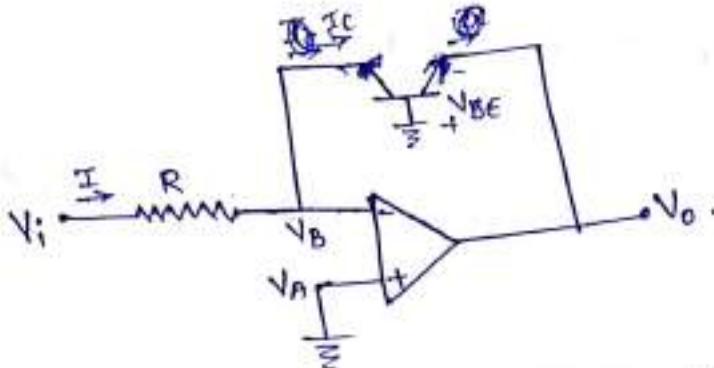
$$\frac{V_0}{mV_T} = \ln \frac{I_0 R}{V_i}$$

$$V_o = \eta V_T \ln \frac{I_o R}{V_i}$$

$$V_o = -\eta V_T \ln \frac{V_i}{I_o R}$$

$$\therefore V_o \propto \ln(V_i)$$

13/09/19
Friday
logarithmic Amplifier using transistor & OP-Amp!



$\therefore V_A = 0; V_B = 0$ (virtual short circuit)

$I = I_c$ (from figure)

$$I = \frac{V_i - V_B}{R} = \frac{V_i}{R}$$

$$I_c = I_s \cdot e^{\frac{V_B}{V_T}}$$

from the figure

$$V_o = V_{BE}$$

$$I_c = I_s \left(e^{\frac{-V_o}{V_T}} \right)$$

$$\frac{V_i}{R} = I_s \cdot e^{-\frac{V_o}{V_T}}$$

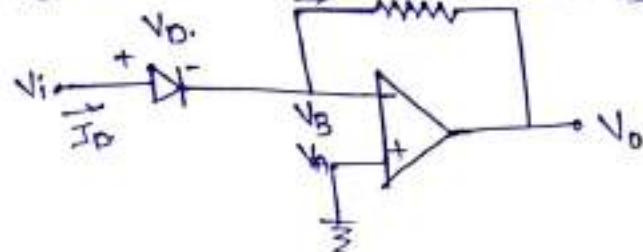
$$\frac{V_i}{R I_s} = e^{-\frac{V_o}{V_T}}$$

$$\ln \left(\frac{V_i}{R I_s} \right) = \ln e^{-\frac{V_o}{V_T}}$$

$$\ln \left(\frac{V_i}{R I_s} \right) = -\frac{V_o}{V_T}$$

$$\frac{1}{V_o} = -\frac{V_T}{V_o} \ln \left(\frac{V_i}{R I_s} \right)$$

Anti-logarithmic amplifier using diode & amplifier:



The above circuit represents anti-logarithmic amplifier using diode and amplifier

$$V_A = 0, V_B = 0$$

$$I_D = I$$

$$I_D = I_0 e^{\frac{V_D}{2kT}} = I_0 \cdot e^{\frac{V_i - V_B}{2kT}}$$

$$\Rightarrow I_D = I_0 e^{\frac{V_i}{2kT}}$$

$$I = \frac{V_B - V_0}{R} = -\frac{V_0}{R}$$

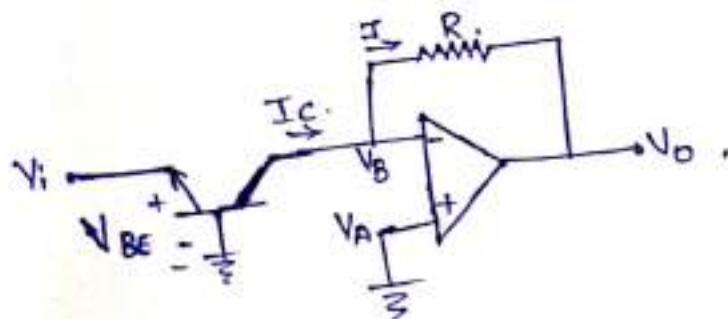
$$I_0 e^{\frac{V_i}{2kT}} = -\frac{V_0}{R}$$

$$V_0 = -R I_0 e^{\frac{V_i}{2kT}}$$

$$V_0 \propto e^{\frac{V_i}{2kT}}$$

∴ In this circuit, output voltage is proportional to anti-logarithmic of input voltage.

Anti-logarithmic amplifier using transistor & OP-Amp:-



$$V_A = 0; V_B = 0$$

$$V_i = V_{BE}$$

$$I_C = I$$

$$I_S e^{\frac{V_B - V_o}{N_T}} = \frac{V_B - V_o}{R}$$

$$I_S e^{\frac{V_i}{N_T}} = -\frac{V_o}{R}$$

$$V_o = -R I_S e^{\frac{V_i}{N_T}}$$

$$\boxed{V_o \propto e^{\frac{V_i}{N_T}}}$$

∴ In this circuit, output voltage is proportional to anti-logarithm of input voltage.

Unit - 4

Active filters And IC 555

Topics :-

- * Introduction
- * Advantages & Disadvantages of Active filter
- * Frequency response characteristics of Active filter
- * 1st Order Low pass Butterworth filter
- * Problems on 1st Order Low pass "
- * 2nd Order Low pass "
- * Problems on "
- * High pass filter
- * Band pass filter * Band Reject filter
- * All pass filters.

Introduction :-

→ Filter is a electronic device (SI) Ckt that is design to pass a specified band of frequencies while attenuating signals outside the band.

- There are '2' types of filters
1. Active filter
 2. Passive filter

→ If the filters are designed (SI) made up of active Components like op-Amp's. Then it is called

Active filter otherwise it is called Passive filter.

Advantages of active filters :-

→ Small in size, less weight.

→ Active filters are easily tunable for gain & frequency adjustments.

→ The max value of transfer function gain is always > 1 .

$$\text{i.e., } |A| \geq 1$$

→ Complex filters can be easily realized using active filters.

→ The response of active filter is more improved when compared to passive filters.

Limitations (Disadvantages) of active filters :-

→ Design of active filters at high frequencies is costly.

→ Active filters are more sensitive to temperature, environmental changes.

→ Active filters need dual channel power supply.

→ The band width of A.F is limited by slew rate of gain B.W product of OP-AMP.

frequency response characteristics of active filters :-

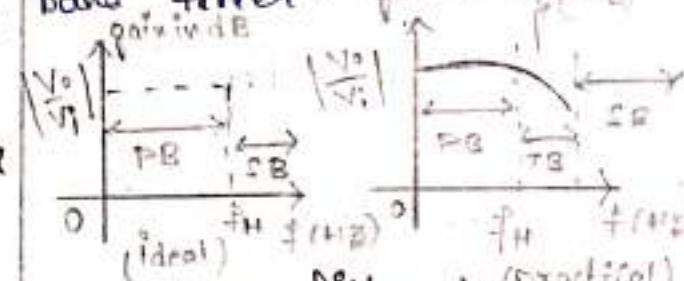
→ The most commonly used filters are LPF, HPF, BPF, BEF, All pass filter.

Low pass filter :-

→ A LPF passes all the low frequency components (0 to f_H) and attenuates all the high frequency components.

→ Here the frequency from 0 to f_{HB} is called pass band & the frequency above f_{HB} is called stop band filter.

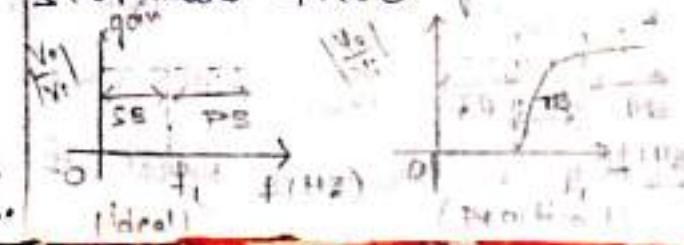
→ Gain in dB

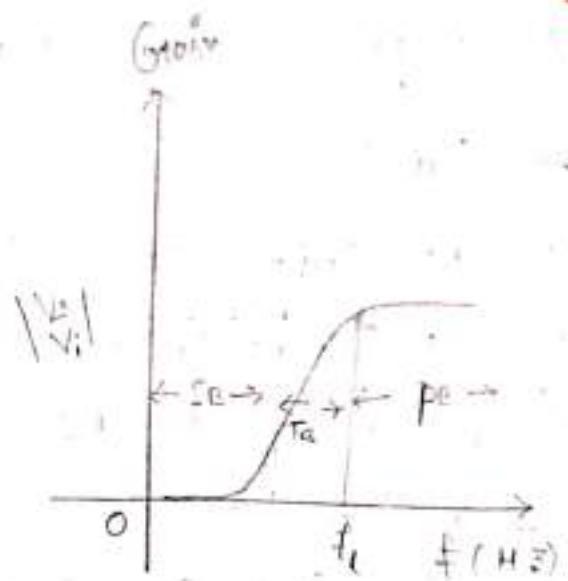
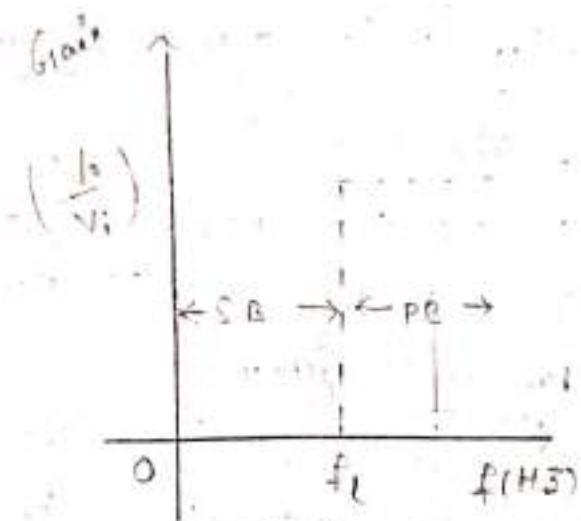


High pass filter :-

→ A HPF passes all the high frequency components (f_H to ∞) and attenuates all the low frequency components.

→ f_H to ∞ is called pass band & above f_{HB} is called stop band filter.

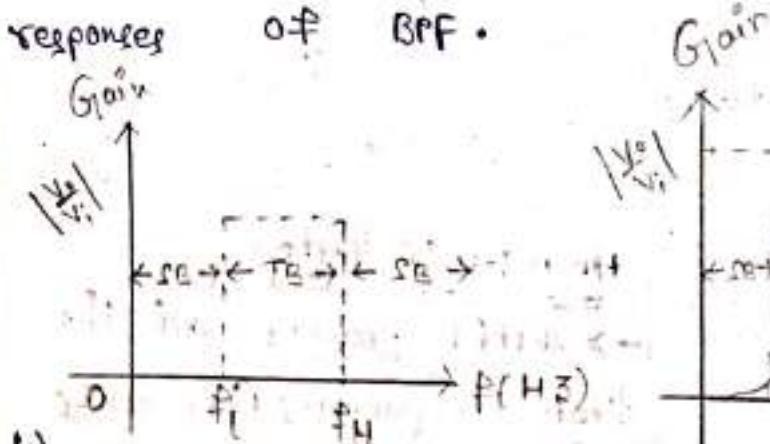




Band pass filter :-

→ A BPF is a combination of HPF and LPF and it allows only specified range of frequencies f_L & f_H .

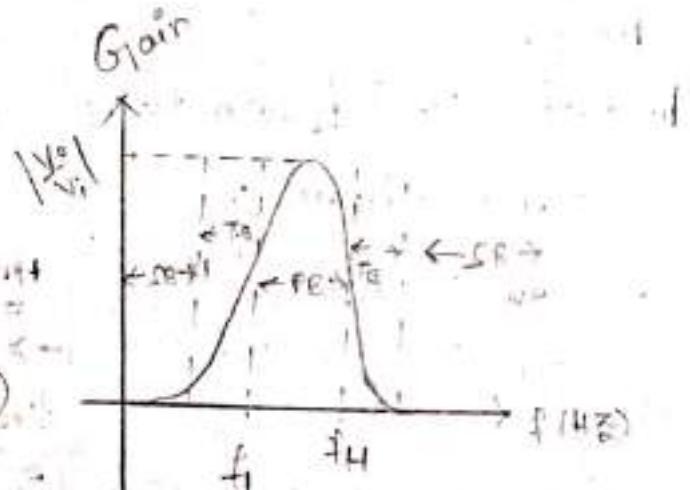
→ Here the BPF has one P.B and two S.B
→ The figure shows ideal and practical responses of BPF.

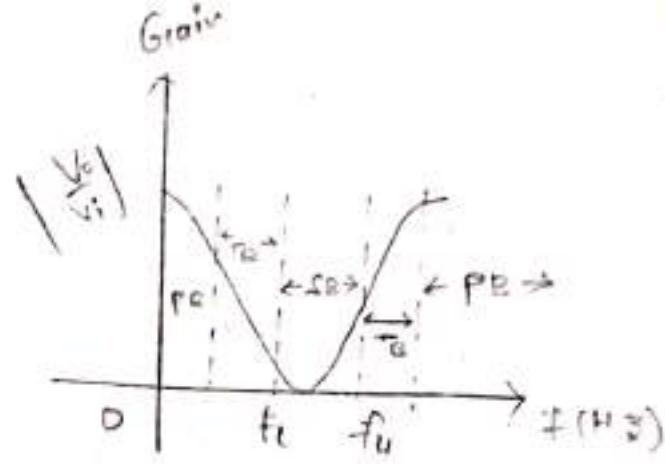
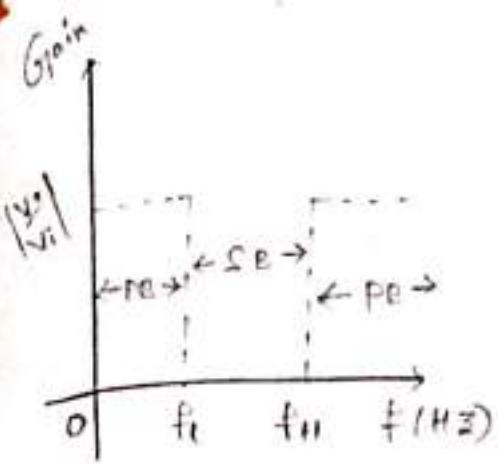


4)

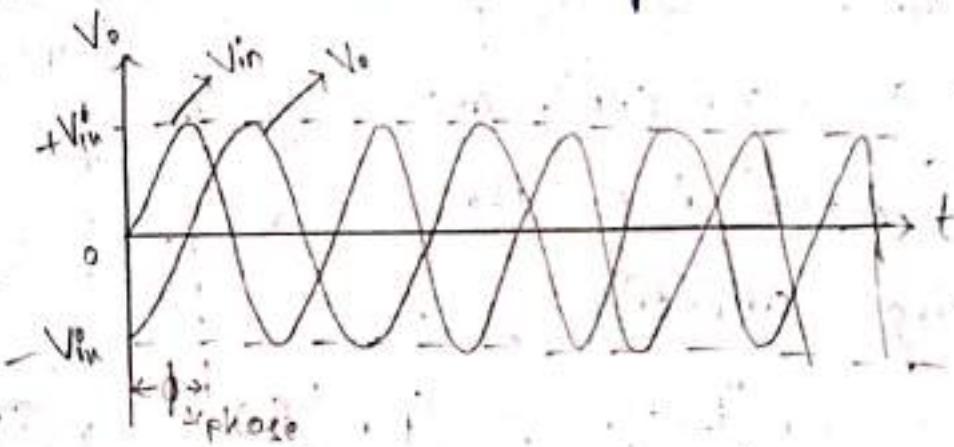
Band elimination filter :- The Band reject filter is the logical inverse of band pass filter which do not allow specified range of frequencies to pass through the filter.

→ Here BRF has two pass bands of one stop band
→ The fig shows ideal & practical responses of BRF





5. All pass filter :- an APF passes all the frequencies from ip to op without changing frequency in amplitude and frequency. But there is a small change in phase.

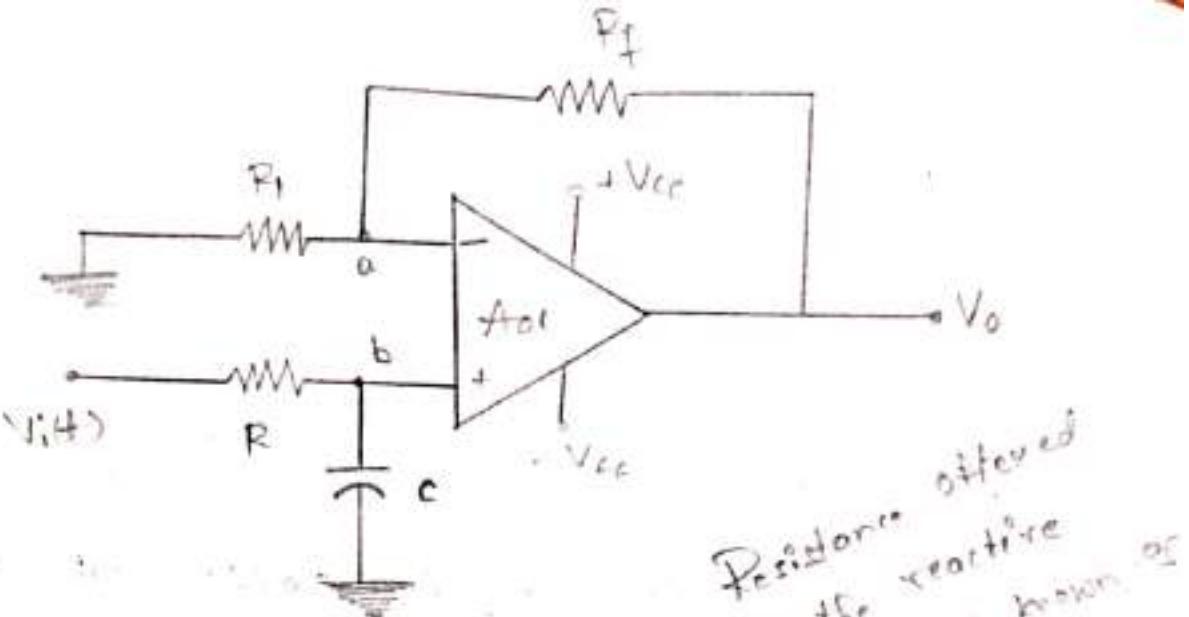


first Order low pass Butterworth filter :-

frequency response :-

→ The figure shows first order low pass Butterworth filter.

→ Here a RC Network is connected to the non-inverting ip terminal of OP-amp.



Resistor offered
by the reactive
elements known as
Resistance.

Operation :-

→ Case (ii) for low frequencies from 0 → f_H . the Capacitor (C) acts like a Open ckt. and LPF is Connected into the non-inverting amplifier.

$$\left\{ \begin{array}{l} X_C = \frac{1}{j\omega C} \\ X_C = \frac{1}{j2\pi f C} \\ X_C \propto \frac{1}{f} \end{array} \right.$$

$$\therefore V_o = \left(1 + \frac{R_f}{R_1}\right) V_i = \left(1 + \frac{R_f}{R_1}\right) V_b \rightarrow ①$$

Case (iii) :- for High frequencies from f_H to ∞ the Capacitor (C) acts like a short ckt and then entire op Voltage V_b is Grounded.

then

$$V_o(t) = \left(1 + \frac{R_f}{R_1}\right) 0 = 0V \rightarrow ②$$

$$\therefore V_o(t) = \left(1 + \frac{R_f}{R_1}\right) V_b + 0 = \left(1 + \frac{R_f}{R_1}\right) V_b$$

Analysis :-

from the figure the o/p Voltage

$$V_o(t) = \left(1 + \frac{R_f}{R_i}\right) V_b \rightarrow ①$$

$$\text{Here } V_b = \frac{V_i(t)/SCR}{R + 1/SCR} = \frac{V_i(t)}{1 + SCR}$$

$$\Rightarrow V_o(t) = \left(1 + \frac{R_f}{R_i}\right) \frac{V_i(t)}{1 + SCR}$$

$$\Rightarrow A = \frac{V_o(s)}{V_i(s)} = \frac{(1 + R_f/R_i)}{1 + SCR} = \frac{A_0}{1 + SCR} \quad (\because A_0 = \frac{A_0}{(1 + R_f/R_i)})$$

$$\begin{aligned} A &= \frac{V_o(j\omega)}{V_i(j\omega)} = \frac{A_0}{1 + j\omega CR} \\ &= \frac{A_0}{1 + j\omega RC} \\ &= \frac{A}{1 + j(f/f_H)} \quad (\because f_H = 1/\omega RC) \end{aligned}$$

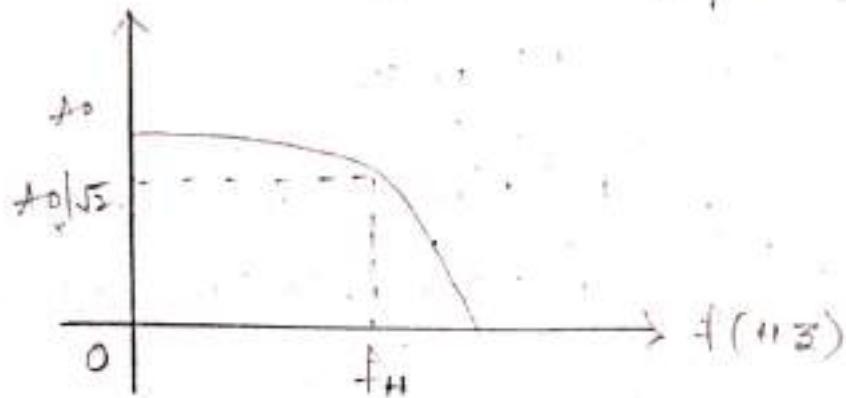
$$\text{Here } \text{Magnitude} = |A| = \left| \frac{V_o(j\omega)}{V_i(j\omega)} \right| = \frac{A_0}{\sqrt{(1 + f/f_H)^2}} \rightarrow ②$$

$$\phi = \angle A = \angle \frac{V_o(j\omega)}{V_i(j\omega)} = \frac{\angle -\tan^{-1}(f/f_H)}{\angle \tan^{-1}(f/f_H)} = -\angle \tan^{-1}(f/f_H) \rightarrow ③$$

$$\text{Put } f=0 \quad \text{③} \Rightarrow \left| \frac{V_o(j\omega)}{V_i(j\omega)} \right| = A_0$$

$$f=f_H \quad \text{③} \Rightarrow \left| \frac{V_o(j\omega)}{V_i(j\omega)} \right| = A_0 / \sqrt{2} = \frac{1}{1.414} A_0 \\ = 0.707 A_0$$

$$f=\infty \quad \text{③} \Rightarrow \left| \frac{V_o(j\omega)}{V_i(j\omega)} \right| \rightarrow \left| \frac{V_o(j\omega)}{V_i(j\omega)} \right| = 0$$



Design procedure for 1st order low pass

Butterworth filter

1. Choose an upper Cut off frequency f_H .
2. choose a Capacitor Value C typically less than 1 MF. Generally choose $C = 1 \mu F$.
3. Now Calculate the Resistance Value R by using the formula

$$f_H = \frac{1}{2\pi RC}$$

4. Select proper values for R_i and R_f
depending on the required pass band gain.

$$\text{i.e., } A_o = \left(1 + \frac{R_f}{R_i}\right)$$

Here the value of R_i is b/w 10-100

Typical Value of R_i is $10k\Omega$

Design a 1st order low pass filter having
a cut off frequency of 1kHz and pass
band gain of 2.

Here $f_c = 1\text{kHz}$, $A_o = 2$, $C = 1\mu\text{F}$

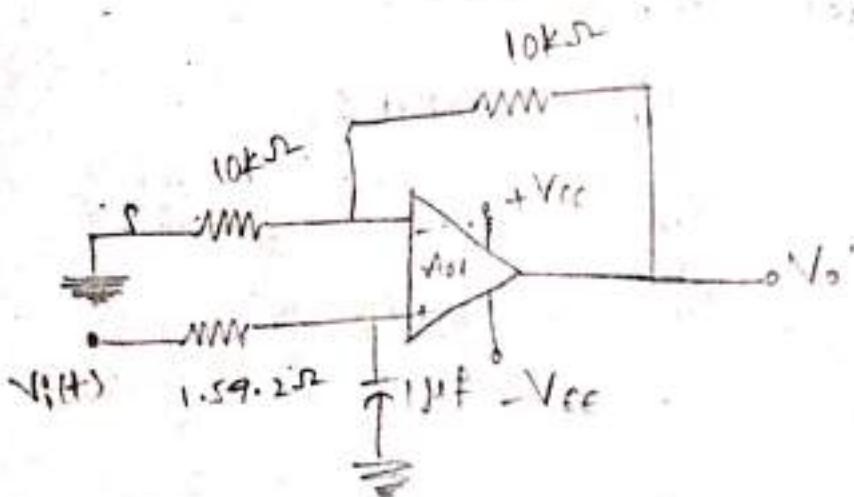
$$f_H = \frac{1}{2\pi R C} \Rightarrow R = \frac{1}{2\pi f_H C} = \frac{1}{2\pi \times 1\text{K} \times 1\mu\text{F}}$$

$$= \cancel{159.2}$$

$$A_o = 1 + R_f/R_i \quad | 59.2$$

$$\text{Here } A_o = 2 \text{ & } R_i = 10k\Omega \Rightarrow 2 = 1 + R_f/R_i$$

$$\Rightarrow R_f = 10k\Omega$$



→ frequency scaling :- once the filter is design sometimes it is necessary to change the cut-off frequency (f_H) .

→ The Method used to change the Original Cut off frequency (f_H) to a new Cut off frequency (f'_H) is called frequency Scaling.

→ In frequency Scaling the 1st step is find out the value of k such that

$$\therefore k = \frac{f_H}{f'_H} \text{ where ,}$$

Multiply k with either R or C but not with both (with change the Origin)

problem :-

wing frequency Scaling technique Convert 1KHz Cut off frequency to 1.6KHz for the above problem.

Given that $f_H = 1\text{KHz}$

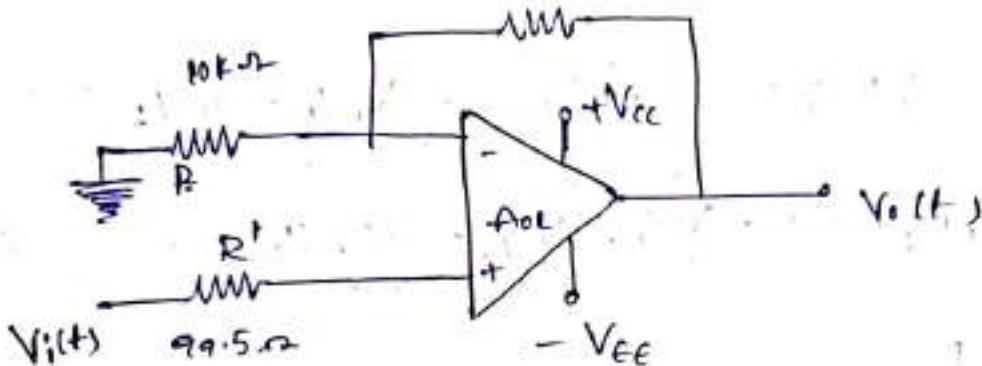
$$f'_H = 1.6\text{KHz}$$

$$k = \frac{f_H}{f'_H} = \frac{1\text{KHz}}{1.6\text{KHz}} = 0.625$$

$$R = 159.2 \Omega, C = 1 \mu F, R_i = 10 k\Omega, R_f = 10 k\Omega$$

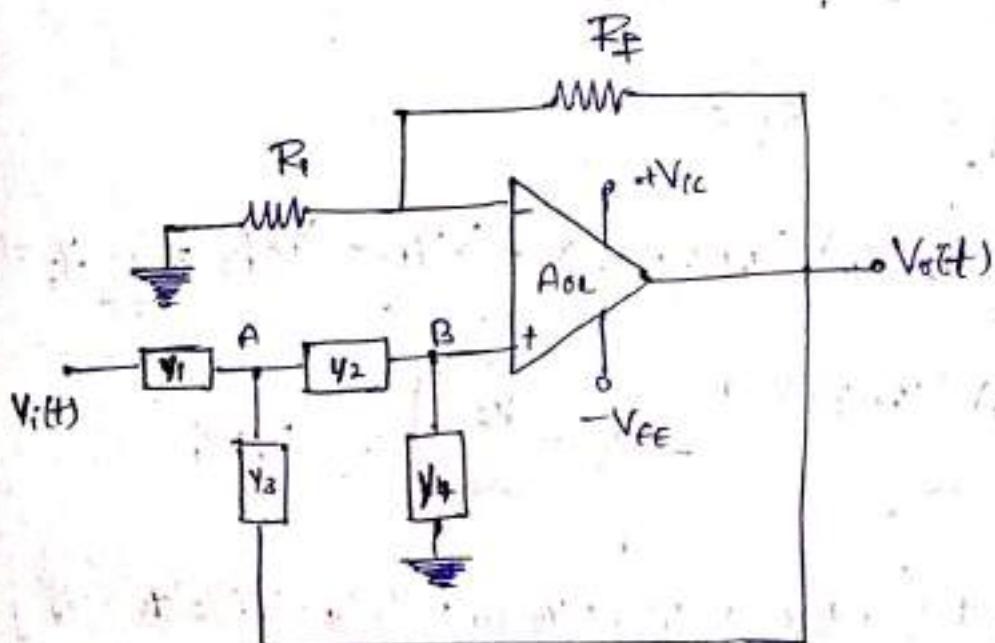
Hence $R' = kR$

$$R' = 0.625 \times 159.2 \Omega = 99.5 \Omega$$



Second Order Butterworth Low pass filter :-

The figure shows ckt diagram of Second Order Low pass Butter width filter.



*IMP

Analysis :-

From the figure the Op-amp is used in non-inverting configuration then.

$$V_o = \left(1 + \frac{R_f}{R_i}\right) V_B$$

$$= A_o V_B \Rightarrow V_B = \frac{V_o}{A_o} \rightarrow ①$$

Apply KCL at Node 'A'.

$$\Rightarrow (V_A - V_i) Y_1 + (V_A - V_o) Y_3 + (V_A - V_B) Y_2 = 0$$

$$V_A (Y_1 + Y_2 + Y_3) - V_o Y_3 - V_i Y_1 - V_B Y_2 = 0$$

$$V_A (Y_1 + Y_2 + Y_3) - V_i Y_1 - V_o Y_3 - \frac{V_o}{A_o} Y_2 = 0 \rightarrow ②$$

at Node B

$$\Rightarrow (V_B - V_A) Y_2 + V_B \cdot Y_4 = 0$$

$$V_B (Y_2 + Y_4) - V_A Y_2 = 0$$

$$\frac{V_o}{A_o} (Y_2 + Y_4) = V_A Y_2 \rightarrow ③$$

Sub Eq ③ in Eq ②

$$\Rightarrow \frac{V_o}{A_o Y_2} (Y_2 + Y_4) \cdot (Y_1 + Y_2 + Y_3) - V_i Y_1 - V_o Y_3 - \frac{V_o}{A_o} Y_2 = 0$$

$$\Rightarrow V_o \left[\frac{(Y_2 + Y_4)(Y_1 + Y_2 + Y_3)}{A_o Y_2} - Y_3 - \frac{Y_2}{A_o} \right] = V_i Y_1$$

$$\Rightarrow V_o \left[Y_1 Y_2 + Y_2^2 + Y_2 Y_3 + Y_1 Y_4 + Y_2 Y_4 + Y_3 Y_4 - A_o Y_2 Y_3 - Y_2^2 \right] = V_i Y_1 Y_2 A_o$$

$$\Rightarrow \frac{V_o}{V_i} = \frac{A_o Y_1 Y_2}{Y_1 Y_2 + (1 - A_o) Y_2 Y_3 + Y_2 (Y_1 + Y_2 + Y_3)} \rightarrow ④$$

To make a 2nd order LPF choose $Y_1 = Y_2 = 1/R$
and $Y_3 = Y_4 = \frac{1}{SC}$

$$\text{Eq(4)} \Rightarrow A = \frac{V_o}{V_i} = \frac{A_0 1/R^2}{1/R^2 + (1-A_0) 1/R \cdot \frac{1}{SC} + \frac{1}{SC} \left(\frac{1}{R} + \frac{1}{R} + \frac{1}{SC} \right)}$$

$$= \frac{A_0 (R^2)}{\frac{1}{R^2} + (1-A_0) \frac{SC}{R} + SC \cdot \left(\frac{2+SCR}{R} \right)}$$

$$\frac{V_o(s)}{V_i(s)} = \frac{A_0}{1 + (1-A_0) SCR + SCR (2 + SCR)}$$

$$\Rightarrow \frac{V_o(s)}{V_i(s)} = \frac{A_0}{(SCR)^2 + SCR (3 - A_0) + 1}$$

$$= \frac{A_0 / (RC)^2}{s^2 + (3 - A_0) \frac{1}{RC} + \left(\frac{1}{RC} \right)^2} \quad \rightarrow ⑤$$

Now Compare Eq(5) with 2nd order Transfer function

$$\therefore H(s) = \frac{-A_0 \omega_n^2}{s^2 + \alpha \omega_n s + \omega_n^2}$$

$$\text{Here } \omega_n^2 = (1/RC)^2$$

$$\alpha = 3 - A_0$$

$$\text{For 2nd order System } \alpha = 1.414$$

$$A_0 = 3 - \alpha = 1.586$$

$$\text{Eq. 5} \Rightarrow \frac{V_o(j\omega)}{V_i(j\omega)} = \frac{\frac{A_0 \omega_n^2}{(j\omega)^2 + \alpha j\omega \omega_n + \omega_n^2}}{\sqrt{\left(\frac{j\omega \omega_n^2}{\omega_n^2} + \alpha \frac{j\omega}{\omega_n} + 1\right)}} \\ = \frac{A_0 \omega_n}{\left(1 - \left(\frac{\omega}{\omega_n}\right)^2\right)^{\frac{1}{2}} + \alpha \frac{j\omega}{\omega_n}}$$

$$\left| \frac{V_o(j\omega)}{V_i(j\omega)} \right| = \left| \frac{A_0}{\left(1 - \left(\frac{\omega}{\omega_n}\right)^2\right)^{\frac{1}{2}} + \alpha \frac{j\omega}{\omega_n}} \right|$$

$$\frac{A_0}{\sqrt{\left(1 - \left(\frac{\omega}{\omega_n}\right)^2\right)^2 + \left(\alpha \frac{\omega}{\omega_n}\right)^2}}$$

$$\left| \frac{V_o(j\omega)}{V_i(j\omega)} \right| = \frac{A_0}{\sqrt{1 + \left(\frac{\omega}{\omega_n}\right)^2 - 2 \left(\frac{\omega}{\omega_n}\right)^2 + 2 \left(\frac{\omega}{\omega_n}\right)^2}}$$

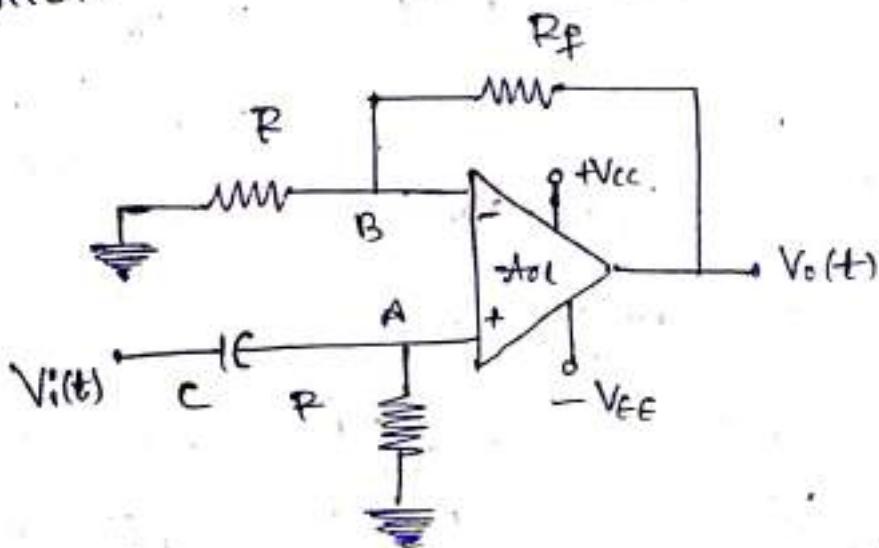
$$\left| \frac{V_o(j\omega)}{V_i(j\omega)} \right| = \frac{A_0}{\sqrt{1 + \left(\frac{\omega}{\omega_n}\right)^4}}$$

For n^{th} Order

$$\Rightarrow \boxed{\left| \frac{V_o(j\omega)}{V_i(j\omega)} \right| = \frac{A_0}{\sqrt{1 + \left(\frac{\omega}{\omega_n}\right)^{2n}}}}$$

1st order Butterworth high pass filter :-

The figure shows the 1st order high pass filter.



Hence the RC network is connected to the non-inverting input terminal.

Operation :-

Case i :- for low frequencies the capacitor acts like a short circuit.

Open ckt then $V_i = 0$,

the o/p voltage $V_o = (1 + R_f/R_i) V_A = 0$

Case ii :-

for high frequencies the capacitor acts like an open circuit.

o Short ckt then $V_o = (1 + R_f/R_i) V_A$

$$V_o = A_o V_A$$

$$\text{Analysis :- } V_A = \frac{V_i(t) \cdot R}{R + 1/sC} = \frac{V_i(t) \cdot sCR}{1 + sCR}$$

$$\text{Here } V_o(s) = \left(1 + \frac{R_f}{R_i}\right) V_A = A_o V_A$$

$$(\because A_o = 1 + \frac{R_f}{R_i})$$

$$\Rightarrow V_o(s) = \frac{A_o \cdot V_i(t) \cdot sCR}{1 + sCR}$$

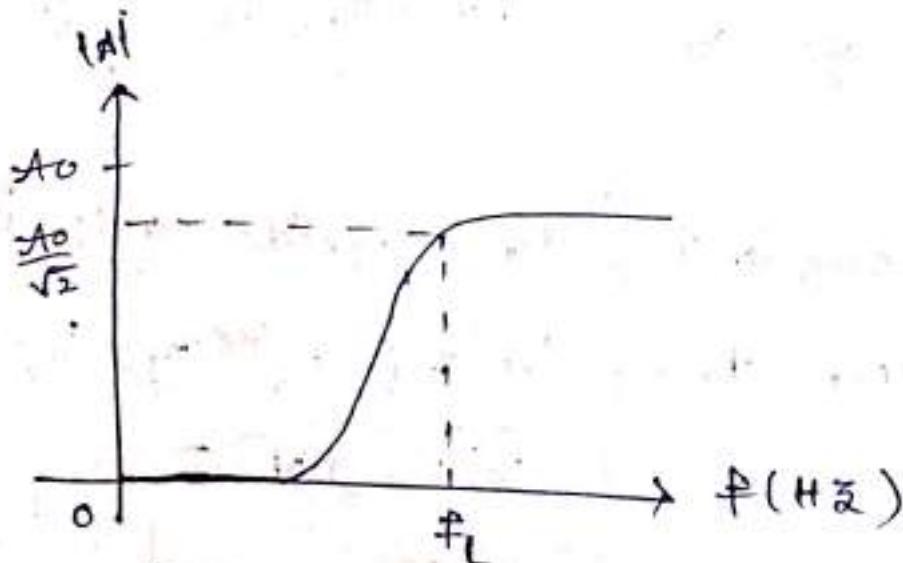
$$A = \frac{V_o(s)}{V_i(s)} = \frac{A_o \cdot sCR}{1 + sCR}$$

$$H(j\omega) = \left| \frac{V_o(j\omega)}{V_i(j\omega)} \right| = \left| \frac{A_o (f/f_L)}{\sqrt{1 + (f/f_L)^2}} \right| \quad \left\{ f_L = \frac{1}{2\pi RC} \right.$$

$$\text{Put } f=0 \Rightarrow |A| = 0$$

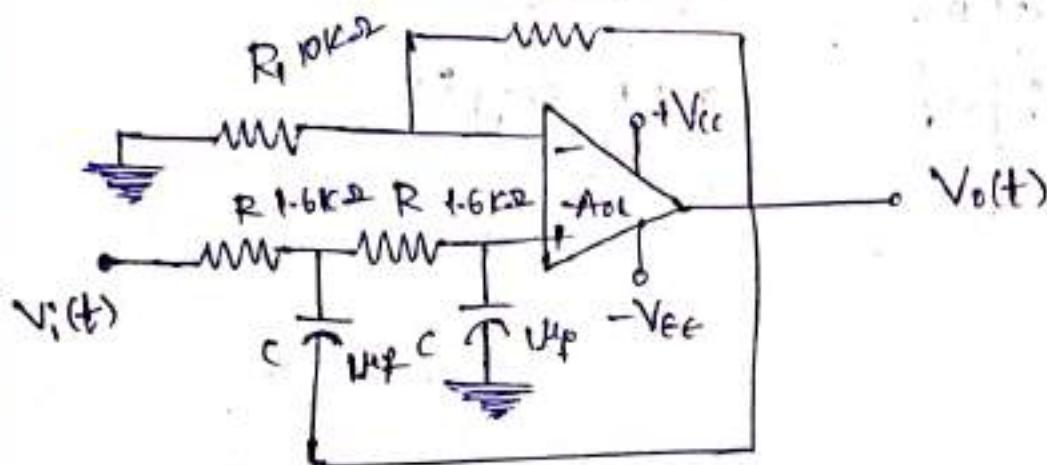
$$f=f_L \Rightarrow |A| = A_o \sqrt{2}$$

$$f=\infty \Rightarrow |A| = \infty$$



problem :- Design the 2nd order low pass butterworth filter having upper cut off frequency of $f_H = 1\text{kHz}$ and determine frequency response.

The figure shows 2nd order low pass butterworth filter



Given that $f_H = 1\text{kHz}$

$$f_H = \frac{1}{2\pi R C}$$

$$\text{choose } C = 1\mu F \Rightarrow f_H = \frac{1}{2\pi R C} = 1.6\text{kHz}$$

for 2nd order LPF, $n=2$ & $\alpha = 1.414$

$$A_O = 3 - \alpha = 3 - 1.414 = 1.586$$

$$A_O = 1 + \frac{R_p}{R_1}$$

$$1.586 = 1 + \frac{R_p}{10k}$$

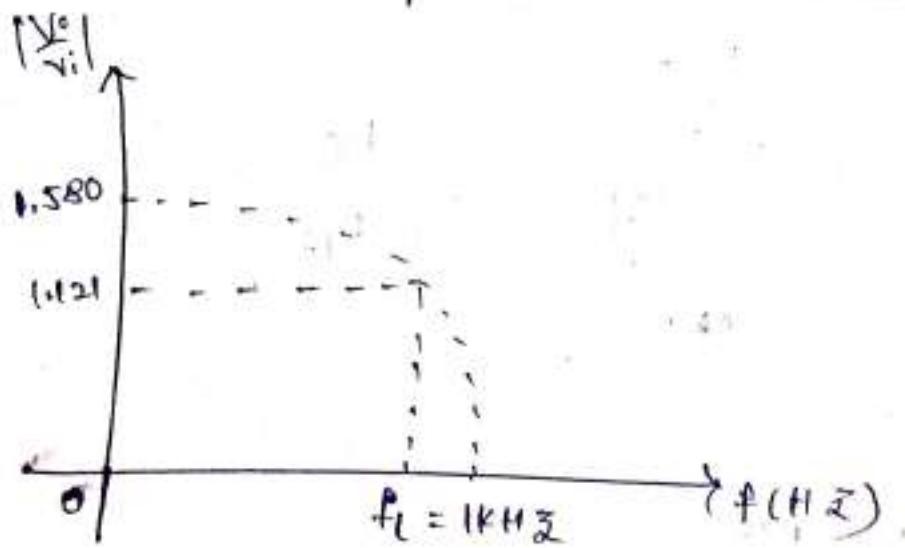
$$\text{choose } R_1 = 10k\Omega$$

$$R_p = 5.86k\Omega$$

frequency Response :-

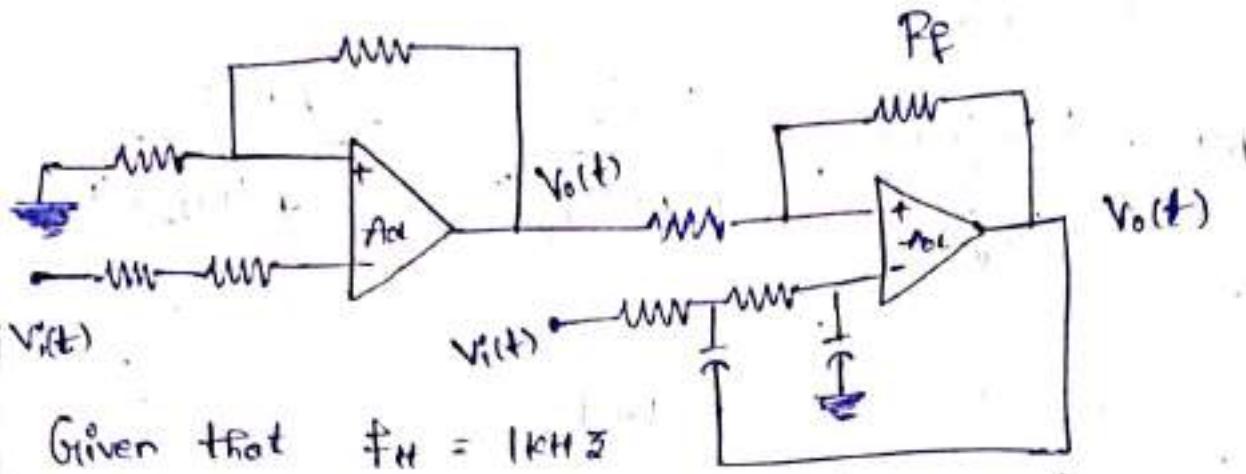
$$|A| = \left| \frac{V_o(j\omega)}{V_i(j\omega)} \right| = \frac{A_0}{\sqrt{1 + (\frac{\omega}{\omega_n})^4}} = \frac{1.586}{\sqrt{1 + (\frac{\omega}{1K})^4}}$$

$f(Hz)$	$ A_0 (dB)$	$\left \frac{V_o(j\omega)}{V_i(j\omega)} \right $
0	0	1.586
5	-	1.586
10	-	1.585
100	-	1.585
500	-	1.538
1K	-	1.121
2K	-	0.786
5K	-	0.06



Design a 4th order butter with low pass filter for the cut off frequency of 1kHz

The figure shows low pass butter with filter.



Given that $f_H = 1\text{kHz}$

$$f_H = \frac{1}{2\pi RC} \quad \& \quad C = 1\mu\text{F}$$

$$\Rightarrow R = \frac{1}{2\pi f_H C} = 0.16\text{ k}\Omega$$

for 4th Butterworth LPF

$$\alpha_1 = 0.765 \quad \& \quad \alpha_2 = 1.848$$

$$A_{01} = 3 - \alpha_1 = 2.235$$

$$A_{02} = 3 - \alpha_2 = 1.157$$

$$\text{Also } A_{01} = 1 + \frac{R_{f1}}{R_{11}} \quad \& \quad A_{02} = \frac{R_{f2}}{R_{12}}$$

choose $R_{11} = R_{12} = 10\text{k}\Omega$

$$R_{f1} = 12.35\text{k}\Omega$$

$$R_{f2} = 1.52\text{k}\Omega$$

Band pass filter :-

→ A band pass filter is basically a frequency selector.

→ It allows one particular band of frequencies to pass from ilp to olp.

→ Any frequency outside that band is attenuated

(8) Eliminated:

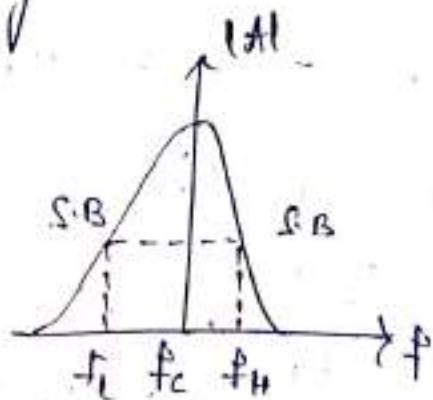
→ The pass band which is in bw f_H & f_L
is called band width.

→ The frequency at the Centre of the passband
is called as centre frequency (f_0)

$$\text{i.e., } f_0 = \sqrt{f_H \cdot f_L}$$

→ And also quality factor

$$Q = \frac{f_c}{B.W}$$

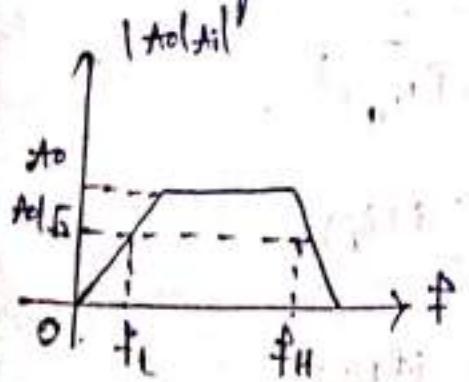


→ Based on the Q-value band pass filter
is divided into two types.

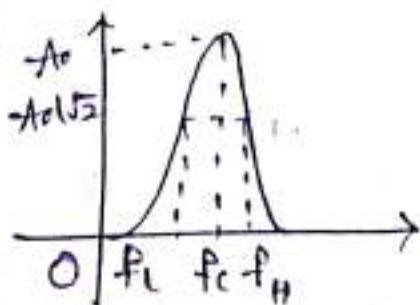
i. Wide band pass filter ($Q < 10$)

ii. Narrow " " " " " ($Q > 10$)

→ The fig shows frequency response of



WBP



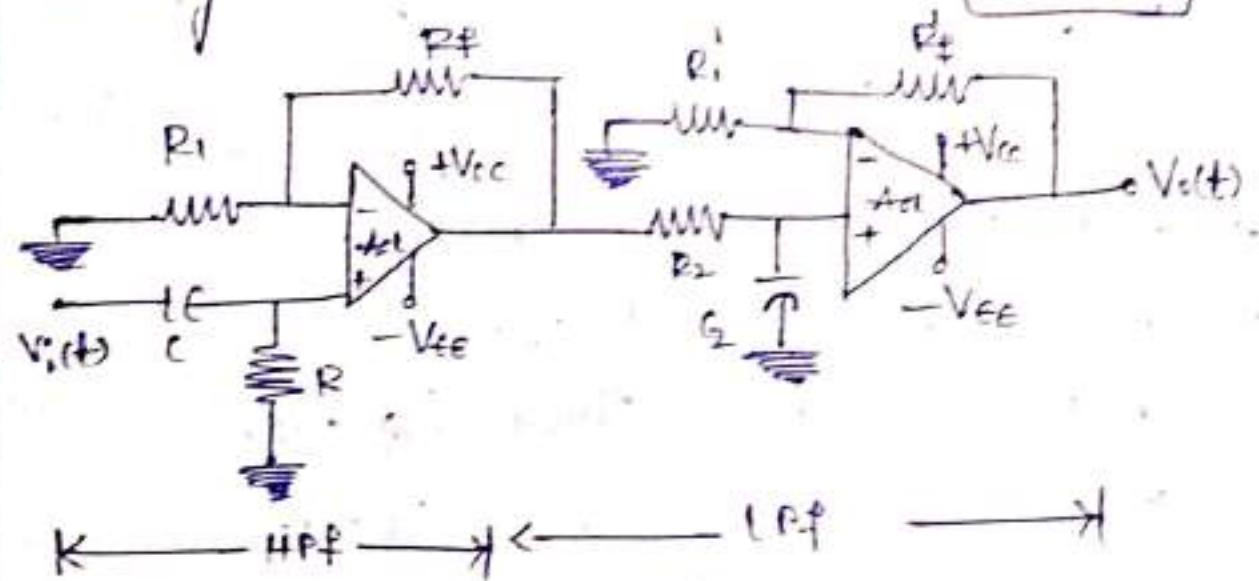
NBP

Wide band pass filter :- (WBPF)

- The wide band pass filter can be formed by cascading a HPF & LPF of required orders.
- The fig shows, the ckt diagram of WBPF.



The only Condition for this is $f_L < f_H$



$$\rightarrow \text{for LPF } A_1 = \frac{A_{d1}}{\sqrt{1 + (\frac{f}{f_{L1}})^2}}$$

$$\rightarrow \text{for HPF } A_2 = \frac{A_{d2}(\frac{f}{f_{H1}})}{\sqrt{1 + (\frac{f}{f_{H1}})^2}}$$

→ The gain of WBPF given as

$$A = A_1 \times A_2$$

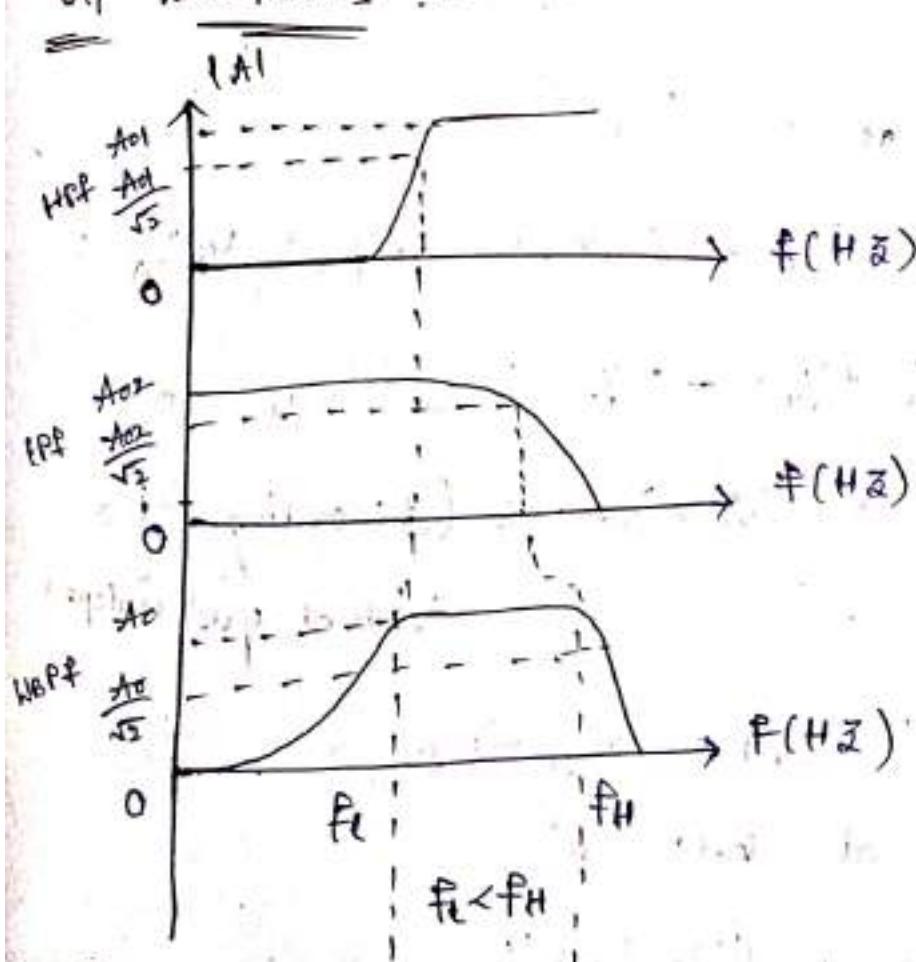
$$= \frac{A_{01}}{\sqrt{1 + (\frac{f}{f_H})^2}} \cdot \frac{A_{02}}{\sqrt{1 + (\frac{f}{f_L})^2}}$$

$$\therefore A = \frac{A_0 \left(\frac{f}{f_L} \right)}{\sqrt{1 + (\frac{f}{f_H})^2} \sqrt{1 + (\frac{f}{f_L})^2}} \quad \left(\because A_0 = A_{01} \times A_{02} \right)$$

$$\frac{f}{f_H} = \frac{1}{\omega R_C C}$$

$$\frac{f}{f_L} = \frac{1}{\omega R_C}$$

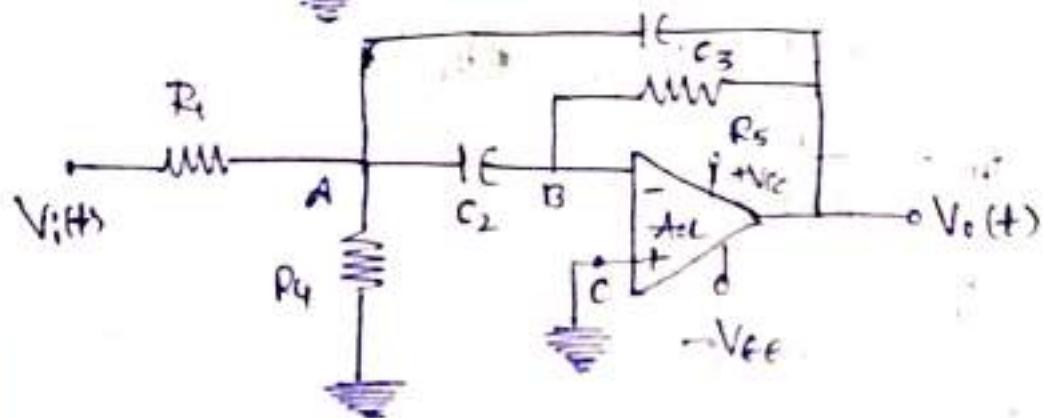
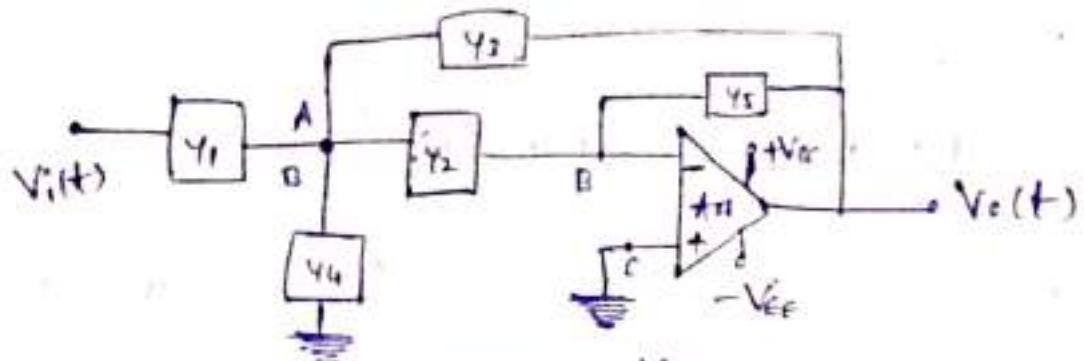
OLP waveforms :-



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NBPF :-

→ The fig shows 2nd order NBPF



Analysing :-

apply kcl at node 'A'

$$(V_A - V_1(t))Y_1 + (V_A - V_B)Y_2 + (V_A - V_0)Y_3 + Y_4 V_A = 0$$

$$V_A(Y_1 + Y_2 + Y_3 + Y_4) - V_1 Y_1 - V_B Y_2 - V_0 Y_3 = 0$$

Here $V_{ic} = 0 \Rightarrow V_B = V_c = 0$ (According to
virtual ground concept)

$$V_A(Y_1 + Y_2 + Y_3 + Y_4) - V_1 Y_1 - V_0 Y_3 = 0 \rightarrow ①$$

apply kcl at node 'B'

$$(V_B - V_A)Y_2 + (V_B - V_0)Y_5 = 0$$

$$V_B(Y_2 + Y_5) - V_A Y_2 - V_0 Y_5 = 0$$

$$V_A = -\frac{V_0 Y_5}{Y_2} \rightarrow ② \quad (\because V_B = 0)$$

$$\textcircled{1} \Rightarrow -\frac{V_0 Y_5}{Y_2} (Y_1 + Y_2 + Y_3 + Y_4) - V_i Y_1 - V_0 Y_3 = 0$$

$$\Rightarrow -V_0 \left(\frac{Y_1 Y_5}{Y_2} + \frac{Y_2 Y_5}{Y_2} + \frac{Y_3 Y_5}{Y_2} + \frac{Y_4 Y_5}{Y_2} + Y_3 \right) = V_i Y_1$$

$$\frac{V_0}{V_i} = -V_0 \left(\frac{Y_5}{Y_2} (Y_1 + Y_2 + Y_3 + Y_4) + Y_3 \right) = V_i Y_1$$

$$= \frac{-Y_1 Y_2}{Y_5 (Y_1 + Y_2 + Y_3 + Y_4) + Y_2 Y_3} \rightarrow \textcircled{3}$$

for obtaining 2nd order NBF put

$$Y_1 = G_{11}$$

$$Y_2 = L C_2$$

$$Y_3 = L C_3$$

$$Y_4 = G_{14}$$

$$Y_5 = G_{15} \quad \text{in Eq } \textcircled{3}$$

$$\text{Eq } \textcircled{3} \Rightarrow \frac{V_0(\omega)}{V_i(\omega)} = \frac{-G_{11} \cdot L C_2}{G_{15}(G_{11} + L C_2 + L C_3 + G_{14}) + L C_2 \cdot L C_3}$$

$$\frac{V_0(\omega)}{V_i(\omega)} = \frac{-L C_2 \cdot G_{11}}{L^2 C_2 \cdot C_3 + G_{15}(G_{11} + L C_2 + L C_3 + G_{14})}$$

$$= \frac{-L C_2 \cdot G_{11}}{L^2 C_2 C_3 + G_{15}(G_{14} + G_{11}) + L C_{15}(C_2 + C_3)}$$

$$= \frac{-G_{11}}{L C_3 + \frac{G_{15}(G_{14} + G_{11})}{L C_2} + G_{15} \left(\frac{C_2 + C_3}{C_2} \right)}$$

put $s = j\omega$

$$\frac{V_o(j\omega)}{V_i(j\omega)} = \frac{-G_{11}}{j\omega C_3 + \frac{G_{15}(C_2 + C_3)}{2} + \frac{(G_{11} + G_{14})G_{15}}{j\omega C_3}}$$

$$\Rightarrow \frac{V_o(j\omega)}{V_i(j\omega)} = \frac{-G_{11}}{\frac{G_{15}(C_2 + C_3)}{C_2} + i\left(\omega C_3 - \frac{G_{15}(G_{11} + G_{14})}{\omega C_2}\right)} \rightarrow ④$$

At resonant frequency the imaginary part = 0

$$\text{i.e., } ④ \Rightarrow \omega_0 C_3 - \frac{G_{15}(G_{11} + G_{14})}{\omega_0 C_2} = 0$$

$$\omega_0^2 C_2 C_3 = G_{15}(G_{11} + G_{14})$$

$$\omega_0^2 = \frac{G_{15}(G_{11} + G_{14})}{C_2 C_3}$$

$$H(j\omega) = \frac{V_o(j\omega)}{V_i(j\omega)} = \frac{-\frac{G_{11}C_2}{G_{15}(C_2 + C_3)}}{}$$

Band Elimination (BE) Band Reject filter

The Operation of Band Elimination filter

is exactly Opposite operation of Band Pass filter.

→ It has 2 pass bands and 1 stop band
and it eliminates the frequencies b/w
 f_L and f_H .

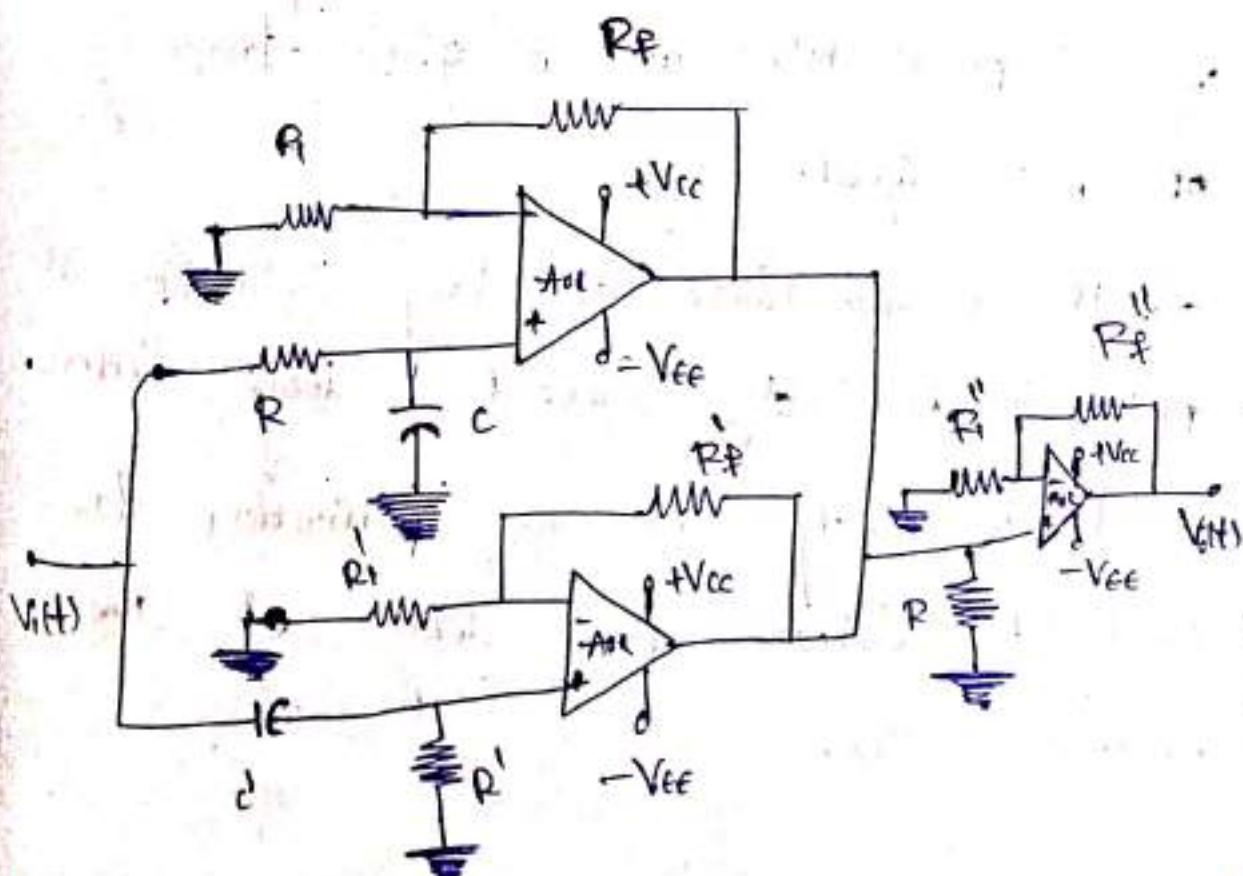
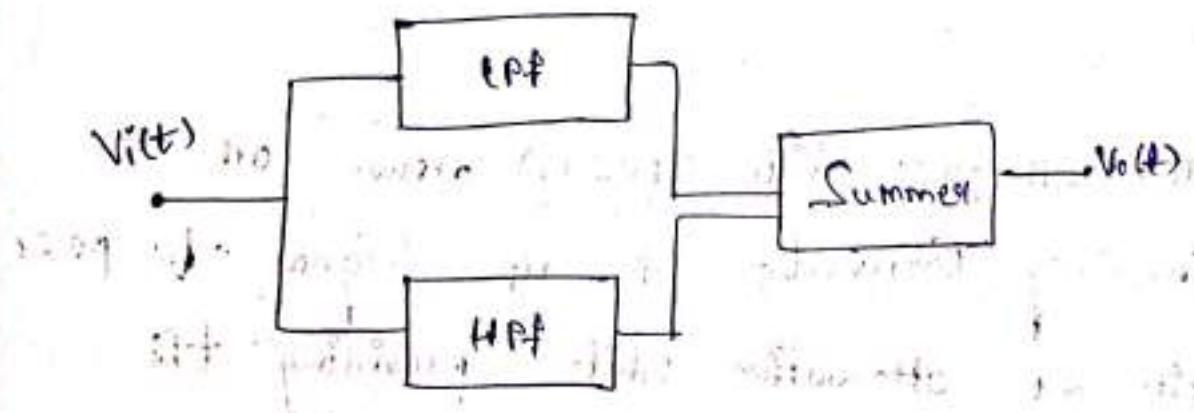
→ It is divided into two types.

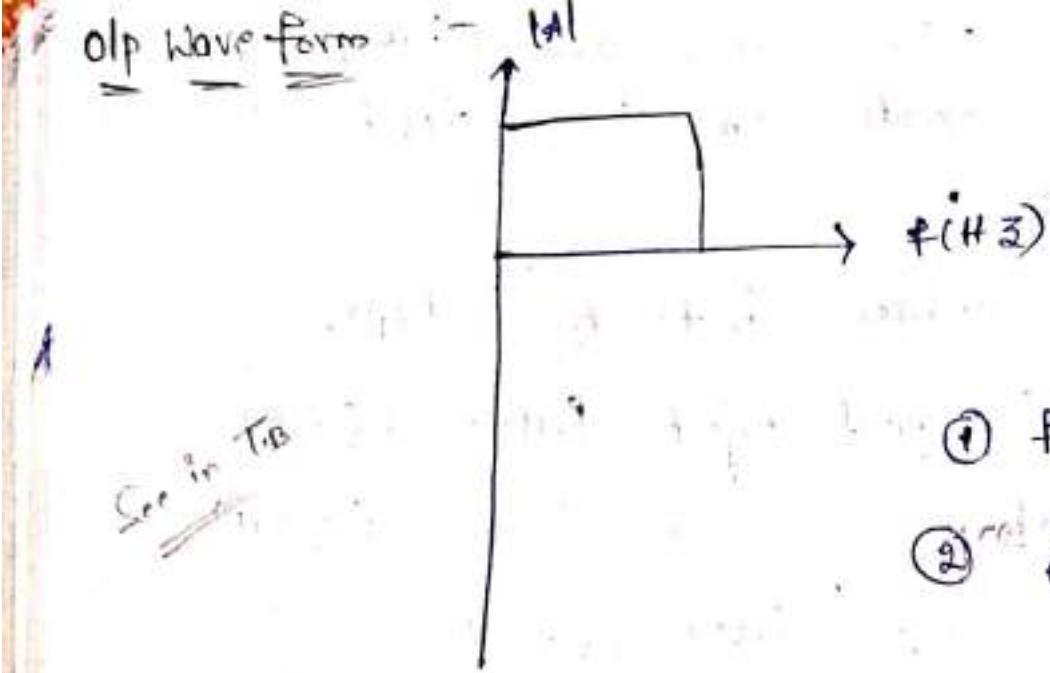
1. wide band reject filter ($Q < 10$)

2. Narrow " " " " ($Q > 10$)

wide band reject filter ($Q < 10$) :-

The fig shows wide band reject filter





$$\textcircled{1} \quad f_L < f_H$$

$$\textcircled{2} \quad A_{o1} = A_{o2}$$

NBF - Notch filter (T.B)

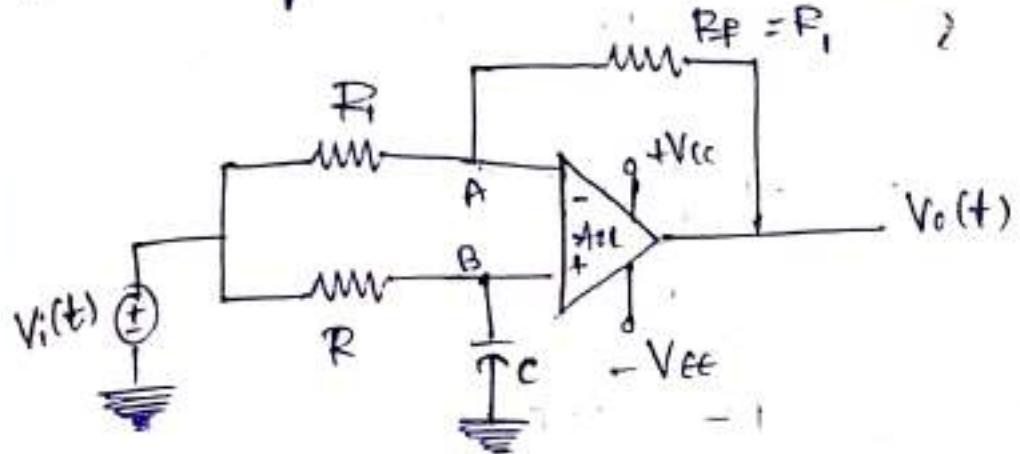
All pass filter :-

The 'All-pass' filter (pass) allows all the frequency components of ilp signal to pass with out attenuation while providing the required phase shift at a given frequency of ilp signal.

→ It is also called as delay equalizer or phase corrector (dc), constant delay filter.

→ It is widely used in publications to avoid dc to eliminate phase delay at the receiver side.

→ The fig shows all pass filter.



Analyse :-

By applying Superposition principle

Case (i) Inverting = active & Non-inverting = quid
then all pass filter becomes inverting amplifier.

$$V_{o1} = -\frac{R_f}{R_1} V_i = -\frac{R_f}{R_1} \cdot V_i(t) = -V_i(t) \rightarrow ①$$

Case (ii) Inverting = quid, Non-inverting = active
then all pass filter becomes non-inverting amplifier

$$V_o = \left(1 + \frac{R_f}{R_1}\right) V_B$$

$$V_B = \frac{V_i(t) \cdot 1/sC}{R + 1/sC} = \frac{-V_i(t)}{1 + sCR} = \frac{V_i(t)}{1 + j\omega fRC}$$

$$\therefore V_o(t) = V_{o1} + V_{o2}$$

$$= -V_i(t) + \left(1 + \frac{R_f}{R_1}\right) \cdot \frac{V_i(t)}{1 + j\omega fRC}$$

$$\frac{V_o(s)}{V_i(s)} = \left(-1 + \frac{s^2}{1+j\omega RC} \right)$$

$$= \frac{-1 - j\omega RC + 2}{1 + j\omega RC}$$

$$\boxed{\frac{V_o(s)}{V_i(s)} = \frac{1 - j\omega RC}{1 + j\omega RC}}$$

$$M = \left| \frac{V_o(j\omega)}{V_i(j\omega)} \right| = \left| \frac{1 - j\omega RC}{1 + j\omega RC} \right|$$

$$= \frac{\sqrt{1 + (\omega RC)^2}}{\sqrt{1 + (\omega RC)^2}}$$

$$\left| V_o(j\omega) \right| = \left| V_i(j\omega) \right|$$

$$\phi = \angle \frac{V_o(j\omega)}{V_i(j\omega)} = \angle \frac{1 - j\omega RC}{1 + j\omega RC}$$

$$= \angle \tan^{-1} \left(\frac{-\omega RC}{1} \right)$$

$$\angle \tan^{-1} \left(\frac{\omega RC}{1} \right)$$

$$\phi = -2 \angle \tan^{-1} (\omega RC)$$

from the above expression the required amount of phase shift can be produced by choosing proper values for R and c.

→ we can also introduce the phase shift by interchanging the position of R & c

24/08/19
Saturday

6. Digital to Analog & Analog to Digital Converter

D to A converter :-



The above figure shows a block diagram of D/A converter.
The relationship between output analog signal and input digital bits is given by

$$V_0 = K V_{FS} (b_1 \bar{2}^1 + b_2 \bar{2}^2 + b_3 \bar{2}^3 + \dots + b_n \bar{2}^n)$$

where $V_0 \rightarrow$ output analog voltage.

$V_{FS} \rightarrow$ Full scale voltage of D/A converter.

(It is also called as reference voltage V_R).

$K \rightarrow$ scaling factor.

$b_1, b_2, b_3, \dots, b_n \rightarrow$ input digital code.

$b_1 \rightarrow$ MSB

$b_n \rightarrow$ LSB.

Transfer curve of D/A converter (DAC) :

Let us consider a 3 bit DAC.

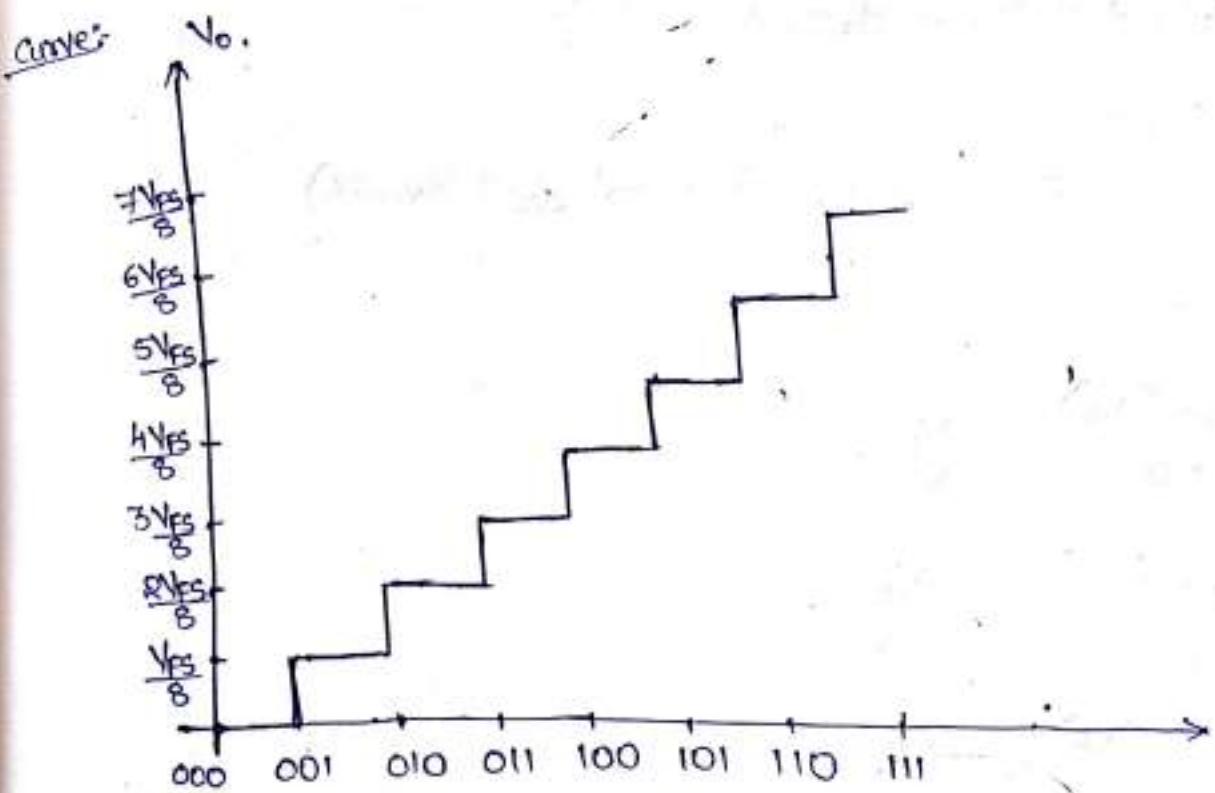


$$\therefore V_0 = K V_{FS} (b_1 \bar{2}^1 + b_2 \bar{2}^2 + b_3 \bar{2}^3)$$

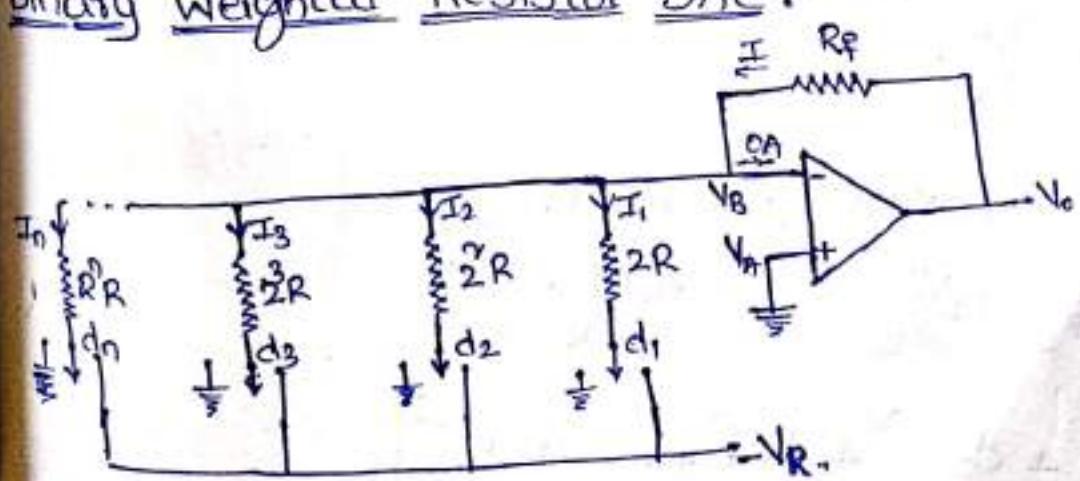
Let $K=1$

$$V_0 = V_{FS} (b_1 \bar{2}^1 + b_2 \bar{2}^2 + b_3 \bar{2}^3)$$

b_1	b_2	b_3	V_o
0	0	0	0
0	0	1	$\frac{V_{FS}}{8}$
0	1	0	$\frac{V_{FS}}{4} = \frac{2V_{FS}}{8}$
0	1	1	$\frac{3V_{FS}}{8}$
1	0	0	$\frac{4V_{FS}}{8}$
1	0	1	$\frac{5V_{FS}}{8}$
1	1	0	$\frac{6V_{FS}}{8}$
1	1	1	$\frac{7V_{FS}}{8}$



Binary Weighted Resistor DAC :-



- * The above figure a binary weighted DAC circuit consists of an inverting summing amplifiers with binary weighted resistor network.
- * It has electronic switches $d_1, d_2, d_3, \dots, d_n$, which are controlled by the input digital code. These switches are OPST type.
- * If the code corresponding to a switch is one, it connects the resistor to the reference voltage $-V_R$.
- * If the code corresponding to a switch is zero, the switch connects the resistor to $0V(GND)$.

\therefore The total current I can be written as

$$I = d_1 I_1 + d_2 I_2 + d_3 I_3 + \dots + d_n I_n \quad \text{---(1)}$$

From the circuit

$$V_A = 0, \text{ But } V_A = V_B \text{ (virtual short circuit)}$$

$$\therefore V_B = 0$$

$$I_1 = \frac{V_B - (-V_R)}{2R} = \frac{V_R}{2R}$$

$$I_2 = \frac{V_B - (-V_R)}{2^2 R} = \frac{V_R}{2^2 R}$$

$$I_3 = \frac{V_B - (-V_R)}{2^3 R} = \frac{V_R}{2^3 R}$$

$$\therefore I = \frac{V_B - V_B}{R_F} = \frac{V_B}{R_F}$$

\therefore substituting the above values in (1).

$$\frac{V_B}{R_F} = d_1 \frac{V_R}{2R} + d_2 \frac{V_R}{2^2 R} + d_3 \frac{V_R}{2^3 R} + \dots + d_n \frac{V_R}{2^n R}$$

$$\frac{V_B}{R_F} = \frac{V_R}{R} \left[d_1 \frac{1}{2} + d_2 \frac{1}{2^2} + d_3 \frac{1}{2^3} + \dots + d_n \frac{1}{2^n} \right]$$

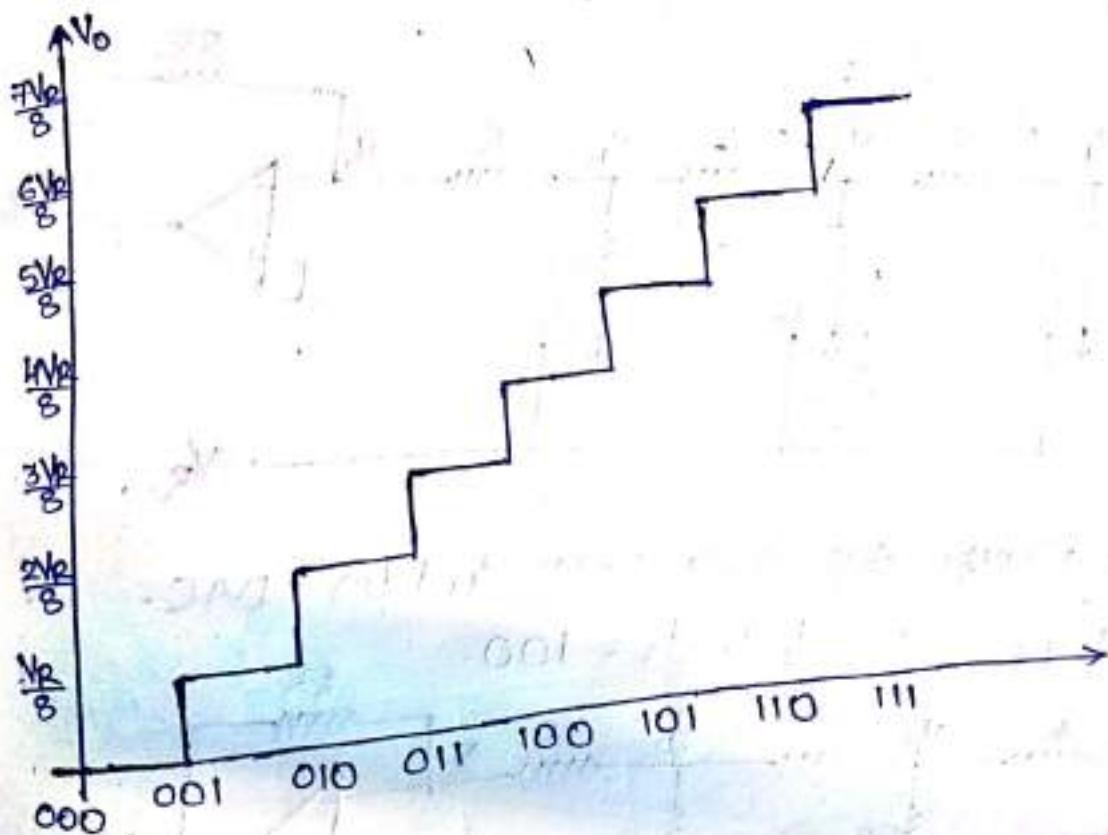
$$V_o = \left(\frac{R_F}{R}\right) (V_R) [d_1 2^1 + d_2 2^2 + d_3 2^3 + \dots + d_n 2^n].$$

∴ the above equation is general equation of n bit DAC.
If we take a 3 bit DAC, then the output voltage for various input ports is given by. $V_o = \left(\frac{R_F}{R}\right) V_R [d_1 2^1 + d_2 2^2 + d_3 2^3]$.

d_1	d_2	d_3	V_o
0	0	0	0
0	0	1	$V_R/8$
0	1	0	$2V_R/8$
0	1	1	$3V_R/8$
1	0	0	$4V_R/8$
1	0	1	$5V_R/8$
1	1	0	$6V_R/8$
1	1	1	$7V_R/8$

Let $R_F = R$.
 $V_o = V_R (d_1 2^1 + d_2 2^2 + d_3 2^3)$

The transfer curve is given as.

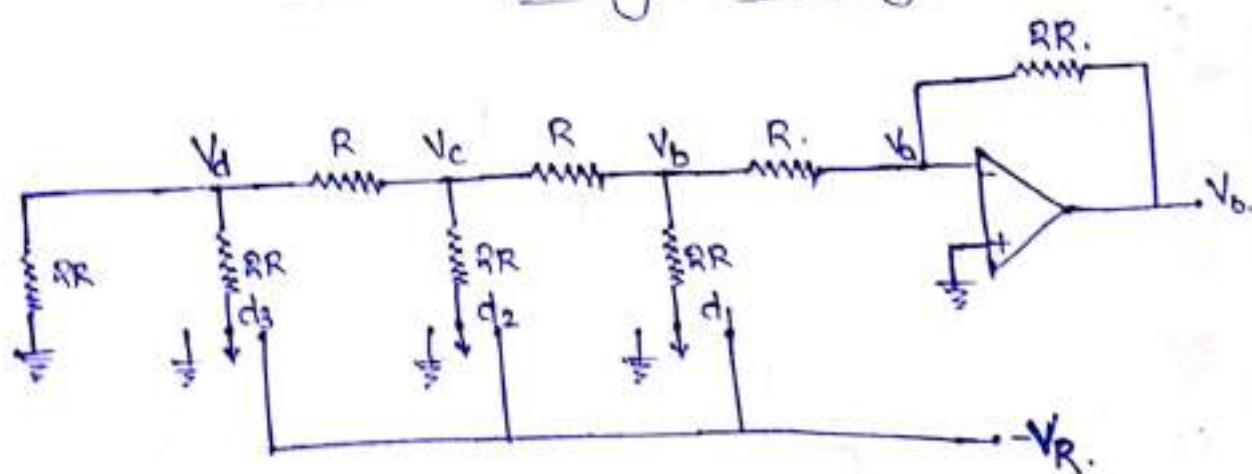


Refresher
Monday

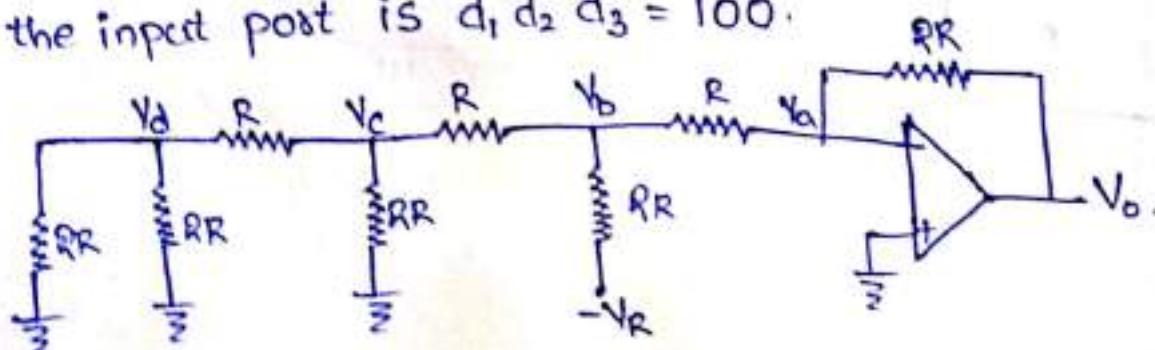
Disadvantages of Binary weighted DAC:

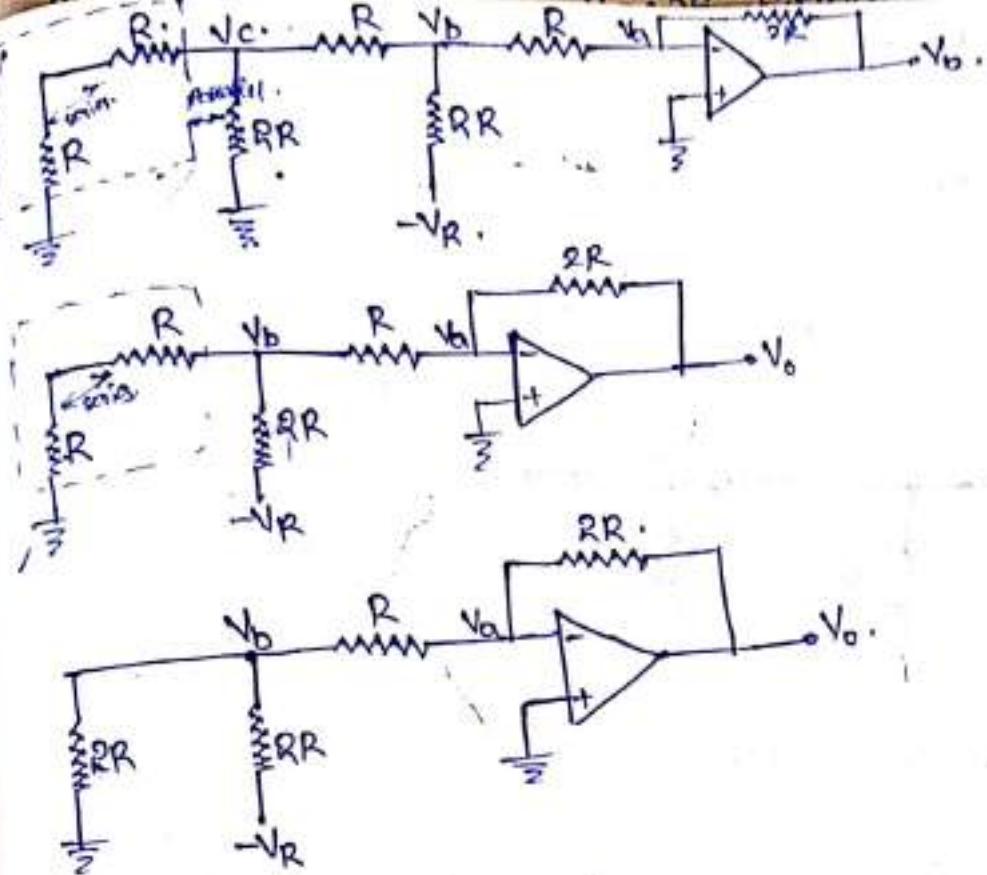
- * As the number of input bits increases, the size of the required resistors increases.
- For a 12 bit DAC biggest resistor required is 2^R , which is very large.
- Large resistor occupies large chip area. Hence it is not economical.
- * If the particular bit is alternatively change between 0 and 1. The current through the particular resistor has to change between 0Amp - $\frac{V_R}{2^R}$ amp. This sudden change in current may cause IR loss, excessive heat in the chip.

R-2R Ladder DAC (Voltage steering DAC):



The above figure shows a R-2R ladder DAC.
Let the input port is $d_1, d_2, d_3 = 100$.





$$V_{A'} = 0 \text{ (virtual ground)}$$

Writing KCL at node B.

$$\frac{V_b}{RR} + \frac{V_b - (-V_R)}{RR} + \frac{V_b - V_A}{R} = 0.$$

$$\frac{V_b}{RR} + \frac{V_b + V_R}{RR} + \frac{V_b}{R} = 0.$$

$$\frac{V_b + V_b + V_R + 2V_b}{RR} = 0.$$

$$4V_b + V_R = 0 \Rightarrow 4V_b = -V_R$$

$$V_b = -\frac{V_R}{4} \rightarrow \textcircled{1}$$

Writing KCL at node A.

$$\frac{V_a - V_b}{R} + \frac{V_a - V_o}{RR} = 0$$

$$-\frac{V_b}{R} - \frac{V_o}{RR} = 0 \Rightarrow \frac{-2V_b - V_o}{2R} = 0,$$

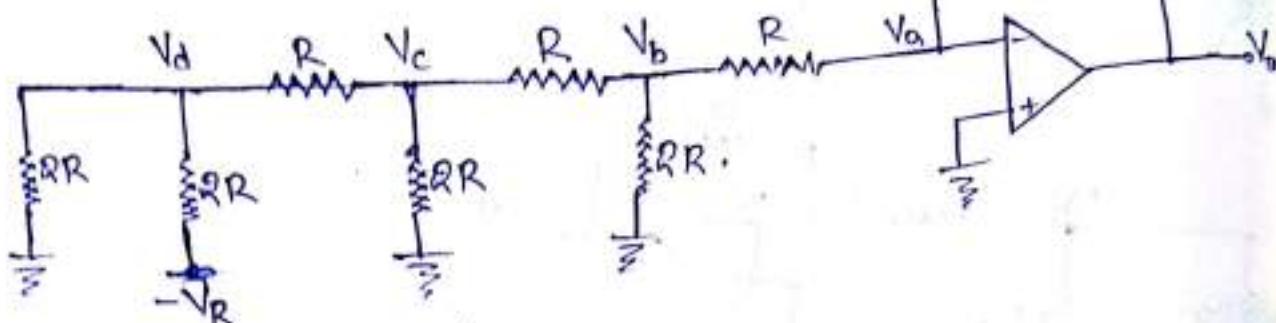
$$\Rightarrow -2V_b - V_o = 0.$$

$$V_o = -2V_b \rightarrow \textcircled{2}.$$

$$V_o = -2 \times \left(\frac{-V_R}{R} \right) = \frac{V_R}{R} .$$

$$\therefore V_o = \frac{V_R}{R} = \frac{4VR}{8} .$$

The input code is $d_1 d_2 d_3 = 001$



By applying KCL at node A.

$$\frac{V_a - V_b}{R} + \frac{V_a - V_o}{2R} = 0 .$$

But $V_a = 0$ (virtual ground)

$$-\frac{V_b}{R} - \frac{V_o}{2R} = 0$$

$$-2V_b - V_o = 0$$

$$V_o = -2V_b .$$

$$V_b = -\frac{V_o}{2} \rightarrow ③$$

By applying KCL at node B.

$$\frac{V_b - V_a}{R} + \frac{V_b - V_c}{R} + \frac{V_b - 0}{2R} = 0 .$$

$$\text{But } V_a = 0$$

$$\frac{V_b}{R} + \frac{V_b - V_c}{R} + \frac{V_b - 0}{2R} = 0$$

$$2V_b + 2V_b - 2V_c + V_b = 0 .$$

$$5V_b - 2V_c = 0$$

$$5V_b = 2V_c .$$

$$V_c = \frac{5}{2}V_b .$$

$$V_C = \frac{5}{8} * \left(-\frac{V_O}{R}\right)$$

$$V_C = -\frac{5V_O}{4} \longrightarrow \textcircled{4}$$

By applying KCL at node C.

$$\frac{V_C - V_B}{R} + \frac{V_C - 0}{2R} + \frac{V_C - V_D}{R} = 0$$

$$2V_C - 2V_B + V_C + 2V_C - 2V_D = 0$$

$$5V_C - 2V_B - 2V_D = 0$$

$$5\left(-\frac{5V_O}{4}\right) - 2\left(-\frac{V_O}{R}\right) - 2V_D = 0$$

$$-\frac{25V_O}{4} + V_O - 2V_D = 0$$

$$-25V_O + 4V_O - 8V_D = 0$$

$$8V_D = -21V_O$$

$$V_D = -\frac{21}{8}V_O \longrightarrow \textcircled{5}$$

By applying KCL at node D.

$$\frac{V_D - V_C}{R} + \frac{V_D - (-V_R)}{2R} + \frac{V_D - 0}{2R} = 0$$

$$\frac{V_D - V_C}{R} + \frac{V_D + V_R}{2R} + \frac{V_D}{2R} = 0$$

$$2V_D - 2V_C + V_D + V_R + V_D = 0$$

$$4V_D - 2V_C + V_R = 0$$

$$4\left(-\frac{21}{8}V_O\right) - 2\left(-\frac{5}{4}V_O\right) + V_R = 0$$

$$-\frac{21}{8}V_O + \frac{5}{2}V_O + V_R = 0$$

$$-2V_O + 5V_O + 2V_R = 0$$

$$-16V_O + 2V_R = 0$$

$$16V_O = 2V_R$$

$$V_O = \frac{2V_R}{16}$$

$$\boxed{V_O = \frac{V_R}{8}}$$

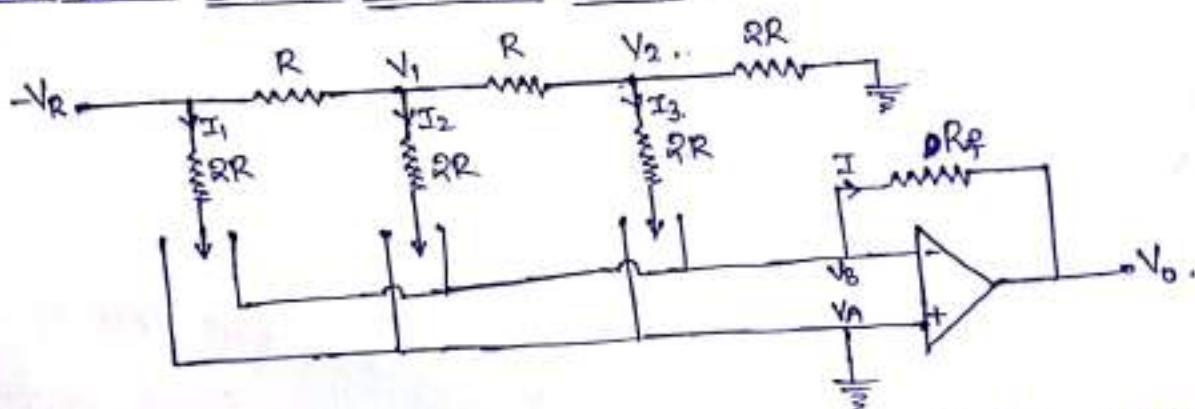
Similarly we get the following outputs for other combinations

$d_1 \ d_2 \ d_3$	V_o
0 0 0	0
0 0 1	$\frac{VR}{8}$
0 1 0	$\frac{2VR}{8}$
0 1 1	$\frac{3VR}{8}$
1 0 0	$\frac{4VR}{8}$
1 0 1	$\frac{5VR}{8}$
1 1 0	$\frac{6VR}{8}$
1 1 1	$\frac{7VR}{8}$

07/08/19
Tuesday.

→

Inverted R-2R ladder DAC:

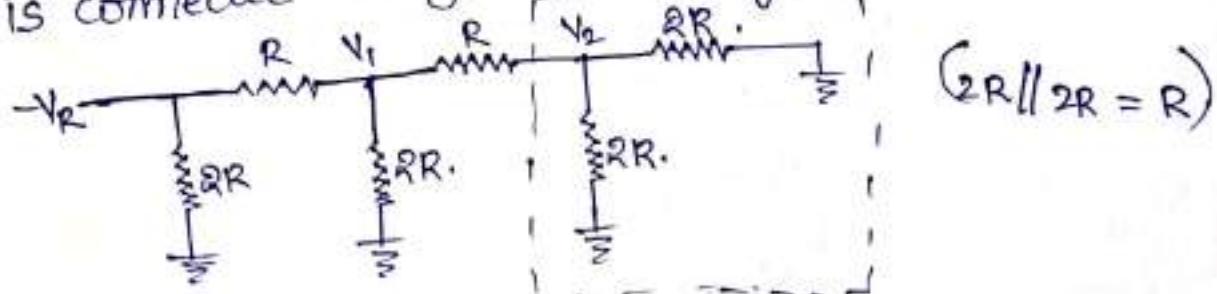


The above figure shows a inverted R-2R ladder DAC.

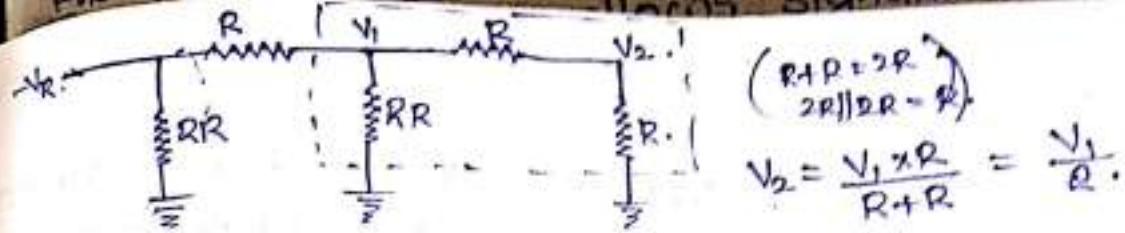
$$V_A = 0$$

$\therefore V_B = 0$ (virtual Ground)

Irrespective of whether a bit is zero or one the switch is connected to ground always.

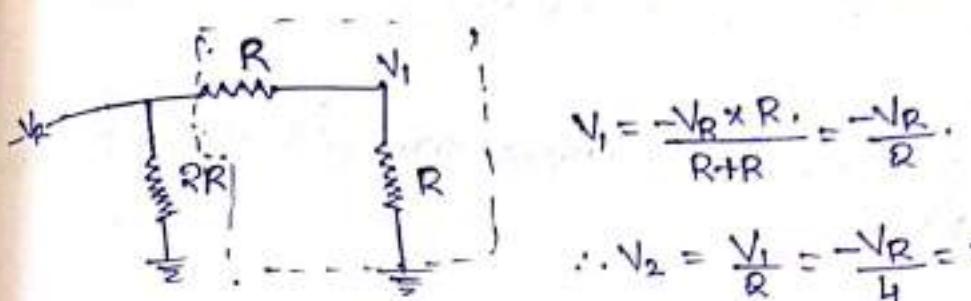


$$(2R \parallel 2R = R)$$



$$(R+R=2R)$$

$$V_2 = \frac{V_1 \times R}{R+R} = \frac{V_1}{2}$$



$$(R+R=2R)$$

$$V_1 = \frac{-V_R \times R}{R+R} = -\frac{V_R}{2}$$

$$\therefore V_2 = \frac{V_1}{2} = -\frac{V_R}{4} = -\frac{V_R}{2^2}$$

The current I_1 is

$$I_1 = \frac{-V_R - 0}{RR} = \frac{-V_R}{RR}$$

$$I_2 = \frac{V_1 - 0}{2R} = \frac{V_1}{RR} = \frac{(-V_R/2)}{2R} = \frac{-V_R}{2^2 R}$$

$$I_3 = \frac{V_2 - 0}{RR} = \frac{V_2}{RR} = \frac{(-V_R/2^2)}{2R} = \frac{-V_R}{2^3 R}$$

$$I = \frac{V_B - V_0}{R_F} = \frac{V_0}{R_F}$$

From figure

$$I = d_1 I_1 + d_2 I_2 + d_3 I_3$$

$$\frac{-V_0}{R_F} = d_1 \left(\frac{-V_R}{RR} \right) + d_2 \left(\frac{-V_R}{2^2 R} \right) + d_3 \left(\frac{-V_R}{2^3 R} \right)$$

$$V_0 = \frac{R_F}{R} \left(V_R \frac{d_1}{2} + V_R \frac{d_2}{2^2} + V_R \frac{d_3}{2^3} \right)$$

$$V_0 = \left(\frac{R_F}{R} \right) V_R \left(d_1 \cdot 2^{-1} + d_2 \cdot 2^{-2} + d_3 \cdot 2^{-3} \right)$$



18/08/2019
Wednesday

IC1408 DAC :-

IC1408 is an 8 bit R-2R ladder DAC, which is compatible with TTL and CMOS logic. It provides high speed performance with low cost.

* Important specifications of IC1408 are (Electrical characteristics of IC1408)

1. Reference current = 2mA .
2. Supply voltage $\Rightarrow V_{cc} = 5\text{V}$ & $V_{EE} = -15\text{V}$
3. Full scale output current = 1.992mA .
4. Output voltage swing = $+5\text{V}$ to -5V .
5. Multiplying speed = $4\text{mA}/\mu\text{sec}$.

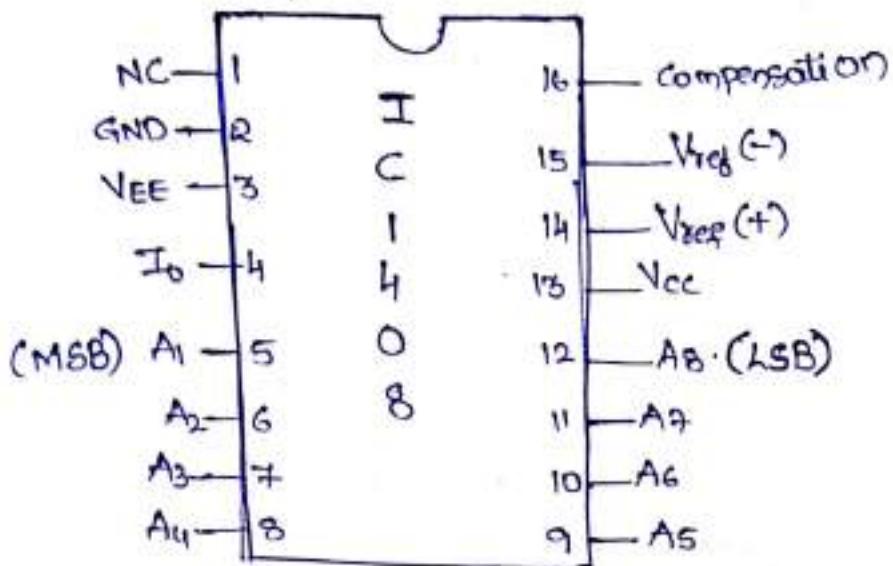
6. Accuracy = 0.19%

7. Settling time = 300nsec .

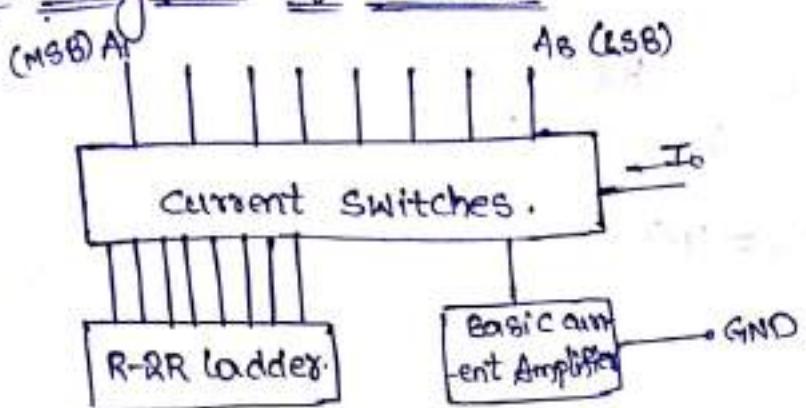
Applications of IC1408 :-

1. Tracking ADC's.
2. Digital panel meters.
3. Digital volt meters.
4. Waveform synthesizing circuits.
5. Sample & hold & peak detector circuits.
6. Arduino
6. Audio digitizing and decoding circuits.
7. Programmable power supplies.
8. Analog & digital arithmetic operations.

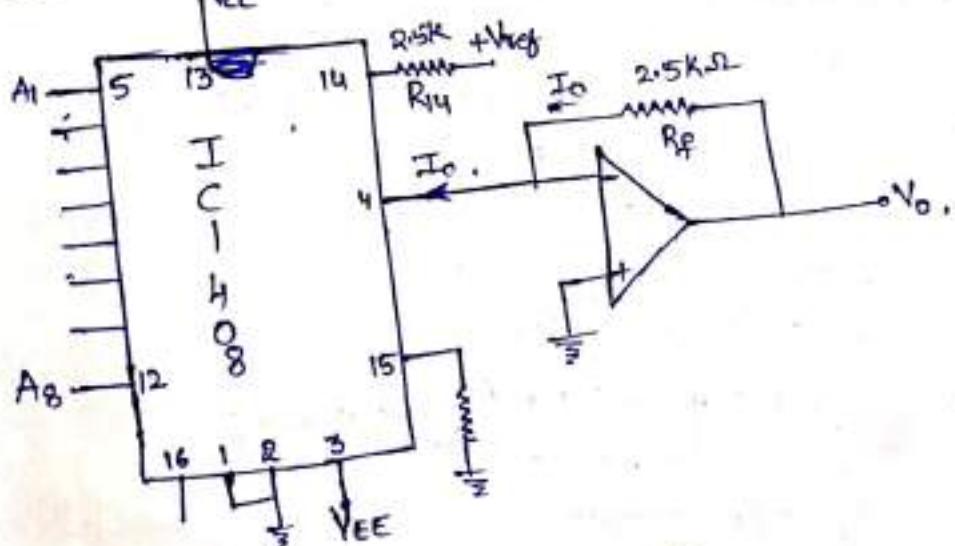
IC1408 Pin diagram :-



Block diagram of IC1408 :-



Typical circuit of a DAC using IC1408 :-



$$I_o = \frac{V_{ref}}{R_{14}} \left(\frac{A_1}{2^1} + \frac{A_2}{2^2} + \dots + \frac{A_8}{2^8} \right)$$

This is the maximum output current of DAC
dependent on maximum digital input

when all switches are closed

$$A_1 = A_2 = \dots = A_8 = 1.$$

$$\therefore I_o = \frac{V_{ref}}{2.5k} \left(\frac{1}{2} + \frac{1}{2^2} + \frac{1}{2^3} + \dots + \frac{1}{2^5} \right)$$

$$I_o = \frac{V_{ref}}{2.5k} \left(\frac{255}{256} \right)$$

$$= \frac{+5V}{2.5k} \cdot \frac{255}{256}$$

$$I_o = 1.992 \text{ mA.} \quad (\text{When } V_{ref} = +5V)$$

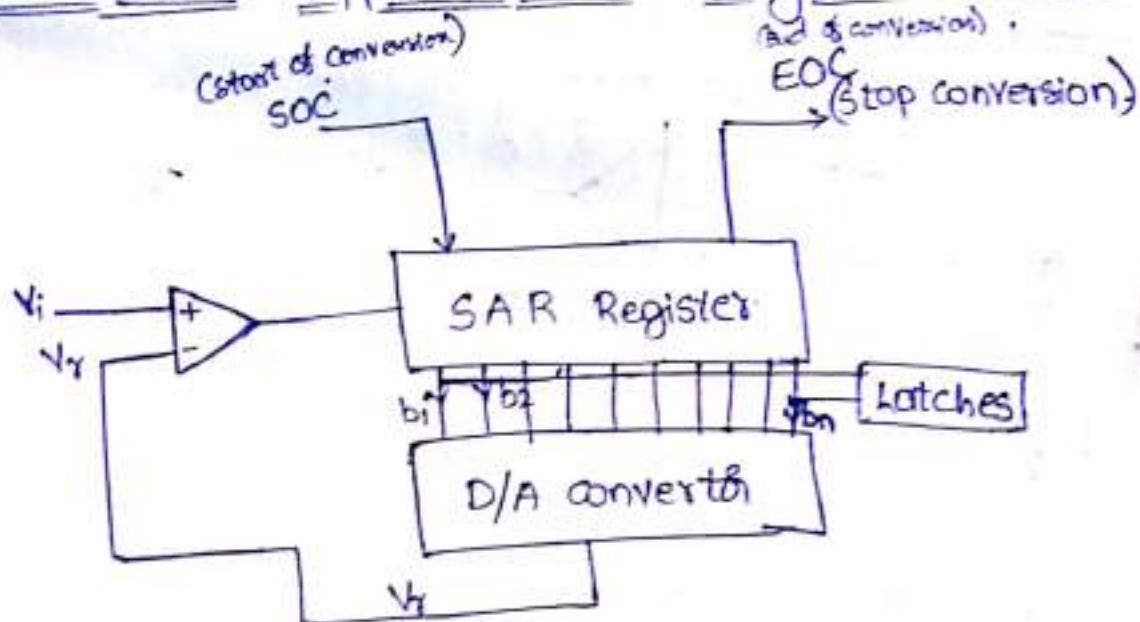
From the op-Amp

$$I_o = \frac{V_o - 0}{R_F} \Rightarrow V_o = I_o R_F \\ \Rightarrow V_o = (1.992 \text{ mA}) (2.5k) \\ \Rightarrow V_o = 4.98 \text{ V.}$$

zobosha
Friday

Analog to Digital converter (ADC) :-

Successive Approximation Register ADC (SAR ADC)

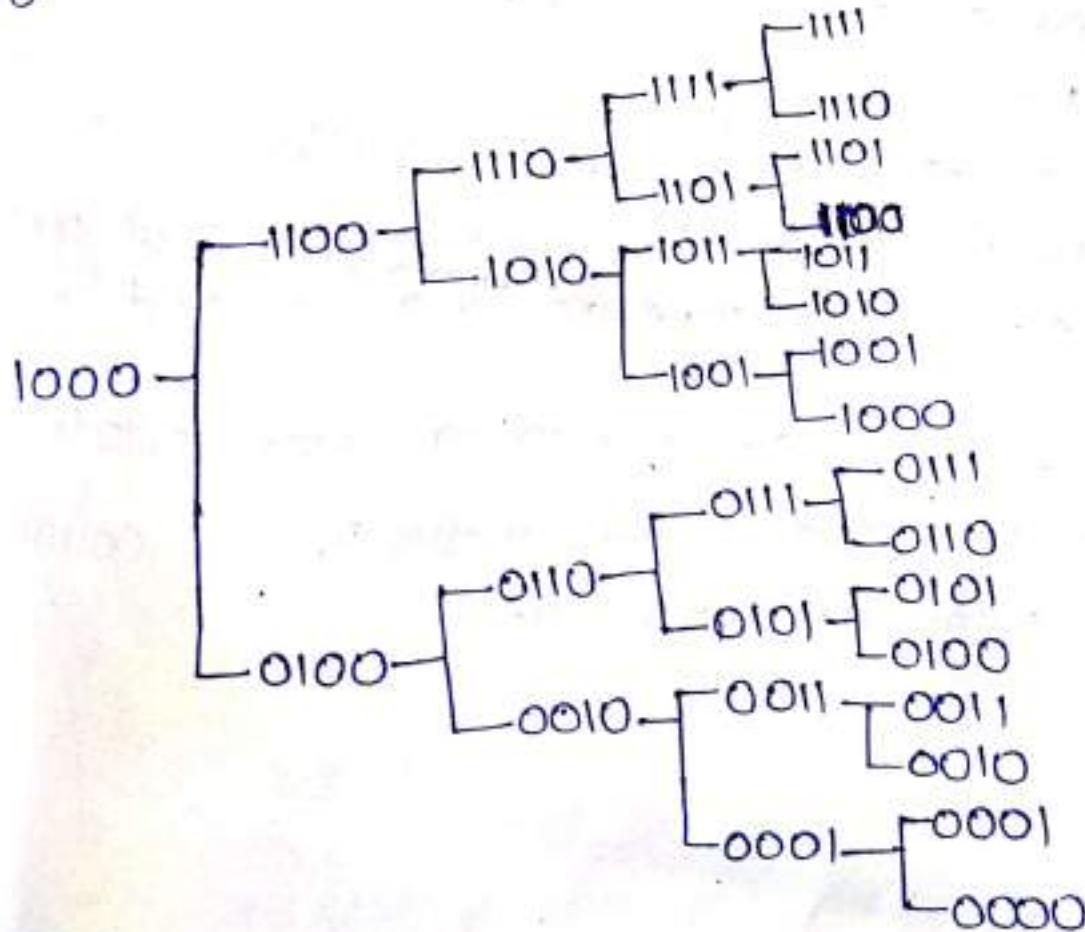


The above figure shows the block diagram of SAR ADC. In this ADC, the conversion time depends upon no. of bits.

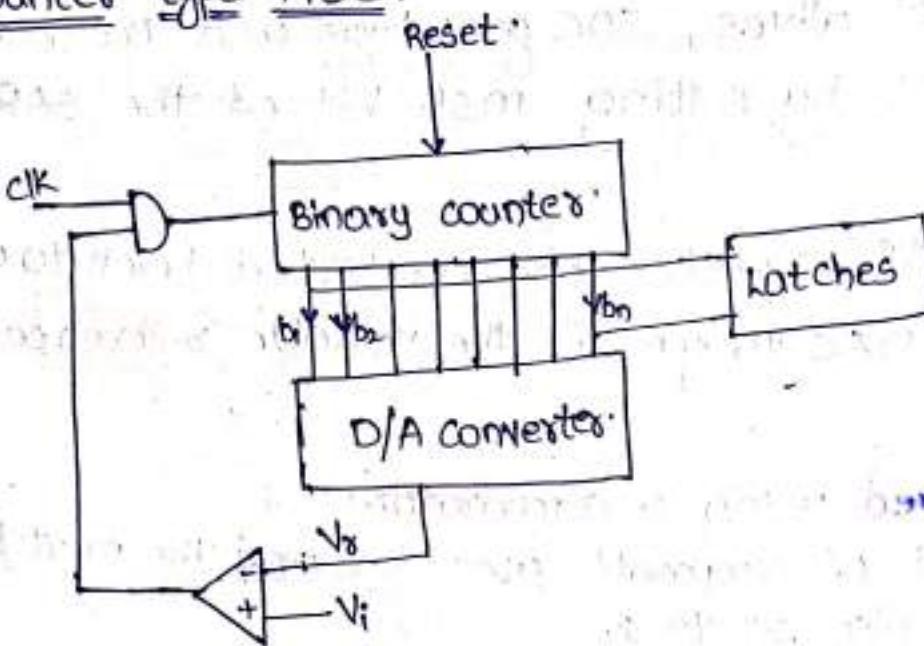
For n bits SAR ADC, the conversion time is n clock pulses.
When input signal arrives, SOC goes high and the conversion process begins by setting msb bit of the SAR register to 1.

- ② contents of SAR register are converted back to an analog signal by DAC to generate the variable reference signal V_r .
- ③ V_i, V_r are compared using a comparator.
- ④ If $V_i > V_r$, output of comparator goes high and the next bit of SAR Register is also set to 1.
- ⑤ If $V_i < V_r$, the previous bit which is set to '1' is made '0' and the next bit of the SAR register is set to '1'.
- ⑥ This process is repeated for n clock cycles.

At the end of n^{th} clock cycle, whatever is present in the SAR Register is taken as the final code.



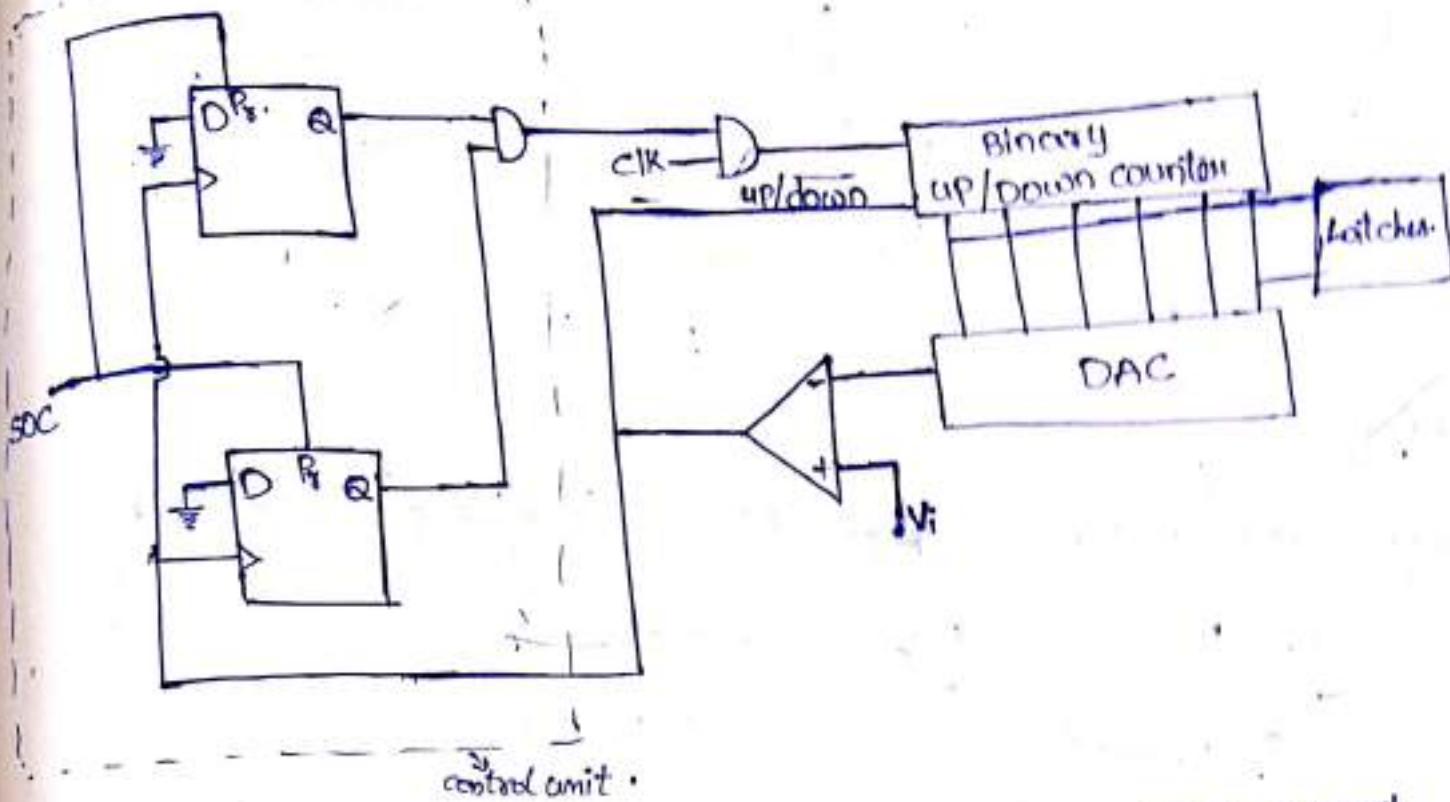
counter type ADC:-



- * The above figure shows a counter type ADC. consists of a binary counter, DAC and a comparator.
- * When input signal is arrived, the counter is reset to zero.
- * The output bits of the counter are inputs to the DAC and the DAC output is compared with input signal (V_i).
- * If $V_i > V_R$, comparator output is high and clock is applied to the binary counter, and binary counter increases its count by 1 bit.
- * This process is repeated until $V_i < V_R$.
- * As soon as V_i is less than V_R , comparator output goes low and the binary counter stops receiving clock and conversion ends.
- * The contents of binary counter are copied into latches.
- * As soon as the next sample arrives, the counter is reset and same cycle repeats.

>

~~Saturday~~
Tracking ADC:



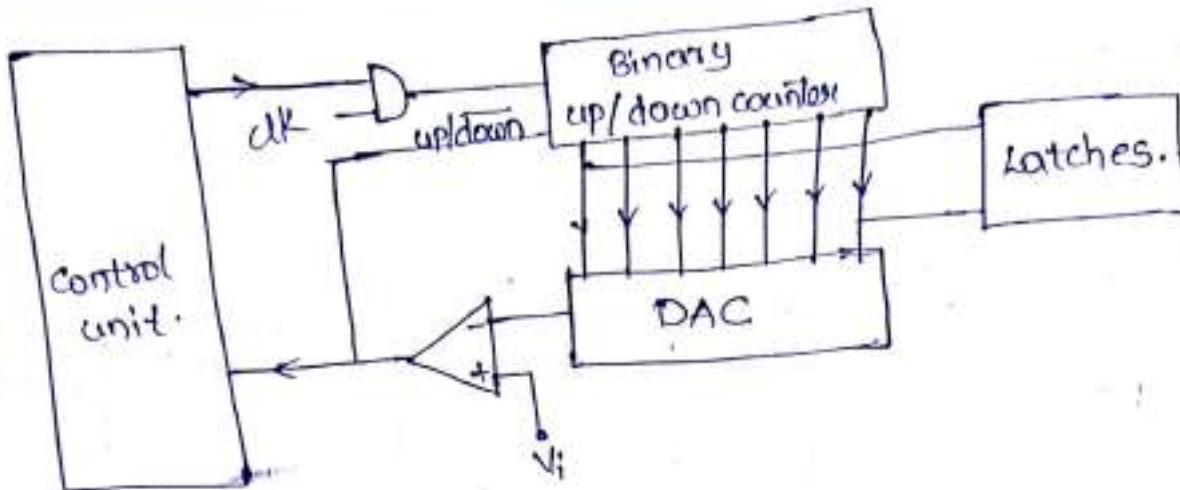
Tracking ADC is same as a counter type ADC except that the counter is up/down counter. In tracking ADC whenever a new sample appears the counter is reset to zero. the counting begins from all zeros.

* But in tracking ADC whenever a new sample appears , the counter begins to count from the previous count.

* If the present sample is more than the previous sample, counter counts upwards.

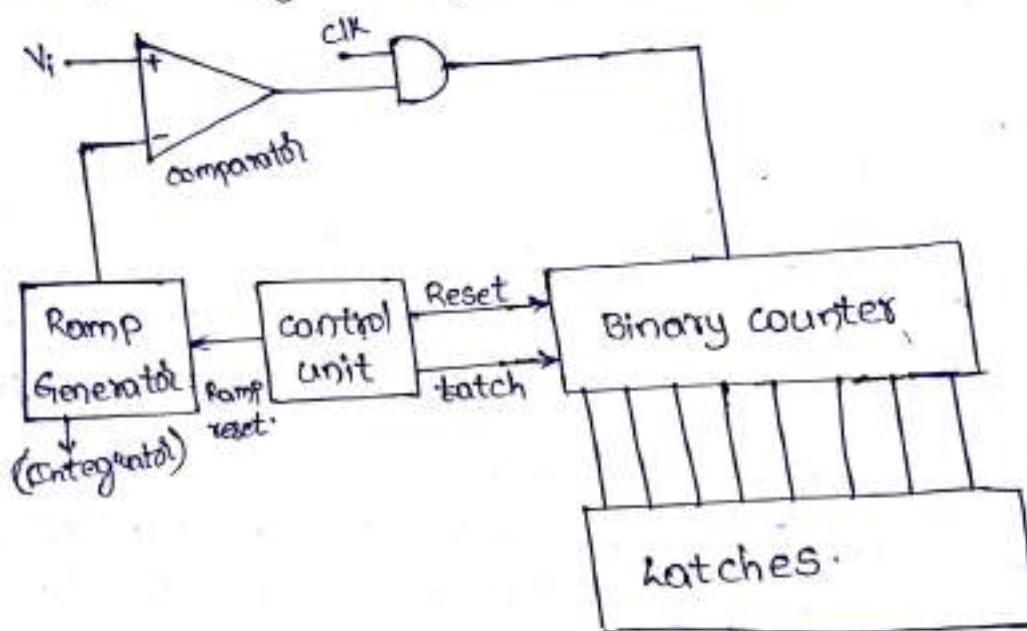
* If present sample is less than the previous sample the counter counts downwards.

* The conversion time of tracking ADC is much less compared to the counted type ADC.



03/09/19
Tuesday

single slope Integrator type ADC & single slope ADC:



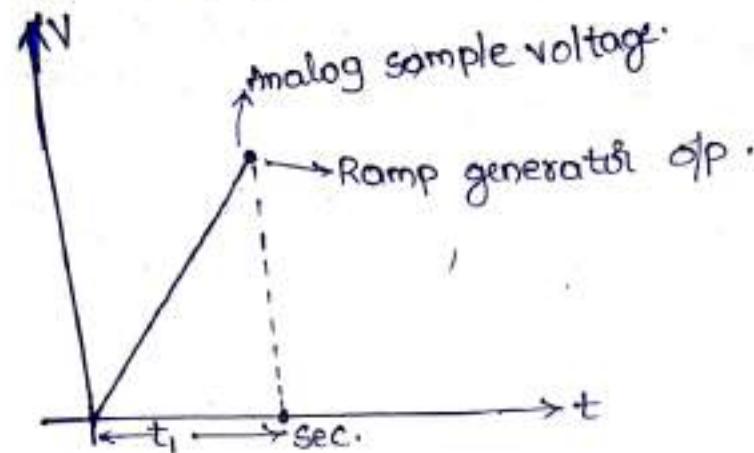
The above figure shows a single slope ~~integrator~~^{type} ADC. It consists of a binary counter, a ramp generator (Integrated), a comparator, a control unit and latches.

When a sample appears, the binary counter starts with all zeros, the ramp generator starts generating a ramp signal, and the output of the ramp generator is compared with the input sample V_i .

As long as $V_i > V_r$, the ramp generator continues to generate the ramp signal and the counter continues

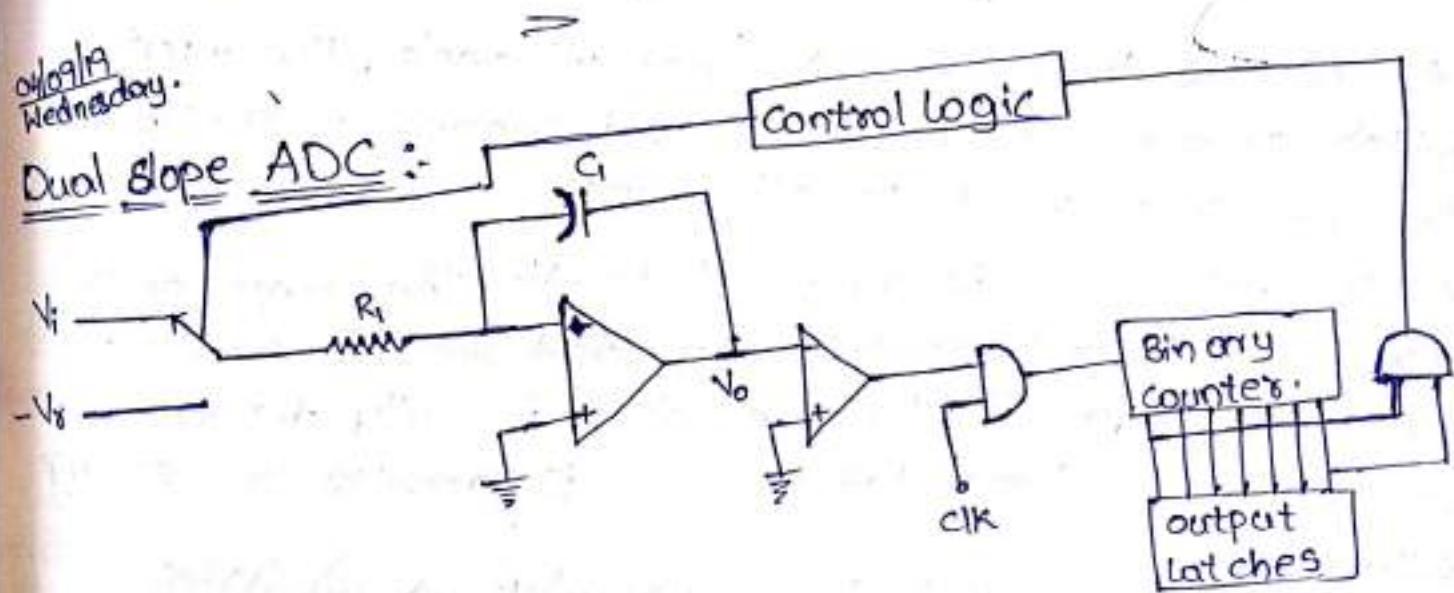
to count upwards.

As soon as the ramp output exceeds V_i , the comparator output goes low and the counter stops, and the count is copied into latches, and the ramp generator and the binary counter are reset. The same cycle is repeated for next sample.



$T \rightarrow$ time period of the clock.

$$\text{Digital count in the counter} = \frac{t_1 \text{ sec}}{T \text{ sec}}$$



The above figure shows a dual slope integrating type ADC.

It consists of integrator, binary counter, latches, comparator and a control unit that controls the input switch.

- * Initially the binary counter is reset to all zero's.
 - * When an input sample v_i arrives, the input switch is connected to v_i , and the capacitor C_1 begins to charge.
- The switch v_i
- At the same time the counter begins to count.
- * The switch is kept at v_i till the binary counter shows all ones. At this point the output voltage of the integrator is given by v_o (t_1 is the time taken for counter to reach all ones)

$$V_o = - \int_{0}^{t_1} \frac{1}{R_1 C_1} v_i dt$$

$$V_o = - \frac{1}{R_1 C_1} v_i \int_0^t dt$$

$$V_o(t_1) = - \frac{v_i t_1}{R_1 C_1}$$

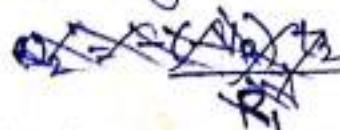
- * The total charge deposited on the capacitor during t_1 is

$$Q_1 = C_1 V_o = - \frac{v_i t_1}{R_1 C_1} \times C_1 = - \frac{v_i t_1}{R_1}$$

- * As soon as the counter reaches all one's, the input switch changes its position and connected to $-V_R$ and the counter is reset to all zeros.

- * As the integrator is connected to $-V_R$, the charge on the capacitor C_1 begins to discharge and simultaneously counter starts counting till the capacitor is fully discharged. Let t_2 be the time taken for this capacitor to discharge fully.

The total charge discharged during t_2 is given by.



During the period from t_1 to t_2 V_o is given by

$$V_o = - \int_{t_1}^{t_2} \frac{1}{R_1 C_1} (-V_R) dt + V_o(t_1)$$

$$V_o = \frac{1}{R_1 C_1} V_R (t_2 - t_1) + V_o(t_1)$$

$$V_o = \frac{V_R(T)}{R_1 C_1} + V_o(t_1)$$

$$V_o = \frac{1}{R_1 C_1} V_R(T) - \frac{V_i t_1}{R_1 C_1}$$

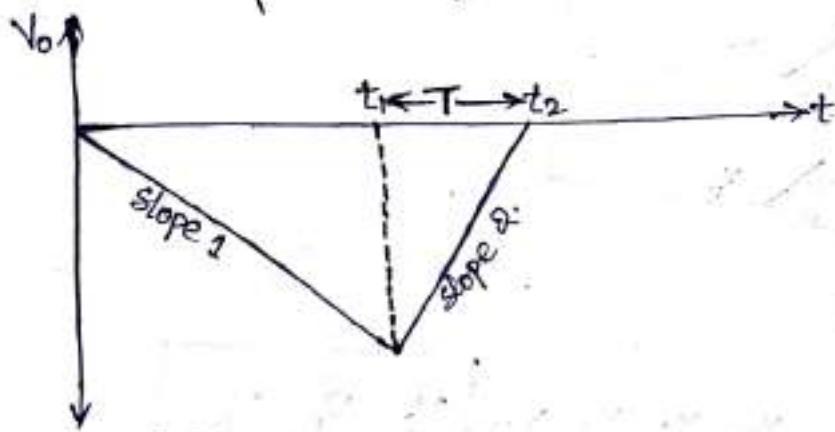
At t_2 $V_o = 0$

$$0 = \frac{V_R T}{R_1 C_1} - \frac{V_i t_1}{R_1 C_1}$$

$$V_R T = V_i t_1$$

$$T = \frac{V_i t_1}{V_R}$$

$$\text{Digital count} = \left(\frac{T}{\text{clock period}} \right)$$



Advantages :-

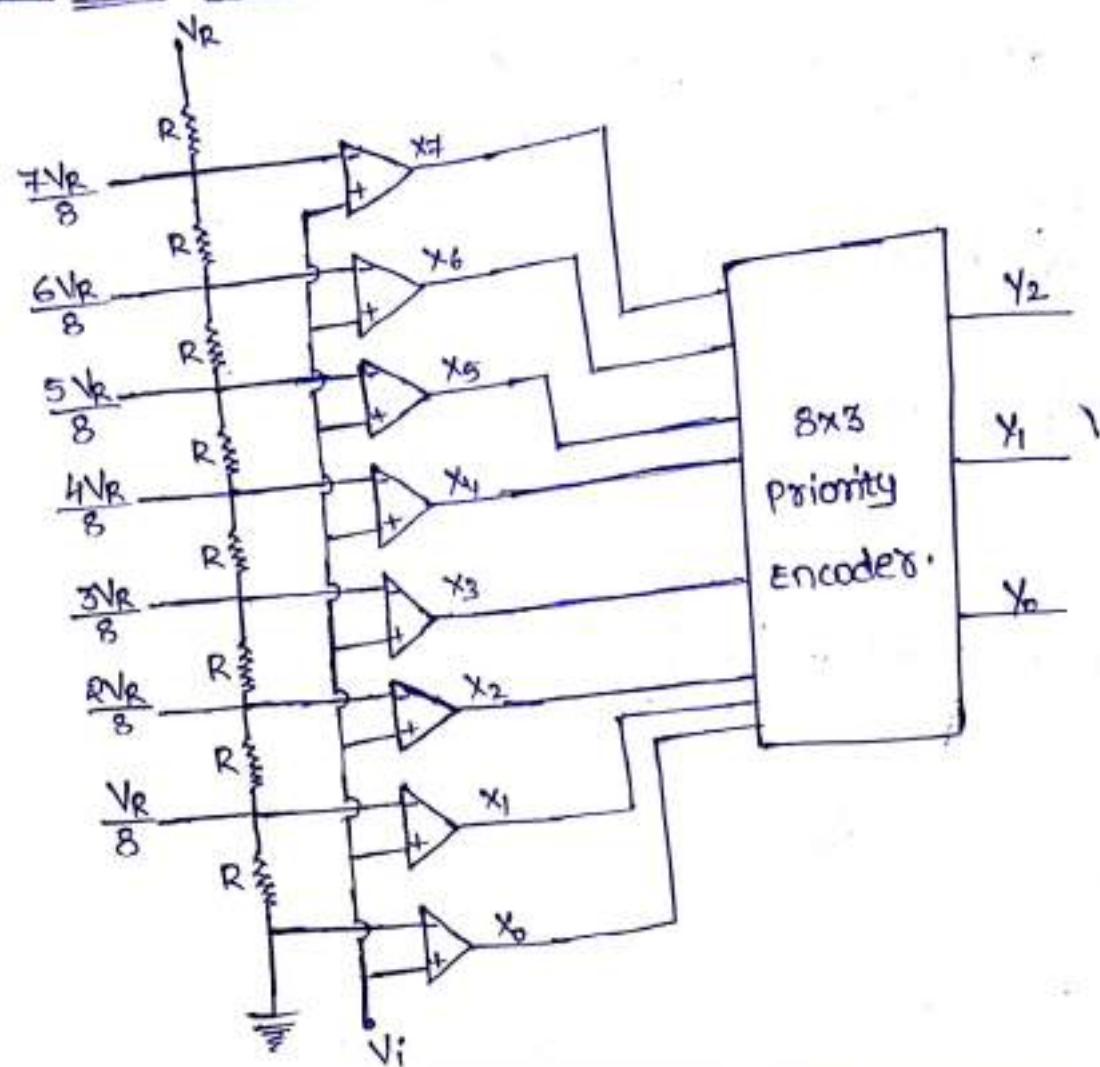
- * It is highly accurate.
- * Its cost is low.
- * It is immune to temperature effects on R, & C.



05/09/19

Thursday.

Flash ADC (8i) parallel comparator ADC :-



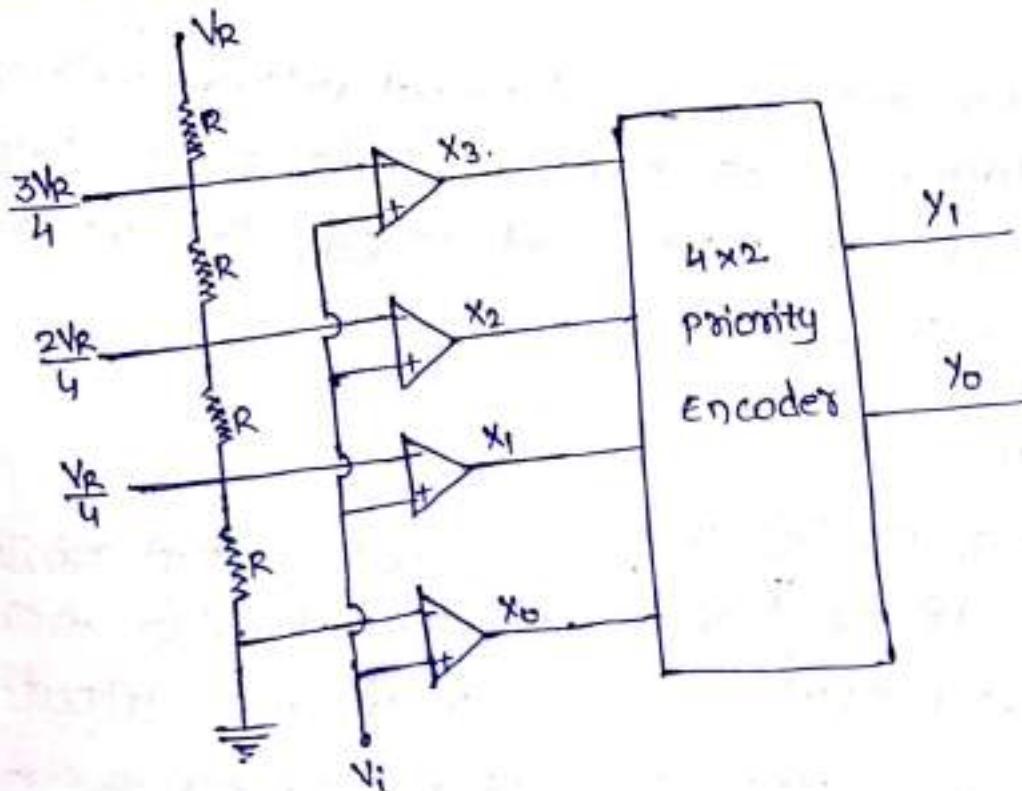
V_i	X_7	X_6	X_5	X_4	X_3	X_2	X_1	X_0	Y_2	Y_1	Y_0
$V_i < 0$	0	0	0	0	0	0	0	0	x	x	x
$0 < V_i < \frac{V_R}{8}$	0	0	0	0	0	0	0	1	0	0	0
$\frac{V_R}{8} < V_i < \frac{2V_R}{8}$	0	0	0	0	0	0	1	1	0	0	1
$\frac{2V_R}{8} < V_i < \frac{3V_R}{8}$	0	0	0	0	0	1	1	1	0	1	0
$\frac{3V_R}{8} < V_i < \frac{4V_R}{8}$	0	0	0	0	1	1	1	1	0	1	1
$\frac{4V_R}{8} < V_i < \frac{5V_R}{8}$	0	0	0	1	1	1	1	1	1	0	0
$\frac{5V_R}{8} < V_i < \frac{6V_R}{8}$	0	0	1	1	1	1	1	1	1	0	1
$\frac{6V_R}{8} < V_i < \frac{7V_R}{8}$	0	1	1	1	1	1	1	1	1	1	0
$\frac{7V_R}{8} < V_i < V_R$	1	1	1	1	1	1	1	1	1	1	1

- * The above figure shows a 3-bit flash ADC. An n bit flash ADC will have 2^n comparators.
- * Each non-inverting input of each comparator is connected to V_i .
- * The inverting input of comparator is connected to potential divider.
- * Depending upon the node at which the comparator is connected, the inverting terminals of the comparator will have a reference voltage between 0 & $\frac{7V_R}{8}$.
- * When the input sample V_i appears, the various comparator outputs are as follows depending upon the V_i as shown in table.
- * The comparator outputs are given to an encoder, which converts them into a binary code.

Disadvantages:

- * It requires more number of comparators when the bit size increases.

2-bit Flash ADC :-



V_i	x_3	x_2	x_1	x_0	y_1	y_0
$0 < V_i < \frac{V_R}{4}$	0	0	0	1	0	0
$\frac{V_R}{4} < V_i < \frac{2V_R}{4}$	0	0	1	1	0	1
$\frac{2V_R}{4} < V_i < \frac{3V_R}{4}$	0	1	1	1	1	0
$\frac{3V_R}{4} < V_i < V_R$	1	1	1	1	1	1

06/09/19
Friday.



Performance specifications of DAC & ADC:

Resolution:

It is defined as the change in the analog voltage which results from the change of one LSB in the digital signal.

$$\text{Resolution} = \frac{V_{FS}}{2^n}$$



Accuracy:

It is a comparison of actual output voltage with respected output voltage. It is expressed in percentage. In the most common DAC and ADC's, the accuracy shall be within \pm half LSB.

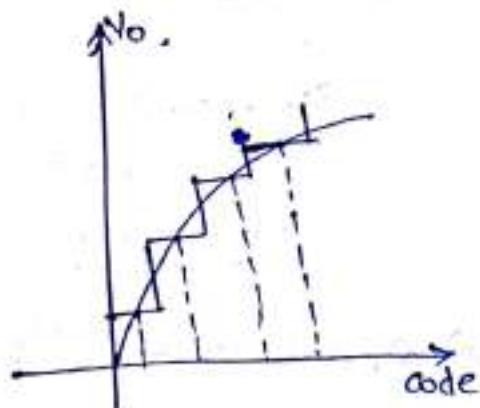
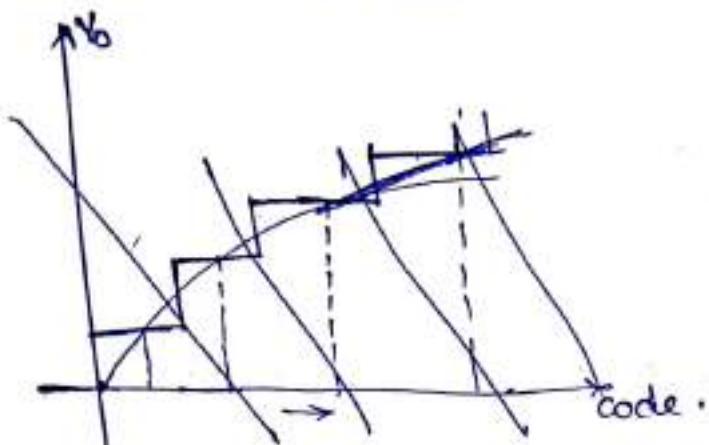


Monotonicity:-

Monotonicity indicates that the input, output relationship is such that if input increases, output also increases and for every input there is a unique output.

For a DAC, the input code is increasing, the output analog voltage also increases. No two codes should result in the same output voltage.

For an ADC, if input voltage is increasing the output code should increase. No two samples with different voltage should have the same code.



Converting time:

It is the time required for converting analog voltage into digital code by the ~~SN74LS18~~ ADC.

It is the time required for converting the digital code into analog voltage by DAC.

Settling time:

It is the time required for DAC or ADC for the output to settle within \pm half LSB of the final value.

Quantisation Error:

It is the difference between the actual voltage of the sample and its quantized level. The quantisation error should always be within \pm half LSB.

Problem:

A 8 bit ADC, outputs all ones. when $V_i = 5.1V$

a) Find its Resolution

b) Find the digital output when $V_i = 1.28V$.

A. 8bit

$$V_i = 5.1V \quad 1111111$$

$$\frac{255}{256} V_R = 5.1$$

$$V_R = \frac{5.1 \times 256}{255}$$

$$V_R = 5.12V$$

a) Resolution = $\frac{V_R}{2^n} = \frac{5.12}{2^8} = 0.02 = 20mV$

b) when input voltage is 1.28V

$$\text{Digital count} = \frac{1.28}{20m} = (64)_{10}$$
$$= \underline{0100} \underline{0000}$$

=

01/09/19
Saturday.

1. calculate the maximum quantisation error for 8 bit ADC with full scale input voltage 4096V.

$$1LSB = \frac{V_R}{2^{12}} = \frac{4.096}{2^{12}} = 1mA$$

$$\text{Maximum Quantisation error} = \pm \frac{1}{2} LSB$$
$$= \pm \frac{1}{2} (1mA)$$
$$= \pm 0.5mA$$

=

2. How many bits are required to design a DtoA converter that can have a resolution of 5mV. If DAC ladder has +8V full scale voltage

$$A. \frac{V_{fs}}{2^n} = 5mV$$

$$\frac{8}{2^n} = 5mV$$

$$R^{\eta} = \frac{8}{5m}$$

$$R^{\eta} = 1600$$

$$n = \log_2 1600$$

$$n = 10.64 \approx 11 \text{ bits}$$

3. The maximum output voltage of a η bit DAC is 25.4V.
What is the smallest change in output as the binary count increases.

A. Resolution = $\frac{V_{FS}}{2^n} = \frac{25.4}{2^7} = 0.1984 \approx 0.20$.

4. Determine the output voltage produced by a 4-bit DAC at which output voltage ranges from 0 to 10V when the input binary number is 0110.

A. 1111 \rightarrow 10V

$$0001 \rightarrow ? = \frac{0001}{1111} \times 10 = \frac{1}{15} \times 10 = 0.667$$

$$\therefore \text{for } 0110 \Rightarrow 6 \times 0.667 = 4V$$

5. A dual slope ADC, $t_1 = 83.33\text{msec}$ & reference voltage = 100mV. calculate t_2 if (i) $V_i = 100\text{mV}$
(ii) $V_i = 200\text{mV}$

A. $\frac{V_i t_1}{R_1 C_1} = \frac{V_R t_2}{R_2 C_1}$

$$V_i t_1 = V_R t_2$$

(i) $100\text{mV} \times t_1 = 100\text{mV} (t_2)$

$$t_2 = t_1$$

$$t_2 = 83.33\text{msec}$$

$$(ii) V_i t_1 = V_R t_2$$

$$200 \text{ mV} \times 83.33 \text{ msec} = 100 \text{ mV} \times t_2$$

$$t_2 = 166.66 \text{ msec}$$

\Rightarrow