

# UNIT – I

## LINEAR WAVESHAPING

*High pass, low pass RC circuits, their response for sinusoidal, step, pulse, square and ramp inputs. RC network as differentiator and integrator, attenuators, its applications in CRO probe, RL and RLC circuits and their response for step input, Ringing circuit.*

A linear network is a network made up of linear elements only. A linear network can be described by linear differential equations. The principle of superposition and the principle of homogeneity hold good for linear networks. In pulse circuitry, there are a number of waveforms, which appear very frequently. The most important of these are sinusoidal, step, pulse, square wave, ramp, and exponential waveforms. The response of *RC*, *RL*, and *RLC* circuits to these signals is described in this chapter. Out of these signals, the sinusoidal signal has a unique characteristic that it preserves its shape when it is transmitted through a linear network, i.e. under steady state, the output will be a precise reproduction of the input sinusoidal signal. There will only be a change in the amplitude of the signal and there may be a phase shift between the input and the output waveforms. The influence of the circuit on the signal may then be completely specified by the ratio of the output to the input amplitude and by the phase angle between the output and the input. No other periodic waveform preserves its shape precisely when transmitted through a linear network, and in many cases the output signal may bear very little resemblance to the input signal.

*The process whereby the form of a non-sinusoidal signal is altered by transmission through a linear network is called linear wave shaping.*

### THE LOW-PASS *RC* CIRCUIT

Figure 1.1 shows a low-pass *RC* circuit. A low-pass circuit is a circuit, which transmits only low-frequency signals and attenuates or stops high-frequency signals.

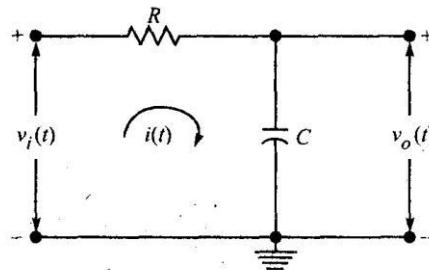
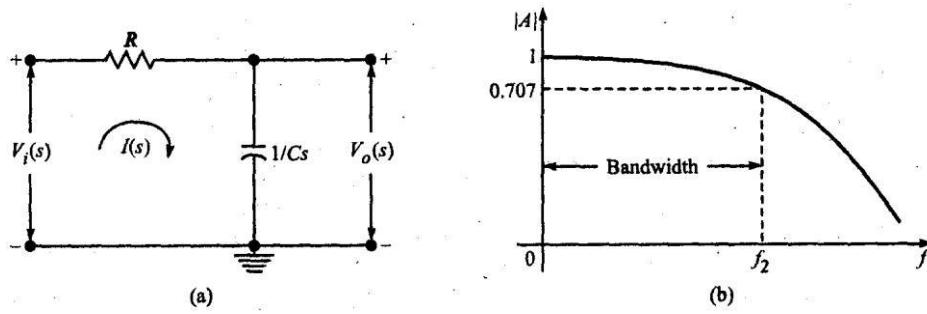


Figure 1.1 The low-pass *RC* circuit.

At zero frequency, the reactance of the capacitor is infinity (i.e. the capacitor acts as an open circuit) so the entire input appears at the output, i.e. the input is transmitted to the output with zero attenuation. So the output is the same as the input, i.e. the gain is unity. As the frequency increases the capacitive reactance decreases and so the output decreases. At very high frequencies the capacitor virtually acts as a short-circuit and the output falls to zero.

### Sinusoidal Input

The Laplace transformed low-pass  $RC$  circuit is shown in Figure 1.2(a). The gain versus frequency curve of a low-pass circuit excited by a sinusoidal input is shown in Figure 1.2(b). This curve is obtained by keeping the amplitude of the input sinusoidal signal constant and varying its frequency and noting the output at each frequency. At low frequencies the output is equal to the input and hence the gain is unity. As the frequency increases, the output decreases and hence the gain decreases. The frequency at which the gain is  $1/\sqrt{2}$  ( $= 0.707$ ) of its maximum value is called the cut-off frequency. For a low-pass circuit, there is no lower cut-off frequency. It is zero itself. The upper cut-off frequency is the frequency (in the high-frequency range) at which the gain is  $1/\sqrt{2}$ , i.e. 70.7%, of its maximum value. The bandwidth of the low-pass circuit is equal to the upper cut-off frequency  $f_2$  itself.



**Figure 1.2** (a) Laplace transformed low-pass  $RC$  circuit and (b) its frequency response.

For the network shown in Figure 1.2(a), the magnitude of the steady-state gain  $A$  is given by

$$A = \frac{V_o(s)}{V_i(s)} = \frac{\frac{1}{Cs}}{R + \frac{1}{Cs}} = \frac{1}{1 + RCs} = \frac{1}{1 + j\omega RC} = \frac{1}{1 + j2\pi fRC}$$

$$|A| = \frac{1}{\sqrt{1 + (2\pi fRC)^2}}$$

$$\text{At the upper cut-off frequency } f_2, |A| = \frac{1}{\sqrt{2}}$$

$$\therefore \frac{1}{\sqrt{2}} = \frac{1}{\sqrt{1 + (2\pi f_2 RC)^2}}$$

Squaring both sides and equating the denominators,

$$2 = 1 + (2\pi f_2 RC)^2$$

$$\therefore \text{The upper cut-off frequency, } f_2 = \frac{1}{2\pi RC}.$$

So

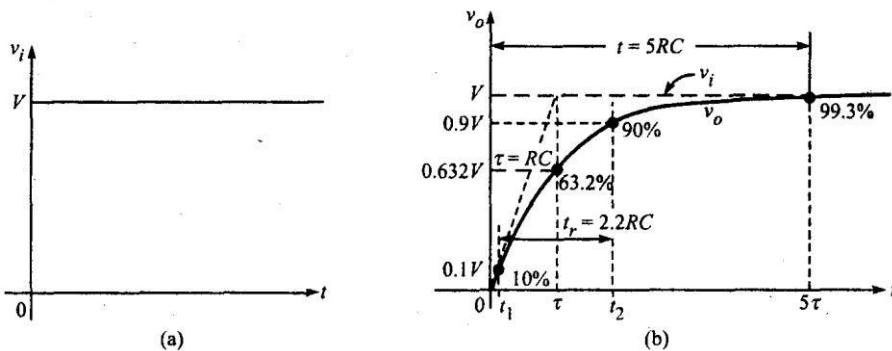
$$A = \frac{1}{1 + j \frac{f}{f_2}} \quad \text{and} \quad |A| = \frac{1}{\sqrt{1 + \left(\frac{f}{f_2}\right)^2}}$$

The angle  $\theta$  by which the output leads the input is given by

$$\theta = \tan^{-1} \frac{f}{f_2}$$

## Step-Voltage Input

A step signal is one which maintains the value zero for all times  $t < 0$ , and maintains the value  $V$  for all times  $t > 0$ . The transition between the two voltage levels takes place at  $t = 0$  and is accomplished in an arbitrarily small time interval. Thus, in Figure 1.3(a),  $v_i = 0$  immediately before  $t = 0$  (to be referred to as time  $t = 0^-$ ) and  $v_i = V$ , immediately after  $t = 0$  (to be referred to as time  $t = 0^+$ ). In the low-pass  $RC$  circuit shown in Figure 1.1, if the capacitor is initially uncharged, when a step input is applied, since the voltage across the capacitor cannot change instantaneously, the output will be zero at  $t = 0$ , and then, as the capacitor charges, the output voltage rises exponentially towards the steady-state value  $V$  with a time constant  $RC$  as shown in Figure 1.3(b).



**Figure 1.3** (a) Step input and (b) step response of the low-pass  $RC$  circuit.

Let  $V'$  be the initial voltage across the capacitor. Writing KVL around the loop in Figure 1.1.

$$v_i(t) = Ri(t) + \frac{1}{C} \int i(t) dt$$

Differentiating this equation,

$$\frac{dv_i(t)}{dt} = R \frac{di(t)}{dt} + \frac{1}{C} i(t)$$

Since

$$v_i(t) = V, \quad \frac{dv_i(t)}{dt} = 0$$

$$\therefore 0 = R \frac{di(t)}{dt} + \frac{1}{C} i(t)$$

Taking the Laplace transform on both sides,

$$0 = R[sI(s) - I(0^+)] + \frac{1}{C} I(s)$$

$$\therefore I(0^+) = I(s) \left( s + \frac{1}{RC} \right)$$

The initial current  $I(0^+)$  is given by

$$I(0^+) = \frac{V - V'}{R}$$

$$\therefore I(s) = \frac{I(0^+)}{s + \frac{1}{RC}} = \frac{V - V'}{R \left( s + \frac{1}{RC} \right)}$$

and  $V_o(s) = V_i(s) - I(s)R = \frac{V}{s} - \frac{(V - V')R}{R \left( s + \frac{1}{RC} \right)} = \frac{V}{s} - \frac{V - V'}{s + \frac{1}{RC}}$

Taking the inverse Laplace transform on both sides,

$$v_o(t) = V - (V - V')e^{-t/RC}$$

where  $V'$  is the initial voltage across the capacitor ( $V_{\text{initial}}$ ) and  $V$  is the final voltage ( $V_{\text{final}}$ ) to which the capacitor can charge.

So, the expression for the voltage across the capacitor of an  $RC$  circuit excited by a step input is given by

$$v_o(t) = V_{\text{final}} - (V_{\text{final}} - V_{\text{initial}})e^{-t/RC}$$

If the capacitor is initially uncharged, then  $v_o(t) = V(1 - e^{-t/RC})$

## Expression for rise time

When a step signal is applied, the rise time  $t_r$  is defined as the time taken by the output voltage waveform to rise from 10% to 90% of its final value: It gives an indication of how fast the circuit can respond to a discontinuity in voltage. Assuming that the capacitor in Figure 1.1 is initially uncharged, the output voltage shown in Figure 1.3(b) at any instant of time is given by

$$v_o(t) = V(1 - e^{-t/RC})$$

At  $t = t_1$ ,  $v_o(t) \neq 10\%$  of  $V = 0.1\text{V}$

$$\therefore 0.1V = V(1 - e^{-t_1/RC})$$

$$\therefore e^{-t_1/RC} = 0.9 \quad \text{or} \quad e^{t_1/RC} = \frac{1}{0.9} = 1.11$$

$$\therefore t_1 = RC \ln (1.11) = 0.1RC$$

At  $t = t_2$ ,  $v_o(t) = 90\%$  of  $V = 0.9\text{V}$

$$\therefore 0.9V = V(1 - e^{-t_2/RC})$$

$$\therefore e^{-t_2/RC} = 0.1 \quad \text{or} \quad e^{t_2/RC} = \frac{1}{0.1} = 10$$

$$\therefore t_2 = RC \ln 10 = 2.3RC$$

$$\therefore \text{Rise time, } t_r = t_2 - t_1 = 2.2RC$$

This indicates that the rise time  $t_r$  is proportional to the time constant  $RC$  of the circuit.

The larger the time constant, the slower the capacitor charges, and the smaller the time constant, the faster the capacitor charges.

### **Relation between rise time and upper 3-dB frequency**

We know that the upper 3-dB frequency (same as bandwidth) of a low-pass circuit is

$$f_2 = \frac{1}{2\pi RC} \quad \text{or} \quad RC = \frac{1}{2\pi f_2}$$

$$\therefore \text{Rise time, } t_r = 2.2RC = \frac{2.2}{2\pi f_2} = \frac{0.35}{f_2} = \frac{0.35}{\text{BW}}$$

Thus, the rise time is inversely proportional to the upper 3-dB frequency.

The *time constant* ( $T = RC$ ) of a circuit is defined as the time taken by the output to rise to 63.2% of the amplitude of the input step. It is same as the time taken by the output to rise to 100% of the amplitude of the input step, if the initial slope of rise is maintained. See Figure 1.3(b). The Greek letter T is also employed as the symbol for the time constant.

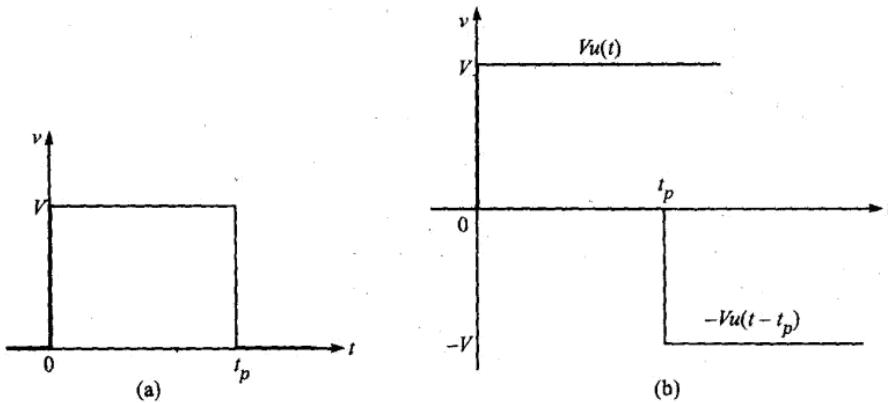
### **Pulse Input**

The pulse shown in Figure 1.4(a) is equivalent to a positive step followed by a delayed negative step as shown in Figure 1.4(b). So, the response of the low-pass  $RC$  circuit to a pulse for times less than the pulse width  $t_p$  is the same as that for a step input and is given by

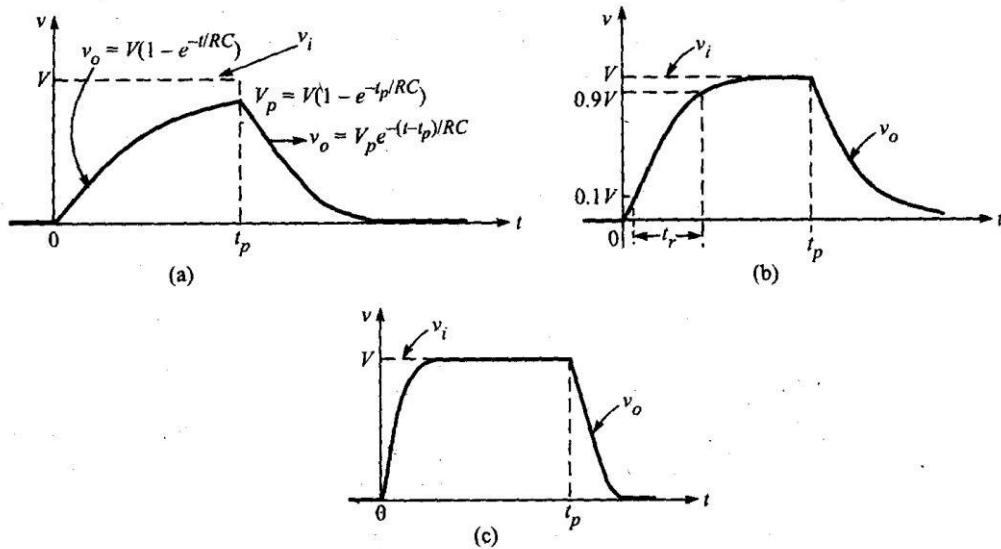
$v_o(t) = V(1 - e^{-t/RC})$ . The responses of the low-pass  $RC$  circuit for time constant  $RC \gg t_p$ ,  $RC$  smaller than  $t_p$  and  $RC$  very small compared to  $t_p$  are shown in Figures 1.5(a), 1.5(b), and 1.5(c) respectively.

If the time constant  $RC$  of the circuit is very large, at the end of the pulse, the output voltage will be  $V_p(t) = V(1 - e^{-t_p/RC})$ , and the output will decrease to zero from this value with a

time constant  $RC$  as shown in Figure 1.5(a). Observe that the pulse waveform is distorted when it is passed through a linear network. The output will always extend beyond the pulse width  $t_p$ , because whatever charge has accumulated across the capacitor  $C$  during the pulse cannot leak off instantaneously.



**Figure 1.4** (a) A pulse and (b) a pulse in terms of steps.



**Figure 1.5** Pulse response for (a)  $RC \gg t_p$ , (b)  $RC < t_p$ , and (c)  $RC \ll t_p$ .

If the time constant  $RC$  of the circuit is very small, the capacitor charges and discharges very quickly and the rise time  $t_r$  will be small and so the distortion in the wave shape is small. For minimum distortion (i.e. for preservation of wave shape), the rise time must be small compared to the pulse width  $t_p$ . If the upper 3-dB frequency  $f_2$  is chosen equal to the reciprocal of the pulse width  $t_p$ , i.e. if  $f_2 = 1/t_p$  then  $t_r = 0.35t_p$  and the output is as shown in Figure 1.5(b), which for many applications is a reasonable reproduction of the input. As a rule of thumb, we can say:

*A pulse shape will be preserved if the 3-dB frequency is approximately equal to the reciprocal of the pulse width.*

Thus to pass a 0.25  $\mu$ s pulse reasonably well requires a circuit with an upper cut-off frequency of the order of 4 MHz.

### Square-Wave Input

A square wave is a periodic waveform which maintains itself at one constant level  $V'$  with respect to ground for a time  $T_1$  and then changes abruptly to another level  $V''$ , and remains constant at that level for a time  $T_2$ , and repeats itself at regular intervals of  $T = T_1 + T_2$ . A square wave may be treated as a series of positive and negative steps. The shape of the output waveform for a square wave input depends on the time constant of the circuit. If the time constant is very small, the rise time will also be small and a reasonable reproduction of the input may be obtained.

For the square wave shown in Figure 1.6(a), the output waveform will be as shown in Figure 1.6(b) if the time constant  $RC$  of the circuit is small compared to the period of the input waveform. In this case, the wave shape is preserved. If the time constant is comparable with the period of the input square wave, the output will be as shown in Figure 1.6(c). The output rises and falls exponentially. If the time constant is very large compared to the period of the input waveform, the output consists of exponential sections, which are essentially linear as indicated in Figure 1.6(d). Since the average voltage across  $R$  is zero, the dc voltage at the output is the same as that of the input. This average value is indicated as  $V\&$ . in all the waveforms of Figure 1.6.

In Figure 1.6(c), the equation for the rising portion is

$$v_{01} = V' - (V' - V_2)e^{-t/RC}$$

where  $V_2$  is the voltage across the capacitor at  $t = 0$ , and  $V'$  is the level to which the capacitor can charge.

The equation for the falling portion is

$$v_{02} = V'' - (V'' - V_1)e^{-(t - T_1)/RC}$$

where  $V_1$  is the voltage across the capacitor at  $t = T_1$  and  $V''$  is the level to which the capacitor can discharge.

Setting  $v_{01} = V_1$  at  $t = T_1$ ,

$$V_1 = V' - (V' - V_2)e^{-T_1/RC} = V'(1 - e^{-T_1/RC}) + V_2e^{-T_1/RC}$$

Setting  $v_{02} = V_2$  at  $t = T_1 + T_2$ ,

$$V_2 = V'' - (V'' - V_1)e^{-(T_1+T_2-T_1)/RC} = V''(1 - e^{-T_2/RC}) + V_1e^{-T_2/RC}$$

Substituting this value of  $V_2$  in the expression for  $V_1$ ,

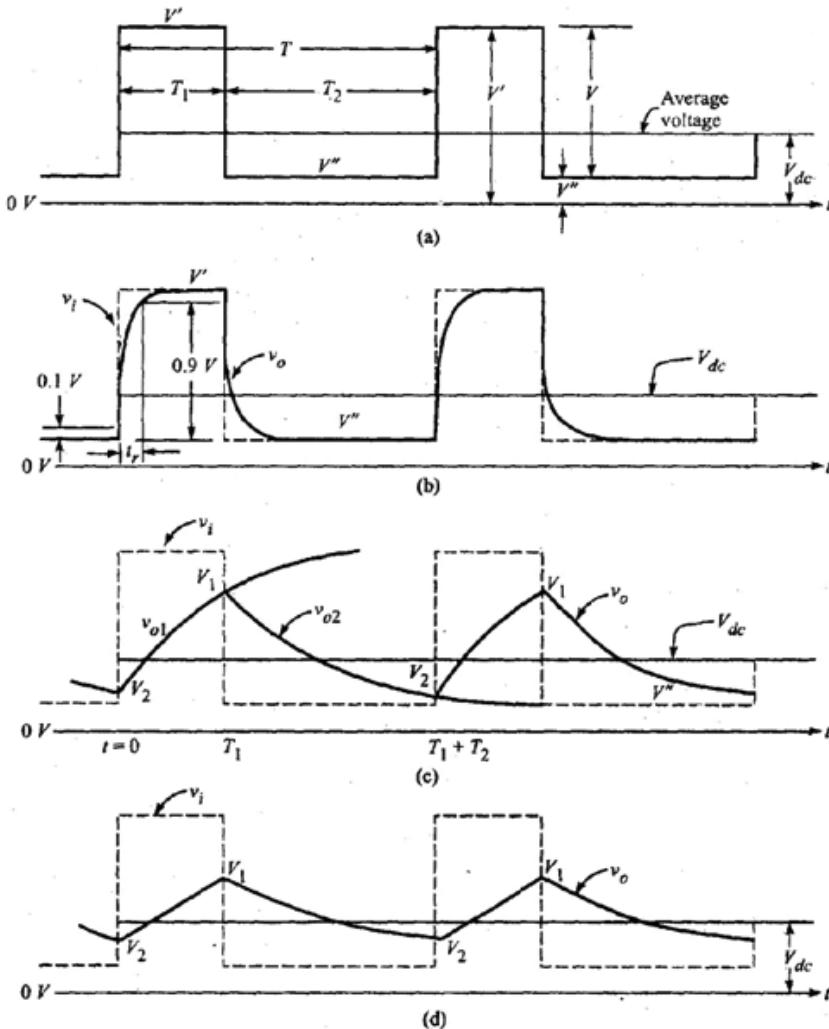
$$V_1 = V'(1 - e^{-T_1/RC}) + [V''(1 - e^{-T_2/RC}) + V_1 e^{-T_2/RC}] e^{-T_1/RC}$$

i.e.

$$V_1 = \frac{V'(1 - e^{-T_1/RC}) + V''(1 - e^{-T_2/RC}) e^{-T_1/RC}}{1 - e^{-(T_1 + T_2)/RC}}$$

Similarly substituting the value of  $V_1$  in the expression for  $V_2$ ,

$$V_2 = \frac{V''(1 - e^{-T_2/RC}) + V'(1 - e^{-T_1/RC}) e^{-T_2/RC}}{1 - e^{-(T_1 + T_2)/RC}}$$



**Figure 1.6** Response of a low-pass  $RC$  circuit to a square wave input: (a) square-wave input wave form, (b) output waveform for  $RC \ll T$ , (c) output waveform for  $RC = T$ , and (d) output waveform for  $RC \gg T$ .

For a symmetrical square wave with zero average value,

$$T_1 = T_2 = \frac{T}{2} \quad \text{and} \quad V' = -V'' = \frac{V}{2}. \quad \text{So, } V_2 \text{ will be equal to } -V_1$$

$$V_1 = \frac{\frac{V}{2}(1 - e^{-T/2RC}) - \frac{V}{2}(1 - e^{-T/2RC}) e^{-T/2RC}}{1 - e^{-T/RC}}$$

$$\begin{aligned}
&= \frac{V}{2} \frac{1 - e^{-T/2RC} - e^{-T/2RC} + e^{-T/RC}}{1 - e^{-T/RC}} \\
&= \frac{V}{2} \frac{(1 - e^{-T/2RC})^2}{(1 + e^{-T/2RC})(1 - e^{-T/2RC})} \\
&= \frac{V}{2} \left( \frac{1 - e^{-T/2RC}}{1 + e^{-T/2RC}} \right) \\
&= \frac{V}{2} \left( \frac{e^{T/2RC} - 1}{e^{T/2RC} + 1} \right) \\
&= \frac{V}{2} \left( \frac{e^{2x} - 1}{e^{2x} + 1} \right) = \frac{V}{2} \tanh x
\end{aligned}$$

where  $x = \frac{T}{4RC}$  and  $T$  is the period of the square wave.

Now,  $V_2 = -V_1 = -\frac{V}{2} \left( \frac{1 - e^{-T/2RC}}{1 + e^{-T/2RC}} \right) = \frac{V}{2} \left( \frac{1 - e^{T/2RC}}{1 + e^{T/2RC}} \right)$

### 1.1.5 Ramp Input

When a low-pass  $RC$  circuit shown in Figure 1.1 is excited by a ramp input, i.e.

$$v_i(t) = \alpha t, \text{ where } \alpha \text{ is the slope of the ramp}$$

we have,

$$V_i(s) = \frac{\alpha}{s^2}$$

From the frequency domain circuit of Figure 1.2(a), the output is given by

$$\begin{aligned}
V_o(s) &= V_i(s) \frac{\frac{1}{Cs}}{R + \frac{1}{Cs}} = \frac{\alpha}{s^2} \cdot \frac{1}{1 + RCs} = \frac{\alpha}{RC} \frac{1}{s^2 \left( s + \frac{1}{RC} \right)} \\
&= \frac{\alpha}{RC} \left[ \frac{-(RC)^2}{s} + \frac{RC}{s^2} + \frac{(RC)^2}{s + \frac{1}{RC}} \right]
\end{aligned}$$

$$\text{i.e. } V_o(s) = \frac{-\alpha RC}{s} + \frac{\alpha}{s^2} + \frac{\alpha RC}{s + \frac{1}{RC}}$$

Taking the inverse Laplace transform on both sides,

$$\begin{aligned} v_o(t) &= -\alpha RC + \alpha t + \alpha R C e^{-t/RC} \\ &= \alpha(t - RC) + \alpha R C e^{-t/RC} \end{aligned}$$

If the time constant  $RC$  is very small,  $e^{-t/RC} \approx 0$

$$\therefore v_o(t) = \alpha(t - RC)$$

When the time constant is very small relative to the total ramp time  $T$ , the ramp will be transmitted with minimum distortion. The output follows the input but is delayed by one time constant  $RC$  from the input (except near the origin where there is distortion) as shown in Figure 1.7(a). If the time constant is large compared with the sweep duration, i.e. if  $RC/T \gg 1$ , the output will be highly distorted as shown in Figure 1.7(b).

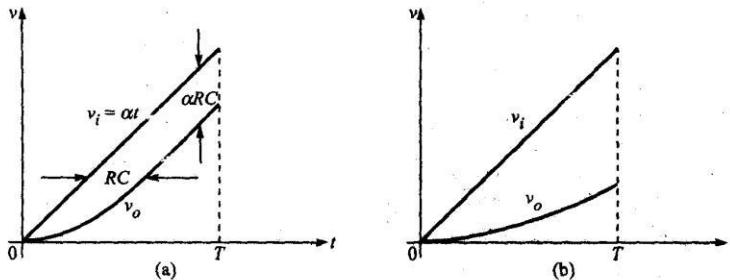


Figure 1.7 Response of a low-pass  $RC$  circuit for a ramp input for (a)  $RC/T \ll 1$  and (b)  $RC/T \gg 1$ .

Expanding  $e^{-t/RC}$  into an infinite series in  $t/RC$  in the above equation for  $v_o(t)$ ,

$$\begin{aligned} v_o(t) &= \alpha(t - RC) + \alpha RC \left( 1 - \frac{t}{RC} + \left( \frac{t}{RC} \right)^2 \frac{1}{2!} - \left( \frac{t}{RC} \right)^3 \frac{1}{3!} + \dots \right) \\ &= \alpha t - \alpha RC + \alpha RC - \alpha t + \frac{\alpha t^2}{2RC} - \dots \\ &\approx \frac{\alpha t^2}{2RC} \approx \frac{\alpha}{RC} \left( \frac{t^2}{2} \right) \end{aligned}$$

This shows that a quadratic response is obtained for a linear input and hence the circuit acts as an integrator for  $RC/T \gg 1$ .

The transmission error  $e_t$  for a ramp input is defined as the difference between the input and the output divided by the input at the end of the ramp, i.e. at  $t = T$ .  
For  $RC/T \ll 1$ ,

$$\begin{aligned} e_t &= \frac{\alpha t - (\alpha t - \alpha RC)}{\alpha t} \Big|_{t=T} \\ &= \frac{\alpha RC}{\alpha T} = \frac{RC}{T} = \frac{1}{2\pi f_2 T} \end{aligned}$$

where  $f_2$  is the upper 3-dB frequency. For example, if we desire to pass a 2 ms pulse with less than 0.1% error, the above equation yields  $f_2 > 80$  kHz and  $RC < 2 \mu\text{s}$ .

## THE LOW-PASS $RC$ CIRCUIT AS AN INTEGRATOR

If the time constant of an  $RC$  low-pass circuit is very large, the capacitor charges very slowly and so almost all the input voltage appears across the resistor for small values of time. Then, the current in the circuit is  $v_i/R$  and the output signal across  $C$  is

$$v_o(t) = \frac{1}{C} \int i(t) dt = \frac{1}{C} \int \frac{v_i(t)}{R} dt = \frac{1}{RC} \int v_i(t) dt$$

Hence the output is the integral of the input, i.e. if  $v_i(t) = \alpha t$ , then

$$v_o(t) = \frac{\alpha t^2}{2RC}$$

As time increases, the voltage drop across  $C$  does not remain negligible compared with that across  $R$  and the output will not remain the integral of the input. The output will change from a quadratic to a linear function of time. *If the time constant of an  $RC$  low-pass circuit is very large in comparison with the time required for the input signal to make an appreciable change, the circuit acts as an integrator.* A criterion for good integration in terms of steady-state analysis is as follows: The low-pass circuit acts as an integrator provided the time constant of the circuit  $RC > 15T$ , where  $T$  is the period of the input sine wave. When  $RC > 15T$ , the input sinusoid will be shifted at least by  $89.4^\circ$  (instead of the ideal  $90^\circ$  shift required for integration) when it is transmitted through the network.

An  $RC$  integrator converts a square wave into a triangular wave. Integrators are almost invariably preferred over differentiators in analog computer applications for the following reasons:

1. It is easier to stabilize an integrator than a differentiator because the gain of an integrator decreases with frequency whereas the gain of a differentiator increases with frequency.
2. An integrator is less sensitive to noise voltages than a differentiator because of its limited bandwidth.
3. The amplifier of a differentiator may overload if the input waveform changes very rapidly.
4. It is more convenient to introduce initial conditions in an integrator.

**EXAMPLE 1.1** A pulse generator with an output resistance  $R_S = 500 \Omega$  is connected to an oscilloscope with an input capacitance of  $C_i = 30 \text{ pF}$ . Determine the fastest rise time that can be displayed.

**Solution:** The circuit works as a low-pass filter shown in Figure 1.1 with a time constant

$$R_S C_i = 500 \Omega \times 30 \text{ pF} = 15 \text{ ns}$$

$$\therefore \text{Fastest rise time, } t_r = 2.2RC = 2.2 \times 15 \text{ ns} = 33 \text{ ns}$$

**EXAMPLE 1.2** A 10 V step is switched on to a  $50 \text{ k}\Omega$  resistor in series with a  $500 \text{ pF}$  capacitor. Calculate the rise time of the capacitor voltage, the time for the capacitor to charge to 63.2% of its maximum voltage, and the time for the capacitor to be completely charged.

**Solution:** The circuit acts as a low-pass filter shown in Figure 1.1.

(a) The rise time of the capacitor voltage is

$$t_r = 2.2RC = 2.2 \times 50 \text{ k}\Omega \times 500 \text{ pF} = 55 \mu\text{s}$$

(b) The time for the capacitor to charge to 63.2% of the maximum voltage is

$$\tau = RC = 50 \text{ k}\Omega \times 500 \text{ pF} = 25 \mu\text{s}$$

(c) The time for the capacitor to be completely charged (99% value) is

$$5\tau = 5RC = 5 \times 25 \mu\text{s} = 125 \mu\text{s}$$

## THE HIGH-PASS RC CIRCUIT

Figure 1.30 shows a high-pass  $RC$  circuit. At zero frequency the reactance of the capacitor is infinity and so it blocks the input and hence the output is zero. Hence, this capacitor is called the *blocking capacitor* and this circuit, also called the *capacitive coupling circuit*, is used to provide dc isolation between the input and the output. As the frequency increases, the reactance of the capacitor decreases and hence the output and gain increase. At very high frequencies, the capacitive reactance is very small so a very small voltage appears across  $C$  and, so the output is almost equal to the input and the gain is equal to 1. Since this circuit attenuates low-frequency signals and allows transmission of high-frequency signals with little or no attenuation, it is called a high-pass circuit.

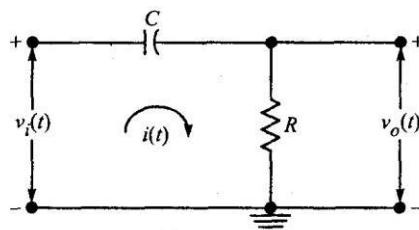
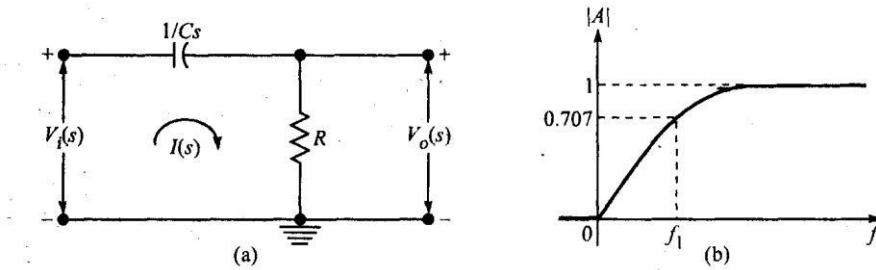


Figure 1.30 The high-pass  $RC$  circuit.

## Sinusoidal Input

Figure 1.31 (a) shows the Laplace transformed high-pass  $RC$  circuit. The gain versus frequency curve of a high-pass circuit excited by a sinusoidal input is shown in Figure 1.31(b). For a sinusoidal input  $v_i$ , the output signal  $v_o$  increases in amplitude with increasing frequency. The frequency at which the gain is  $1/\sqrt{2}$  of its maximum value is called the lower cut-off or lower 3-dB frequency. For a high-pass circuit, there is no upper cut-off frequency because all high frequency signals are transmitted with zero attenuation. Therefore,  $f_2 = f_1$ . Hence bandwidth  $B.W = f_2 - f_1 = \infty$



**Figure 1.31** (a) Laplace transformed high-pass circuit and (b) gain versus frequency plot.

### Expression for the lower cut-off frequency

For the high-pass  $RC$  circuit shown in Figure 1.31 (a), the magnitude of the steady-state gain  $A$ , and the angle  $\theta$  by which the output leads the input are given by

$$A = \frac{V_o(s)}{V_i(s)} = \frac{R}{R + \frac{1}{Cs}} = \frac{1}{1 + \frac{1}{RCs}}$$

Putting

$$s = j\omega, \quad A = \frac{1}{1 - j\frac{1}{\omega RC}} = \frac{1}{1 - j\frac{1}{2\pi f RC}}$$

$$\therefore |A| = \frac{1}{\sqrt{1 + \left(\frac{1}{2\pi f RC}\right)^2}} \quad \text{and} \quad \theta = -\tan^{-1} \frac{1}{2\pi f RC}$$

At the lower cut-off frequency  $f_1$ ,  $|A| = 1/\sqrt{2}$

$$\therefore \frac{1}{\sqrt{1 + \left(\frac{1}{2\pi f_1 RC}\right)^2}} = \frac{1}{\sqrt{2}}$$

Squaring and equating the denominators,

$$\frac{1}{2\pi f_1 RC} = 1 \quad \text{i.e.} \quad f_1 = \frac{1}{2\pi RC}$$

This is the expression for the lower cut-off frequency of a high-pass circuit.

### Relation between $f_1$ and tilt

The lower cut-off frequency of a high-pass circuit is  $f_1 = \frac{1}{2\pi RC}$ . The lower cut-off frequency produces a tilt. For a 10% change in capacitor voltage, the time or pulse width involved is

$$t = 0.1RC = PW$$

$$\therefore \frac{PW}{RC} = 0.1 = \text{Fractional tilt}$$

$$\therefore \text{Fractional tilt} = \frac{PW}{RC} = 2\pi f_1 \cdot PW$$

This equation applies only when the tilt is 10% or less. When the tilt exceeds 10%, the voltage should be treated as exponential instead of linear and the equation  $v_o = V_f - (V_f - V_i)e^{-t/RC}$  should be applied.

### Step Input

When a step signal of amplitude  $V$  volts shown in Figure 1.32(a) is applied to the high-pass  $RC$  circuit of Figure 1.30, since the voltage across the capacitor cannot change instantaneously the output will be just equal to the input at  $t = 0$  (for  $f < 0$ ,  $v_- = 0$  and  $v_a = 0$ ). Later when the capacitor charges exponentially, the output reduces exponentially with the same time constant  $RC$ . The expression for the output voltage for  $t > 0$  is given by

$v_o(t) = V_f - (V_f - V_i)e^{-t/RC} = 0 - (0 - V)e^{-t/RC} = Ve^{-t/RC}$  Figure 1.32(b) shows the response of the circuit for large, small, and very small time constants. For  $t > 5f$ , the output will reach more than 99% of its final value. Hence although the steady state is approached asymptotically, for most applications we may assume that the final value has been reached after  $5f$ . If the initial slope of the exponential is maintained, the output falls to zero in a time  $t = T$ .

The voltage across a capacitor can change instantaneously only when an infinite current passes through it, because for any finite current  $i(t)$  through the capacitor, the instantaneous

change in voltage across the capacitor is given by  $\frac{1}{C} \int_0^t i(t) dt = 0$ .

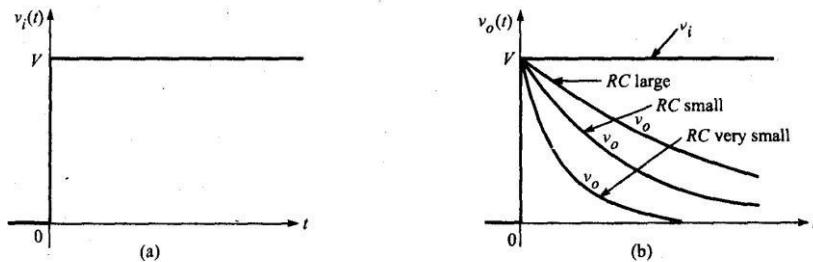
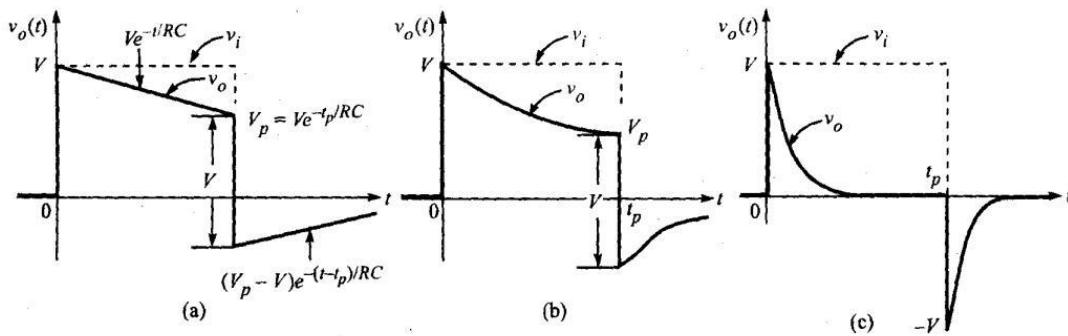


Figure 1.32 (a) Step input and (b) step response for different time constants.

## Pulse Input

A pulse of amplitude  $V$  and duration  $t_p$  shown in Figure 1.4(a) is nothing but the sum of a positive step of amplitude  $V$  starting at  $t = 0$  and a negative step of amplitude  $V$  starting at  $t_p$  as shown in Figure 1.4(b). So, the response of the circuit for  $0 < t < t_p$ , for the pulse input is the same as that for a step input and is given by  $v_o(t) = Ve^{-t/RC}$ . At  $t = t_p$ ,  $v_o(t) = V = Ve^{-t_p/RC}$ . At  $t = t_p$ , since the input falls by  $V$  volts suddenly and since the voltage across the capacitor cannot change instantaneously, the output also falls suddenly by  $V$  volts to  $V_p - V$ . Hence at  $t = t_p^+$ ,  $v_o(t) = Ve^{-t_p/RC} - V$ . Since  $V_p < V$ ,  $V_p - V$  is negative. So there is an undershoot at  $t = t_p$  and hence for  $t > t_p$ , the output is negative. For  $t > t_p$ , the output rises exponentially towards zero with a time constant  $RC$  according to the expression  $(Ve^{-t_p/RC} - V)e^{-(t-t_p)/RC}$ .

The output waveforms for  $RC \gg t_p$ ,  $RC$  comparable to  $t_p$  and  $RC \ll t_p$  are shown in Figures 1.33(a), (b), and (c) respectively. There is distortion in the outputs and the distortion is the least when the time constant is very large. Observe that there is positive area and negative area in the output waveforms. The negative area will always be equal to the positive area. So if the time constant is very large the tilt (the almost linear decrease in the output voltage) will be small and hence the undershoot will be very small, and for  $t > t_p$ , the output rises towards the zero level very very slowly. If the time constant is very small compared to the pulse width (i.e.  $RC/t_p \ll T$ ), the output consists of a positive spike or pip of amplitude  $V$  volts at the beginning of the pulse and a negative spike of the same amplitude at the end of the pulse. Hence a high-pass circuit with a very small time constant is called a *peaking circuit* and this process of converting pulses into pips by means of a circuit of short time constant is called peaking.



**Figure 1.33** Pulse response for (a)  $RC \gg t_p$ , (b)  $RC$  comparable to  $t_p$  and (c)  $RC \ll t_p$ .

## Square-Wave Input

A square wave shown in Figure 1.34(a) is a periodic waveform, which maintains itself at one constant level  $V$  with respect to ground for a time  $T_1$  and then changes abruptly to another level  $V''$  and remains constant at that level for a time  $T_2$ , and then repeats itself at regular intervals of  $T = T_1 + T_2$ . A square wave may be treated as a series of positive and negative steps. The shape of the output depends on the time constant of the circuit. Figures 1.34(b), 1.34(c), 1.34(d), and 1.34(e) show the output waveforms of the high-pass  $RC$  circuit under steady-state conditions for the cases (a)  $RC \gg T$ , (b)  $RC > T$ , (c)  $RC \sim T$ , and (d)  $RC \ll T$  respectively. When the time constant is arbitrarily large (i.e.  $RC/T_1$  and  $RC/T_2$  are very very large in comparison to unity) the output is same as the input but with zero dc level. When  $RC > T$ , the output is in the form of a tilt. When  $RC$  is comparable to  $T$ , the output rises and falls exponentially. When  $RC \ll T$  (i.e.  $RC/T_1$  and  $RC/T_2$  are very small in comparison to unity), the output consists of alternate positive and negative spikes. In this case the peak-to-peak amplitude of the output is twice the peak-to-peak value of the input. In fact, for any periodic input waveform under steady-state conditions, the average level of the output waveform from the high-pass circuit of Figure 1.30 is always zero independently of the dc level of the input. The proof is as follows: Writing KVL around the loop of Figure 1.30,

$$\begin{aligned} v_i(t) &= \frac{1}{C} \int i(t) dt + v_o(t) \\ &= \frac{1}{RC} \int v_o(t) dt + v_o(t) \quad \left( \because i(t) = \frac{v_o(t)}{R} \right) \end{aligned}$$

Differentiating,

$$\frac{dv_i(t)}{dt} = \frac{v_o(t)}{RC} + \frac{dv_o(t)}{dt}$$

Multiplying by  $dt$  and integrating this equation over one period  $T$ ,

$$\int_{t=0}^{t=T} dv_i(t) = \int_{t=0}^{t=T} \frac{v_o(t) dt}{RC} + \int_{t=0}^{t=T} dv_o(t)$$

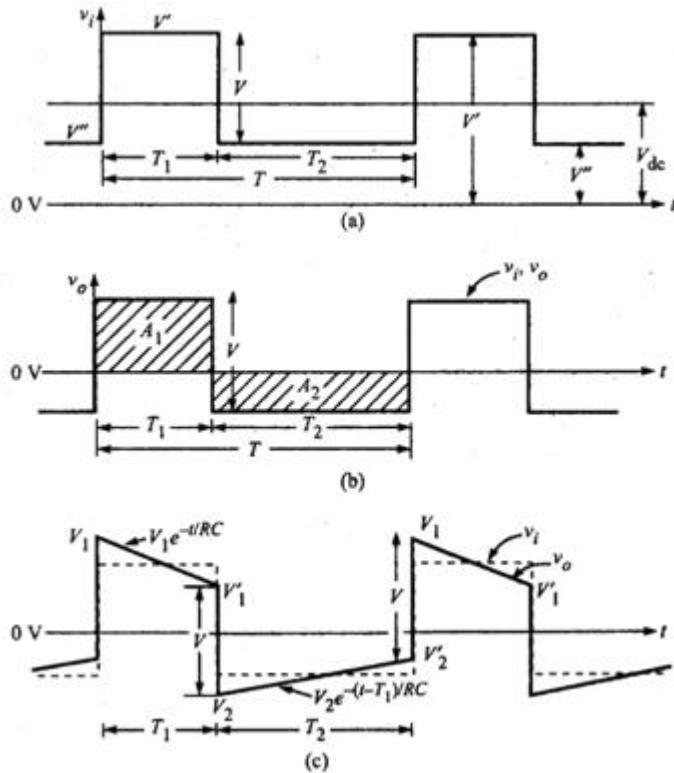
$$\text{i.e. } v_i(T) - v_i(0) = \frac{1}{RC} \int_0^T v_o(t) dt + v_o(T) - v_o(0)$$

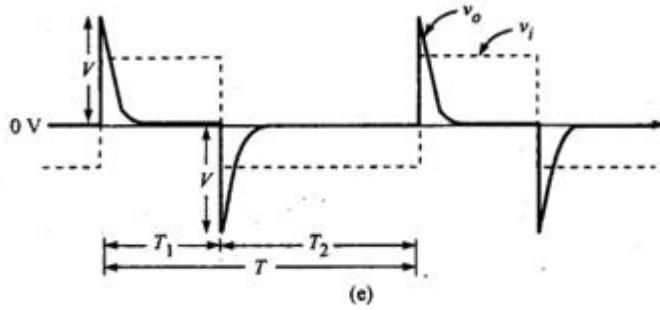
Under steady-state conditions, the output waveform (as well as the input signal) is repetitive with a period  $T$  so that  $v_o(T) = v_o(0)$  and  $v_i(T) = v_i(0)$ .

Under steady-state conditions, the output waveform (as well as the input signal) is repetitive with a period  $T$  so that  $v_o(T) = v_o(0)$  and  $v_i(T) = v_i(0)$ .

Hence  $\int_0^T v_o(t) dt = 0$ . Since this integral represents the area under the output waveform over one cycle, we can say that the average level of the steady-state output signal is always zero. This can also be proved based on frequency domain analysis as follows. The periodic input signal may be resolved into a Fourier series consisting of a constant term and an infinite number of sinusoidal components whose frequencies are multiples of  $f = 1/T$ . Since the blocking capacitor presents infinite impedance to the dc input voltage, none of these dc components reach the output under steady-state conditions. Hence the output signal is a sum of sinusoids whose frequencies are multiples of  $f$ . This waveform is therefore periodic with a fundamental period  $T$  but without a dc component. With respect to the high-pass circuit of Figure 1.30, we can say that:

1. The average level of the output signal is always zero, independently of the average level of the input. The output must consequently extend in both negative and positive directions with respect to the zero voltage axis and the area of the part of the waveform above the zero axis must equal the area which is below the zero axis.
2. When the input changes abruptly by an amount  $V$ , the output also changes abruptly by an equal amount and in the same direction.
3. During any finite time interval when the input maintains a constant level, the output decays exponentially towards zero voltage.





**Figure 1.34** (a) A square wave input, (b) output when  $RC$  is arbitrarily large, (c) output when  $RC > T$ , (d) output when  $RC$  is comparable to  $T$ , and (e) output when  $RC \ll T$ .

Under steady-state conditions, the capacitor charges and discharges to the same voltage levels in each cycle. So the shape of the output waveform is fixed.

For  $0 < t < T_1$ , the output is given by  $v_{o1} = V_1 e^{-t/RC}$

At  $t = T_1$ ,  $v_{o1} = V'_1 = V_1 e^{-T_1/RC}$

For  $T_1 < t < T_1 + T_2$ , the output is  $v_{o2} = V_2 e^{-(t-T_1)/RC}$

At  $t = T_1 + T_2$ ,  $v_{o2} = V'_2 = V_2 e^{-T_2/RC}$

Also  $V'_1 - V'_2 = V$  and  $V_1 - V'_2 = V$

From these relations  $V_1$ ,  $V'_1$ ,  $V_2$  and  $V'_2$  can be computed.

### Expression for the percentage tilt

We will derive an expression for the percentage tilt when the time constant  $RC$  of the circuit is very large compared to the period of the input waveform, i.e.  $RC \gg T$ . For a symmetrical square wave with zero average value

$$V_1 = -V_2, \text{ i.e. } V_1 = |V_2|, V'_1 = -V'_2, \text{ i.e. } V'_1 = |V'_2|, \text{ and } T_1 = T_2 = \frac{T}{2}$$

The output waveform for  $RC \gg T$  is shown in Figure 1.35. Here,

$$V'_1 = V_1 e^{-T/2RC} \quad \text{and} \quad V'_2 = V_2 e^{-T/2RC}$$

$$V_1 - V'_2 = V$$

$$\text{i.e. } V_1 - V_2 e^{-T/2RC} = V_1 + V_1 e^{-T/2RC} = V$$

$$\therefore V_1 = \frac{V}{1 + e^{-T/2RC}} \quad \text{or} \quad V = V_1(1 + e^{-T/2RC})$$

$$\% \text{ tilt, } P = \frac{V_1 - V'_1}{\frac{V}{2}} \times 100\% = \frac{V_1 - V_1 e^{-T/2RC}}{V_1(1 + e^{-T/2RC})} \times 200\% = \frac{1 - e^{-T/2RC}}{1 + e^{-T/2RC}} \times 200\%$$

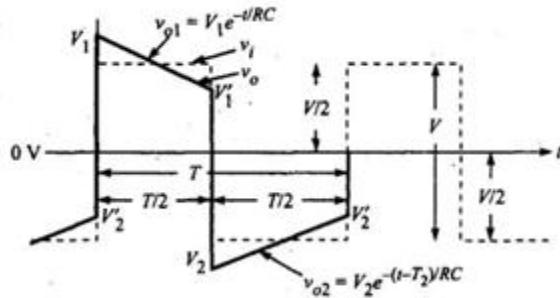


Figure 1.35 Linear tilt of a symmetrical square wave when  $RC \gg T$ .

When the time constant is very large, i.e.  $\frac{T}{RC} \ll 1$

$$\begin{aligned}
 P &= \frac{1 - \left[ 1 + \left( \frac{-T}{2RC} \right) + \left( \frac{-T}{2RC} \right)^2 \frac{1}{2!} + \dots \right]}{1 + 1 + \left( \frac{-T}{2RC} \right) + \left( \frac{-T}{2RC} \right)^2 \frac{1}{2!} + \dots} \times 200\% \\
 &= \frac{\frac{T}{2RC}}{2} \times 200\% \\
 &= \frac{T}{2RC} \times 100\% \\
 &= \frac{\pi f_1}{f} \times 100\%
 \end{aligned}$$

where  $f_1 = \frac{1}{2\pi RC}$  is the lower cut-off frequency of the high-pass circuit.

## Ramp Input

A waveform which is zero for  $t < 0$  and which increases linearly with time for  $t > 0$  is called a ramp or sweep voltage.

When the high-pass  $RC$  circuit of Figure 1.30 is excited by a ramp input  $v_i(t) = at$ , where  $a$  is the slope of the ramp, then

$$V_i(s) = \frac{\alpha}{s^2}$$

From the Laplace transformed circuit of Figure 1.31(a),

$$\begin{aligned}
 V_o(s) &= V_i(s) \frac{R}{R + \frac{1}{Cs}} = \frac{\alpha}{s^2} \frac{RCs}{1 + RCs} \\
 &= \frac{\alpha}{s \left( s + \frac{1}{RC} \right)} = \alpha RC \left( \frac{1}{s} - \frac{1}{s + \frac{1}{RC}} \right)
 \end{aligned}$$

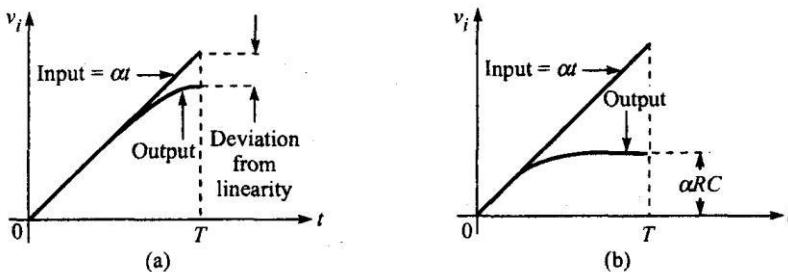
Taking the inverse Laplace transform on both sides,

$$v_o(t) = \alpha RC(1 - e^{-t/RC})$$

For times  $t$  which are very small in comparison with  $RC$ , we have

$$\begin{aligned} v_o(t) &= \alpha RC \left[ 1 - \left\{ 1 + \left( \frac{-t}{RC} \right) + \left( \frac{-t}{RC} \right)^2 \frac{1}{2!} + \left( \frac{-t}{RC} \right)^3 \frac{1}{3!} + \dots \right\} \right] \\ &= \alpha RC \left[ \frac{t}{RC} - \frac{t^2}{2(RC)^2} + \dots \right] \\ &= \alpha t - \frac{\alpha t^2}{2RC} = \alpha t \left( 1 - \frac{t}{2RC} \right) \end{aligned}$$

Figure 1.36 shows the response of the high-pass circuit for a ramp input when (a)  $RC \gg T$ , and (b)  $RC \ll T$ , where  $T$  is the duration of the ramp. For small values of  $T$ , the output signal falls away slightly from the input as shown in the Figure 1.36(a).



**Figure 1.36** Response of the high-pass circuit for a ramp input when (a)  $RC \gg T$  and (b)  $RC \ll T$ .

When a ramp signal is transmitted through a linear network, the output departs from the input. A measure of the departure from linearity expressed as the transmission error  $e$ , is defined as the difference between the input and the output divided by the input. The transmission error at a time

$$e_t = \left. \frac{v_i - v_o}{v_i} \right|_{t=T} \approx \left. \frac{\alpha t - \alpha t \left( 1 - \frac{t}{2RC} \right)}{\alpha t} \right|_{t=T} \approx \frac{T}{2RC} = \pi f_1 T$$

where  $f_1 = \frac{1}{2\pi RC}$  is the lower 3-dB frequency of the high-pass circuit.

$t = T$  is then

For large values of  $t$  in comparison with  $RC$ , the output approaches the constant value  $\alpha RC$  as indicated in Figure 1.36(b).

## THE HIGH-PASS RC CIRCUIT AS A DIFFERENTIATOR

When the time constant of the high-pass RC circuit is very very small, the capacitor charges very quickly; so almost all the input  $v_i(0)$  appears across the capacitor and the voltage across the resistor will be negligible compared to the voltage across the capacitor. Hence the current is determined entirely by the capacitance. Then the current

$$i(t) = C \frac{dv_i(t)}{dt}$$

and the output signal across  $R$  is

$$v_o(t) = RC \frac{dv_i(t)}{dt}$$

Thus we see that the output is proportional to the derivative of the input. ***The high-pass RC circuit acts as a differentiator provided the RC time, constant of the circuit is very small in comparison with the time required for the input signal to make an appreciable change.*** The

derivative of a step signal is an impulse of infinite amplitude at the occurrence of the discontinuity of step. The derivative of an ideal pulse is a positive impulse followed by a delayed negative impulse, each of infinite amplitude and occurring at the points of discontinuity. The derivative of a square wave is a waveform which is uniformly zero except, at the points of discontinuity. At these points, precise differentiation would yield impulses of infinite amplitude, zero width and alternating polarity. For a square wave input, an  $RC$  high-pass circuit with very small time constant will produce an output, which is zero except at the points of discontinuity. At these points of discontinuity, there will be peaks of finite amplitude  $V$ . This is because the voltage across  $R$  is not negligible compared with that across  $C$ . An  $RC$  differentiator converts a triangular wave into a square wave. For the ramp  $v_i = at$ , the value of  $RC(dv/dt) = aRC$ . This is true except near the origin. The output approaches the proper derivative value only after a lapse of time corresponding to several time constants. The error near  $\theta = 0$  is again due to the fact that in this region the voltage across  $R$  is not negligible compared with that across  $C$ .

If we assume that the leading edge of a pulse can be approximated by a ramp, then we can measure the rate of rise of the pulse by using a differentiator. The peak output is measured on an oscilloscope, and from the equation  $= aRC$ , we see that this voltage divided by the product  $RC$  gives the slope  $a$ . A criteria for good differentiation in terms of steady-state sinusoidal analysis is, that if a sine wave is applied to the high-pass  $RC$  circuit, the output will be a sine

$$\tan \theta = \frac{X_C}{R} = \frac{1}{\omega RC}$$

wave shifted by a leading angle  $\theta$  such that: with the output being proportional to  $\sin(a>t + \theta)$ . In order to have true differentiation, we must obtain  $\cos \omega t$ . In other words,  $\theta$  must equal  $90^\circ$ . This result can be obtained only if  $R = 0$  or  $C = 0$ .

However, if  $\omega RC = 0.01$ , then  $1/\omega RC = 100$  and  $\theta = 89.4^\circ$ , which is sufficiently close to  $90^\circ$  for most purposes. If  $\omega RC = 0.1$ , then  $90 - 84.3^\circ$  and for some applications this may be close enough

to  $90^\circ$ . If the peak value of input is  $V_m$ , the output is and if  $\omega RC \ll 1$ , then the output is approximately  $V_m\omega RC \cos(\omega t)$ . This result agrees with the expected value  $RC(dv_t/dt)$ . If  $\omega RC = 0.01$ , then the output amplitude is 0.01 times the input amplitude.

$$v_o = \frac{V_m R}{\sqrt{R^2 + \frac{1}{\omega^2 C^2}}} \sin(\omega t + \theta)$$

## ATTENUATORS

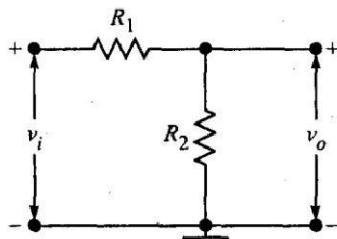
Attenuators are resistive networks, which are used to reduce the amplitude of the input signal. The simple resistor combination of Figure 1.61 (a) would multiply the input signal by the ratio  $a = R_2/(R_1 + R_2)$  independently of the frequency. If the output of the attenuator is feeding a stage of amplification, the input capacitance  $C_2$  of the amplifier will be the stray capacitance shunting the resistor  $R_2$  of the attenuator and the attenuator will be as shown in Figure 1.61(b), and the attenuation now is not independent of frequency. Using Thevenin's theorem, the circuit in Figure 1.61(b) may be replaced by its equivalent circuit shown in Figure 1.61(c), in which  $R$  is equal to the parallel combination of  $R_1$  and  $R_2$ .

Normally  $R_1$  and  $R_2$  must be large so that the nominal input impedance of the attenuator is large enough to prevent loading down the input signal. But if  $R_1$  and  $R_2$  are large, the rise time  $t_r = 2.2[(R_1//R_2)*C_2]$  will be large and a large rise time is normally unacceptable. The attenuator may be compensated by shunting  $R_1$  by a capacitor  $C_1$  as shown in Figure 1.61(d), so that its attenuation is once again independent of frequency. The circuit has been drawn in Figure 1.61(e) to suggest that the two resistors and the two capacitors may be viewed as the four arms of a bridge. If  $R_1C_1 = R_2C_2$ , the bridge will be balanced and no current will flow in the branch connecting the point  $X$  to the point  $Y$ . For the purpose of computing the output, the branch  $X-Y$  may be omitted and the output will again be equal to  $C_M$ , independent of the frequency. In practice,  $C_1$  will ordinarily have to be made adjustable.

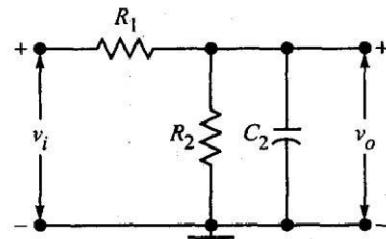
Suppose a step signal of amplitude  $V$  volts is applied to the circuit. As the input changes abruptly by  $V$  volts at  $t = 0$ , the voltages across  $C_1$  and  $C_2$  will also change abruptly. This happens because at  $t = 0$ , the capacitors act as short-circuits and a very large (ideally infinite) current flows through the capacitors for an infinitesimally small time so that a finite charge  $q = \int_{0^-}^{0^+} i(t) dt$  is delivered to each capacitor. The initial output voltage is determined by the capacitors.

Since the same current flows through the capacitors  $C_1$  and  $C_2$ , we have

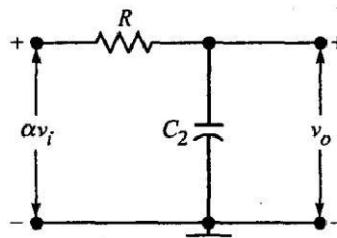
$$\text{Charge accumulated in capacitor } C_1 = \int_{0^-}^{0^+} i(t) dt = q$$



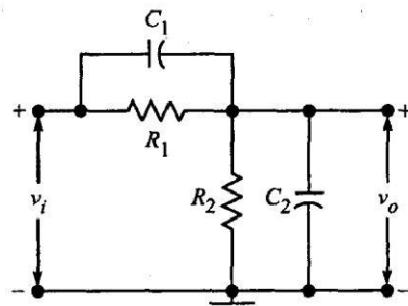
(a)



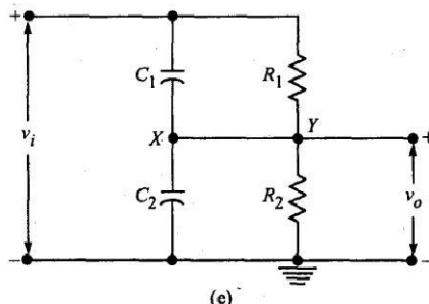
(b)



(c)



(d)



(e)

**Figure 1.61** An attenuator: (a) ideal circuit, (b) actual circuit, (c) equivalent circuit, (d) compensated attenuator, and (e) compensated attenuator redrawn as a bridge.

$$\therefore \text{Initial voltage across } C_1 = \frac{q}{C_1} = V_i$$

Charge accumulated in capacitor  $C_2 = \int_{0^-}^{0^+} i(t) dt = q$

$$\text{Initial voltage across } C_2 = \frac{q}{C_2} = V_2 = v_o(0^+)$$

$$\text{Input signal, } V = V_1 + V_2 = \frac{q}{C_1} + \frac{q}{C_2} = q \left( \frac{C_1 + C_2}{C_1 C_2} \right)$$

$$\frac{v_o(0^+)}{V} = \frac{\frac{q}{C_2}}{q \left( \frac{C_1 + C_2}{C_1 C_2} \right)} = \frac{C_1}{C_1 + C_2}$$

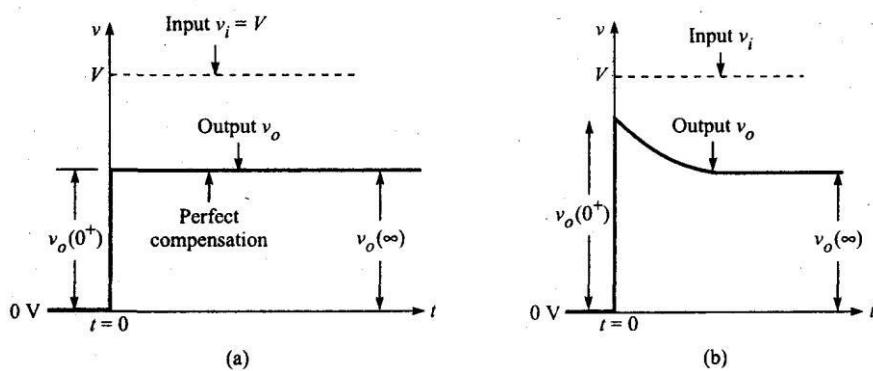
Or

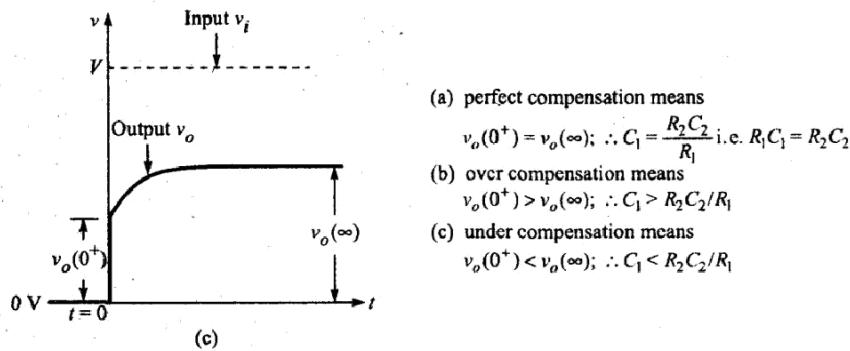
$$v_o(0^+) = V \frac{C_1}{C_1 + C_2} = v_i \frac{C_1}{C_1 + C_2}$$

The final output voltage is determined by the resistors  $R_1$  and  $R_2$ , because the capacitors  $C_1$  and  $C_2$  act as open circuits for the applied dc voltage under steady-state conditions. Hence

$$v_o(\infty) = V \frac{R_2}{R_1 + R_2} = v_i \frac{R_2}{R_1 + R_2}$$

Looking back from the output terminals (with the input short circuited) we see a resistor  $R = R_1 R_2 / (R_1 + R_2)$  in parallel with  $C = C_1 + C_2$ . Hence the decay or rise of the output (when the attenuator is not perfectly compensated) from the initial to the final value takes place exponentially with a time constant  $r = RC$ . The responses of an attenuator for  $C_j$  equal to, greater than, and less than  $R_2 C_2 / R_1$  are indicated in Figure 1.62.





**Figure 1.62** Response of compensated attenuator: (a) perfect compensation, (b) over compensation, and (c) under compensation.

Perfect compensation is obtained if  $v_o(0^+) = v_o(\infty)$ , that is, if the rise time  $t_r = 0$

$$\therefore V \frac{C_1}{C_1 + C_2} = V \frac{R_2}{R_1 + R_2}$$

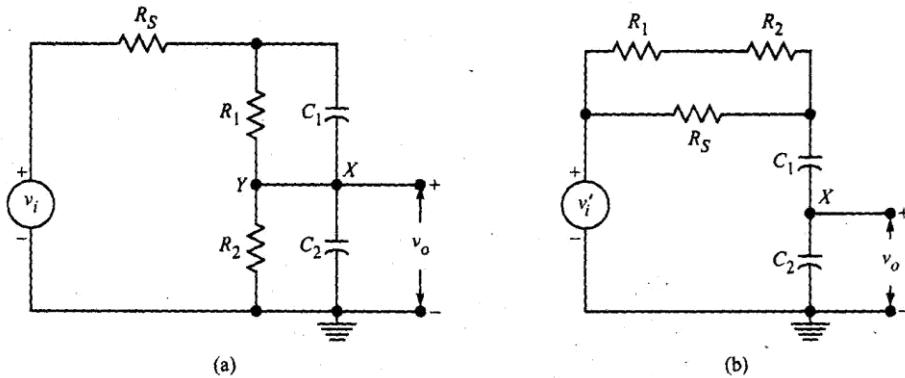
i.e.  $R_1 C_1 + R_2 C_1 = R_2 C_1 + R_2 C_2$

i.e.  $R_1 C_1 = R_2 C_2 \quad \text{or} \quad C_1 = \frac{R_2 C_2}{R_1}$

This is the balanced bridge condition. The extreme values of  $v_o(0^+)$  are 0 for  $C_1 = 0$ . In the above analysis we have assumed that an infinite current flows through the capacitors at  $t = 0^+$  and hence the capacitors get charged instantaneously. This is valid only if the generator resistance is zero. In general, the output resistance of the generator is not zero but is of some finite value. Hence the impulse response is physically impossible. So, even though the attenuator is compensated, the ideal step response can never be obtained. Nevertheless, an improvement in rise time does result if a compensated attenuator is used. For example, if the output is one-tenth of the input, then the rise time of the output using the attenuator is one-tenth of what it would be without the attenuator.

The compensated attenuator will reproduce faithfully the signal, which appears at its input terminals. However, if the output impedance of the generator driving the attenuator is not zero, the signal will be distorted right at the input to the attenuator. This situation is illustrated in Figure 1.63(a) in which a generator of step voltage  $V$  and of source resistance  $R_s$  is connected to the attenuator. Since the lead which joins the point X and point Y may be open circuited, the circuit may be redrawn as in Figure 1.63(b). Usually  $R_s \ll R_1 + R_2$ , so the input to the attenuator will be an exponential of time constant  $R_s C'$ , where  $C'$  is the capacitance of the series combination of  $C_1$  and  $C_2$  i.e.  $C' = C_1 C_2 / (C_1 + C_2)$ . It is this exponential waveform rather than the step, which the attenuator will transmit faithfully. If the generator terminals were

connected directly to the terminals to which the attenuator output is connected, the generator would see a capacitance  $C_2$ . In this case the waveform at these terminals would be an exponential with time constant  $T = R_S C_2$ .



**Figure 1.63** (a) Compensated attenuator including source resistance  $R_S$  and (b) its equivalent circuit with  $v'_i = V(R_1 + R_2)/(R_S + R_1 + R_2)$ .

When the attenuator is used<sup>a</sup> the time constant is  $\tau' = R_S C'$ .  $\frac{\tau'}{\tau} = \frac{C'}{C_2} = \frac{C_1}{C_1 + C_2} = a$  an improvement in waveform results. For example, if the attenuation is equal to 10( $a = 1/10$ ), then the rise time of the waveform would be divided by a factor 10.-

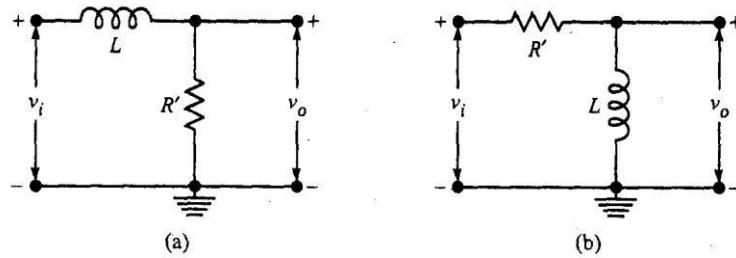
## RL CIRCUITS

In previous session we discussed the behaviour of  $RC$  low-pass and high-pass circuits for various types of input waveforms. Suppose the capacitor  $C$  and-resistor  $R$  in those circuits are replaced by a resistor  $R'$  and an inductor  $L$  respectively, then, if the time constant  $LIR'$  equals the time constant  $RC$ , all the preceding results remain unchanged.

When a large time constant is required, the inductor is rarely used because a large value of inductance can be obtained only with an iron-core inductor which is physically large, heavy and expensive relative to the cost of a capacitor for a similar application. Such an iron-cored inductor will be shunted with a large amount of stray distributed capacitance. Also the nonlinear properties of the iron cause distortion, which may be undesirable. If it is required to pass very low frequencies through a circuit in which  $L$  is a shunt element, then the inductor may become prohibitively large. Of course in circuits where a small value of  $L$  is tolerable, a more reasonable value of inductance may be used. In low time constant applications, a small inexpensive air-cored inductor may be used.

Figure 1.73(a) shows the  $RL$  low-pass circuit. At very low frequencies the reactance of the inductor is small, so the output across the resistor  $R'$  is almost equal to the input. As the frequency increases, the reactance of the inductor increases and so the signal is attenuated. At

very high frequencies the output is almost equal to zero. So the circuit in Figure 1.73(a) acts as a low-pass filter. The circuit of Figure 1.73(b) acts as a high-pass circuit because at low frequencies, since the reactance of the inductor is small, the output across the inductor is small and the output increases as the frequency increases because the reactance of the inductor increases as the frequency increases and at high frequencies the output is almost equal to the input.

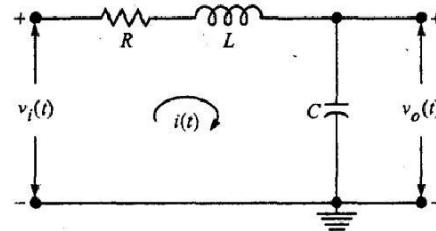


**Figure 1.73** (a) *RL* low-pass circuit and (b) *RL* high-pass circuit.

## RLC CIRCUITS

### RLC Series Circuit

Consider a series *RLC* circuit shown in Figure 1.75.



**Figure 1.75** A series *RLC* circuit.

Writing the KVL around the loop, we obtain

$$v_i(t) = Ri(t) + L \frac{di(t)}{dt} + \frac{1}{C} \int i(t) dt$$

Taking the Laplace transform on both sides,

$$V_i(s) = I(s) \left[ R + Ls + \frac{1}{Cs} \right] = \frac{I(s)}{Cs} [Ls^2 + Rcs + 1]$$

$$V_o(s) = I(s) \frac{1}{Cs}$$

The transfer function of the circuit of Figure 1.75 is

$$\frac{V_o(s)}{V_i(s)} = \frac{1}{LC \left[ s^2 + \frac{R}{L}s + \frac{1}{LC} \right]}$$

The roots of the characteristic equation  $s_1$  and  $s_2$  are the values of  $s$  satisfying the equation

$$s^2 + \frac{R}{L}s + \frac{1}{LC} = 0$$

$$\therefore s_1, s_2 = \frac{-R}{2L} \pm \sqrt{\left(\frac{R}{2L}\right)^2 - \frac{1}{LC}}$$

If  $(R/2L)^2 > 1/LC$ , i.e.  $R > 2\sqrt{L/C}$ , both the roots are real and different. The circuit is overdamped and there are no oscillations in the output. If  $(R/2L)^2 = 1/LC$ , i.e.  $R = 2\sqrt{L/C}$ , both the roots are real and equal. The circuit is critically damped. If  $(R/2L)^2 < 1/LC$ , i.e.  $R < 2\sqrt{L/C}$ , the roots are complex conjugate of each other. The circuit is underdamped and there will be oscillations in the output. The output is a sinusoid whose amplitude decays with time.

The term  $\sqrt{L/C}$  is known as the *characteristic impedance* of the circuit.

For a step input of amplitude  $V$ ,  $V_i(s) = \frac{V}{s}$

$$\therefore V_o(s) = \left( \frac{V}{LC} \right) \left( \frac{1}{s \left[ s^2 + \frac{R}{L}s + \frac{1}{LC} \right]} \right)$$

and

$$I(s) = \frac{V}{L \left[ s^2 + \frac{R}{L}s + \frac{1}{LC} \right]}$$

The current response is:

Case (a): overdamped circuit,  $R > 2\sqrt{L/C}$

$$i(t) = \frac{V}{2AL} \left[ e^{-s_1 t} - e^{-s_2 t} \right], \quad \text{here } s_1 > s_2$$

$$\text{where } A = \sqrt{\left(\frac{R}{2}\right)^2 - \frac{1}{LC}}$$

Case (b): critically damped circuit,  $R = 2\sqrt{L/C}$

$$i(t) = \frac{Vt}{L} e^{-Rt/2L}$$

Case (c): underdamped circuit,  $R < 2\sqrt{L/C}$

$$i(t) = \frac{V}{BL} e^{-Rt/2L} \sin Bt \quad \text{where } B = \sqrt{\frac{1}{LC} - \left(\frac{R}{2L}\right)^2}$$

The response of  $i(t)$  and the response of  $v_o(t)$  for the above three cases are shown in Figures 1.76(a) and 1.76(b) respectively.

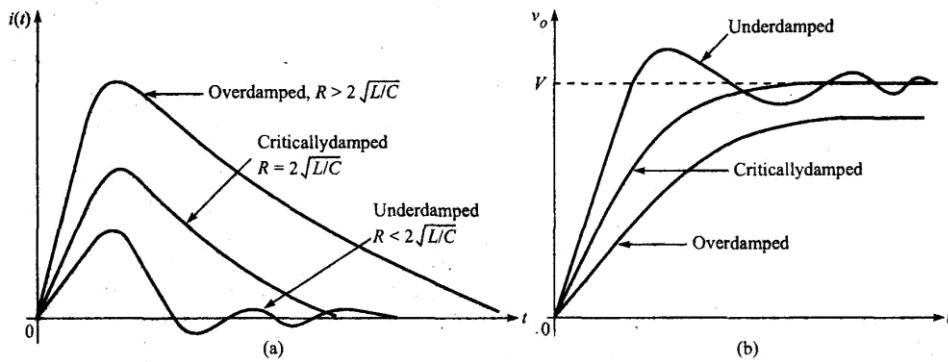


Figure 1.76 (a) Current response and (b) voltage response of series  $RLC$  circuit to a step voltage.

### **RLC Parallel Circuit**

In the  $RL$  circuit shown in Figure 1.73(b), to include the effect of coil winding capacitance, output capacitance and stray capacitance to ground, a capacitor is added across the output. So, the  $RLC$  circuit shown in Figure 1.77(a) results. In terms of a current source, the equivalent circuit shown in Figure 1.77(b) results.

The transfer function of the network of Figure 1.77(a) is

$$\frac{V_o(s)}{V_i(s)} = \frac{1}{RC} \left( \frac{s}{s^2 + \frac{1}{RC}s + \frac{1}{LC}} \right)$$

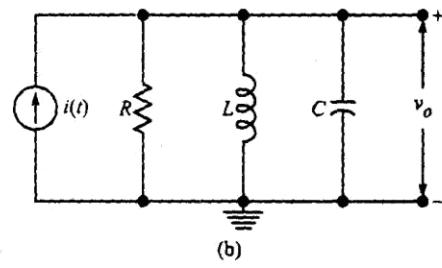
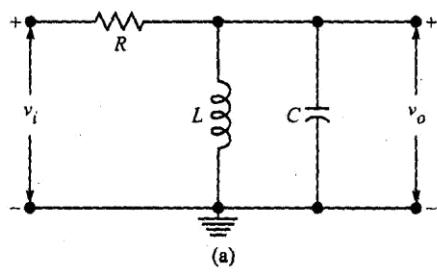
The roots of the characteristic equation are

$$s_1, s_2 = -\frac{1}{2RC} \pm \sqrt{\left(\frac{1}{2RC}\right)^2 - \frac{1}{LC}}$$

These are also the characteristic roots of the network in Figure 1.77(b).

The circuit is overdamped if  $R < \frac{1}{2}\sqrt{L/C}$ , critically damped if  $R = \frac{1}{2}\sqrt{L/C}$  and underdamped if  $R > \frac{1}{2}\sqrt{L/C}$ . The response to the voltage across the  $RLC$  parallel circuit is similar to that to the current through the  $RLC$  series circuit with the difference that the input to the  $RLC$  parallel circuit is a step current.

In the series  $RLC$  network, the current response to a step input voltage ultimately dies to zero because of the capacitor in series. In the parallel  $RLC$  circuit the voltage across the  $RLC$  network is zero because of the inductance.



**Figure 1.77** (a)  $v_i$  is applied through  $R$  to a parallel  $LC$  circuit and (b) parallel  $RLC$  circuit driven by a current source.

## UNIT – II

# NON LINEAR WAVESHAPING

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*Diode clippers, Transistor clippers, clipping at two independent levels, Transfer characteristics of clippers, Emitter coupled clipper, Comparators, applications of voltage comparators, clamping operation, clamping circuits using diode with different inputs, Clamping circuit theorem, practical clamping circuits, effect of diode characteristics on clamping voltage, Transfer characteristics of clampers.*

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In the previous chapter we discussed about linear wave shaping. We saw how a change of wave shape was brought about when a non-sinusoidal signal is transmitted through a linear network like  $RC$  low pass and high pass circuit. In this chapter, we discuss some aspects of nonlinear wave shaping like clipping and clamping. The circuits for which the outputs are non-sinusoidal for sinusoidal inputs are called nonlinear wave shaping circuits, for example clipping circuits and clamping circuits.

Clipping means cutting and removing a part. A clipping circuit is a circuit which removes the undesired part of the waveform and transmits only the desired part of the signal which is above or below some particular reference level, i.e. it is used to select for transmission that part of an arbitrary waveform which lies above or below some particular reference. Clipping circuits are also called *voltage* (or current) *limiters, amplitude selectors or slicers*.

Nonlinear wave shaping circuits may be classified as clipping circuits and clamping circuits. Clipping circuits may be single level clippers or two level clippers.

Single level clippers may be series diode clippers with and without reference or shunt diode clippers with and without reference. Clipping circuits may use diodes or transistors.

Clamping circuits may be negative clampers (positive peak clampers) with and without reference or positive clampers (negative peak clampers) with and without reference.

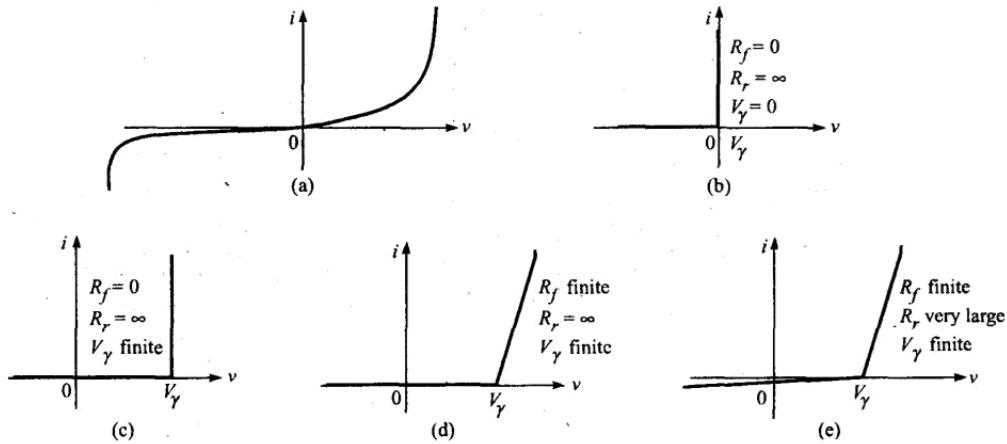
### **CLIPPING CIRCUITS**

In general, there are three basic configurations of clipping circuits.

1. A series combination of a diode, a resistor and a reference voltage.
2. A network consisting of many diodes, resistors and reference voltages.
3. Two emitter coupled transistors operating as a differential amplifier.

## Diode Clippers

Figure 2.1(a) shows the v-i characteristic of a practical diode. Figures 2.1(b), (c), (d), and (e) show the  $v$ - $i$  characteristics of an idealized diode approximated by a curve which is piece-wise linear and continuous. The break point occurs at  $V_r$ , where  $V_r = 0.2$  V for Ge and  $V_r = 0.6$  V for Si. Usually  $V_r$  is very small compared to the reference voltage  $V_R$  and can be neglected.



**Figure 2.1**  $v$ - $i$  characteristics of a diode.

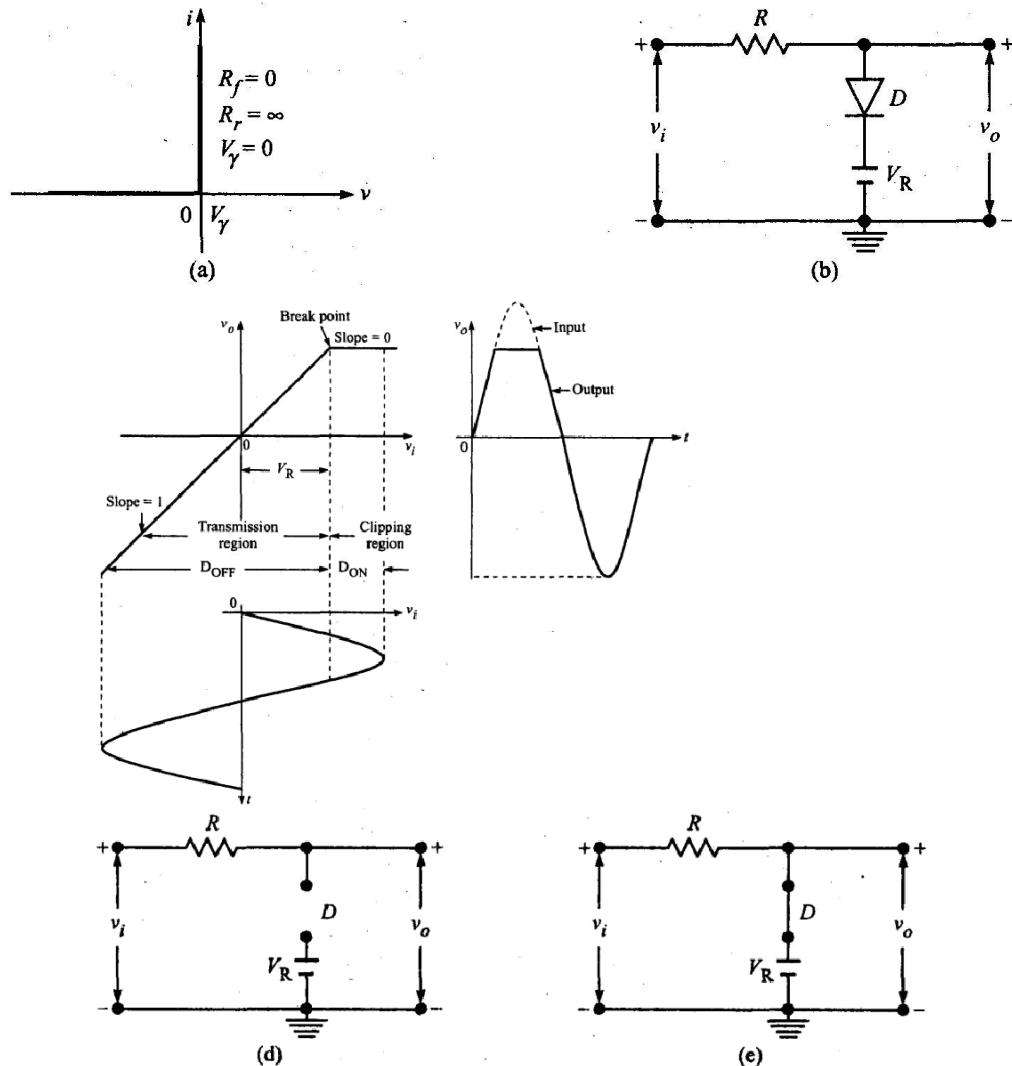
## Shunt Clippers

### Clipping above reference level

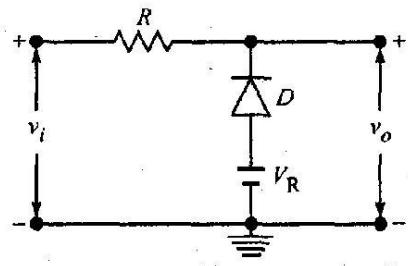
Using the ideal diode characteristic of Figure 2.2(a), the clipping circuit shown in Figure 2.2(b), has the transmission characteristic shown in Figure 2.2(c). The transmission characteristic which is a plot of the output voltage  $v_o$  as a function of the input voltage  $v$ , also exhibits piece-wise linear discontinuity. The break point occurs at the reference voltage  $V_R$ . To the left of the break point i.e. for  $v_t < V_R$  the diode is reverse biased (OFF) and the equivalent circuit shown in Figure 2.2(d) results. In this region the signal  $v$ , may be transmitted directly to the output, since there is no load across the output to cause a drop across the series resistor  $R_s$ . To the right of the break point i.e. for  $v_t > V_R$  the diode is forward biased (ON) and the equivalent circuit shown in Figure 2.2(e) results and increments in the inputs are totally attenuated and the output is fixed at  $V_R$ . Figure 2.2(c) shows a sinusoidal input signal of amplitude large enough so that the signal makes excursions past the break point. The corresponding output exhibits a suppression of the positive peak of the signal. The output will appear as if the positive peak had been *clipped off* or *sliced off*.

## Clipping below reference level

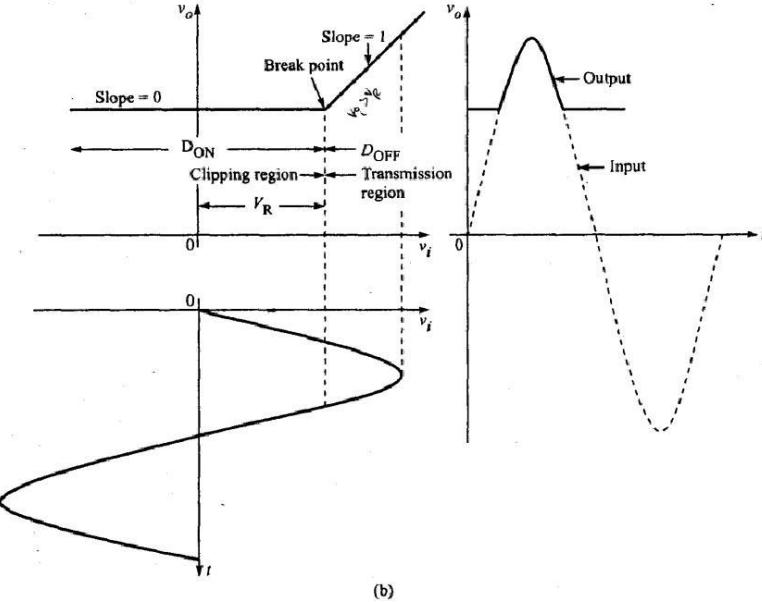
If this clipping circuit of Figure 2.2(b), is modified by reversing the diode as shown in Figure 2.3(a), the corresponding piece-wise linear transfer characteristic and the output for a sinusoidal input will be as shown in Figure 2.3(b). In this circuit, the portion of the waveform more positive than  $V_R$  is transmitted without any attenuation but the portion of the waveform less positive than  $V_R$  is totally suppressed. For  $V_j < V_R$ , the diode conducts and acts as a short circuit and the equivalent circuit shown in Figure 2.3(c) results and the output is fixed at  $V_R$ . For  $v_j > V_R$ , the diode is reverse biased and acts as an open circuit and the equivalent circuit shown in Figure 2.3(d) results and the output is the same as the input.



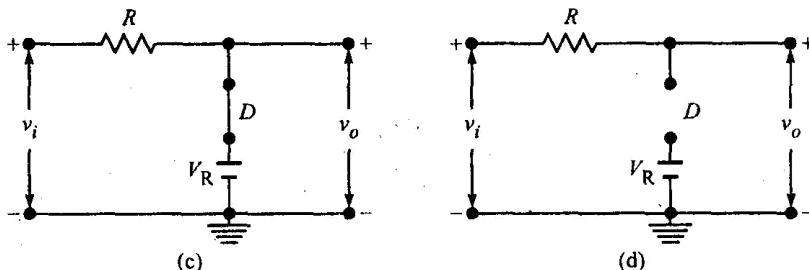
**Figure 2.2** (a)  $v$ - $i$  characteristic of an ideal diode, (b) diode clipping circuit, which removes that part of the waveform that is more positive than  $V_R$ , (c) the piece-wise linear transmission characteristic of the circuit, a sinusoidal input and the clipped output, (d) equivalent circuit for  $v_i < V_R$ , and (e) equivalent circuit for  $v_i > V_R$ .



(a)



(b)



(c)

(d)

**Figure 2.3** (a) A diode clipping circuit, which transmits that part of the sine wave that is more positive than  $V_R$ , (b) the piece-wise linear transmission characteristic, a sinusoidal input and the clipped output, (c) equivalent circuit for  $v_i < V_R$ , and (d) equivalent circuit for  $v_i > V_R$ .

In Figures 2.1(b) and 2.2(a), we assumed that  $R_r = \infty$  and  $R_f = 0$ . If this condition does not apply, the transmission characteristic must be modified. The portions of those curves which are indicated as having unity slope must instead be considered as having a slope of  $R_r l(R_r + R)$ , and those, having zero slope as having a slope of  $1/(R_r + R)$ . In the transmission region of a diode clipping circuit, it is required that  $R_r \gg R$ , i.e.  $R_r = kR$ , where  $k$  is a large number, and in the attenuation region, it is required that  $R \gg R_f$ . From

these equations we can deduce that  $R = J R_r x R^{\wedge}$ , i.e. the external resistance  $R$  is to be selected as the geometric mean of  $R_f$  and  $/?.$ . The ratio  $R_r I R_f$  serves as a figure of merit for the diodes used in these applications. A zener diode may also be used in combination with a *p-n* junction diode to obtain single-ended clipping, i.e. one-level clipping.

## Series Clippers

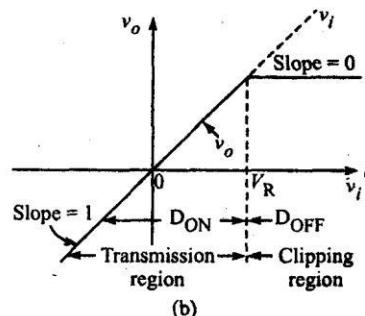
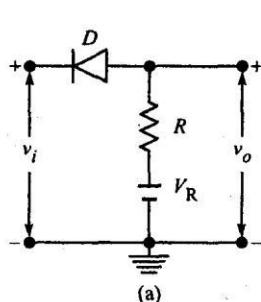
### Clipping above the reference voltage $V_R$

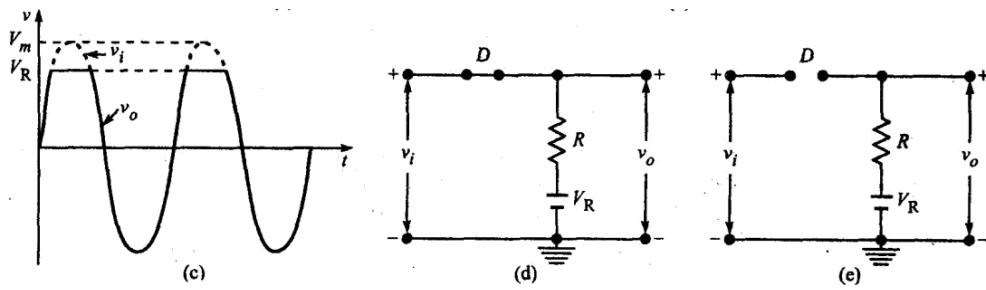
Figure 2.4(a) shows a series clipper circuit using a *p-n* junction diode.  $V_R$  is the reference voltage source. The diode is assumed to be ideal ( $/? = 0$ ,  $R_r = \infty$ ,  $V_y = 0$ ) so that it acts as a short circuit when it is ON and as an open circuit when it is OFF. Since the diode is in the series path connecting the input and the output it is called a series clipper. The  $v_o$  versus  $v_i$  characteristic called the *transfer characteristic* is shown in Figure 2.4(b). The output for a sinusoidal input is shown in Figure 2.4(c).

The circuit works as follows:

For  $v_i < V_R$ , the diode  $D_j$  is forward biased because its anode is at a higher potential than its cathode. It conducts and acts as a short circuit and the equivalent circuit shown in Figure 2.4(d) results. The difference voltage between the input  $v_i$  and the reference voltage  $V_R$  i.e.  $(V_R - v_i)$  is dropped across . Therefore  $v_o = v_i$  and the slope of the transfer characteristic for  $v_i < V_R$  is 1. Since the input signal is transmitted to the output without any change, this region is called the transmission region.

–  $v_i$ ) is dropped across . Therefore  $v_o = v_i$  and the slope of the transfer characteristic for  $v_i < V_R$  is 1. Since the input signal is transmitted to the output without any change, this region is called the transmission region.



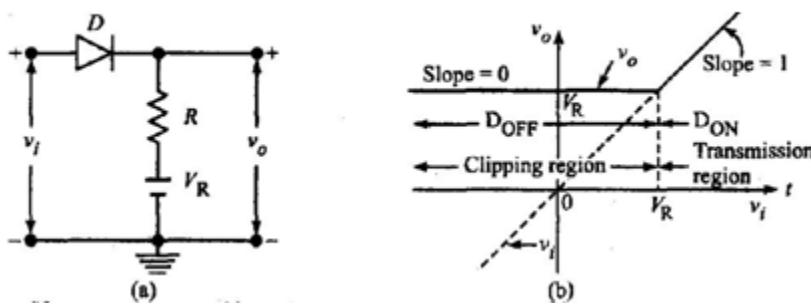


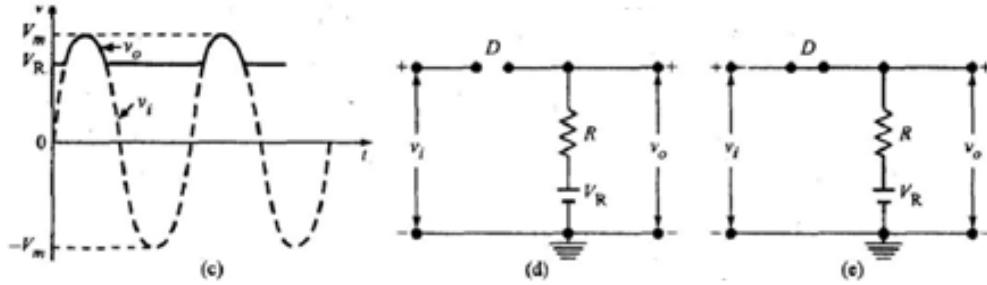
**Figure 2.4** (a) Diode series clipper circuit diagram, (b) transfer characteristic, (c) output waveform for a sinusoidal input, (d) equivalent circuit for  $v_i < V_R$ , and (e) equivalent circuit for  $v_i > V_R$ .

For  $v_i > V_R$ , the diode is reverse biased because its cathode is at a higher potential than its anode, it does not conduct and acts as an open circuit and the equivalent circuit shown in Figure 2.4(e) results. No current flows through  $R$  and so no voltage drop across it. So the output voltage  $v_o = V_R$  and the slope of the transfer characteristic is zero. Since the input signal above  $V_R$  is clipped OFF for  $v_i > V_R$ , this region is called the *clipping region*. The equations  $V_0=V_i$  for  $V_i < V_R$  and  $V_0=V_R$  for  $V_i > V_R$  are called the transfer characteristic equations.

### Clipping below the reference voltage $V_B$

Figure 2.5(a) shows a series clipper circuit using a p-n junction diode and a reference voltage source  $V_R$ . The diode is assumed to be ideal ( $R_f = 0$ ,  $R_r = \infty$ ,  $V_y = 0$ ) so that it acts as a short circuit when it is ON and as an open circuit when it is OFF. Since the diode is in the series path connecting the input and the output it is called a series clipper. The transfer characteristic is shown in Figure 2.5(b). The output for a sinusoidal input is shown in Figure 2.5(c).





**Figure 2.5** (a) Diode series clipper circuit diagram, (b). transfer characteristics, (c) output for a sinusoidal input, (d) equivalent circuit for  $v_i < V_R$ , and (e) equivalent circuit for  $v_i > V_R$ .

The circuit works as follows:

For  $v_i < V_R$ , D is reverse biased because its anode is at a lower potential than its cathode. The diode does not conduct and acts as an open circuit and the equivalent circuit shown in Figure 2.5(d) results. No current flows through  $R$  and hence no voltage drop across  $R$  and hence  $v_o = V_R$ . So the slope of the transfer characteristic is zero for  $v_i < V_R$ . Since the input is clipped off for  $v_i < V_R$ , this region is called the clipping region.

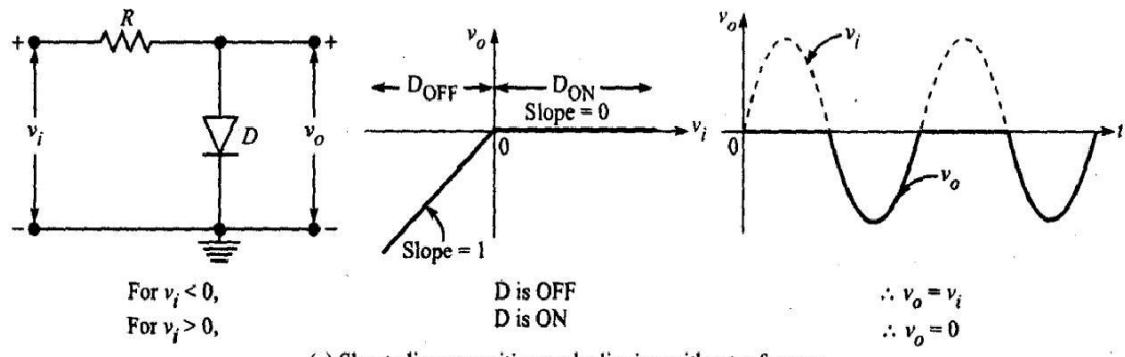
For  $v_i > V_R$ , the diode is forward biased because its anode is at a higher potential than its cathode. The diode conducts and acts as a short circuit and the equivalent circuit shown in Figure 2.5(e) results. Current flows through  $R$  and the difference voltage between the input and the output voltages  $v_i - V_R$  drops across  $R$  and the output  $v_o = v_i$ . The slope of the transfer characteristic for  $v_i > V_R$  is unity. Since the input is transmitted to the output for  $v_i > V_R$ , this region is called the transmission region. The equations are called the transfer characteristic equations.

$$v_o = V_R \text{ for } v_i < V_R$$

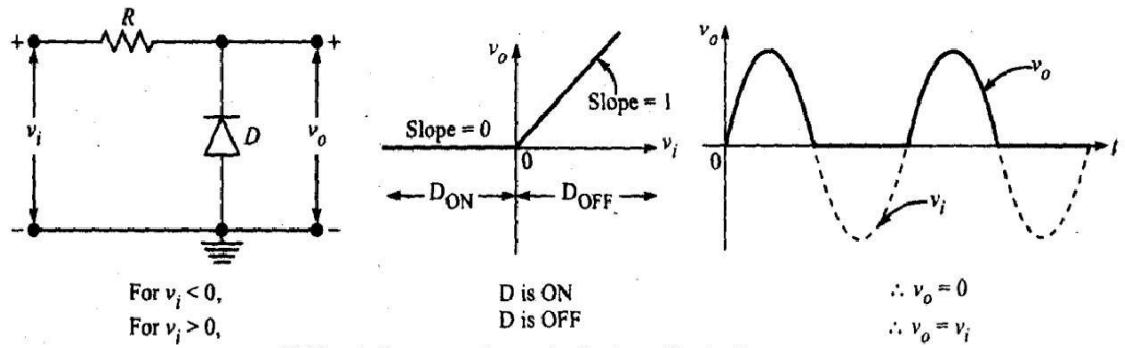
$$v_o = v_i \text{ for } v_i > V_R$$

Some single-ended diode clipping circuits, their transfer characteristics and the output waveforms for sinusoidal inputs are shown below (Figure 2.6).

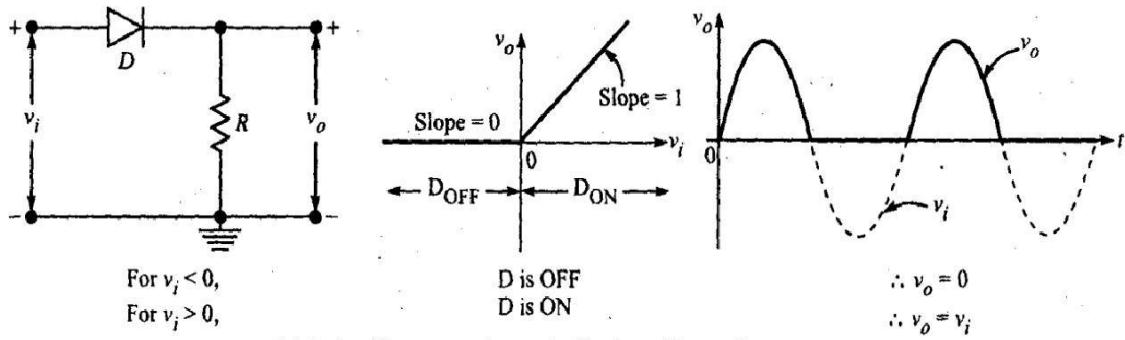
## Some single-ended clipping circuits



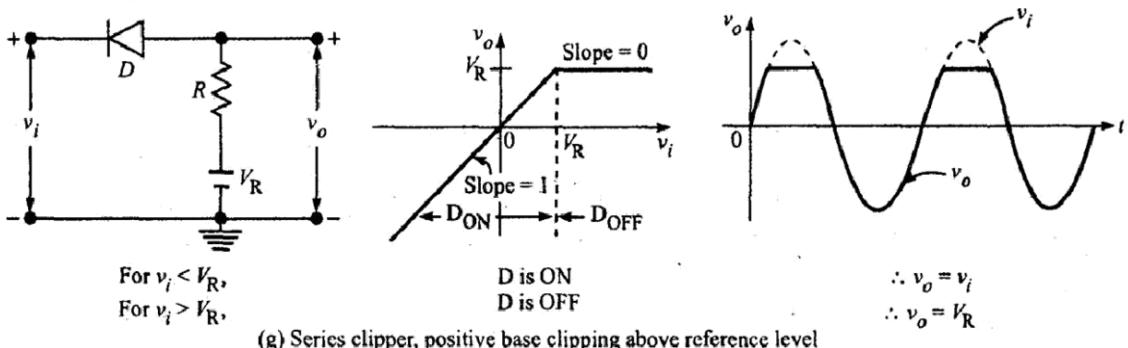
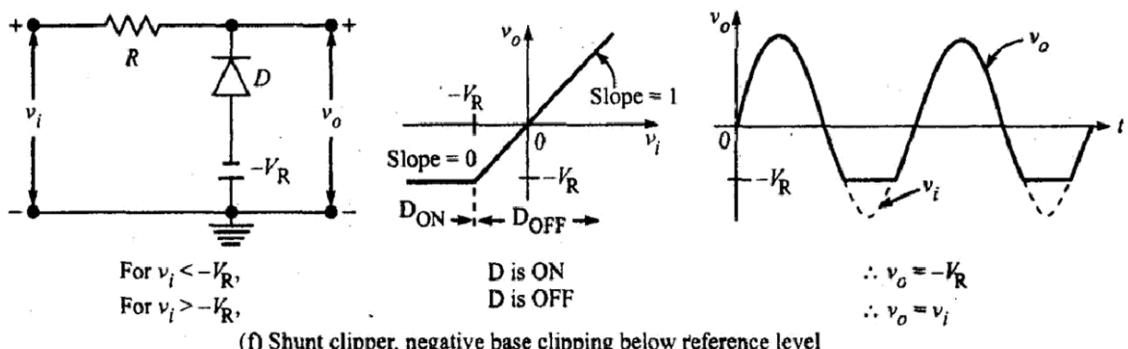
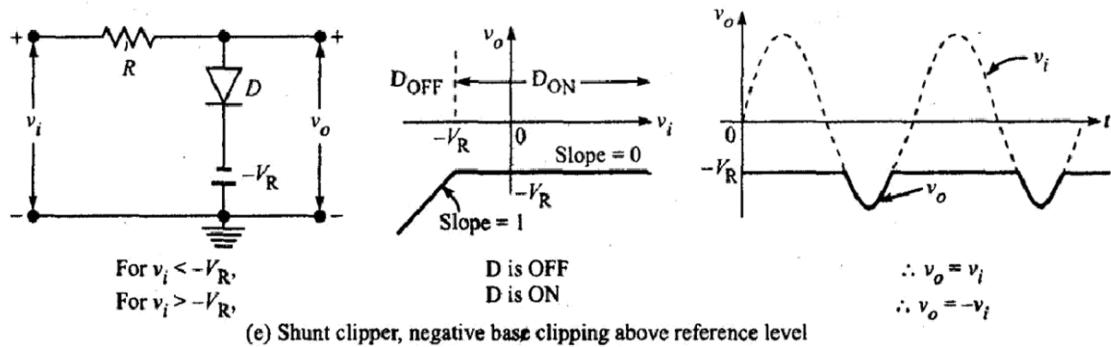
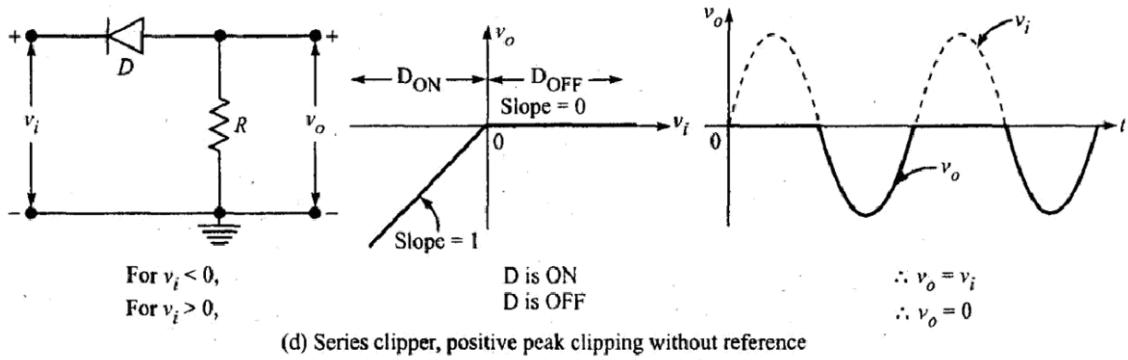
(a) Shunt clipper, positive peak clipping without reference

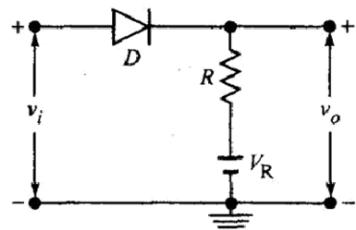


(b) Shunt clipper, negative peak clipping without reference

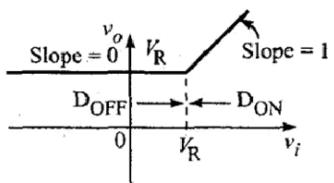


(c) Series clipper, negative peak clipping without reference

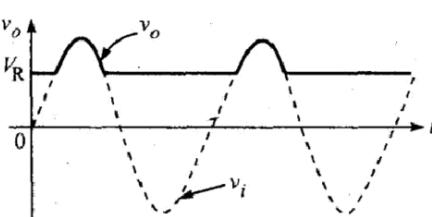




For  $v_i < V_R$ ,  
For  $v_i > V_R$ ,

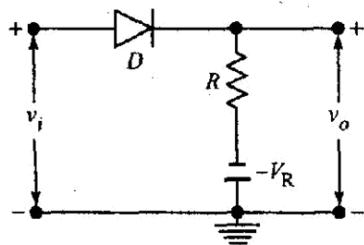


D is OFF  
D is ON

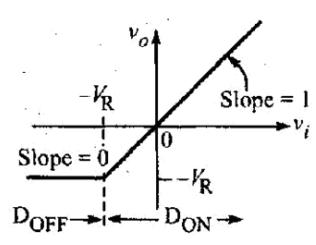


$\therefore v_o = V_R$   
 $\therefore v_o = v_i$

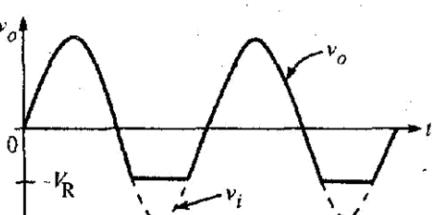
(h) Series clipper, positive base clipping before reference level



For  $v_i < -V_R$ ,  
For  $v_i > -V_R$ ,

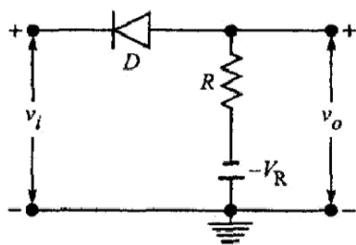


D is OFF  
D is ON

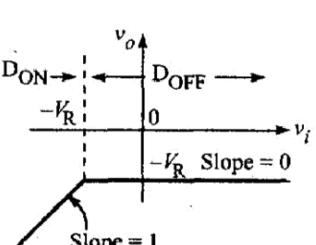


$\therefore v_o = -V_R$   
 $\therefore v_o = v_i$

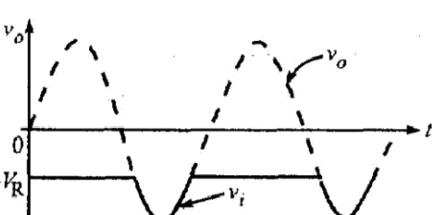
(i) Series clipper, negative base clipping above reference level



For  $v_i < -V_R$ ,  
For  $v_i > -V_R$ ,

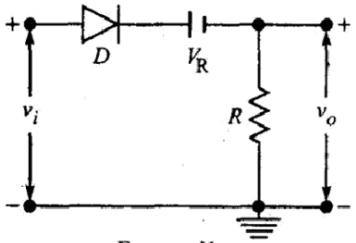


D is ON  
D is OFF

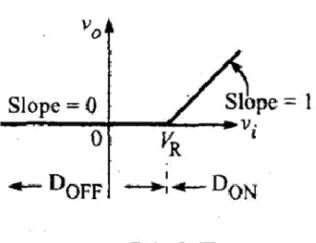


$\therefore v_o = v_i$   
 $\therefore v_o = -V_R$

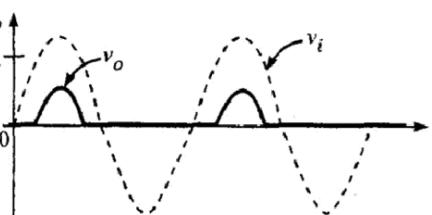
(j) Series clipper, negative base clipping above reference level



For  $v_i < V_R$ ,  
For  $v_i > V_R$ ,

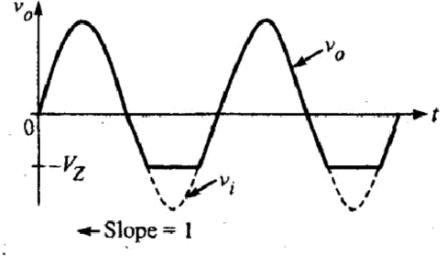
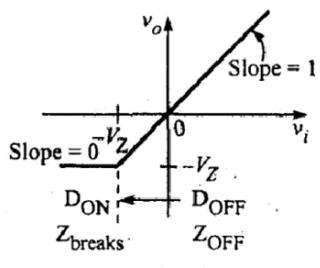
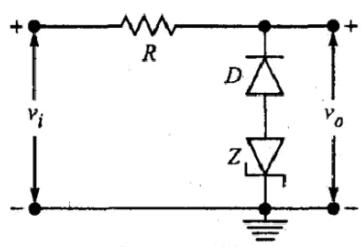
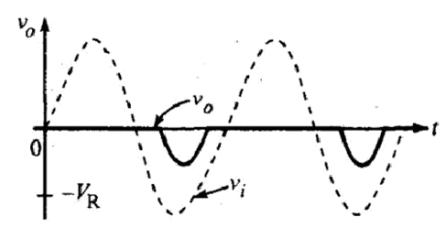
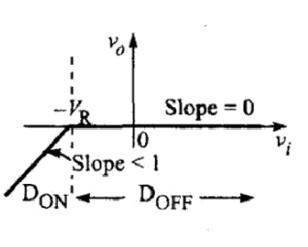
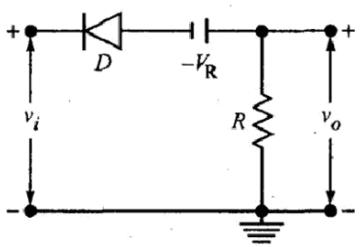
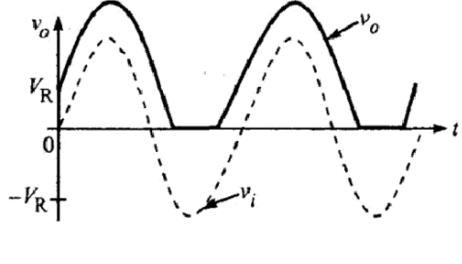
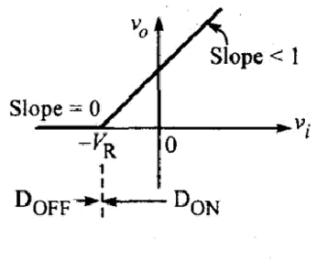
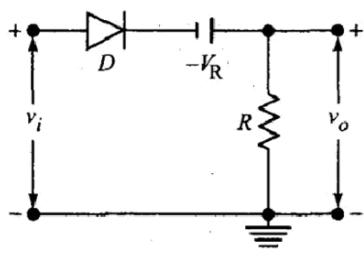
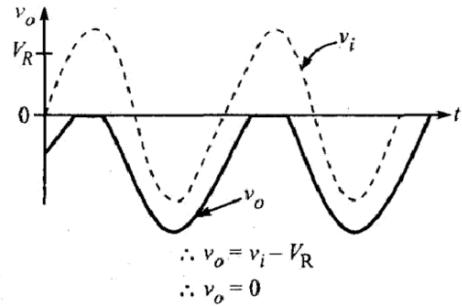
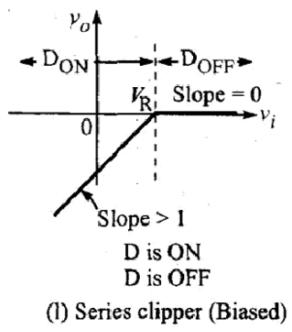
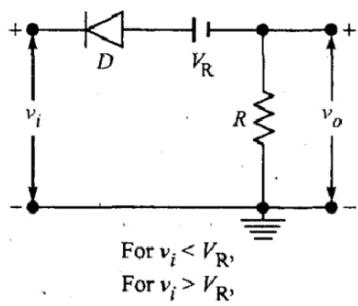


D is OFF  
D is ON

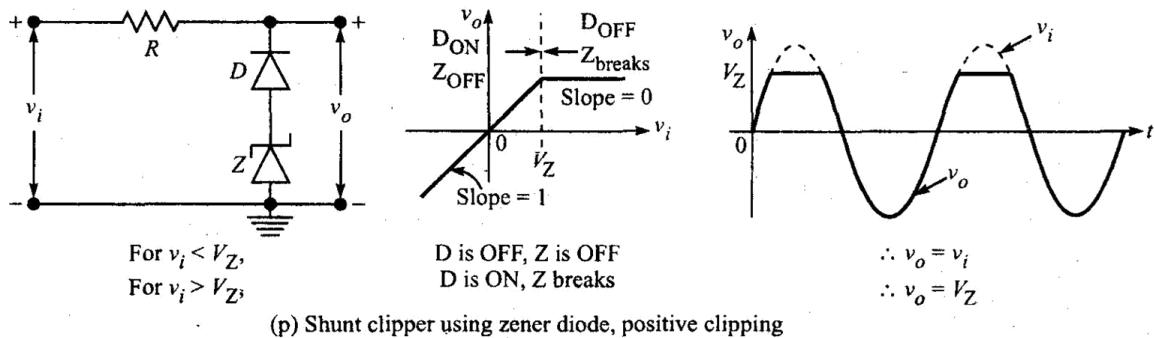


$\therefore v_o = 0$   
 $\therefore v_o = v_i - V_R$

(k) Series clipper (Biased)



(o) Shunt clipper using zener diode, negative clipping



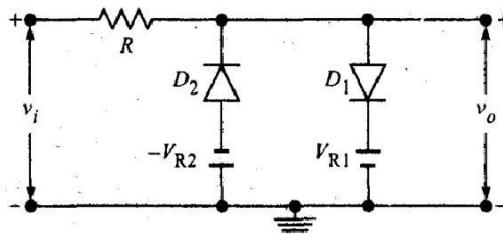
**Figure 2.6** Examples of single-ended clipping circuits.

In the clipping circuits, the diode may appear as a series element or as a shunt element. The use of the diode as a series element has the disadvantage that when the diode is OFF and it is intended that there be no transmission, fast signals or high frequency waveforms may be transmitted to the output through the diode capacitance. The use of the diode as a shunt element has the disadvantage that when the diode is open and it is intended that there be transmission, the diode capacitance together with all other capacitances in shunt with the output terminals will round off the sharp edges of the input waveforms and attenuate the high frequency signals.

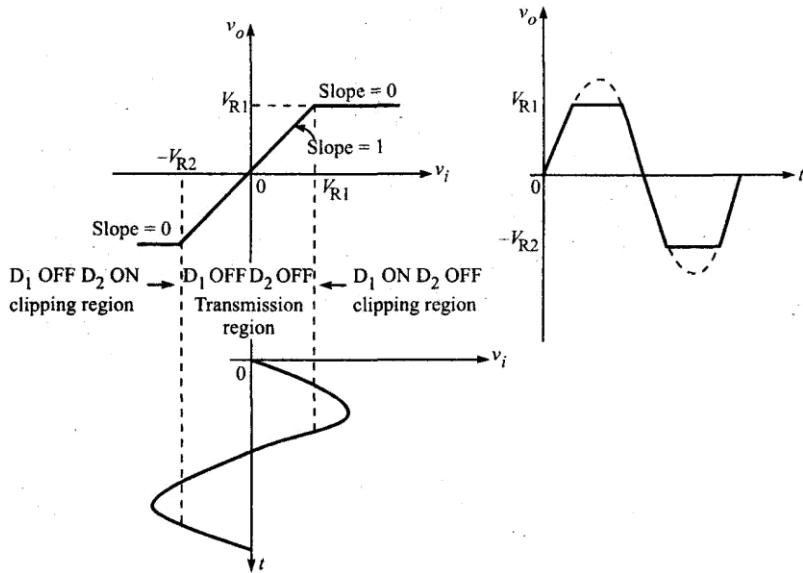
### Clipping at Two Independent Levels

A parallel, a series, or a series-parallel arrangement may be used in double-ended limiting at two independent levels. A parallel arrangement is shown in Figure 2.7. Figure 2.8 shows the transfer characteristic and the output for a sinusoidal input. The input-output characteristic has two breakpoints, one at  $v_0 = v_+ = V_{R1}$  and the second at  $v_0 = v_- = -V_{R2}$  and has the following characteristics.

<i>Input</i> $v_i$	<i>Output</i> $v_o$	<i>Diode status</i>
$v_i > V_{R1}$	$v_o = V_{R1}$	$D_1$ ON, $D_2$ OFF
$-V_{R2} < v_i < V_{R1}$	$v_o = v_i$	$D_1$ OFF, $D_2$ OFF
$v_i < -V_{R2}$	$v_o = -V_{R2}$	$D_1$ OFF, $D_2$ ON

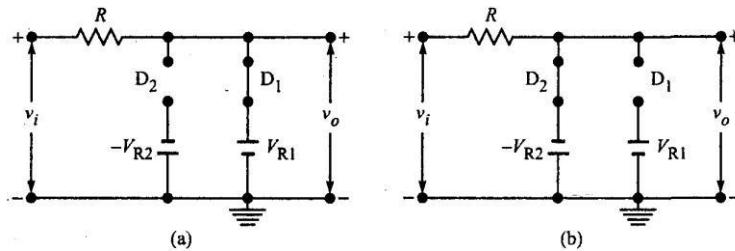


**Figure 2.7** A diode clipper which limits at two independent levels.



**Figure 2.8** The piece-wise linear transfer curve, the input sinusoidal waveform and the corresponding output for the clipper of Figure 2.7.

The two level diode clipper shown in Figure 2.8 works as follows. For  $v_i > V_{R1}$ , D1 is ON and D2 is OFF and the equivalent circuit shown in Figure 2.9(a) results. So the output  $v_o = V_{R1}$  and the slope of the transfer characteristic is zero.

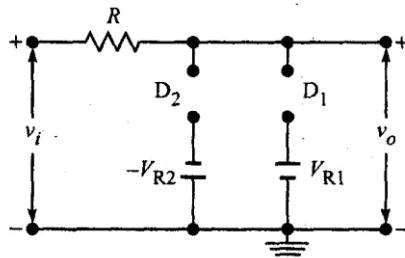


**Figure 2.9** (a) Equivalent circuit for  $v_i > V_{R1}$  and (b) equivalent circuit for  $v_i < -V_{R2}$ .

For  $v_i < -V_{R2}$ , D1 is OFF and D2 is ON and the equivalent circuit shown in Figure 2.9(b) results. So the output  $v_o = -V_{R2}$  and the slope of the transfer characteristic is zero. For  $-V_{R2} < v_i < V_{R1}$ , D1 is OFF and D2 is OFF and the equivalent circuit shown in Figure 2.10 results. So the output  $v_o = v_i$  and the slope of the transfer characteristic is one.

The circuit of Figure 2.7 is called a slicer because the output contains a slice of the input between two reference levels  $V_{R1}$  and  $V_{R2}$ . Looking at the input and output waveforms, we observe that this circuit may be used to convert a sine wave into a square wave, if  $V_{DI} = V_m$  and if the amplitude of the input signal is very large compared with the difference in the

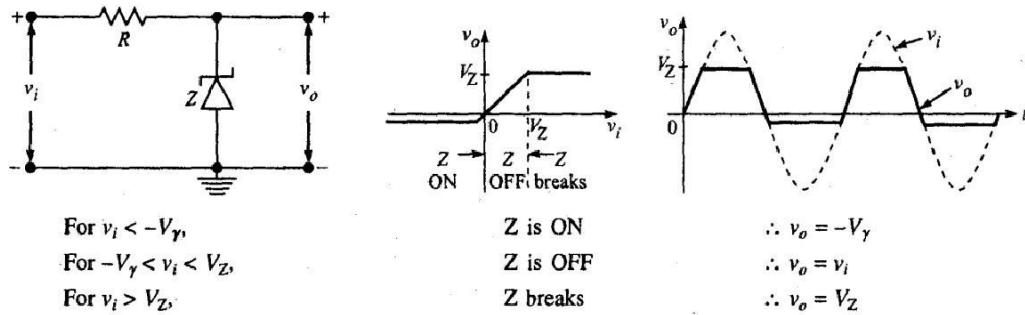
reference levels, the output will be a symmetrical square wave. Two zener diodes in series opposing may also be used to form a double-ended clipper.



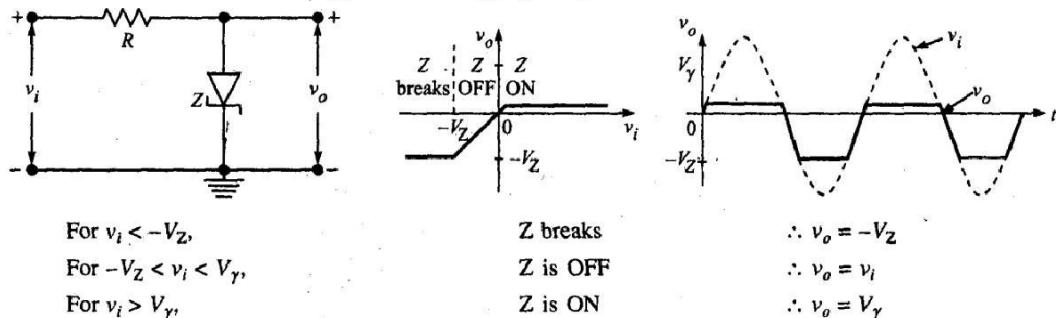
**Figure 2.10** Equivalent circuit for  $-V_{R2} < v_i < V_{R1}$ .

If the diodes have identical characteristics, then, a symmetrical limiter is obtained. Some double-ended clippers, their transfer characteristics and the outputs for sine wave inputs are shown in Figure 2.11.

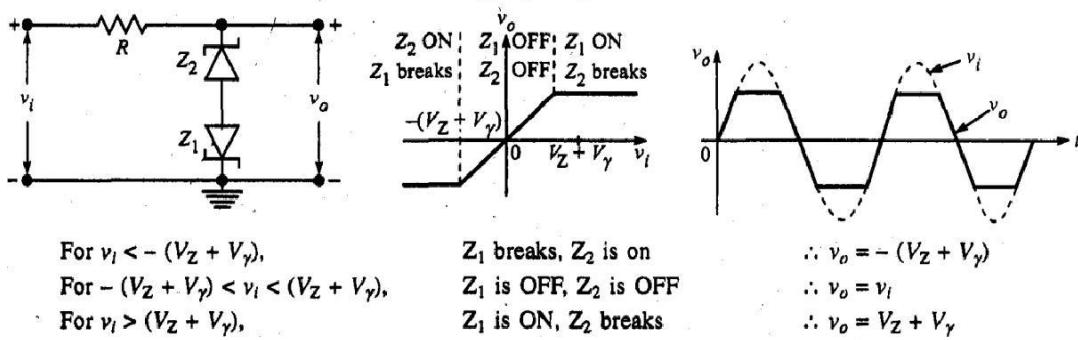
### Some double-ended clipping circuits



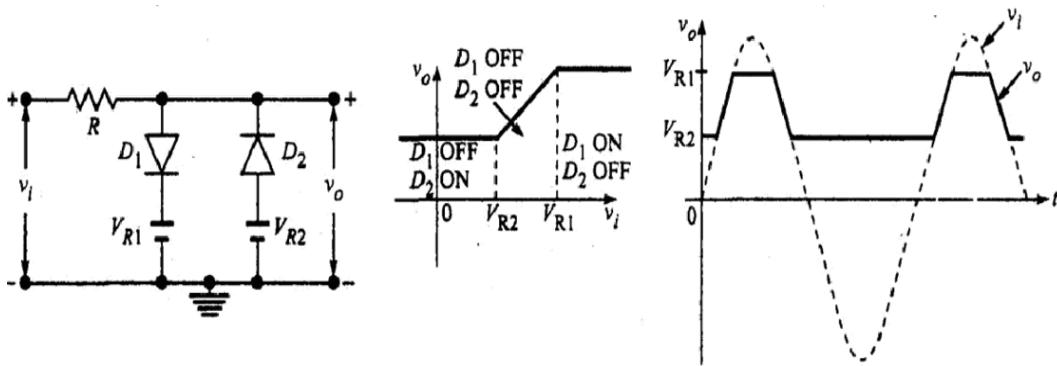
(a) Two level clipping using a zener diode



(b) Two level clipping using one zener diode



(c) Two level clipping using two zener diodes



$$V_{R2} < V_{R1}$$

For  $v_i < V_{R2}$ ,

$D_1$  is OFF,  $D_2$  is ON

$$\therefore v_o = V_{R2}$$

For  $V_{R2} < v_i < V_{R1}$ ,

$D_1$  is OFF,  $D_2$  is OFF

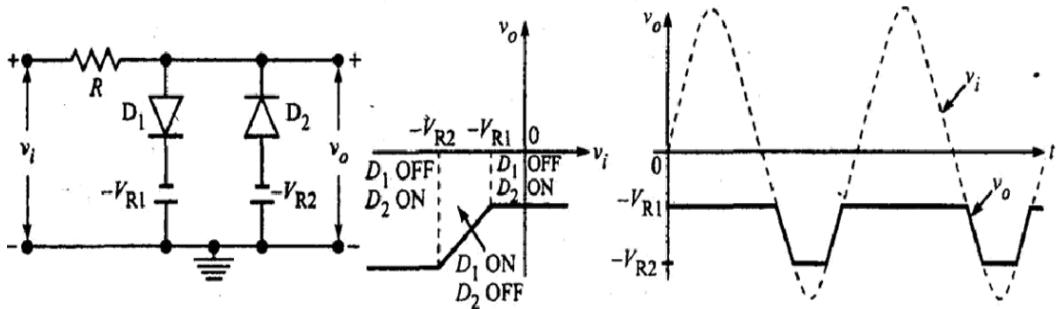
$$\therefore v_o = v_i$$

For  $v_i > V_{R1}$ ,

$D_1$  is ON,  $D_2$  is OFF

$$\therefore v_o = V_{R1}$$

(d) Two level clipping using two diodes and two positive reference voltage sources.



$$-V_{R2} < -V_{R1}$$

For  $v_i < -V_{R2}$ ,

$D_1$  is OFF,  $D_2$  is ON

$$\therefore v_o = -V_{R2}$$

For  $-V_{R2} < v_i < -V_{R1}$ ,

$D_1$  is OFF,  $D_2$  is OFF

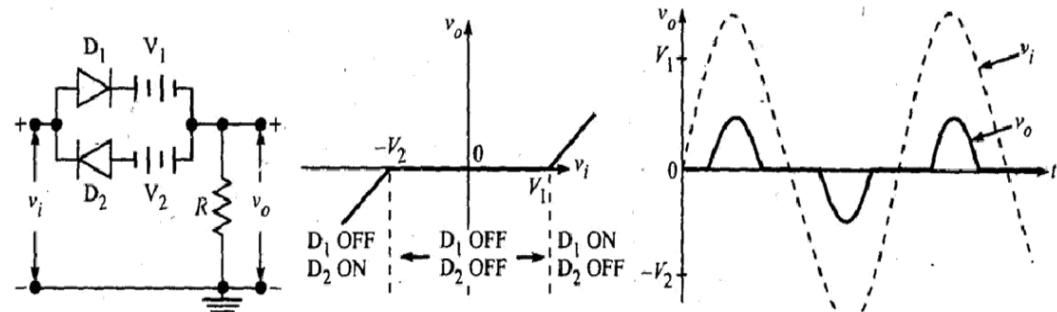
$$\therefore v_o = v_i$$

For  $v_i > -V_{R1}$ ,

$D_1$  is ON,  $D_2$  is OFF

$$\therefore v_o = -V_{R1}$$

(e) Two level clipping using two diodes and two negative reference voltage sources.



For  $v_i < -V_2$ ,

$D_1$  is OFF,  $D_2$  is ON

$$\therefore v_o = v_i + V_2$$

For  $-V_2 < v_i < V_1$ ,

$D_1$  is OFF,  $D_2$  is OFF

$$\therefore v_o = 0$$

For  $v_i > V_1$ ,

$D_1$  is ON,  $D_2$  is OFF

$$\therefore v_o = v_i - V_1$$

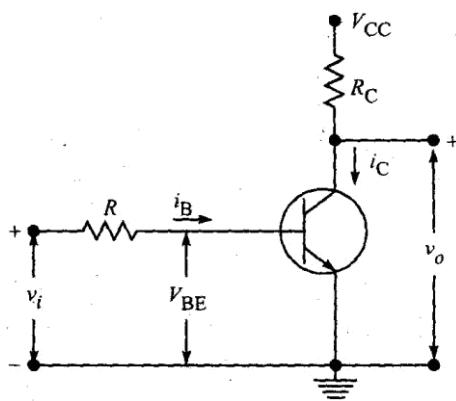
(f) Double ended series biased clipper

Figure 2.11 Examples of double-ended clippers.

## Transistor Clippers

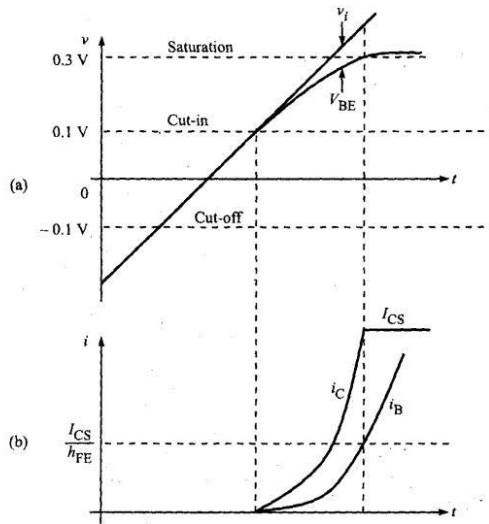
A nonlinear device is required for clipping purposes. A diode exhibits a nonlinearity, which occurs when it goes from OFF to ON. On the other hand, the transistor has two pronounced nonlinearities, which may be used for clipping purposes. One occurs when the transistor crosses from the cut-in region into the active region and the second occurs when the transistor crosses from the active region into the saturation region. Therefore, if the peak-to-peak value of the input waveform is such that it can carry the transistor across the boundary between the cut-in and active regions, or across the boundary between the active and saturation regions, a portion of the input waveform will be clipped. Normally, it is required that the portion of the input waveform, which keeps the transistor in the active region shall appear at the output without distortion. In that case, it is required that the input current rather than the input voltage be the waveform of the signal of interest. The reason for this requirement is that over a large signal excursion in the active region, the transistor output current responds nominally linearly to the input current but is related in a quite nonlinear manner to the input voltage. So, in transistor clippers a current drive needs to be used.

A transistor clipper is shown in Figure 2.19. The resistor  $R$  which represents either the signal source impedance or a resistor deliberately introduced must be large compared with the input resistance of the transistor in the active region. Under these circumstances, the input base current will very nearly have the waveform of the input voltage, because the base current is given by  $i_B = (v_i - V_r)/R$  where  $V_r$  is the base-to-emitter cut-in voltage.  $V_y \gg 0.1$  V for Ge and  $V_y \sim 0.5$  V for Si.



**Figure 2.19** A transistor clipper.

If a ramp input signal  $v_i$  which starts at a voltage below cut-off and carries the transistor into saturation is applied, the base voltage, the base current, and the collector current waveforms of the transistor clipper will be as shown in Figure 2.20.



**Figure 2.20** Waveforms of the transistor clipper of Figure 2.19: (a) voltage  $V_{BE}$  which results when a ramp input drives the transistor from cut-off into saturation, and (b) the base and collector currents.

The waveforms which result when a sinusoidal voltage  $v$ , carries the transistor from cut-off to saturation are shown in Figure 2.21. The base circuit is biased so that cut-in occurs when  $V_{BE}$  reaches the voltage  $V$ .

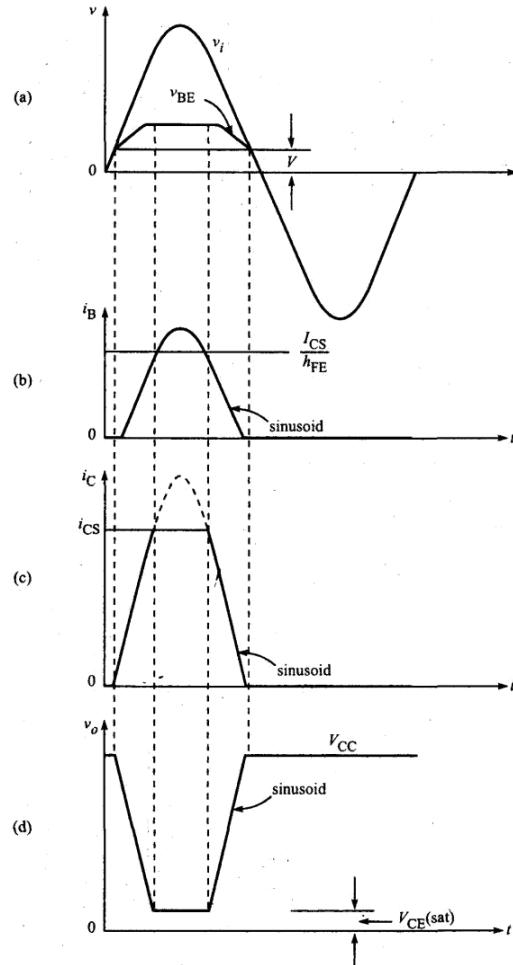


Figure 2.21 Waveforms for the transistor clipper of figure 2.19: (a) input voltage and the base – to-emitter voltage (b) the base current (c) the collector current (d) the output voltage

### Emitter-Coupled Clipper

An emitter-coupled clipper is shown in Figure 2.22. It is a two-level clipper using transistors. The base of Q<sub>2</sub> is fixed at a voltage V<sub>BB2</sub>, and the input is applied to B<sub>1</sub>. If initially the input is negative, Q<sub>1</sub> is OFF and only Q<sub>2</sub> carries the current. Assume that V<sub>BB2</sub> has been adjusted so that Q<sub>2</sub> operates in its active region. Let us assume that the current / in the emitter resistance is constant. This is valid if IV<sub>BE2</sub>I is small compared to V<sub>BB2</sub> + V<sub>EE</sub>. When v<sub>t</sub> is below the cut-off point of Q<sub>1</sub>, all the current I flows through Q<sub>2</sub>. As v<sub>t</sub> increases, Q<sub>1</sub> will eventually come out of cut-off, both the transistors will be carrying currents but the current in Q<sub>2</sub> decreases while the current in Q<sub>1</sub> increases, the sum of the currents in the two transistors remaining constant and equal to I. The input signal appears at the output, amplified but not inverted. As v<sub>1</sub> continues to increase, the common emitter will follow the base of Q<sub>1</sub>. Since the base of Q<sub>2</sub> is fixed, a point will be reached when the rising emitter voltage cuts off Q<sub>2</sub>. Thus, the input signal is amplified but twice limited, once by the cutoff of Q<sub>1</sub> and once by the onset of cut-off in Q<sub>2</sub>. The total range A<sub>v0</sub>, over which the output can follow the input is V<sub>E</sub> and is constant and therefore adjustable through an adjustment of I. The absolute voltage of the portion of the input waveform selected for transmission may be selected through an adjustment of a biasing voltage on which v<sub>t</sub> is superimposed or through an adjustment of V<sub>BB2</sub>. The total range of input voltage A<sub>v</sub>, between the clipping limits is A<sub>v0</sub>/A, where A is the gain of the amplifier stage. Figure 2.23 shows the transfer characteristic of an emitter-coupled clipper.

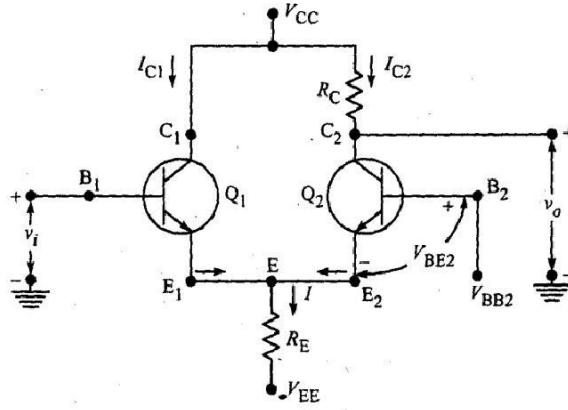


Figure 2.22 An emitter-coupled clipper.

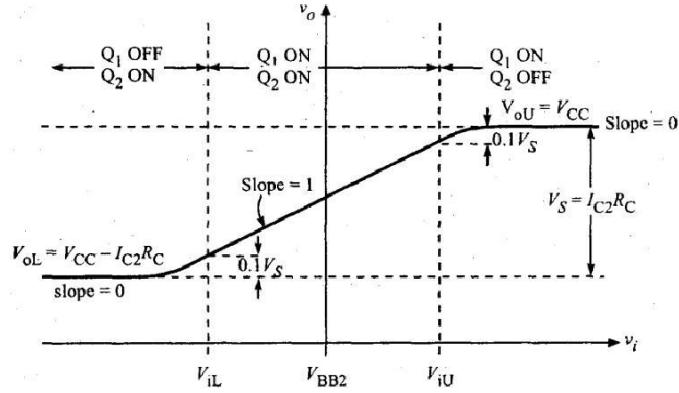


Figure 2.23 The transfer characteristic of the emitter-coupled clipper.

## Comparators

A comparator circuit is one, which may be used to mark the instant when an arbitrary waveform attains some particular reference level. The nonlinear circuits, which can be used to perform the operation of clipping may also be used to perform the operation of comparison. In fact, the clipping circuits become elements of a comparator system and are usually simply referred to as comparators. The distinction between comparator circuits and the clipping circuits is that, in a comparator there is 'no interest in reproducing any part of the signal waveform, whereas in a clipping circuit, part of the signal waveform is needed to be reproduced without any distortion.

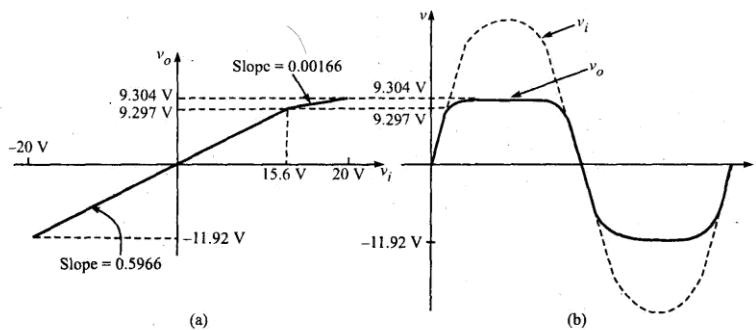


Figure 2.69 Example 2.19: (a) transfer characteristic and (b) output waveform in the presence of  $R_L$ .

Figure 2.70 shows the circuit diagram of a diode comparator. As long as the input voltage  $v_i$  is less than the reference voltage  $V_R$ , the diode D is ON and the output is fixed at  $V_R$ . When  $v_i > V_R$ , the diode is OFF and hence  $v_o = v_i$ . The break occurs at  $v_i = V_R$  at time  $t = t_1$ . So, this circuit can be used to mark the instant at which the input voltage reaches a particular reference level  $V_R$ .

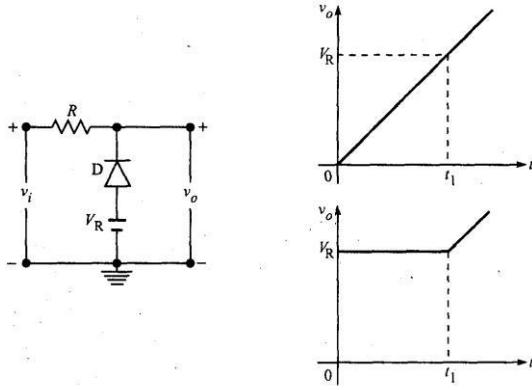


Figure 2.70 Diode comparator.

Comparators may be non-regenerative or regenerative. Clipping circuits fall into the category of non-regenerative comparators. In regenerative comparators, positive feedback is employed to obtain an infinite forward gain (unity loop gain). The Schmitt trigger and the blocking oscillator are examples of regenerative comparators. The Schmitt trigger comparator generates approximately a step input. The blocking oscillator comparator generates a pulse rather than a step output waveform. Most applications of comparators make use of the step or pulse natures of the input. Operational amplifiers and tunnel diodes may also be used as comparators.

### **Applications of voltage comparators**

Voltage comparators may be used:

1. In accurate time measurements
2. In pulse time modulation
3. As timing markers generated from a sine wave.
4. In phase meters
5. In amplitude distribution analyzers
6. To obtain square wave from a sine wave
7. In analog-to-digital converters.

## CLAMPING CIRCUITS

Clamping circuits are circuits, which are used to clamp or fix the extremity of a periodic waveform to some constant reference level  $V_R$ . Under steady-state conditions, these circuits restrain the extremity of the waveform from going beyond  $V_R$ . Clamping circuits may be one-way clamps or two-way clamps. When only one diode is used and a voltage change in only one direction is restrained, the circuits are called one-way clamps. When two diodes are used and the voltage change in both the directions is restrained, the circuits are called two-way clamps.

### The Clamping Operation

When a signal is transmitted through a capacitive coupling network ( $RC$  high-pass circuit), it loses its dc component, and a clamping circuit may be used to introduce a dc component by fixing the positive or negative extremity of that waveform to some reference level. For this reason, the clamping circuit is often referred to as *dc restorer* or *dc inserter*. In fact, it should be called a *dc inserter*, because the dc component introduced may be different from the dc component lost during transmission. The clamping circuit only changes the dc level of the input signal. It does not affect its shape.

### Classification of clamping circuits

Basically clamping circuits are of two types: (1) positive-voltage clamping circuits and (2) negative-voltage clamping circuits.

In positive clamping, the negative extremity of the waveform is fixed at the reference level and the entire waveform appears above the reference level, i.e. the output waveform is positively clamped with respect to the reference level. In negative clamping, the positive extremity of the waveform is fixed at the reference level and the entire waveform appears below the reference, i.e. the output waveform is negatively clamped with respect to the reference level. The capacitors are essential in clamping circuits. The difference between the clipping and clamping circuits is that while the clipper clips off an unwanted portion of the input waveform, the clamper simply clamps the maximum positive or negative peak of the waveform to a desired level. There will be no distortion of waveform.

### Negative Clamp

Figure 3.1 (a) shows the circuit diagram of a basic negative clamper. It is also termed a positive peak clamper since the circuit clamps the positive peak of a signal to zero level. Assume that the signal source has negligible output impedance and that the diode " is ideal,  $R_f = 0 \text{ n}$  and  $V_y = 0 \text{ V}$  in that, it exhibits an arbitrarily sharp break at 0 V, and that its input signal shown in Figure 2.71(b) is a sinusoid which begins at  $t = 0$ . Let the capacitor C be uncharged at  $t = 0$ .

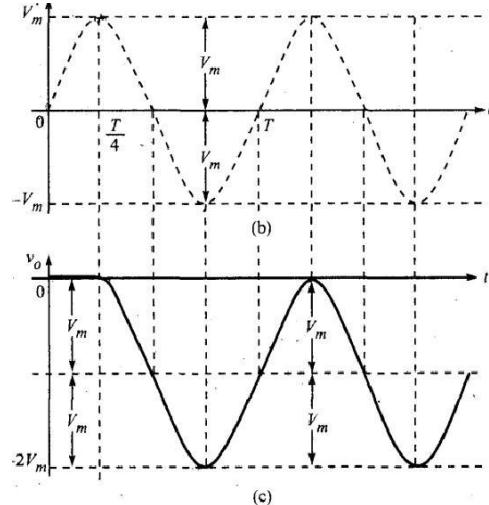
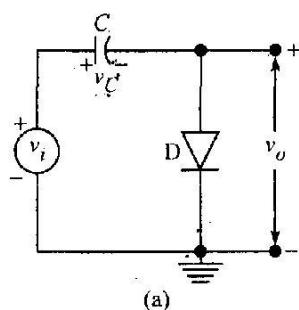
During the first quarter cycle, the input signal rises from zero to the maximum value. The diode conducts during this time and since we have assumed an ideal diode, the voltage across it is zero. The capacitor  $C$  is charged through the series combination of the signal source and the diode and the voltage across  $C$  rises sinusoidally. At the end of the first quarter cycle, the voltage across the capacitor,  $v_C = V_m$ . When, after the first quarter cycle, the peak has been passed and the input signal begins to fall, the voltage  $v_C$  across the capacitor is no longer able to follow the input, because there is no path for the capacitor to discharge. Hence, the voltage across the capacitor remains constant at  $v_C = V_m$ , and the charged capacitor acts as a voltage source of  $V$  volts and after the first quarter cycle, the output is given by  $v_o = v_i - V_m$ . During the succeeding cycles, the positive extremity of the signal will be *clamped* or *restored* to zero and the output

for  $v_i = 0$ ,  $v_o = -V_m$ .

for  $v_i = V_m$ ,  $v_o = 0$ ,

for  $v_i = -V_m$ ,  $v_o = -2V_m$ .

waveform shown in Figure 2.71(c) results. Therefore

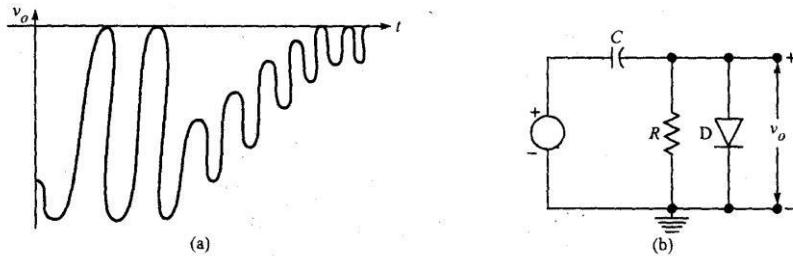


**Figure 2.71** (a) A negative clamping circuit, (b) a sinusoidal input, and (c) a steady-state clamped output.

Suppose that after the steady-state condition has been reached, the amplitude of the input signal is increased, then the diode will again conduct for at most one quarter cycle and the dc voltage across the capacitor would rise to the new peak value, and the positive excursions of the signal would be again restored to zero.

Suppose the amplitude of the input signal is decreased after the steady-state condition has been reached. There is no path for the capacitor to discharge. To permit the voltage across the capacitor to decrease, it is necessary to shunt a resistor across  $C$ , or equivalently to shunt a

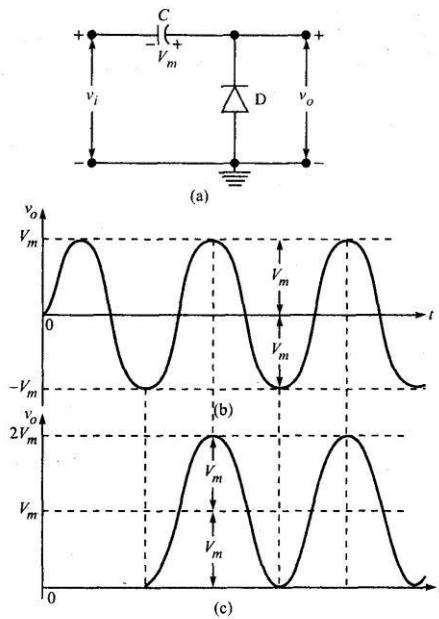
resistor across D. In the latter case, the capacitor will discharge through the series combination of the resistor  $R$  across the diode and the resistance of the source, and in a few cycles the positive extremity would be again clamped at zero as shown in Figure 2.72(b). A circuit with such a resistor ' $R$ ' is shown in Figure 2.72(a).



**Figure 2.72** (a) Clamping circuit with a resistor  $R$  across the diode D and (b) output during transient period.

### Positive Clamper

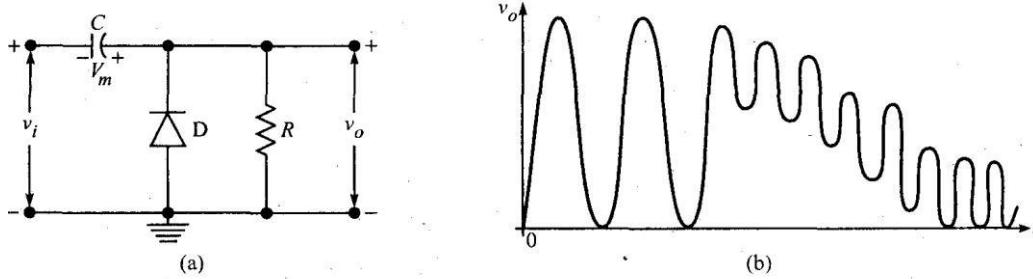
Figure 2.73(a) shows a positive clamper. This is also termed as negative peak clamper since this circuit clamps the negative peaks of a signal to zero level. The negative peak clamper, i.e. the positive clamper introduces a positive dc.



**Figure 2.73** (a) A positive clamping circuit, (b) a sinusoidal input, and (c) a steady-state clamped output.

Let the input voltage be  $v_i = V_m \sin(ot)$  as shown in Figure 2.73(b). When  $v_i$  goes negative, the diode gets forward biased and conducts and in a few cycles the capacitor gets charged to  $V_m$  with the polarity shown in Figure 2.73(a). Under steady-state conditions, the capacitor acts as a constant voltage source and the output is  $v_o = v_i - (-V_m) = v_i + V_m$ .

Based on the above relation between  $v_o$  and  $v_i$ , the output voltage waveform is plotted. As seen in Figure 2.73(c) the negative peaks of the input signal are clamped to zero level. Peak-to-peak value of output voltage = peak-to-peak value of input voltage =  $2V_m$ . There is no distortion of waveform. To accommodate for variations in amplitude of input, the diode D is shunted with a resistor as shown in Figure 2.74(a). When the amplitude of the input waveform is reduced, the output will adjust to its new value as shown in Figure 2.74(b).



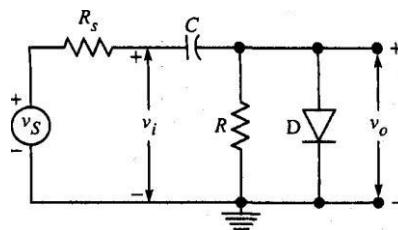
**Figure 2.74** (a) Clamping circuit with a resistor  $R$  across D and (b) output during transient period.

### Biased Clamping

If a voltage source of  $V_R$  volts is connected in series with the diode of a clamping circuit, the input waveform will be clamped with reference to  $V_R$ . Depending on the position of the diode, the input waveform may be positively clamped with reference to  $V_R$ , or negatively clamped with reference to  $V_R$ .

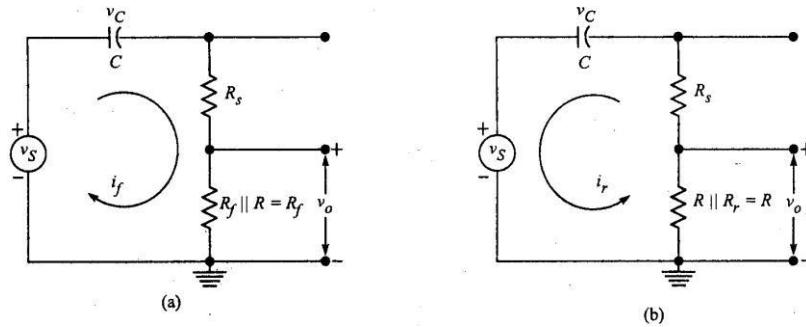
### Clamping Circuit Taking Source and Diode Resistances Into Account

In the discussion of the clamping circuit of Figure 2.71, we neglected the output resistance of the source as well as the diode forward resistance. Many times these resistances cannot be neglected. Figure 2.79 shows a more realistic clamping circuit taking into consideration the output resistance of the source  $R_s$ , which may be negligible or may range up to many thousands of ohms depending on the source, and the diode forward resistance  $R_f$  which may range from tens to hundreds of ohms. Assume that the diode break point  $V_y$  occurs at zero voltage.



**Figure 2.79** Clamping circuit considering the source resistance and the diode forward resistance.

The precision of operation of the circuit depends on the condition that  $R \gg R_f$ , and  $R_r \gg R$ . When the input is positive, the diode is ON and the equivalent circuit shown in Figure 2.80(a) results. When the input is negative, the diode is OFF and the equivalent circuit shown in Figure 2.80(b) results.



**Figure 2.80** (a) Equivalent circuit when the diode is conducting and (b) the equivalent circuit when the diode is not conducting.

### The transient waveform

When a signal is suddenly applied to the circuit shown in Figure 2.79 the capacitor charges (transient period) and gradually the steady-state condition is reached in which the positive peaks will be clamped to zero. The equivalent circuits shown in Figures 2.80(a) and 2.80(b) may be used to calculate the transient response.

### Relation between tilts in forward and reverse directions

**The steady-state output waveform for a square wave input.** Consider that the square wave input shown in Figure 2.82(a) is applied to the clamping circuit shown in Figure 2.79. The general form of the output waveform would be as shown in Figure 2.82(b), extending in both positive and negative directions and is determined by the voltages  $V_1$ ,  $V_2$ ,  $V_1'$ , and  $V_2'$ . These voltages may be calculated as discussed below.

In the interval  $0 < t < T_1$ , the input is at its higher level; so the diode is ON and the capacitor charges with a time constant  $(R_s + R_f)C$ , and the output decays towards zero with the same time constant. Hence,  $V_1' = V_1 e^{-T_1/(R_f+R_s)C}$  ----- (i)

In the interval  $T_1 < t < T_1 + T_2$ , the input is at its lower level; so the diode is OFF and the capacitor discharges with a time constant  $(R + R_s)C$ , and the output rises towards zero with the same time constant. Hence  $V_2' = V_2 e^{-T_2/(R+R_s)C}$  ----- (ii)

**Considering the conditions at  $t=0$ .** At  $t = 0\sim$ ,  $v_s = V''$ ,  $v_0 = V_2$ , the diode D is OFF and the equivalent circuit of Figure 2.80(b) results. The voltage across the capacitor is given by

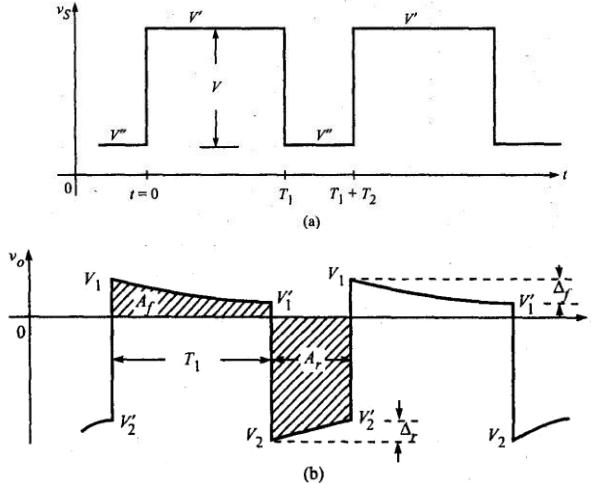
$$v_C = V'' - \frac{V'_2}{R} (R + R_S) \quad \text{---(iii)}$$

At  $t = 0^+$ , the input signal jumps to  $V$ , the output jumps to  $V_t$ , the diode conducts and the equivalent circuit of Figure 2.80(a) results. The voltage across the capacitor is given by

$$v_C = V' - \frac{V_1}{R_f} (R_f + R_S) \quad \text{---(iv)}$$

Since the voltage across the capacitor cannot change instantaneously, equating equations (iii) and (iv), we have

$$\begin{aligned} V' - \frac{V_1(R_f + R_S)}{R_f} &= V'' - \frac{V'_2(R + R_S)}{R} \\ V' - V'' &= V = \frac{V_1(R_f + R_S)}{R_f} - \frac{V'_2(R + R_S)}{R} \end{aligned} \quad \text{---(v)}$$



**Figure 2.82** (a) A square wave input signal of peak-to-peak amplitude  $V$ , (b) the general form of the steady-state output of a clamping circuit with the input as in (a).

**Considering the conditions at  $t = T_r$ .** At  $t = T_r$ ,  $v_s = V$ ,  $v_o = V_1$ , the diode D is ON, and the equivalent circuit of Figure 2.80(a) results. The voltage across the capacitor is given by

$$v_C = V' - \frac{V_1}{R_f} (R_f + R_S) \quad \text{---(vi)}$$

At  $t = T_r$ ,  $v_s = V'' = v_o = V_2$ , the diode D is OFF, and the equivalent circuit of Figure 2.80(b) results.

The voltage across the capacitor is given by

$$v_C = V'' - \frac{V_2}{R} (R + R_S) \quad \text{---(vii)}$$

Since the voltage across the capacitor cannot change instantaneously, equating equations (vi) and (vii), we get

$$V' - \frac{V'_1(R_f + R_s)}{R_f} = V'' - \frac{V_2(R + R_s)}{R}$$

$$V' - V'' = V = \frac{V'_1(R_f + R_s)}{R_f} - \frac{V_2(R + R_s)}{R} \quad \text{-----(viii)}$$

From equations (i), (ii), (v) and (viii), the values  $V_1$ ,  $V'$ ,  $V_2$  and  $V_2'$  can be computed and the output waveform determined.

If the source impedance is taken into account, the output voltage jumps are smaller than the abrupt discontinuity  $V$  in the input. Only if  $R_s = 0$ , are the jumps in input and output voltages equal. Thus, when  $R_s = 0$ ,  $V_1 - V'_1 = V_2 - V_2' = V$ . Observe that the response is independent of the absolute levels  $V'$  and  $V''$  of the input signal and is determined only by the amplitude  $V$ . It is possible, for example, for  $V''$  to be negative or even for both  $V$  and  $V''$  to be negative.

The average level of the input plays no role in determining the steady-state output waveform.

Under steady-state conditions, there is a tilt in the output waveform in both positive and negative directions. The relation between the tilts can be obtained by subtracting Eq. (viii) from Eq. (v), i.e.

$$\frac{R_f + R_s}{R_f}(V_1 - V'_1) - \frac{R + R_s}{R}(V'_2 - V_2) = 0$$

Where,

$$V_1 - V'_1 = \Delta_f = \text{tilt in the forward direction}$$

$$V'_2 - V_2 = \Delta_r = \text{tilt in the reverse direction}$$

$$\therefore \Delta_f = \frac{R_f}{R_f + R_s} \times \frac{R + R_s}{R} \Delta_r$$

Since  $R_s$  is usually much smaller than  $R$ , then, the tilt in the forward direction  $\Delta_f$  is almost always less than the tilt  $\Delta_r$  in the reverse direction. Only when  $R_s \ll R_f$ , are the two tilts almost equal.

### Clamping Circuit Theorem

Under steady-state conditions, for any input waveform, the shape of the output waveform of a clamping circuit is fixed and also the area in the forward direction (when the diode conducts) and the area in the reverse direction (when the diode does not conduct) are related.

*The clamping circuit theorem states that, for any input waveform under steady-state conditions, the ratio of the area  $A_f$  under the output voltage curve in the forward direction to that in the reverse direction  $A_r$  is equal to the ratio  $R//R_f$ .*

This theorem applies quite generally independent of the input waveform and the magnitude of the source resistance. The proof is as follows:

Consider the clamping circuit of Figure 2.79, the equivalent circuits in Figures 2.80(a) and 2.80(b), and the input and output waveforms of Figures 2.82(a) and 2.82(b) respectively.

In the interval  $0 < t < T_f$ , the input is at its upper level, the diode is ON, and the equivalent circuit of Figure 2.80(a) results. If  $v_f(t)$  is the output waveform in the forward direction, then the

capacitor charging current is  $i_f(t) = \frac{v_f(t)}{R_f}$ . Therefore, the charge gained by the capacitor during

$$Q_g = \int_0^{T_f} i_f(t) dt = \frac{1}{R_f} \int_0^{T_f} v_f(t) dt = \frac{A_f}{R_f}$$

the forward interval is

In the interval  $T_f < t < T_f + T_r$ , the input is at its lower level, the diode is OFF, and the equivalent circuit of Figure 2.80(b) results. If  $v_r(t)$  is the output voltage in the reverse direction,

then the current which discharges the capacitor is  $i_r(t) = \frac{v_r(t)}{R}$

Therefore, the charge lost by the capacitor during the reverse interval is

$$Q_r = \int_{T_f}^{T_f + T_r} i_r(t) dt = \frac{1}{R} \int_{T_f}^{T_f + T_r} v_r(t) dt = \frac{A_r}{R}$$

Under steady-state conditions, the net charge acquired by the capacitor over one cycle must be equal to zero. Therefore, the charge gained in the interval  $0 < t < T_f$ , will be equal to the charge lost in the interval  $T_f < t < T_f + T_r$ , i.e.  $Q_g = Q_r$

$$\frac{A_f}{R_f} = \frac{A_r}{R} \quad \text{i.e.} \quad \frac{A_f}{A_r} = \frac{R_f}{R}$$

Multivibrators are electronic circuits that produce non-sinusoidal waveforms, typically square waves, with two distinct output states. They are often used in digital electronics for applications such as clock generation, pulse shaping, and signal generation. There are three main types of multivibrators: astable, monostable, and bistable. Each type has unique characteristics and applications.

### 1. Astable Multivibrator:

- Also known as a free-running multivibrator or oscillator.
- It does not have a stable state; it continuously oscillates between two distinct states (high and low) without any external triggering.
- The output waveform is a continuous square wave.
- Commonly used for generating clock signals, timing pulses, and square wave generators in various digital circuits.
- It consists of two transistors (bipolar or field-effect) or other switching components connected in a feedback loop.

### 2. Monostable Multivibrator:

- Also known as a one-shot or pulse generator.
- It has one stable state and one unstable state. It is triggered into the unstable state by an external input pulse and returns to the stable state after a predetermined time period.
- The output pulse width is determined by external components, such as resistors and capacitors.
- Used for generating single, fixed-width pulses in applications like debounce circuits, time delay generators, and pulse width modulation.

### 3. Bistable Multivibrator:

- Also known as a flip-flop or binary latch.
- It has two stable states and remains in one of these states until an external trigger or signal is applied.
- The output state is determined by the previous state and the input trigger.
- Commonly used in digital logic circuits for memory elements, sequential circuits, and data storage.
- There are various types of bistable multivibrators, including SR flip-flops, D flip-flops, JK flip-flops, and T flip-flops, each with specific characteristics and applications.

Compare the Monostable and bistable multivibrators

Monostable and bistable multivibrators are two distinct types of multivibrator circuits used in electronics, each with its own set of characteristics and applications. Here's a comparison of these two types:

### 1. Operating States:

- **Monostable Multivibrator:**

- Monostable multivibrators have one stable state and one unstable state.
- They are triggered into the unstable state by an external input pulse or trigger.
- After being triggered, they automatically return to the stable state after a fixed time period, which is determined by external components like resistors and capacitors.

- **Bistable Multivibrator:**

- Bistable multivibrators have two stable states, which means they remain in one of these states until an external trigger or signal is applied.
- The output state of a bistable multivibrator is determined by the previous state and the input trigger.

## 2. Number of Output States:

- **Monostable Multivibrator:**

- Has two output states: a stable (quiescent) state and an unstable state.
- It transitions from the unstable state back to the stable state automatically after a specified time.

- **Bistable Multivibrator:**

- Has two stable output states, often referred to as "SET" and "RESET" or "HIGH" and "LOW."
- It remains in one of these two states until an external trigger changes its state.

## 3. Triggering:

- **Monostable Multivibrator:**

- Triggered by an external input pulse.
- Returns to its stable state after a fixed time delay.

- **Bistable Multivibrator:**

- Changes state when an external trigger is applied, typically with separate inputs for setting and resetting.

## 4. Applications:

- **Monostable Multivibrator:**

- Used for generating single, fixed-width pulses or time delays.
- Common applications include debouncing switches, generating precise timing pulses, and pulse width modulation.

- **Bistable Multivibrator:**

- Used for storing binary information, implementing flip-flops in digital logic circuits, and sequential circuitry.
- Found in various memory elements and sequential circuits, such as registers, counters, and state machines.

## 5. Output Waveform:

- **Monostable Multivibrator:**

- Typically produces a single output pulse of a fixed duration.

- **Bistable Multivibrator:**

- Produces two stable output levels, often referred to as HIGH and LOW.

In summary, monostable multivibrators are primarily used for generating single, fixed-duration pulses or time delays, while bistable multivibrators are employed for storing binary information and implementing memory and sequential logic elements in digital circuits. Their key differences lie in the number of stable states and their response to external triggers.