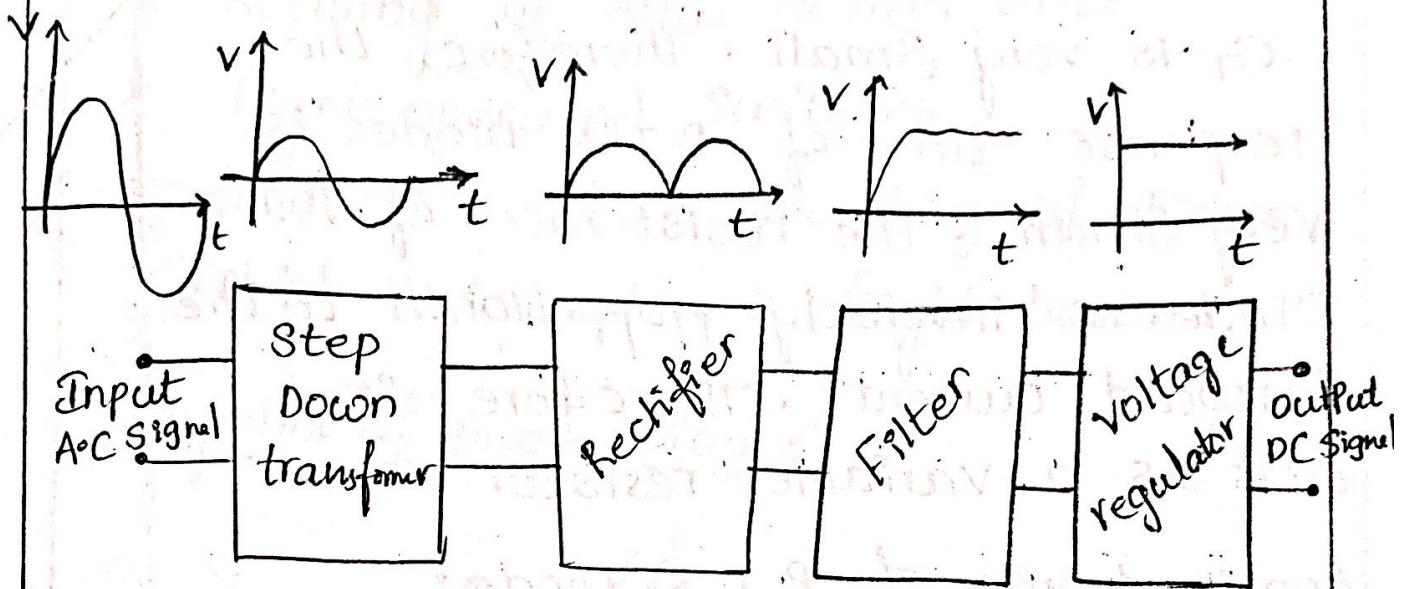


RECTIFIERS:

Regulated Power Supply:

Regulated power Supply is an electronic circuit that converts A.C Signal to pure D.C. Signal.

The block diagram of Regulated Power Supply



The Step-down transformer reduces the amplitude of the input A.C Signal.

The rectifier converts a A.C Signal into pulsating D.C Signal or a Unipolar signal.

The output of rectifier consists of both A.C and D.C components. The A.C component present in the Output of rectifier is called "ripple".

The rectifier output is given to filter. Filter removes the ripple and gives unregulated DC voltage at the output. The Output of filter is given to voltage regulator which gives a regulated pure D.C.

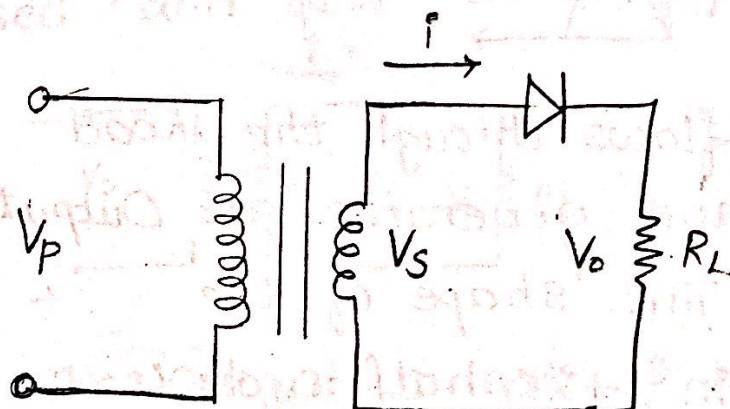
Rectifiers:

Types of rectifiers

- 1 * Half-wave rectifier
- 2 * Full-wave rectifier
- 3 * Bridge rectifier.

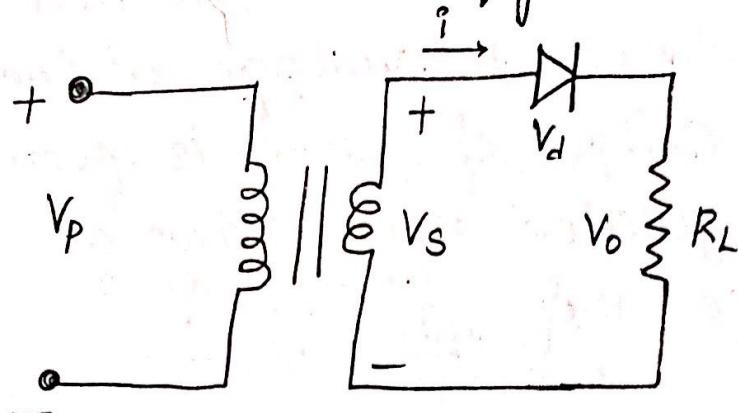
1) Half-wave rectifier:

The circuit Diagram of Half-wave rectifier is as shown in the following figure

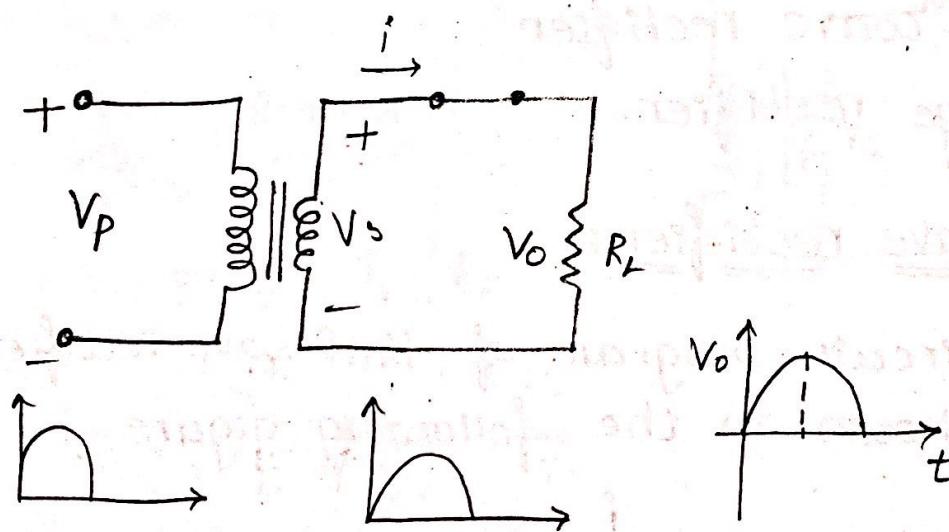


The input to the Half-wave rectifier is a sinusoidal signal. During the positive half cycle, the polarities

at the transformer are as shown in the figure



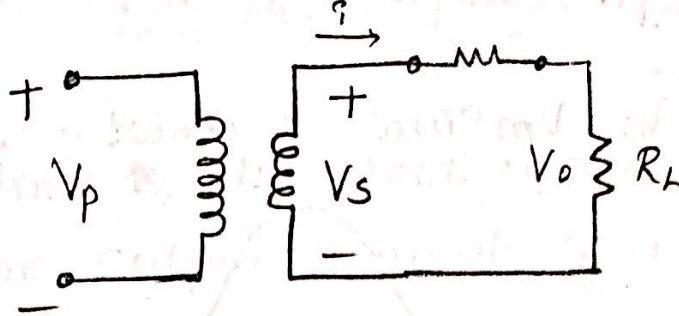
with these polarities, the diode will be forward biased and it acts like a short circuit



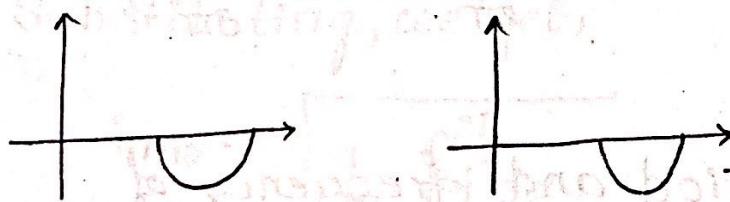
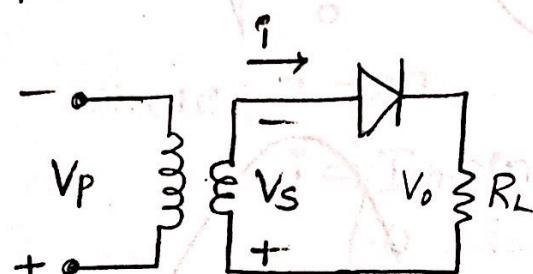
current flows through the load resistance and generates an Output Voltage ' V_o '. The shape of the current ' i ' in +ve half cycle is same as the shape of input signal

Practically, the diode will have a small forward resistance " R_f "

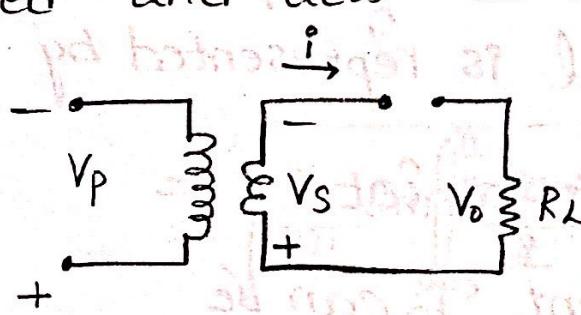
as shown below.



During the negative half-cycle the polarities are as shown below

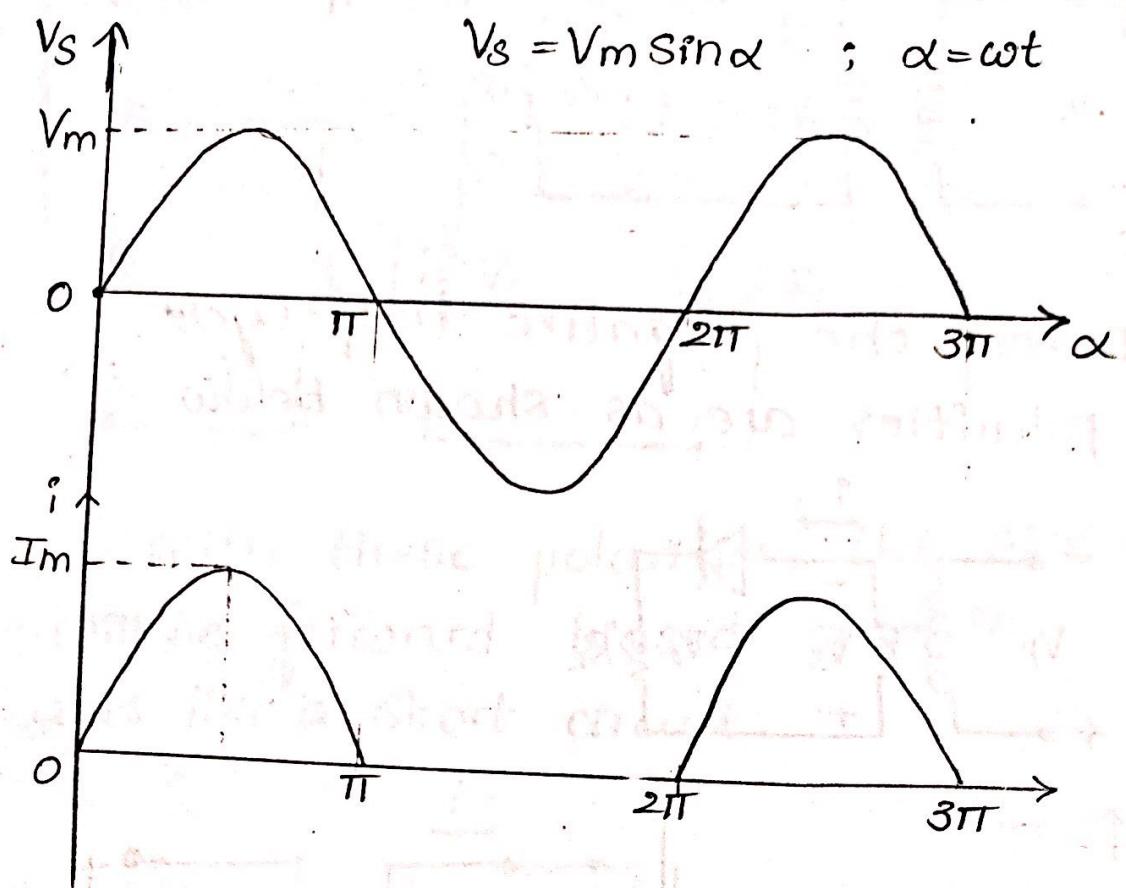


With the polarities shown in the figure, the diode will be reverse biased and acts as an open circuit



The Output current is zero during the negative half cycle and hence, the output voltage is also zero.

Wave Forms of Half-wave rectifier:



The time period and frequency of half-wave rectifier is same as the time period and frequency of the input signal.

The input Signal is represented by

$$V_s = V_m \sin \alpha ; \alpha = \omega t$$

The Output current 'i' can be represented as

$$i = I_m \sin \alpha ; 0 \leq \alpha \leq \pi$$

$$= 0 ; \pi \leq \alpha \leq 2\pi$$

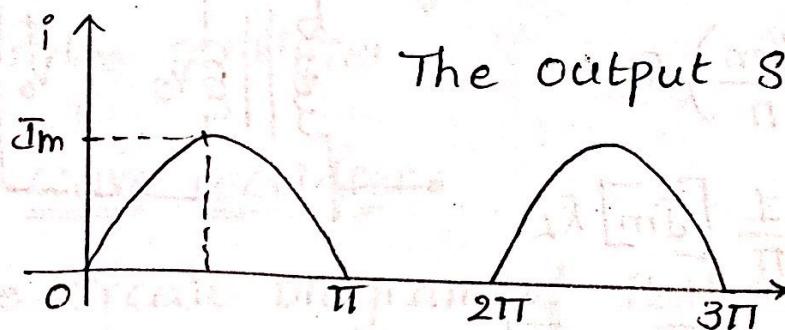
$$\text{current, } i = \frac{V_s}{(R_f + R_L)}$$

$$\Rightarrow I_m = \frac{V_m}{(R_f + R_L)}$$

D.C current: (I_{DC}) [Average value of the Output Current]

The average or the D.C value of the output current in half-wave rectifier is given by I_{DC}

$$I_{DC} = \frac{1}{T} \int_0^T i d\alpha$$



The output Signal is,

Here,

$$T = 2\pi$$

$$i = \begin{cases} I_m \sin \alpha & ; 0 \leq \alpha \leq \pi \\ 0 & ; \pi \leq \alpha \leq 2\pi \end{cases}$$

$$\therefore I_{DC} = \frac{1}{2\pi} \int_0^{2\pi} i d\alpha \quad [\text{where } \alpha = \omega t]$$

$$= \frac{1}{2\pi} \left[\int_0^\pi i d\alpha + \int_\pi^{2\pi} i d\alpha \right]$$

$$= \frac{1}{2\pi} \left[\int_0^{\pi} \Im m \sin \alpha d\alpha + 0 \right]$$

$$I_{DC} = \frac{1}{2\pi} \Im m(-\cos \alpha) \Big|_0^{\pi}$$

$$\Rightarrow \boxed{I_{DC} = \frac{\Im m}{\pi}}$$

* Output D.C voltage (V_{D.C.})

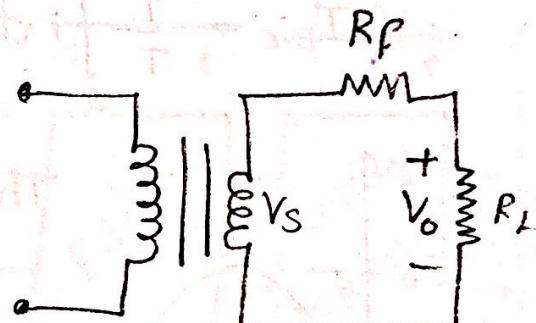
$$V_{DC} = I_{DC} R_L$$

$$= \left(\frac{\Im m}{\pi} \right) R_L$$

$$= \frac{1}{\pi} [\Im m] R_L$$

$$= \frac{1}{\pi} \left[\frac{V_m}{R_f + R_L} \right] R_L$$

$$= \frac{1}{\pi} \left(\frac{V_m}{1 + R_f/R_L} \right)$$



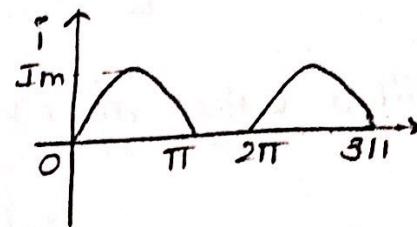
$\because R_f$ is very small,
we can neglect R_f/R_L

$$\Rightarrow \boxed{V_{DC} \approx \frac{V_m}{\pi}}$$

* RMS value of Output current [i_{rms}]

" i_{rms} " is the root mean square value of the output current of a half-wave rectifier

$$i_{rms} = \sqrt{\frac{1}{T} \int_0^T i^2 d\alpha}$$



$$\text{where, } T = 2\pi$$

$$i = \begin{cases} I_m \sin \alpha & 0 \leq \alpha \leq \pi \\ 0 & \pi \leq \alpha \leq 2\pi \end{cases}$$

Substituting, we get,

$$i_{rms} = \sqrt{\frac{1}{2\pi} \int_0^{2\pi} i^2 d\alpha}$$

$$= \sqrt{\frac{1}{2\pi} \int_0^\pi I_m^2 \sin^2 \alpha d\alpha + \int_\pi^{2\pi} 0}$$

$$= \sqrt{\frac{1}{2\pi} I_m^2 \int_0^\pi \left[\frac{1 - \cos 2\alpha}{2} \right] d\alpha}$$

$$= \sqrt{\frac{1}{2\pi} I_m^2 \left[\int_0^\pi \frac{1}{2} d\alpha - \int_0^\pi \frac{\cos 2\alpha}{2} d\alpha \right]}$$

$$= \sqrt{\frac{1}{2\pi} \frac{I_m^2}{2} [\alpha]_0^\pi - 0}$$

$$\Rightarrow i_{rms} = \sqrt{\frac{\hat{I}_m^2}{4}}$$

$$\Rightarrow i_{rms} = \frac{\hat{I}_m}{2}$$

* RMS value of Output Voltage (V_{rms}) :-

$$V_{rms} = i_{rms}(R_L)$$

$$= \left(\frac{\hat{I}_m}{2}\right) R_L$$

$$= \left(\frac{\hat{I}_m}{2}\right) \left(\frac{V_m}{R_f + R_L}\right) (R_L)$$

$$= \frac{V_m}{2(1 + R_f/R_L)}$$

$$\approx \frac{V_m}{2}$$

$$\Rightarrow V_{rms} = \frac{V_m}{2}$$

* DC Output power of Half wave rectifier ($P_{D.C.}$) :-

$$P_{DC} = V_{DC} I_{DC}$$

$$\Rightarrow P_{DC} = \mathcal{P}_{DC}(R_L)$$

$$= \left(\frac{\mathcal{I}_m}{\pi} \right)^2 R_L$$

$$= \left[\frac{1}{\pi} \left(\frac{V_m}{R_f + R_L} \right) \right]^2 R_L$$

$$\Rightarrow P_{DC} = \boxed{\left[\frac{1}{\pi} \left(\frac{V_m}{R_f + R_L} \right) \right]^2 R_L}$$

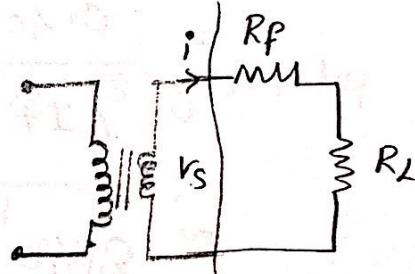
- * A.C Input power of a half-wave rectifier ($P_{A.C}$)

$$P_{A.C} = V_{rms} i_{rms}$$

$$= i_{rms}^2 (R_f + R_L)$$

$$= \left(\frac{\mathcal{I}_m}{2} \right)^2 (R_f + R_L)$$

$$\boxed{P_{A.C} = \left(\frac{\mathcal{I}_m}{2} \right)^2 (R_f + R_L)}$$



- * Rectification Efficiency of Half-wave rectifier:

rectification efficiency is defined as the ratio of output DC power to the input A.C power. It is a figure of

merit for rectifiers.

$$\eta = \frac{\text{D.C Output power}}{\text{A.C Input power}}$$

$$\Rightarrow \eta = \frac{I_{DC}^2 R_L}{I_{rms}^2 (R_f + R_L)}$$

$$= \frac{\left(\frac{Im}{\pi}\right)^2 R_L}{\left(\frac{Im}{2}\right)^2 (R_f + R_L)}$$

$$= \frac{0.4052}{(1 + R_f/R_L)}$$

$$\approx 0.4052$$

\therefore The % of rectifier efficiency
is $\eta = 40.5\%$.

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Ripple Factor:

In a half-wave rectifier, the output is not Pure D.C. It is a pulsating D.C. The output contains A.C component. Called "Ripple". The measure of such ripples present in the output is

given by a factor called "Ripple factor"
It is denoted by ' η '

ripple factor is given by, the ratio of
RMS value of A.C component present in the
output to the D.C component present in
the output.

The output current in a half
wave rectifier is given by,

$$i = i_{AC} + I_{DC}$$

$$i_{AC} = i - I_{DC},$$

The RMS value of I_{AC} is given by.

$$I_{AC} = \sqrt{\frac{1}{T} \int_0^T i_{AC}^2 d\alpha}$$

Substituting i_{AC}

$$\Rightarrow \sqrt{\frac{1}{T} \int_0^T (i - I_{DC})^2 d\alpha}$$

$$\Rightarrow \sqrt{\frac{1}{T} \int_0^T [i^2 + I_{DC}^2 - 2i \cdot I_{DC}] d\alpha}$$

$$= \sqrt{\frac{1}{T} \int_0^T i^2 d\alpha + \frac{1}{T} \int_0^T I_{DC}^2 d\alpha - 2 \cdot \frac{1}{T} \int_0^T i \cdot I_{DC} d\alpha}$$

we know that,

$$\sqrt{\frac{1}{T} \int_0^T i^r d\alpha} = i_{rms}$$

$$\Rightarrow \frac{1}{T} \int_0^T i^r d\alpha = i_{rms}^r \quad \text{--- (1)}$$

and

$$\frac{1}{T} \int_0^T i^r d\alpha = i_{dc}^r \quad \text{--- (2)}$$

Substituting (1) and (2)

$$\begin{aligned} i_{ac rms} &= \sqrt{\frac{1}{T} \int_0^T i^r d\alpha + I_{dc}^r \frac{1}{T} \int_0^T i^r d\alpha - 2 I_{dc} \frac{1}{T} \int_0^T i^r d\alpha} \\ &= \sqrt{i_{rms}^r + I_{dc}^r - 2 I_{dc}} \\ &= \sqrt{i_{rms}^r - I_{dc}^r} \\ i_{ac rms} &= \sqrt{i_{rms}^r - I_{dc}^r} \end{aligned}$$

∴ The ripple factor is

$$r = \frac{i_{ac rms}}{I_{dc}}$$

$$= \frac{\sqrt{i_{rms}^r - I_{dc}^r}}{I_{dc}}$$

$$= \sqrt{\left(\frac{I_{rms}}{I_{DC}}\right)^2 - 1}$$

$$= \sqrt{\left(\frac{\frac{I_m}{2}}{\frac{I_m}{\pi}}\right)^2 - 1}$$

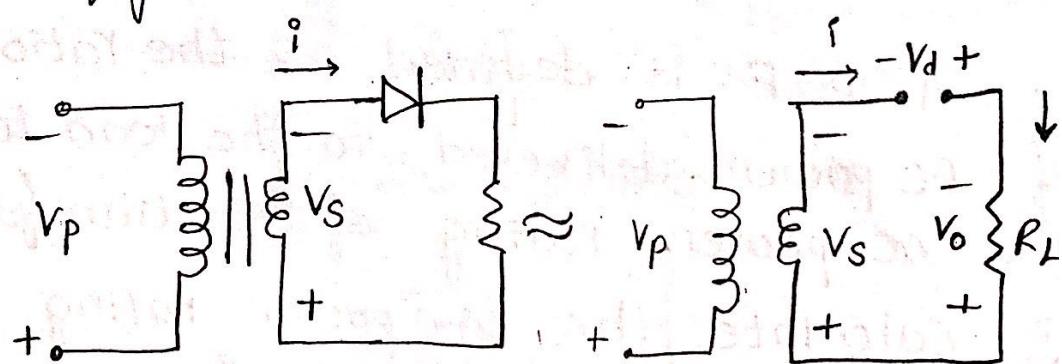
$$= \sqrt{\frac{\pi^2}{4} - 1}$$

$$= 1.21.$$

Peak Inverse voltage:

Peak inverse voltage is defined as the peak voltage across the diode in reverse bias in a rectifier.

Consider the negative half-cycle in the half-wave rectifier. During the negative half-cycle, the diode is reverse biased and the circuit is as shown in the figure.



Applying KVL, we get

$$V_s - V_d - V_o = 0$$

But $V_o = 0$,

$$\Rightarrow V_s = V_d$$

where,

$V_s = V_m \sin \alpha$ is the transformer secondary voltage

The peak value of V_s is V_m

\therefore Peak value of V_d is ' V_m '

\therefore Peak inverse voltage in half wave rectifier is ' V_m '

Transformer utilisation factor:

It is the factor which indicates, how much is the utilisation of the transformer in the rectifier circuit

A T.U.F is defined as the ratio of DC power delivered to the load to the AC power rating of the transformer

To calculate the A.C power rating of the Transformer we must consider RMS value of d.c voltage & current.

$\text{P.O.F} = \frac{\text{D.C power delivered to the load}}{\text{AC power rating of the transformer.}}$

$$\text{D.C power delivered to the load} = V_{\text{DC}} \cdot I_{\text{DC}}$$

$$\Rightarrow I_{\text{DC}}^2 R_L$$

$\text{A.C power rating of the Transformer Secondary} =$

$$\Rightarrow V_{(\text{secondary})\text{rms}} \cdot I_{\text{rms}}$$

$$= \underbrace{\frac{V_m}{\sqrt{2}}}_{\text{on full cycle}} \underbrace{\frac{I_m}{2}}_{\text{on half cycle}}$$

$V_s = \text{Sinusoidal Voltage}$
 $I = \text{Half sinusoidal}$

$$\therefore \text{P.O.F} = \frac{I_{\text{DC}}^2 R_L}{\left(\frac{V_m}{\sqrt{2}} \right) \left(\frac{I_m}{2} \right)}$$

$$\therefore I_m = \frac{V_m}{(R_f + R_L)}$$

$$= \frac{\left(\frac{I_m}{\pi} \right)^2 R_L}{\left(\frac{1}{2\sqrt{2}} \right) I_m \cdot I_m (R_f + R_L)}$$

$$= \frac{2\sqrt{2}}{\pi^2} \left[\frac{1}{1 + (R_f/R_L)} \right]$$

$$\approx 0.287$$

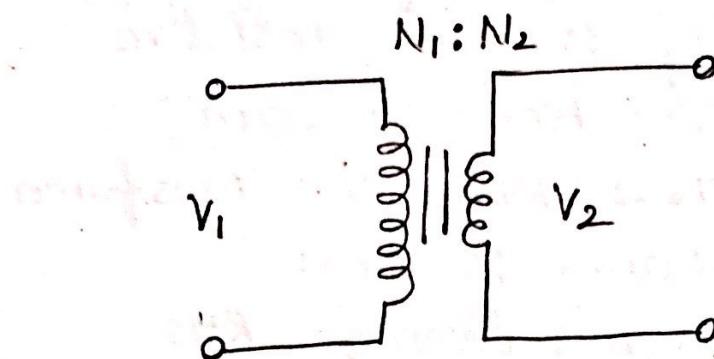
The T.O.F of half-wave rectifier is very small which indicates that the transformer is not fully utilised.

Disadvantages of Half-wave rectifier:

- 1) The ripple-factor of half-wave rectifier is 1.21 which is very high. The output contains lot of ripples
- 2) The rectification efficiency is only 40.5% which is very low.
- 3) The half-wave rectifier is therefore inefficient.
∴ The transformer is not fully utilised
- 4) The output current of half-wave rectifier has both A.C and D.C components.

The D.C component flowing through the transformer secondary winding may cause saturation

of the core of the transformer.



V_1 - Voltage at the primary winding

V_2 - Voltage at the secondary winding

N_1 - no. of turns in primary winding

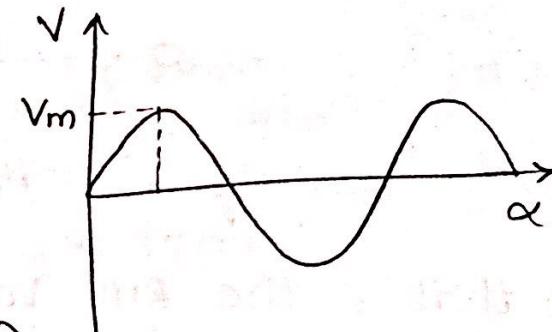
N_2 - no. of turns in secondary winding

Their relation is,

$$\frac{V_1}{V_2} = \frac{N_1}{N_2}$$

$$V_s = V_m \sin \alpha$$

$$(V_s)_{\text{rms}} = \frac{V_m}{\sqrt{2}}$$



$$\Rightarrow V_m = (V_s)_{\text{rms}} (\sqrt{2})$$

* A Half-wave rectifier circuit is supplied from a 230V, 50Hz Supply with a Stepdown ratio of 3:1 to a resistive load of 10k Ω . The Diode forward resistance is 55 Ω while, the transformer secondary resistance is 10 Ω . Calculate maximum, average, RMS value of the current, DC Output voltage, rectification efficiency & Ripple factor.

A)

Given:

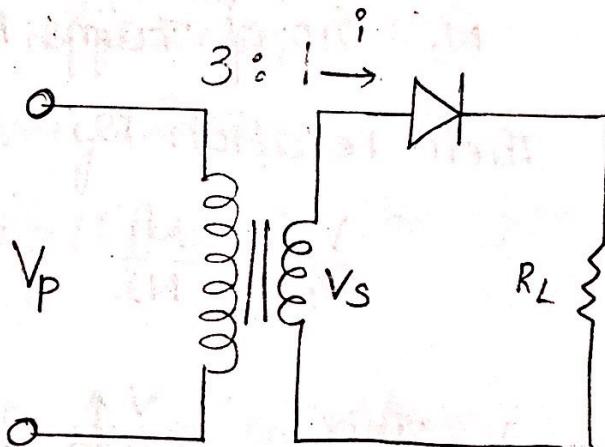
$$(V_p)_{rms} = 230V$$

If it is given as

$$X \sin \alpha$$

the 'X' will be V_m

if it is directly 'x' then 'x' is $(V_p)_{rms}$



Given that, the RMS value of Primary voltage $(V_p)_{rms} = 230V$:

transformer ratio = 3:1

We know that

$$\frac{V_p}{V_s} = \frac{3}{1}$$

$$\Rightarrow V_s = V_p / 3 = \frac{230}{3} = 76.67V$$

'Vs' is a sinusoidal signal

$$\therefore (V_s)_{rms} = \frac{V_m}{\sqrt{2}}$$

$$\Rightarrow V_m = (V_s)_{rms} (\sqrt{2}) V$$

$$= 76.64 (\sqrt{2}) V$$

$$= 108.4 V.$$

$$I_m = \frac{V_m}{R_s + R_f + R_L}$$

Secondary resistance Diode forward resistance

$$\Rightarrow I_m = \frac{108.4}{10 \times 10^3 + 75 + 10} = 0.0107 A$$

$$\Rightarrow I_m = 10.7 mA$$

$$I_{DC} = \frac{I_m}{\pi} = \frac{10.7 \times 10^{-3}}{\pi} = 3.4 mA$$

$$I_{rms} = \frac{I_m}{2} = 5.35 mA$$

$$V_{DC} = I_{DC} \cdot R_L$$

$$\Rightarrow V_{DC} = 3.4 \times 10 \times 10 \times 10^3$$

$$\Rightarrow V_{DC} = 34 V.$$

$$\eta = \frac{\text{D.C Output Power}}{\text{A.C Input power}}$$

$$P_{DC} = V_{DC} \cdot I_{DC}$$

$$= 34(3.4)(10^3)$$

$$= 115.6 \text{ mW.}$$

$$P_{AC} = V_{rms} \cdot I_{rms}$$

$$= I_{rms}(R_f + R_L + R_s)$$

$$= [5.35 \times 10^3] [10 + 75 + 10000]$$

$$= 0.2886 \text{ W}$$

$$= 288.6 \text{ mW.}$$

$$\Rightarrow \eta = \frac{115.6}{288.6} = 40.05\%$$

* A half-wave rectifier circuit is supplied from a 110V, 60Hz sinusoidal signal, the transformer turns ratio is 5:1

Determine

- (a) D.C Current
- (b) RMS Current
- (c) D.C Output Voltage
- (d) RMS Output Voltage
- (e) Output D.C Power

- (f) A.C input power
- (g) Rectification efficiency
- (h) Ripple factor
- (i) Peak inverse voltage

Assume, the diode has a forward resistance of 50Ω & load resistance of $10k\Omega$.

A) Given: that input signal is 110V, 60Hz.

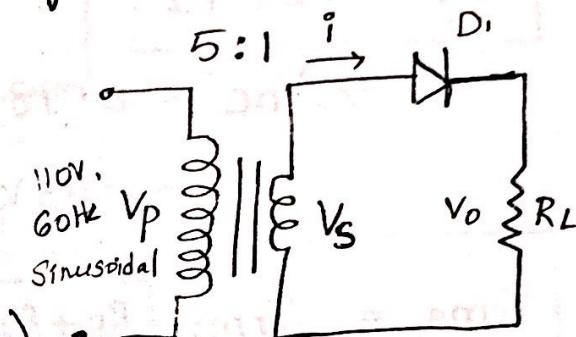
$$\therefore (V_p)_{rms} = 110V$$

$$n_1 : n_2 = 5 : 1$$

$$\left(\frac{V_p}{V_s}_{rms} \right) = \frac{5}{1}$$

$$\Rightarrow V_s_{rms} = 110 \left(\frac{1}{5} \right)$$

$$\Rightarrow V_s_{rms} = 22V.$$



$$(V_s)_{rms} = \frac{V_m}{\sqrt{2}}$$

$$\Rightarrow V_m = V_s(rms) (\sqrt{2})$$

$$= 22(\sqrt{2})$$

$$= 31.11V.$$

$$I_m = \frac{V_m}{R_f + R_L}$$

$$\Rightarrow I_m = \frac{31.11}{50 + 10000} = 3.09 \text{ mA}$$

$$I_{DC} = \frac{Im}{\pi}$$

$$\Rightarrow I_{DC} = \frac{3.09mA}{\pi} = 0.98mA.$$

$$I_{rms} = \frac{Im}{2}$$

$$\Rightarrow I_{rms} = \frac{3.09mA}{2} = 1.545mA$$

$$V_{DC} = I_{DC} \cdot R_L$$

$$\Rightarrow V_{DC} = 0.98 [10^3] \times 10 \times [10^3]$$
$$= 9.8V.$$

$$V_{rms} = I_{rms} [R_F + R_L]$$

$$= 1.545 [50 + 10000]$$

$$= 1.545 [10050]$$

$$= 15.5V.$$

$$P_{DC} = V_{DC} I_{DC}$$

$$= 9.8 [0.98]$$

$$= 9.6mW.$$

$$P_{ac} = V_{rms} \cdot I_{rms}$$

$$= 1.545 [15.5] mA mW$$

$$= 23.9mW.$$

$$\eta = \frac{P_{D.C.}}{P_{A.C.}} = \frac{9.6}{23.9} = 0.406$$

$\Rightarrow 40.6\%$.

In a half-wave rectifier,

$$P \cdot I \cdot V = V_m = 31.11V.$$

$$r = \sqrt{\left(\frac{I_{rms}}{I_{DC}}\right)^2 - 1}$$

$$= \sqrt{\left(\frac{1.545}{0.98}\right)^2 - 1}$$

$$= 1.21$$

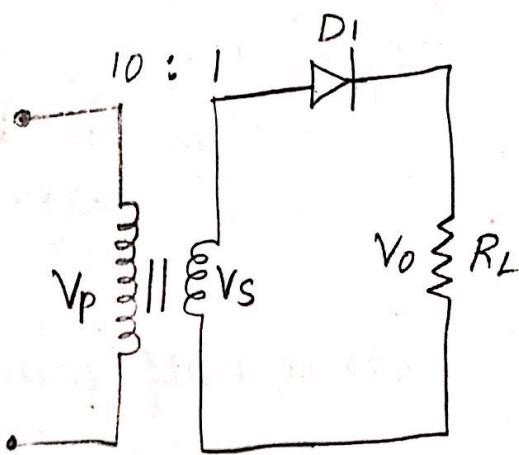
A signal $250 \sin 2\pi \cdot 50t$ is applied to the transformer of a half-wave rectifier with turns ratio 10:1. Assume, a diode forward resistance of 100Ω and load resistance of $10k\Omega$. Determine

- (a) D.C current
- (b) RMS current
- (c) DC Output Voltage
- (d) RMS Output Voltage
- (e) D.C Output power
- (f) A.C input power
- (g) Rectification efficiency
- (h) Ripple factor
- (i) Peak & inverse voltage

Given that, the input signal is

$$250 \sin 2\pi 50t$$

$$\therefore (V_p)_m = 250V.$$



$$\frac{V_p}{V_s} = \frac{10}{1} \Rightarrow V_s = \frac{1}{10}(V_p)$$

$$\Rightarrow (V_s)_m = \frac{1}{10}(250) = 25V$$

$$\therefore V_m = 25V.$$

$$I_m = \frac{V_m}{(R_f + R_L)} = \frac{25}{100 + 10000}$$

$$\Rightarrow I_m = 2.47mA$$

$$I_{DC} = \frac{I_m}{\pi} = \frac{2.47mA}{\pi} = 0.784mA$$

$$I_{rms} = \frac{I_m}{2} = 1.235mA$$

$$V_{oc} = I_{DC} \cdot R_L$$

$$= 0.784 \times 10^3 \times 10 \times 10^3$$

$$= 7.84V.$$

$$V_{rms} = I_{rms} (r_f + r_L)$$

$$= 1.235 \times 10^3 [10 | 100]$$

$$= 12.47V.$$

$$P_{DC} = V_{DC} I_{DC}$$

$$= 7.87 (0.787) \times 10^{-3}$$

$$= 6.17 \text{ mW.}$$

$$P_{AC} = V_{rms} I_{rms}$$

$$= 12.47 [1.235] \times 10^{-3}$$

$$= 15.4 \text{ mW.}$$

$$\eta = \frac{P_{DC}}{P_{AC}} = \frac{6.17}{15.4} = 0.4006$$

$\rightarrow \approx 40\%$

$$\gamma = \sqrt{\left(\frac{I_{rms}}{I_{DC}}\right)^2 - 1} = \sqrt{\left(\frac{1.235}{0.78}\right)^2 - 1} = 1.209$$

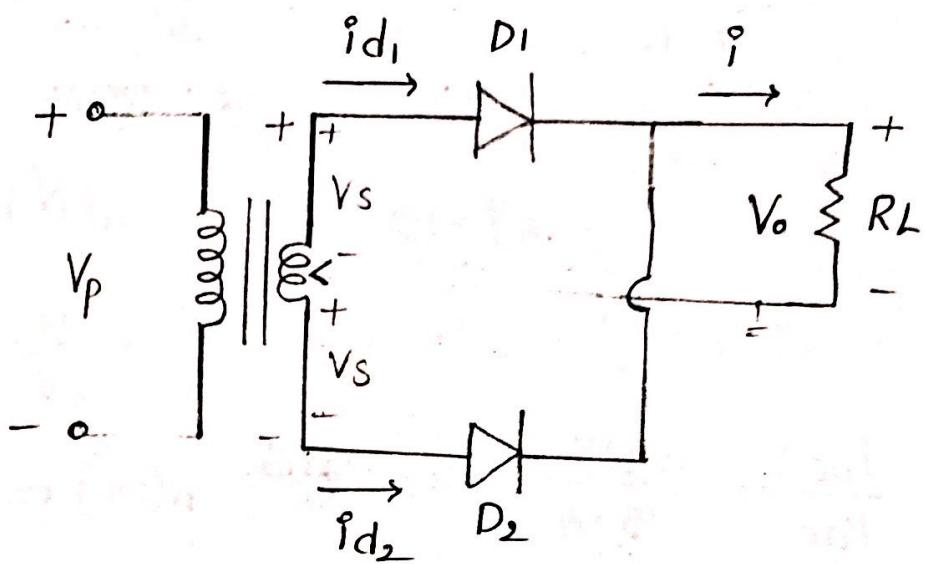
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$$P.I.V = V_m = 250 \text{ V.}$$

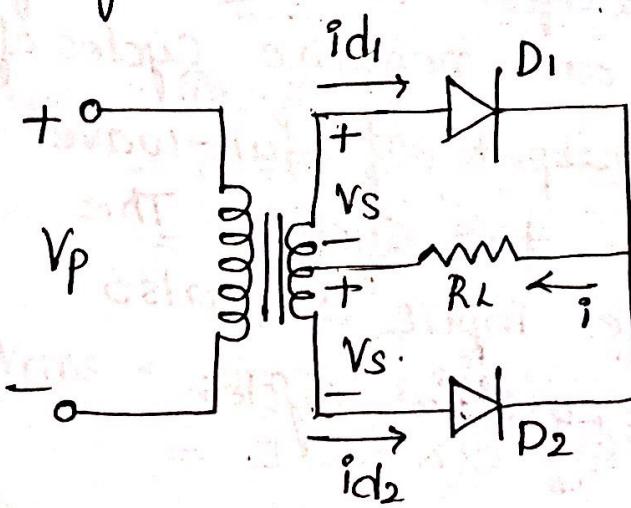
* FULL WAVE RECTIFIER:

A full-wave rectifier conducts during both the positive and negative cycles of the input. The output of full-wave rectifier contains +ve cycles. The -ve cycles of the input are also converted into positive cycles.

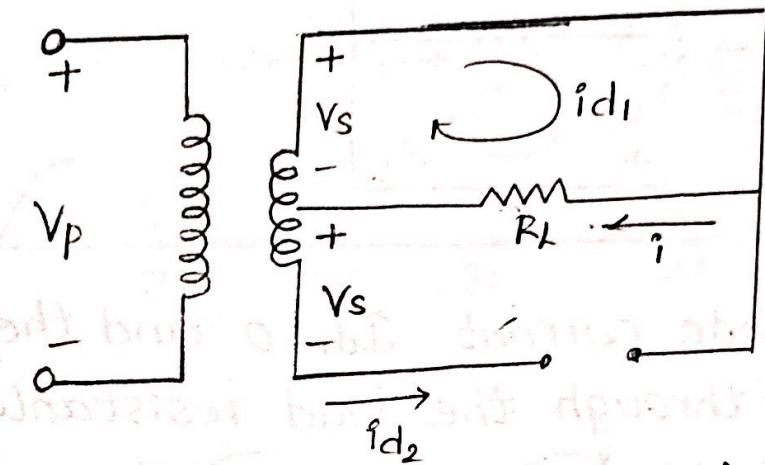
Circuit diagram:



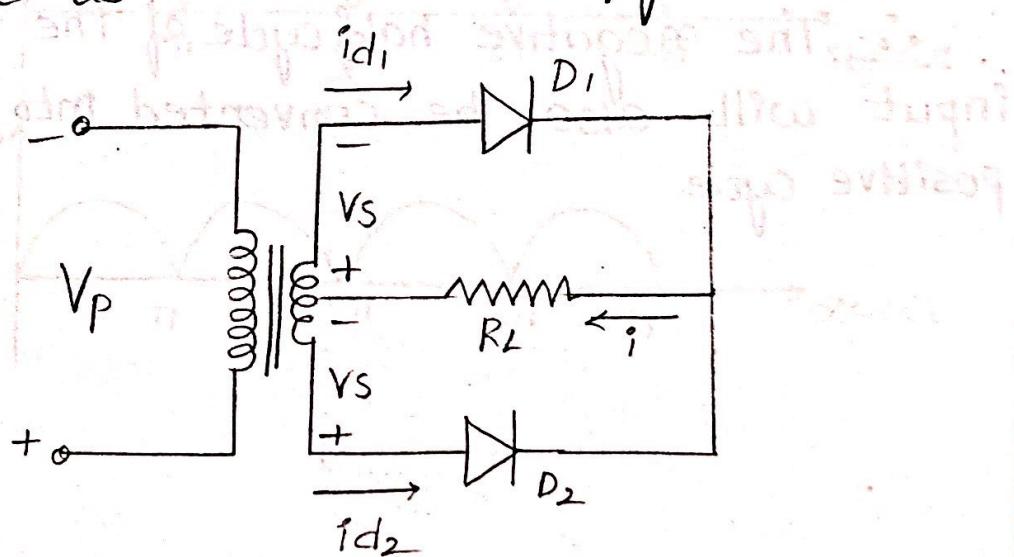
During +ve half cycle, the polarities of the transformer are as shown in the figure



With the above polarities the diode D_1 will be forward Biased and acts as a short circuit. The diode D_2 will be reverse Biased and acts as an open circuit.

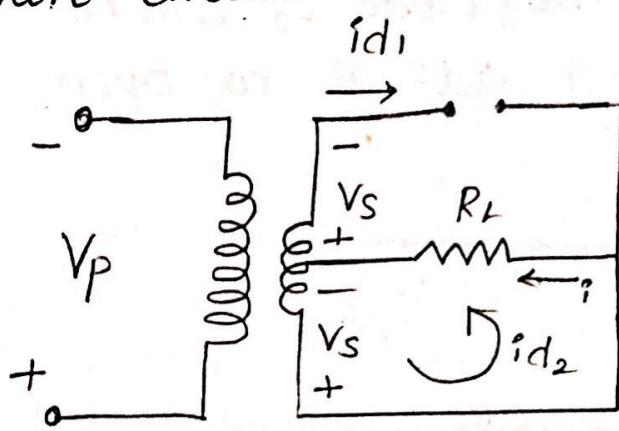


The current $i_{d2} = 0$ and the current through the load resistance R_L is $i = i_{d1}$. During the negative half-cycle, polarities in the transformer are as shown in the figure.



With this polarity, the diode D_1 will be reverse biased and acts as

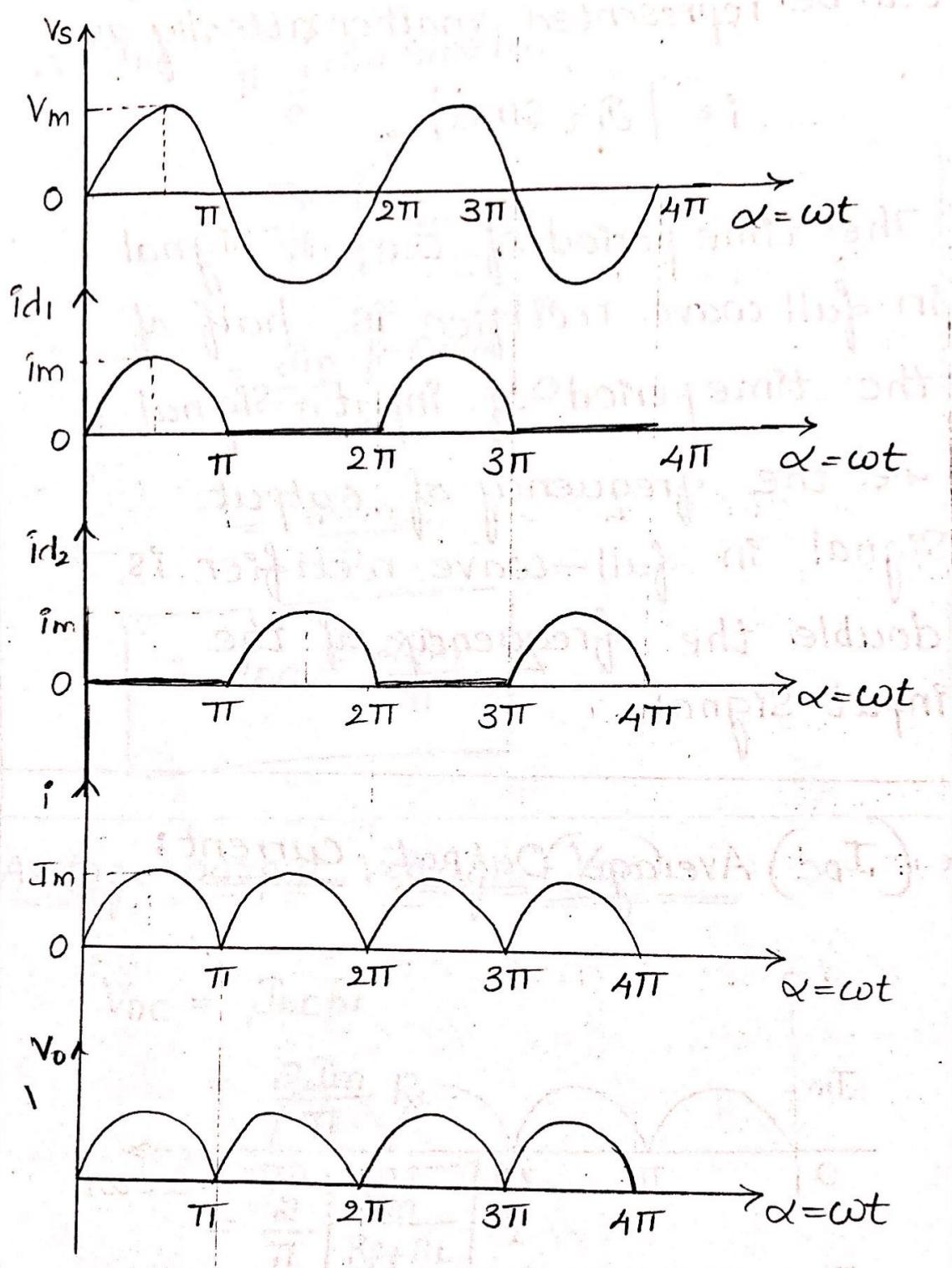
a open circuit and the diode D_2 will be forward biased which acts as a short circuit.



The diode current $I_{d1}=0$ and the current through the load resistance R_L is $i=i_{d2}$. The direction of currents i_{d1} and i_{d2} through the load resistance ' R_L ' is same during +ve and -ve half cycles.

\therefore The negative half cycle of the input will also be converted into positive cycle.

Wave forms of Full-wave Rectifier:

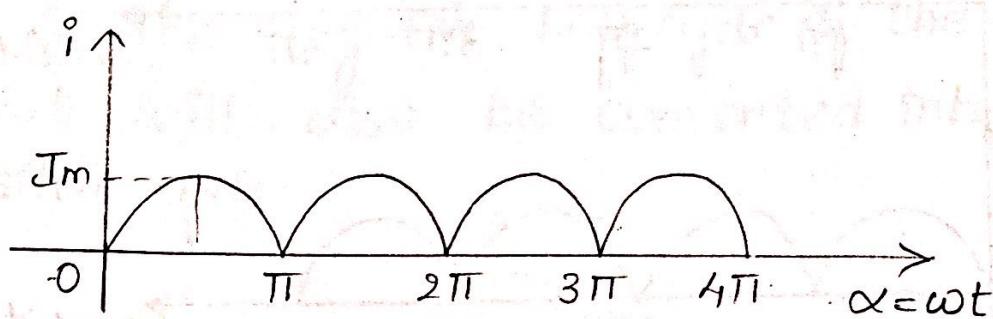


The current in full-wave rectifier
can be represented mathematically as

$$i = |I_m \sin \alpha|$$

The time period of output signal
in full wave rectifier is half of
the time period of input signal
i.e the frequency of output
Signal in full-wave rectifier is
double the frequency of the
input signal

* (I_{DC}) Average Output current:



The average current,

$$I_{DC} = \frac{1}{T} \int_0^T i d\alpha$$

Here, for full-wave rectifier,

Q T=π

$$\therefore I_{DC} = \frac{1}{\pi} \int_0^{\pi} \text{Im} \sin \alpha d\alpha$$

$$= \frac{\text{Im}}{\pi} \int_0^{\pi} \sin \alpha d\alpha$$

$$= \frac{\text{Im}}{\pi} \left[-\cos \alpha \right]_0^{\pi}$$

$$= \frac{2 \text{Im}}{\pi}$$

$$\therefore I_{DC} = \frac{2 \text{Im}}{\pi}$$

* Average output voltage (V_{DC})

$$V_{DC} = I_{DC} R_L$$

$$= \frac{2 \text{Im}}{\pi} R_L$$

$$= \frac{2}{\pi} \left[\frac{V_m}{R_f + R_L} \right] R_L$$

$$V_{DC} = \frac{2 V_m}{\pi} \left[\frac{1}{1 + R_f / R_L} \right]$$

RMS value of Output current:

$$I_{rms} = \sqrt{\frac{1}{T} \int_0^T i^2 d\alpha}$$

Here, $T = \pi$

$$\Rightarrow I_{rms} = \sqrt{\frac{1}{\pi} \int_0^\pi (I_m \sin \alpha)^2 d\alpha}$$

$$= \sqrt{\frac{1}{\pi} \int_0^\pi I_m^2 \sin^2 \alpha d\alpha}$$

$$= I_m \sqrt{\frac{1}{\pi} \int_0^\pi \left(\frac{1 - \cos 2\alpha}{2}\right) d\alpha}$$

$$= \sqrt{\frac{I_m^2}{\pi} \left[\int_0^\pi \frac{1}{2} d\alpha - \int_0^\pi \frac{\cos 2\alpha}{2} d\alpha \right]}$$

$$= \sqrt{\frac{I_m^2}{\pi} \left[\frac{\pi}{2} \right]}$$

$$= \boxed{\frac{I_m^2}{2}} = \frac{I_m}{\sqrt{2}}$$

$$\therefore I_{rms} = \boxed{\frac{I_m}{\sqrt{2}}}$$

RMS value of the Output voltage (V_{rms})

$$V_{rms} = I_{rms} (R_L)$$

$$= \frac{I_m}{\sqrt{2}} (R_L)$$

$$= \frac{R_L}{\sqrt{2}} \left(\frac{V_m}{R_f + R_L} \right)$$

$$= \frac{V_m}{\sqrt{2}} \left[\frac{1}{1 + R_f/R_L} \right]$$

$$\therefore V_{rms} = \frac{V_m}{\sqrt{2}} \cdot \left[\frac{1}{1 + R_f/R_L} \right]$$

D.C output power: (P_{DC})

$$P_{DC} = V_{DC} \cdot I_{DC}$$

A.C component present in the Output

$$= I_{DC} \cdot R_L \cdot I_{DC}$$

$$= I_{DC}^2 R_L$$

$$= \left(\frac{2I_m}{\pi} \right)^2 R_L$$

The output power can be required as

A.C input power: (P_{AC})

$$\begin{aligned} P_{AC} &= V_{rms} I_{rms} \\ &= I_{rms} (R_f + R_L) \\ &= \left(\frac{I_m}{\sqrt{2}}\right)^2 (R_f + R_L) \end{aligned}$$

Rectification Efficiency: (η)

Rectification efficiency is defined as the ratio of DC output power to the A.C input power.

$$\eta = \frac{\text{D.C Output Power}}{\text{A.C Input power}}$$

$$= \frac{V_{DC} \cdot I_{DC}}{V_{rms} I_{rms}}$$

$$= \frac{I_{DC}^2 R_L}{I_{rms}^2 (R_f + R_L)}$$

$$= \frac{\left(\frac{2I_m}{\pi}\right)^2 R_L}{\left(\frac{I_m}{\sqrt{2}}\right)^2 (R_f + R_L)}$$

$$\Rightarrow \eta = \frac{\frac{4}{\pi^2} (R_L)}{\frac{1}{2} (R_F + R_L)}$$

$$= \frac{8}{\pi^2} \left(\frac{1}{1 + R_F/R_L} \right)$$

$$= \frac{0.810}{(1 + R_F/R_L)}$$

$$\approx 0.810$$

$\therefore \%$ of Efficiency,

$$\% \eta = 81\%.$$

Ripple factor: (r)

It is the ratio of RMS value of the A-C component present in the output to the D.C component present in the Output.

$$r = \frac{I_{AC\text{ rms}}}{I_{DC}}$$

The output current can be represented as,

$$i = i_{ac} - i_{dc}$$

$$\Rightarrow i_{ac} = i - i_{dc}$$

The rms value of i_{ac} is

$$i_{ac\text{rms}} = \sqrt{\frac{1}{T} \int_0^T i_{ac}^2 d\alpha}$$

$$= \sqrt{\frac{1}{T} \int_0^T (i - i_{dc})^2 d\alpha}$$

$$= \sqrt{\frac{1}{T} \int_0^T (i^2 + i_{dc}^2 - 2i i_{dc}) d\alpha}$$

$$= \sqrt{\frac{1}{T} \int_0^T i^2 d\alpha + \frac{1}{T} \int_0^T i_{dc}^2 d\alpha - 2 \frac{1}{T} \int_0^T i i_{dc} d\alpha}$$

We know that,

$$I_{rms} = \sqrt{\frac{1}{T} \int_0^T i^2 d\alpha}$$

$$\Rightarrow I_{rms}^2 = \frac{1}{T} \int_0^T i^2 d\alpha$$

$$i_{dc} = \boxed{\sqrt{\frac{1}{T} \int_0^T i^2 d\alpha}}$$

Now,

$$i_{ac(rms)} = \sqrt{\hat{I}_{rms}^2 + \hat{I}_{dc}^2 + \int_0^T i^2 d\alpha - 2 \hat{I}_{dc} \frac{1}{T} \int_0^T i d\alpha}$$

$$= \sqrt{\hat{I}_{rms}^2 + \hat{I}_{dc}^2 - 2 \hat{I}_{dc}^2}$$

$$= \sqrt{\hat{I}_{rms}^2 - \hat{I}_{dc}^2}$$

\therefore ripple factor, $\gamma = \frac{\sqrt{\hat{I}_{rms}^2 - \hat{I}_{dc}^2}}{\hat{I}_{dc}}$

$$= \sqrt{\left(\frac{\hat{I}_{rms}}{\hat{I}_{dc}}\right)^2 - 1}$$

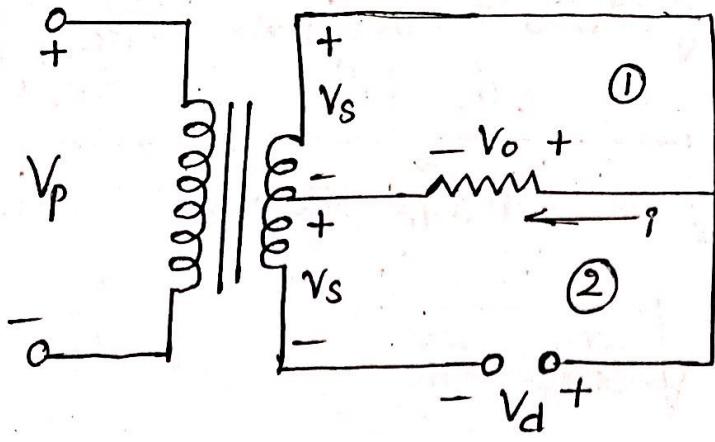
$$= \sqrt{\left(\frac{\hat{I}/\sqrt{2}}{\frac{2\hat{I}_m}{\pi}}\right)^2 - 1}$$

$$= 0.48$$

$$\therefore \gamma = 0.48$$

Peak Inverse Voltage:

It is defined as the maximum voltage across a reverse biased diode in a rectifier.



Writing KVL to loop ①, we get

$$-V_s + V_o = 0$$

$$\Rightarrow V_s = V_o$$

Writing KVL to loop ②, we get

$$-V_s - V_o + V_d = 0$$

$$\Rightarrow V_d = V_s + V_o \quad [\because V_s = V_o]$$

$$\Rightarrow V_d = 2V_s$$

The peak value of 'V_s' is 'V_m'

\therefore The peak value of $V_d = 2V_m$

$$\therefore P.D.V = 2V_m$$

* Transformer utilisation factor [T.U.F]

DC Power delivered to the load

$T.U.F = \frac{\text{AC power rating of the transformer.}}{(V_s)_{\text{rms}} I_{\text{rms}}}$

$$V_{DC} I_{DC}$$

$$= \frac{I_{DC}^2 R_L}{(V_m) \cdot (I_m)}$$

$$\frac{I_{DC}^2 R_L}{(V_m) \cdot (I_m)}$$

$$= \frac{I_{DC}^2 R_L}{\frac{1}{2} \cdot I_m^2 (R_f + R_L)}$$

$$= \left(\frac{2 I_m}{\pi} \right)^2 R_L$$

$$= \frac{1}{2} (I_m)^2 (R_f + R_L)$$

$$= \frac{8}{\pi} \left[\frac{1}{(R_f/R_L + 1)} \right]$$

$$\approx 0.81$$

$\therefore T.U.F \text{ of Secondary} = 0.81$

The T.U.F of half-wave rectifier is 0.287

Full-wave rectifier can be considered as two half-wave rectifiers

$$\therefore \text{T.U.F} = 2(0.287) = 0.574 \quad \boxed{\begin{matrix} \text{T.U.F of} \\ \text{primary} \end{matrix}}$$

The T.U.F of full-wave rectifier is taken as the average of above two values,

$$\therefore \text{T.U.F} = \frac{0.81 + 0.574}{2} = \frac{\frac{\text{TUF at } 2^\circ}{2} + \frac{\text{TUF at } 1^\circ}{2}}{2}$$

$$\Rightarrow \text{T.U.F} = 0.692 \quad \boxed{=} \quad \boxed{\begin{matrix} \text{T.U.F} \\ \text{---} \end{matrix}}$$

* Voltage regulation:

★ Voltage regulation:

In a rectifier, the output voltage should not change w.r.t load current. The voltage regulation is a factor which tells about the change in DC output voltage, when the load changes from no-load to full-load condition.

$$\text{voltage regulation} = \frac{(V_{dc})_{\text{no load}} - (V_{dc})_{F.L.}}{(V_{dc})_{F.L.}} \times 100$$

$V_{dc(N.L)}$ = D.C Output voltage under no load conditions

$V_{dc(F.L.)}$ = D.C Output voltage under full load conditions

for a full-wave rectifier, per is 90

$$V_{dc(N.L)} = \frac{2V_m}{\pi} \cdot \frac{1}{1 + (R_F/R_L)}$$

$$R_F = \infty$$

$$\therefore V_{dc(N.L)} = \frac{2V_m}{\pi}$$

$$V_{dc(F.L.)} = I_{DC} \cdot R_L$$

$$\therefore \text{voltage regulation} = \frac{\frac{2V_m}{\pi} - I_{DC}R_L}{I_{DC}R_L} \times 100$$

$$\Rightarrow \frac{\frac{2V_m}{\pi} - \frac{2I_m}{\pi} R_L}{\frac{2I_m}{\pi} R_L} \times 100$$

$$\Rightarrow \text{Voltage regulation} = \frac{V_m - \bar{I}_m R_L}{\bar{I}_m R_L} \times 100$$

$$\Rightarrow \frac{\bar{I}_m (R_f + R_L) - \bar{I}_m R_L}{\bar{I}_m R_L} \times 100$$

$$\Rightarrow \frac{(R_f + R_L) - R_L}{R_L} \times 100$$

$$\Rightarrow \left(\frac{R_f}{R_L} \right) \times 100$$

* Advantages of Full-wave rectifier over Half-wave rectifier:

- * The rectification efficiency is higher compared to the half-wave rectifier
- * The ripple factor is low compared to half-wave rectifier
- * The DC output voltage and DC output current are higher than in half-wave rectifier

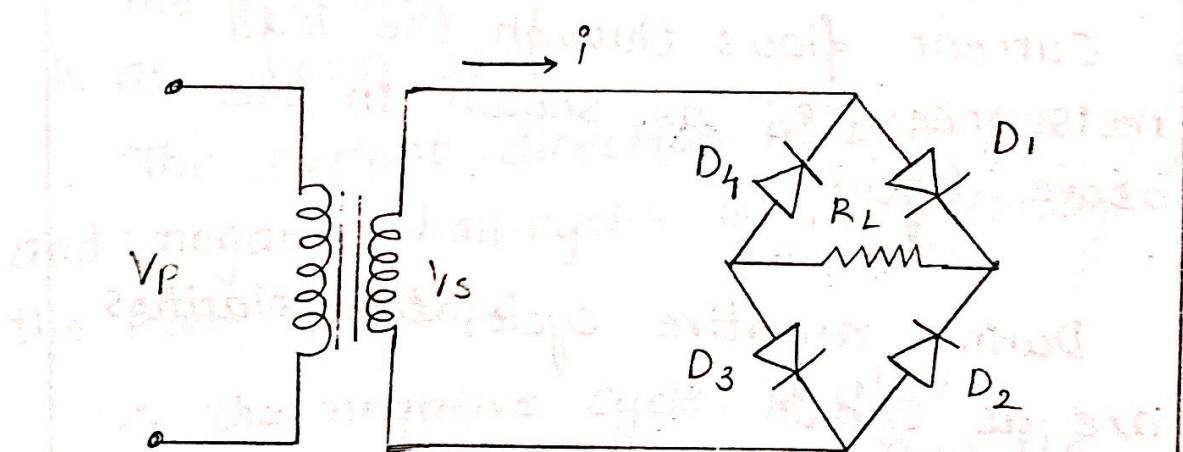
Disadvantages:

- * Full-wave rectifier uses centre tapped transformer which is costlier than normal transformer.

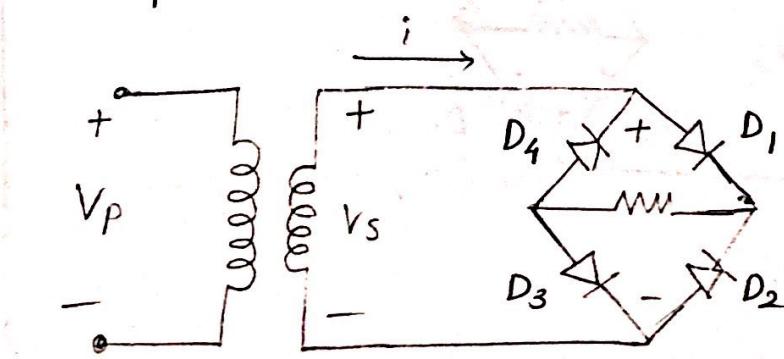
* The peak inverse voltage of full-wave rectifier is $2V_m$ which is twice than the peak inverse voltage in half-wave rectifier

Bridge rectifier:

Bridge rectifier is a full-wave rectifier. It contains four diodes which forms a bridge. The circuit diagram of bridge rectifier is as shown in following figure

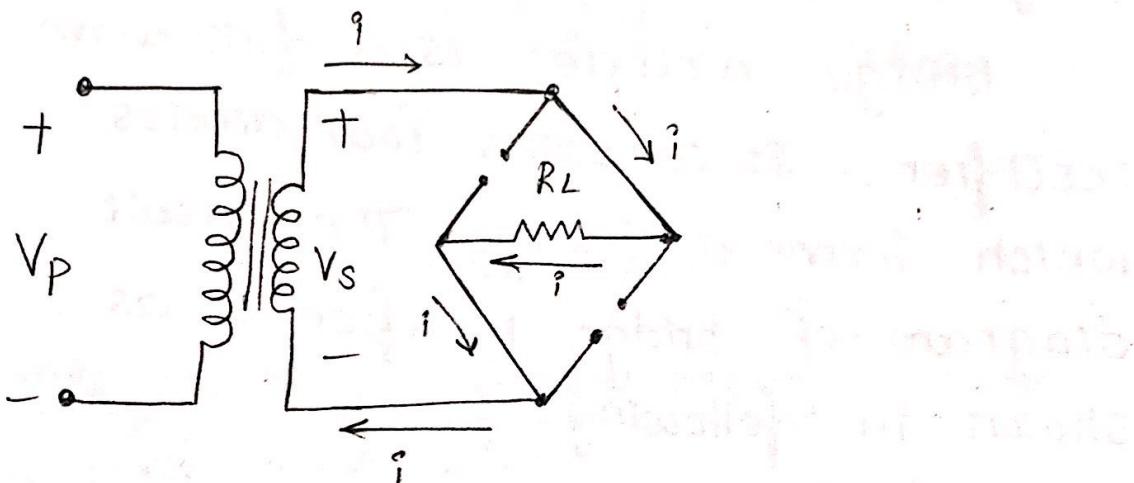


During the positive half-cycle, the polarities are as shown.



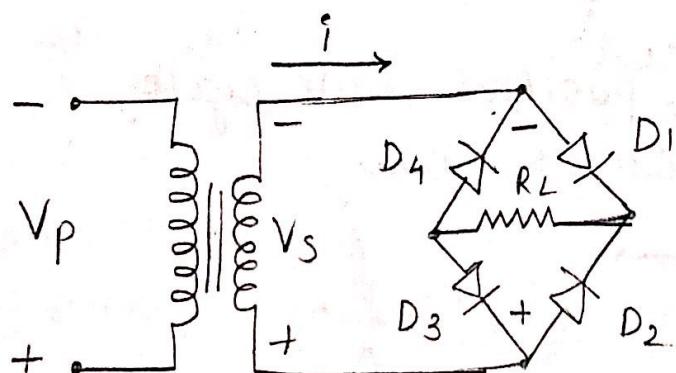
With the polarities shown in the figure, Diodes D₁ and D₃ will be forward biased and acts as short circuit

Diodes D₂ and D₄ will be reverse biased and acts as open circuit



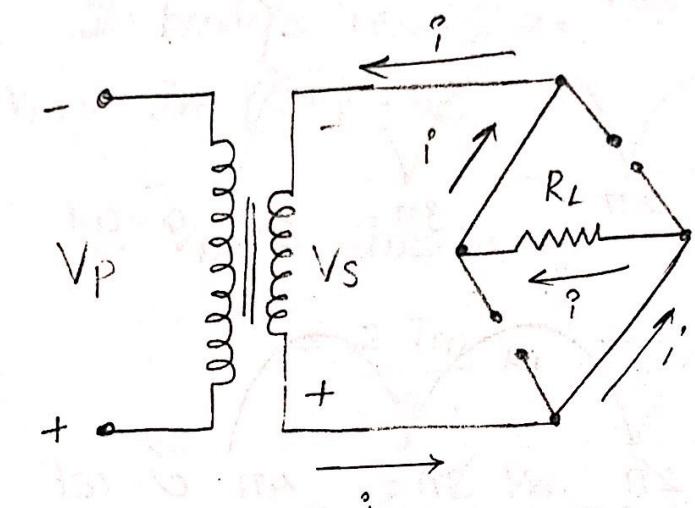
Current flows through the load resistance ' R_L ' as shown in the above figure

During negative cycle, the polarities are as shown



With the above shown polarities, diode D₂ and D₄ will be forward biased and act as short circuits.

Diodes D₁ and D₃ will be reverse Biased and act as open circuits.

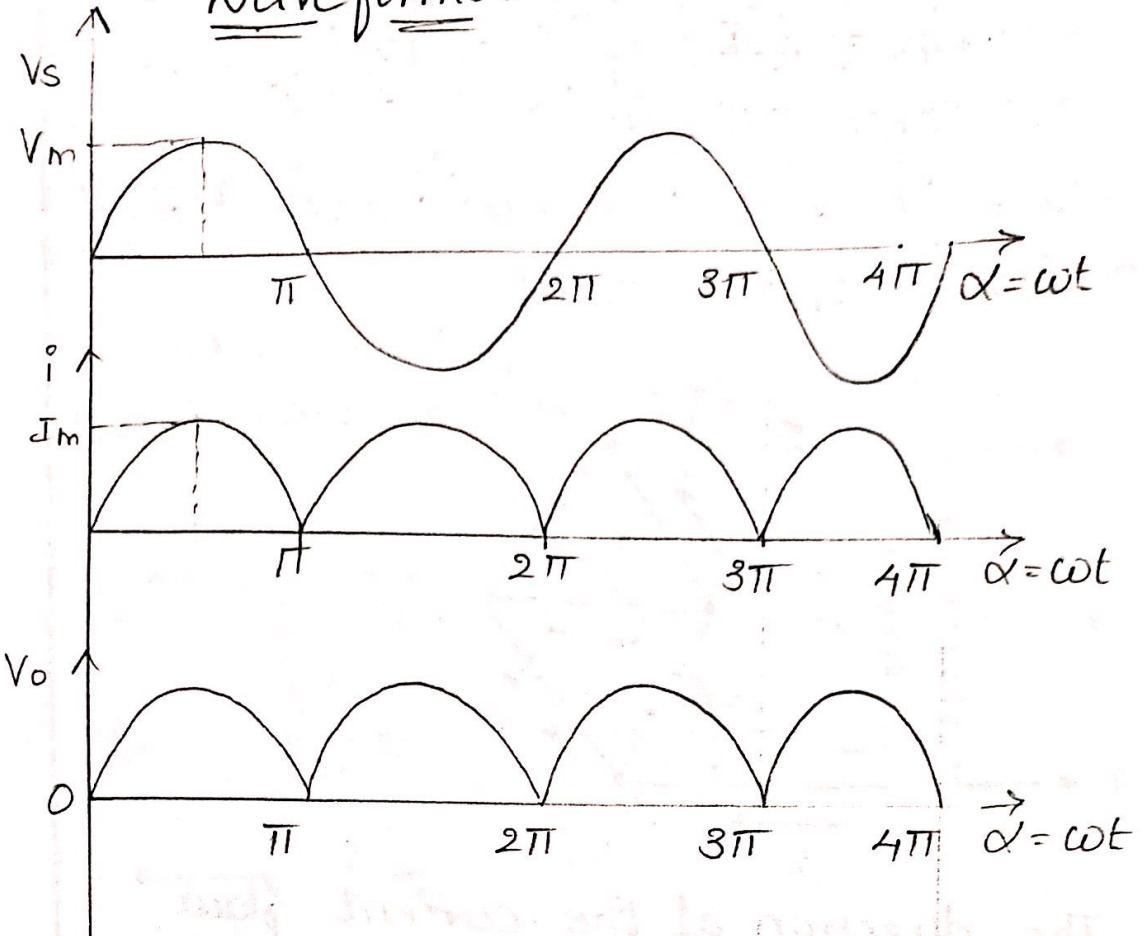


The direction of the current flow is as shown above.

The current direction in both positive and negative half-cycles is same through the load-resistance

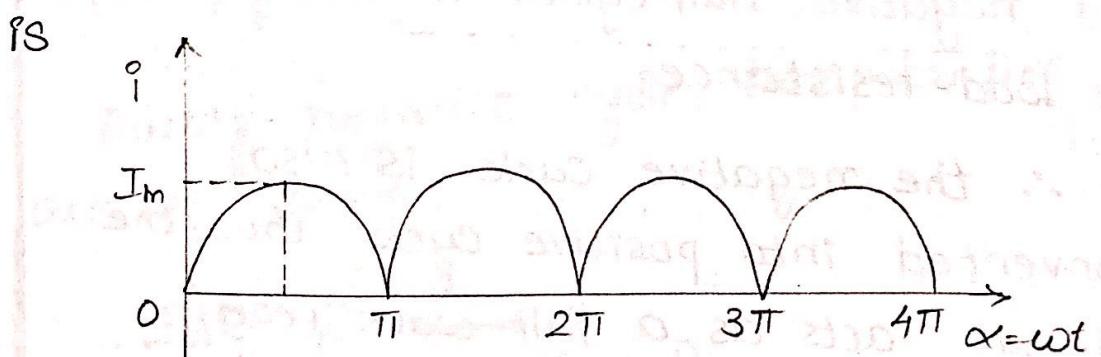
~~RMS value of Output current~~
∴ the negative cycle is also converted into positive cycle. Thus, the circuit acts as a full-wave rectifier.

Waveforms:



DC Output current:

Current wave-form in Bridge rectifier



Mathematically, the current can be represented as,

$$i = I_m \sin \alpha$$

$$I_{DC} = \frac{2Im}{\pi}$$

The derivation is
Same as full
wave rectifier

D.C Output Voltage:

In bridge rectifier, the peak voltage

$$V_m = Im (2R_f + R_L)$$

$$\therefore V_{DC} = I_{DC} R_L$$

$$= \frac{2Im}{\pi} R_L$$

$$= \frac{2}{\pi} \left(\frac{V_m}{2R_f + R_L} \right) R_L$$

$$V_{DC} = \frac{\frac{2V_m}{\pi}}{1 + 2R_f/R_L}$$

RMS value of Output current [I_{rms}]

$$I_{rms} = \frac{Im}{\sqrt{2}}$$

Derivation is same as in full-wave
Rectifier

Output RMS Voltage:

$$V_{rms} = I_{rms} \cdot R_L$$

$$= \left[\frac{I_m}{\sqrt{2}} \right] R_L$$

$$V_{rms} = \frac{V_m}{\sqrt{2} [2R_f + R_L]} R_L$$

D.C Output power [P_{D.C}]

$$P_{DC} = V_{DC} \cdot I_{DC}$$

$$= I_{DC}^2 R_L$$

$$= \left[\frac{\alpha I_m}{\pi} \right]^2 R_L$$

A.C Input power [P_{AC}]:

$$P_{AC} = P_{rms} V_{rms}$$

$$= P_{rms} \left[2R_f + R_L \right]$$

$$= \left(\frac{I_m}{\sqrt{2}} \right)^2 (2R_f + R_L)$$

* rectification efficiency:

$$\eta = \frac{\text{D.C Output power}}{\text{A.C Input power}}$$

$$= \frac{V_{DC} \cdot I_{DC}}{V_{rms} I_{rms}}$$

$$= \frac{I_{DC}^2 R_L}{I_{rms}^2 (2R_f + R_L)}$$

$$= \frac{\left(\frac{2Im}{\pi}\right)^2 R_L}{\left(\frac{Im}{\sqrt{2}}\right)^2 (2R_f + R_L)}$$

$$\text{approx. } \eta = \frac{\frac{8}{\pi^2}}{1 + 2R_f/R_L}$$

$$= \frac{0.81}{1 + 2R_f/R_L}$$

$$\approx 81\%$$

* ripple factor:

$$\gamma = \frac{i_{ac rms}}{I_{DC}} = \sqrt{\left(\frac{I_{rms}}{I_{DC}}\right)^2 - 1}$$

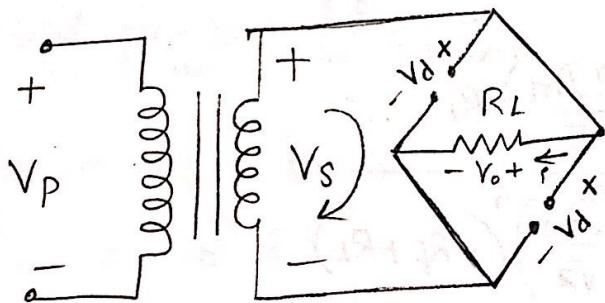
[Derivation is same as in full-wave rectifier]

$$\Rightarrow r = \sqrt{\left(\frac{Im}{\sqrt{2}}\right)^r - 1}$$

$$= \sqrt{\frac{\pi^r}{8} - 1}$$

$$\Rightarrow r = 0.48$$

* Peak Inverse voltage:



The above circuit indicates the polarities of various voltages in positive half cycle.

Applying K.V.L to the loop, as shown in the figure

$$-Vs + Vd = 0$$

$$\Rightarrow Vs = Vd$$

The peak value of 'Vs' is 'Vm'

\therefore Peak value of Vd is 'Vm'

$$\therefore PIV = Vm$$

* Transformer utilisation factor:

T.U.F = DC power delivered to the load

AC power rating of the transformer

$$= \frac{V_{DC} \cdot I_{DC}}{(V_s)_{rms} \cdot I_{rms}}$$

$$= \frac{I_{DC}^2 R_L}{\left(\frac{V_m}{\sqrt{2}}\right) \left(\frac{I_m}{\sqrt{2}}\right)}$$

$$= \frac{\left(\frac{2 I_m}{\pi}\right)^2 R_L}{\frac{1}{2} I_m^2 (2R_f + R_L)}$$

$$= \frac{8/\pi^2}{1+2(R_f/R_L)}$$

$$= \frac{0.81}{1+2R_f/R_L}$$

$$\approx 0.81$$

* Voltage Regulation:

$$\text{Voltage regulation} = \frac{(V_{DC})_{NL} - (V_{DC})_{F.L}}{(V_{DC})_{F.L}}$$

$$= \frac{\frac{2V_m}{\pi} - I_{DC}R_L}{I_{DC}R_L}$$

$$= \frac{\frac{2V_m}{\pi} - \frac{2I_m}{\pi} R_L}{\frac{2I_m}{\pi} R_L}$$

$$= \frac{I_m(2R_f + R_L) - I_m R_L}{I_m R_L}$$

$$= \frac{2R_f}{R_L}$$

Advantages of Bridge Rectifier over full-wave rectifier:

Comparision between Full-wave and Bridge rectifiers:

Full Wave Rectifier	Bridge Rectifier
1) It needs a centre tapped transformer \therefore It is not Economical	1) It does not need a centre tapped transformer \therefore It is Economical
2) The P.I.V of full wave rectifier is $2V_m$ which is high	2) The P.I.V of Bridge rectifier is V_m
3) The current in the transformer Secondary will not alter in each cycle \therefore The core of the transformer may Saturate	3) The current through transformer Secondary winding alters in each cycle \therefore The transformer core will not Saturate
4) The T.U.F of full wave rectifier is 0.692 only.	4) The T.U.F of Bridge rectifier is 0.81 \therefore Bridge rectifier efficiently uses the transformer

Disadvantages of Bridge rectifier

- 1) The Bridge rectifier acquires four diodes as compared to two diodes in full-wave rectifier.

This causes additional voltage drop across the diodes. This reduces the output voltage.

Problems:

→ A full wave rectifier is from a transformer having a centre tapped secondary winding. The rms voltage from either end of secondary to centre tapped is 30V. If the diode forward resistance is 2Ω and [that of the half-secondary is 80Ω] and for a load of $1k$. Calculate

- (a) Power delivered to the load
- (b) % regulation at full load
- (c) Rectification efficiency
- (d) Ripple factor
- (e) T.U.F [Secondary] (f) P.I.V

A) Given,

$$V_{rms} = 30V$$

$$\Rightarrow V_m = V_{rms}(\sqrt{2}) = 30(\sqrt{2}) = 42.42V.$$

(a) Power delivered

$$P_{DC} = V_{DC} I_{DC}$$

$$I_{DC} = \frac{2 I_m}{\pi}; V_{DC} = \frac{2 V_m}{\pi \frac{1+R_f/R_L}{1+R_f/R_L}}$$

$$I_m = V_m / (R_f + R_L)$$

$$\Rightarrow I_m = \left[\frac{42.42}{2+1000} \right] = 0.042A \Rightarrow 42.3mA$$

$$I_{DC} = \frac{2Im}{\pi} = \frac{2(42.3)}{\pi} = 26.9 \text{ mA}$$

$$V_{DC} = I_{DC} R_L$$

$$\Rightarrow V_{DC} = 26.9 \times 10^3 \times 1000$$

$$\Rightarrow V_{DC} = 26.9 \text{ V}$$

$$\therefore P_{DC} = I_{DC} V_{DC}$$

$$= (26.9)(2.6.9) \times 10^3$$

$$= 0.42361$$

$$= 423.61 \text{ mW}$$

(c) Rectification Efficiency

$$\eta = \frac{\text{DC Output Power}}{\text{AC Input Power}} (100)$$

$$\text{DC Output power } P_{DC} = 423.6 \text{ mW}$$

$$\text{AC Input Power } P_{AC} = I_{rms} V_{rms}$$

$$= I_{rms} [R_f + R_L]$$

$$= \left(\frac{Im}{\sqrt{2}} \right)^2 (1002)$$

$$= \frac{(42.3)^2}{2} (1002)$$

$$\therefore P_{AC} = 89.6 \text{ mW}$$

$$\therefore \eta = \frac{723.6}{896.4} (100)$$

$$\Rightarrow \eta = 80.2\%$$

(d) voltage regulation = $\left(\frac{R_f}{R_L} \right) 100$

$$\Rightarrow \% R = \frac{2}{1000} (100)$$

$$\Rightarrow \% R = 0.2\%$$

(e) Ripple factor = $\sqrt{\left(\frac{I_{rms}}{I_{dc}} \right)^2 - 1}$

$$= \sqrt{\frac{8.946 \times 10^4}{7236 \times 10^4} - 1}$$

$$= 0.486.$$

(e) T.O.F (Secondary)

$$T.O.F = \frac{DC \text{ power delivered to the load}}{AC \text{ power rating}}$$

$$= \frac{V_{dc} \cdot I_{dc}}{(V_s)_{rms} \cdot I_{rms}} = \frac{P_{dc}}{30(8m)^2}$$

$$= \frac{723.61}{30(0.029)} = 0.806$$

(c) Peak inverse Voltage = 2Vm

$$\Rightarrow P.I.V = 84.84 V.$$

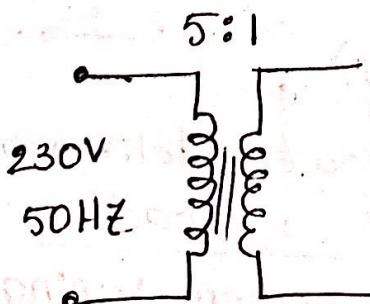
* A $230V$, $50Hz$ A.C Signal is applied to the input of the centre tapped transformer of a full wave rectifier with turns ratio $5:1$. The load resistance is $10k$ and the diode has a forward resistance of 100Ω . Determine

- (a) DC Output current
- (b) Rms output current
- (c) DC power delivered
- (d) Rectification Efficiency
- (e) Ripple factor
- (f) P.I.V

A)

Given,

$$V_{rms} = 230V. \quad (P)$$



$$n_1:n_2 = 5:1$$

$$\Rightarrow \frac{V_p(rms)}{V_{rms}} = \frac{5}{1}$$

$$\Rightarrow V_{rms} = \frac{1}{5} (V_p) = \frac{1}{5} (230) = 46V.$$

$$V_m = V_s(\text{rms}) \sqrt{2} = 46(\sqrt{2}) = 65.05V.$$

$$\Rightarrow V_m = 65.05V.$$

(a) $I_{DC} = \frac{2 I_m}{\pi}$

$$I_m = \frac{V_m}{(R_f + R_L)} = \frac{65.05}{(100 + 10000)}$$

$$\Rightarrow I_m = 6.4 \text{ mA}$$

$$P_{DC} = \frac{\omega (6.4 \times 10^3)^2}{\pi} = 4.1 \text{ mA}$$

(b) $I_{rms} = \frac{I_m}{\sqrt{2}} = \frac{6.4 \times 10^3}{\sqrt{2}} = 4.5 \text{ mA}$

(c) $P_{DC} = \left(\frac{\omega I_m}{\pi} \right)^2 (R_L) = (I_{DC})^2 R_L$

$$= 0.165 \text{ W.} = 168.1 \text{ mW.}$$

(d) $\% \eta = \frac{\text{DC output Power}}{P_{AC}} \times 100$

$$P_{AC} = I_{rms} (R_f + R_L) = (4.5)^2 (100 + 10000)$$

$$\Rightarrow P_{AC} = 206.3 \text{ mW.}$$

$$\therefore \eta = \frac{165.5}{206.3} \times 100 = 80.1\%$$

(e) Ripple factor

Ripple frequency = frequency of
Output signal

→ for full wave rectifier, Output
frequency = α (Input frequency)
 $= \alpha (50 \text{ Hz})$
 $= 100 \text{ Hz}$

(d) $P.I.V = V_m(2) = (65.05)(2)$

$$\Rightarrow P.I.V = 130.10 \text{ V.}$$

* A Signal $110 \sin(\omega t)$ is applied to transformer of a bridge rectifier. The transformer has a turns ratio of 5:1 and a secondary winding resistance of 100Ω . A load resistance is $10k\Omega$ & each diode has R_f of 100Ω . Determine

(a) DC output current
(b) RMS output current

(c) DC power delivered

(d) Rectification Efficiency

(e) Ripple frequency

(f) P.I.V.

A) Given,
 $\text{Signal} = 110 \sin(2\pi 100t)$

turns ratio = 5:1

$$(V_p)_m = 110.$$

$$(V_p)_{\text{rms}} = \frac{110}{\sqrt{2}} = 77.7$$

$$\frac{(V_p)_{\text{rms}}}{(V_s)_{\text{rms}}} = \frac{5}{1}$$

$$\Rightarrow \frac{77.7}{(V_s)_{\text{rms}}} = \frac{5}{1}$$

$$\Rightarrow (V_s)_{\text{rms}} = \frac{1}{5} (77.7) = 15.54 \text{ V.}$$

$$V_m = (V_s)_{\text{rms}} (\sqrt{2}) = 21.97 \text{ V.}$$

(a) $I_{DC} = \frac{2Im}{\pi}$

$$Im = \frac{V_m}{2R_f + R_s + R_L} = \frac{21.97}{200 + 1000 + 100}$$

$$\Rightarrow Im = \frac{21.97}{300 + 10^4} = 2.13 \text{ mA}$$

$$I_{DC} = \frac{2(2.13)}{\pi}$$

$$\Rightarrow I_{DC} = 1.35 \text{ mA.}$$

(b) $I_{\text{rms}} = \frac{Im}{\sqrt{2}} = \frac{2.13}{\sqrt{2}} = 1.50 \text{ mA.}$

$$(c) P_{DC} = V_{DC} [I_{DC}]$$

$$= (I_{DC})^2 R_L$$

$$= (1.35 \times 10^3)^2 \cdot 10^4$$

$$= 18.22 \text{ mW.}$$

$$d) \eta = \frac{P_{DC}}{P_{AC}}$$

$$P_{AC} = V_{rms} [I_{rms}]$$

$$= (I_{rms})^2 (2R_f + R_L + R_s)$$

$$= (1.50 \times 10^3)^2 (300 + 10^4)$$

$$= 23.17 \text{ mW.}$$

$$\therefore \eta = \frac{18.22}{23.17} = 0.786$$

$$\% \eta = 78.6\%$$

$$(e) \text{ ripple frequency} = 2 \times \text{i/p freq}$$

$$\text{each half cycle} = 2(100)$$

$$= 200 \text{ Hz}$$

$$(f) PIV = V_m = 21.97 \text{ V.}$$

$$(g) TUF = \frac{P_{DC}}{(V_s)_{rms} \cdot I_{rms}}$$

$$(h) f_{sw}$$

A) Draw the circuit diagram of a fullwave rectifier using centretap transformer to obtain an Output DC voltage $V_{DC} = 18V$. at 200mA and $(V_{DC})_{no\ load} = 20V$. Assume suitable value of R_f and Transformer resistance and also mention Transformer rating and sketch the Input & Output waveforms.

A) Given that,

$$V_{DC} = 18V$$

$$(V_{DC})_{N.L} = 20V$$

$$V_{DC} = \frac{2V_m/\pi}{1 + R_f/R_L}$$

here, $R_L = \infty$

$$\Rightarrow V_{DC} = \frac{2V_m/\pi}{1 + 0} = 2V_m/\pi$$

$$\Rightarrow 18 = \frac{2V_m}{\pi}$$

$$\Rightarrow V_m = 10\pi$$

$$\Rightarrow V_m = 31.4V$$

$$(V_s)_{rms} = \frac{V_m}{\sqrt{2}} = \frac{31.4}{\sqrt{2}} = 22.21V$$

When there is no capacitor filter, the diode conducts for $\frac{1}{2}\pi$ half cycle and the other half cycle

Transformer Secondary RMS voltage

$$(V_{rms})_S = \omega (Z_2 \cdot Z) = 44.4 \text{ V.}$$

Input primary voltage = 230V.

$$\therefore \text{Winding ratio} = \frac{230}{44.4} \\ = 5.18 \\ \approx 5$$

then, Secondary Voltage = $\frac{230}{5} = 46 \text{ V.}$

\therefore Transformer rating =

Filters:

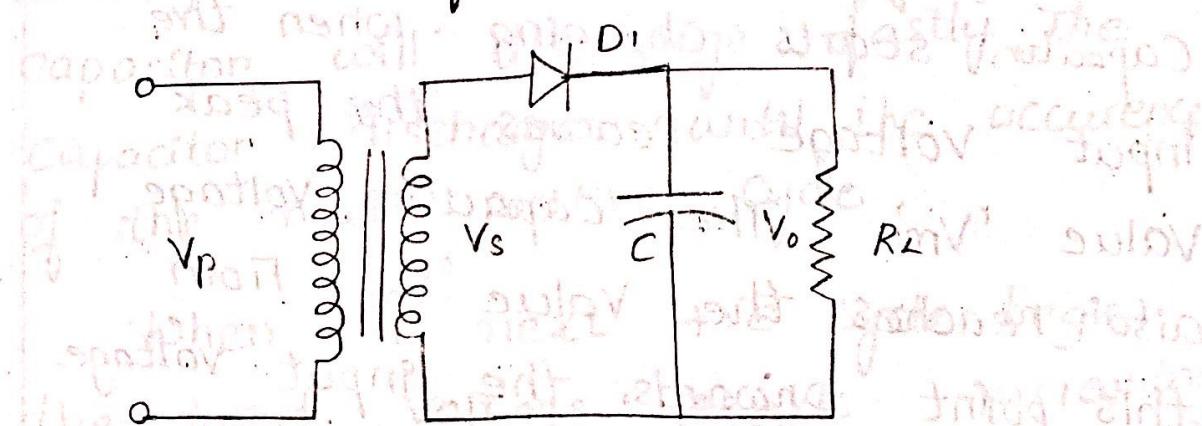
The output of rectifier contains both A.C and D.C components. Filter is an electronic circuit, which is used to reduce A.C components present in the output of the rectifier.

Types of filters:

- 1) Capacitor filter
- 2) Inductor filter
- 3) L-C filter (or) choke input filter.
- 4) C-L-C filter (or) Bi-Section filter.

Capacitor filter:

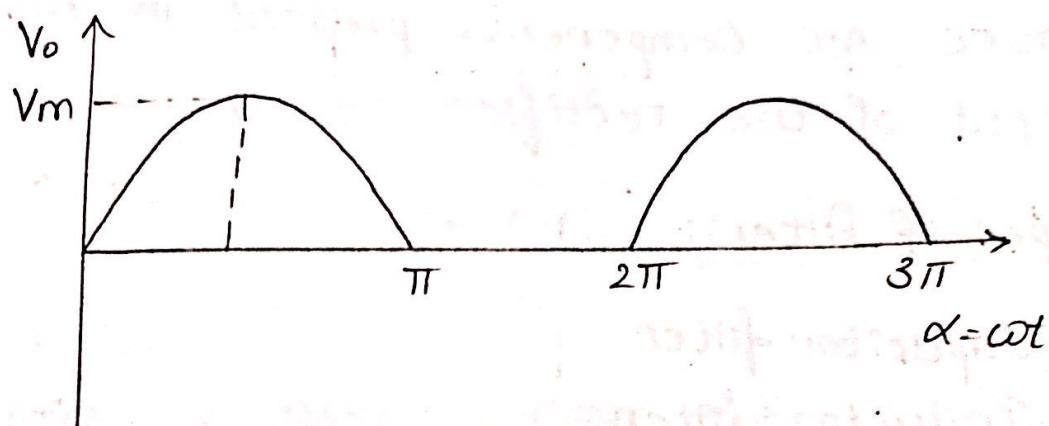
The circuit diagram of half-wave rectifier with capacitor filter, is as shown.



When, there is no capacitor filter, the diode conducts for +ve half cycle and the -ve half-cycle

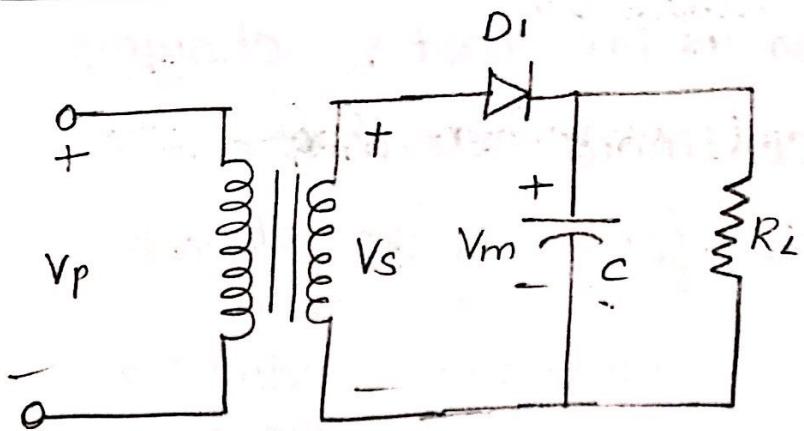
is completely suppressed.

The output waveform look like the following.



now, consider the situation, after adding the capacitor filter. Assume, initially that the capacitor has no charge during the +ve half-cycle, the diode starts conducting and current flows in the circuit and capacitor starts charging. When the input voltage reaches the peak value ' V_m ' The capacitor voltage also reaches the value ' V_m '. From this point onwards, the input voltage starts decreasing.

Whereas the capacitor voltage is at ' V_m '

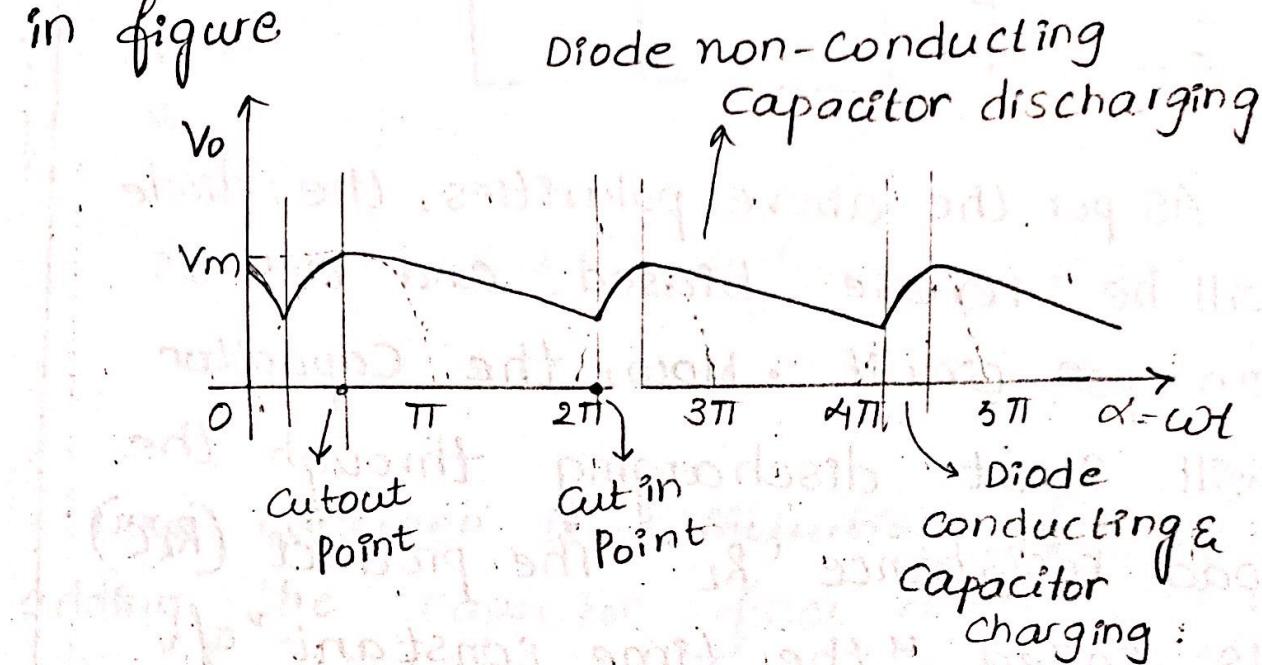


As per the above polarities, the diode will be reverse biased and acts as an open circuit. Now, the capacitor will start discharging through the load resistance ' R_L '. The product ($R_L C$) is called "the time constant" of the circuit.

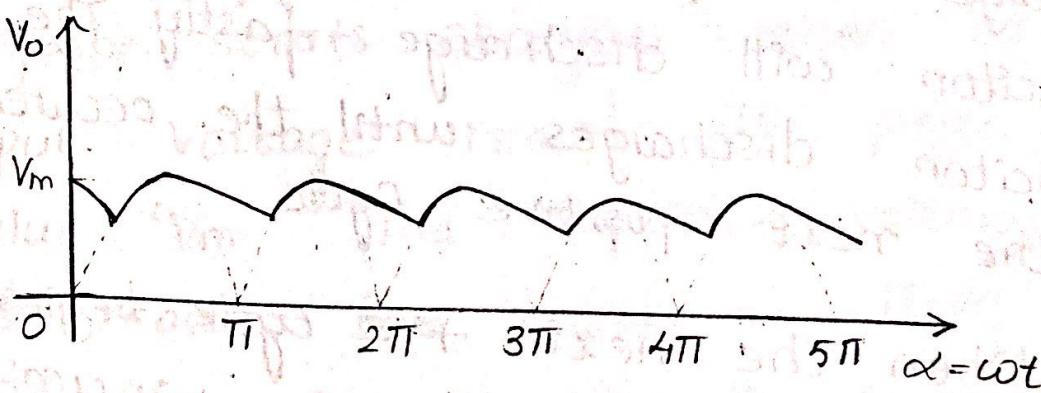
If this is large, capacitor will discharge slowly. If this is small, capacitor will discharge fastly. The capacitor discharges until the occurrence of the next positive cycle.

When the next +ve cycle begins, the input voltage starts increasing. When this voltage exceeds the capacitor voltage, the diode will be forward biased and starts conducting.

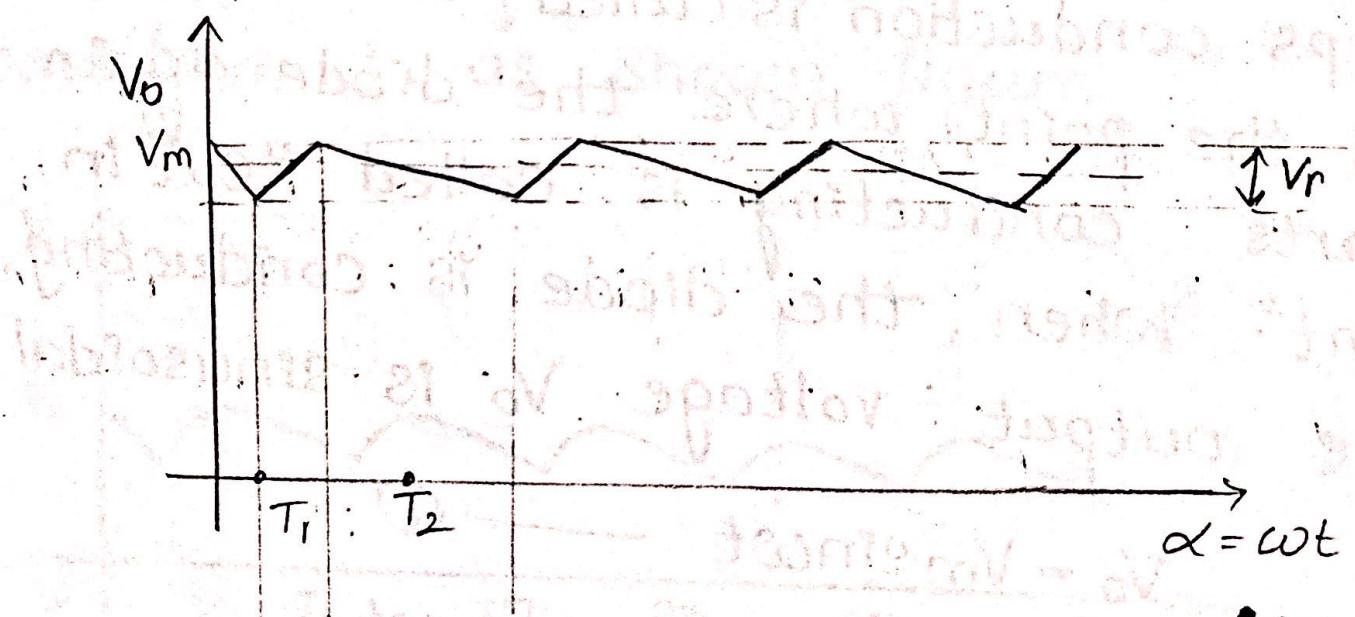
The Capacitor will start charging. This cycle continuous and the resulting wave form is as shown in figure



If the Capacitor filter is used with full-wave rectifier, the associated waveform is as shown figure.



The output of a rectifier, with the capacitor filter can be approximated as a triangular waveform as shown in the figure



$T_1 + T_2 = \text{Total time period } (T)$. [for Output signal]

During T_2 , the capacitor discharges steadily and the current through the capacitor is given by

$$I = \frac{dQ}{dt}$$

$$\Rightarrow dQ = Idt$$

$$\Rightarrow Q = \int_0^{T_2} Idt$$

$$T = T_1 + T_2 \text{ and } T_2 \gg T_1$$

$$\therefore T \approx T_2$$

$$\therefore Q = \int_0^T idt$$

$$\Rightarrow Q = \frac{1}{T}(T) \int_0^T idt$$

$$\Rightarrow Q = T \left[\frac{1}{T} \int_0^T idt \right]$$

$$\Rightarrow Q = T \cdot I_{DC}$$

\therefore The total charge lost by the capacitor is

$$Q = T \cdot I_{DC}$$

As shown in the figure, the capacitor voltage changes by V_r .

\therefore The charge gained by the capacitor, during the period T_1 ,

is given by,

$$Q_g = CV_r.$$

By charge Balance,

charge lost = charge gain

$$\Rightarrow Q_g = Q_L$$

$$\Rightarrow CV_r = T \cdot I_{DC}$$

$$\Rightarrow I_{DC} = \frac{CV_r}{T} \quad \text{--- (3)}$$

Half-wave rectifier:

$$I_{DC} = \frac{CV_r}{T}$$

and

$$T = \frac{1}{f}$$

$$\Rightarrow I_{DC} = CV_r f.$$

$$V_{DC} = I_{DC} R_L$$

$$\Rightarrow V_{DC} = CV_r f R_L \quad \text{--- (4)}$$

Full-wave rectifier:

$$I_{DC} = \frac{CV_r}{T}$$

and

$$T = \frac{1}{2f}$$

$$\Rightarrow I_{DC} = CV_r 2f.$$

$$V_{DC} = I_{DC} R_L$$

$$\Rightarrow V_{DC} = CV_r 2f R_L \quad \text{--- (4)}$$

The triangular wave form shown in the figure has an RMS value of

$$V_{rms} = V_r / 2\sqrt{3}. \quad \text{--- (5)}$$

for both half-wave and full wave rectifiers.

Half-wave rectifier

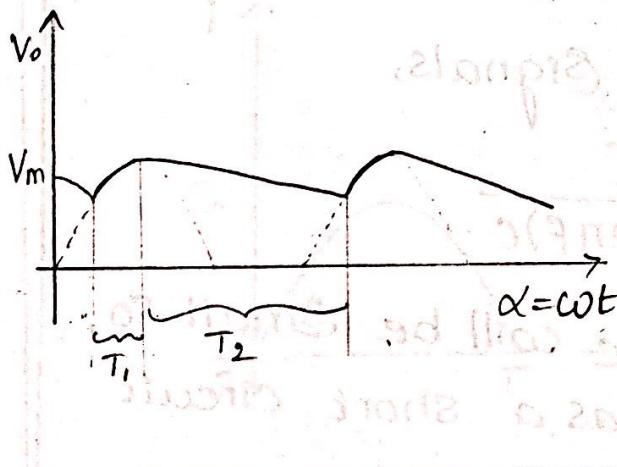
from ⑤, ④ becomes

$$V_{DC} = C f R_L \frac{1}{2\sqrt{3}} V_{rms}$$

$$\Rightarrow \frac{V_{rms}}{V_{DC}} = \frac{1}{2\sqrt{3} f R_L C}$$

\therefore The ripple factor

$$\gamma = \frac{1}{2\sqrt{3} f R_L C}$$



full-wave rectifier

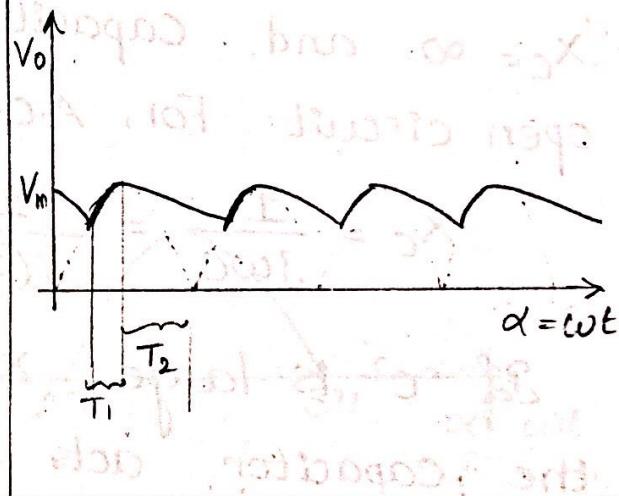
from ⑤, ④ becomes

$$V_{DC} = C f R_L \frac{1}{\sqrt{3}} V_{rms}$$

$$\Rightarrow \frac{V_{rms}}{V_{DC}} = \frac{1}{4\sqrt{3} f R_L C}$$

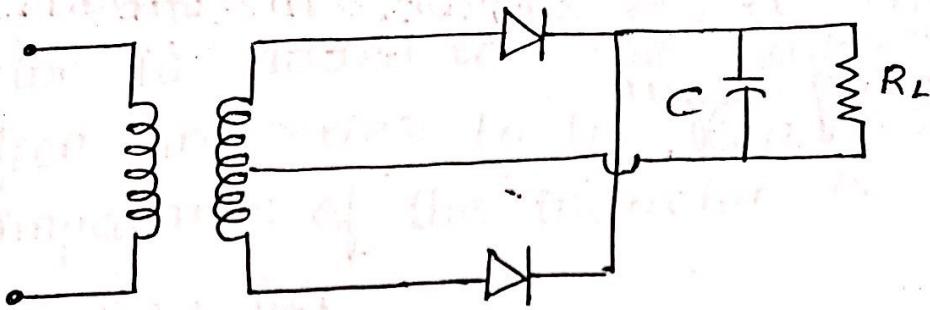
\therefore The ripple factor

$$\gamma = \frac{1}{4\sqrt{3} f R_L C}$$



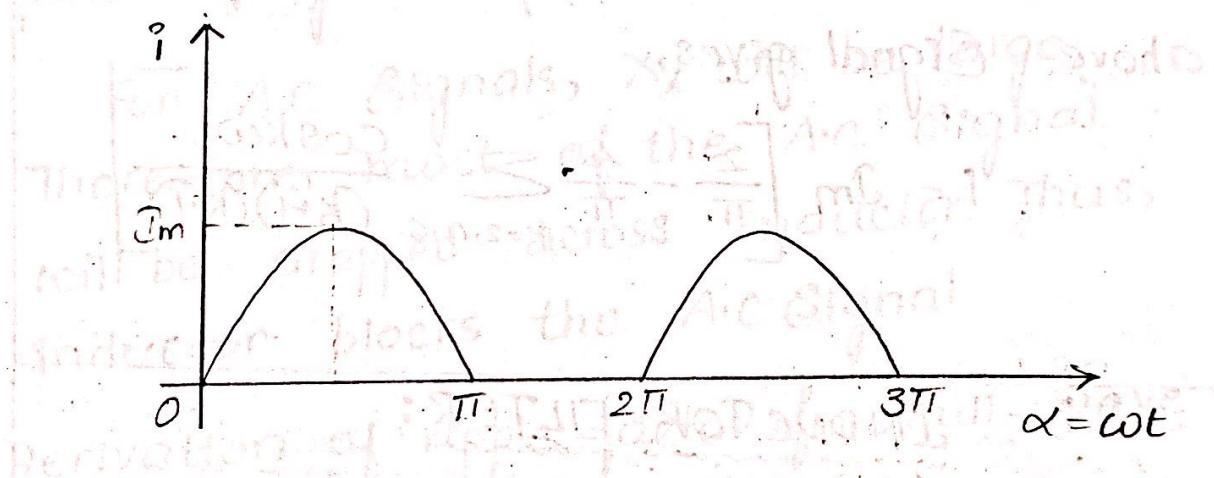
If in question, half-wave rectifier or full-wave rectifier is not given, by default write answer for full-wave rectifier.

* Full-wave rectifier with capacitor filter.



* Harmonic components in rectifier Output:

The output of a half-wave rectifier without filter is plotted in the following figure



The above signal can be represented as a sum of infinite no. of sinusoidal signals given by,

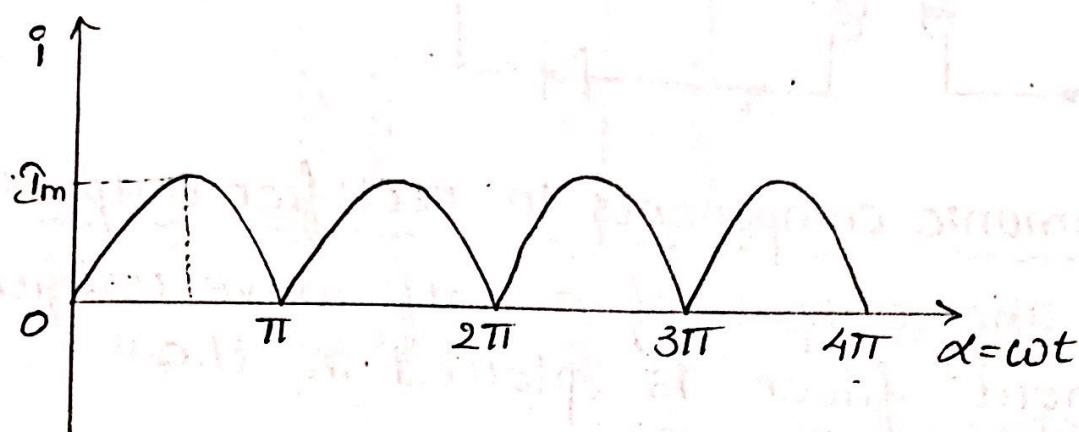
$$i = I_m \left[\frac{1}{\pi} + \frac{1}{2} \sin \omega t - \frac{2}{\pi} \sum_{k=2,4,\dots}^{\infty} \frac{\cos k \omega t}{(k+1)(k-1)} \right]$$

I_m/n
Arg. Value
of current

AC component
Present in
the Signal

Higher order
harmonics
Present in
the signal

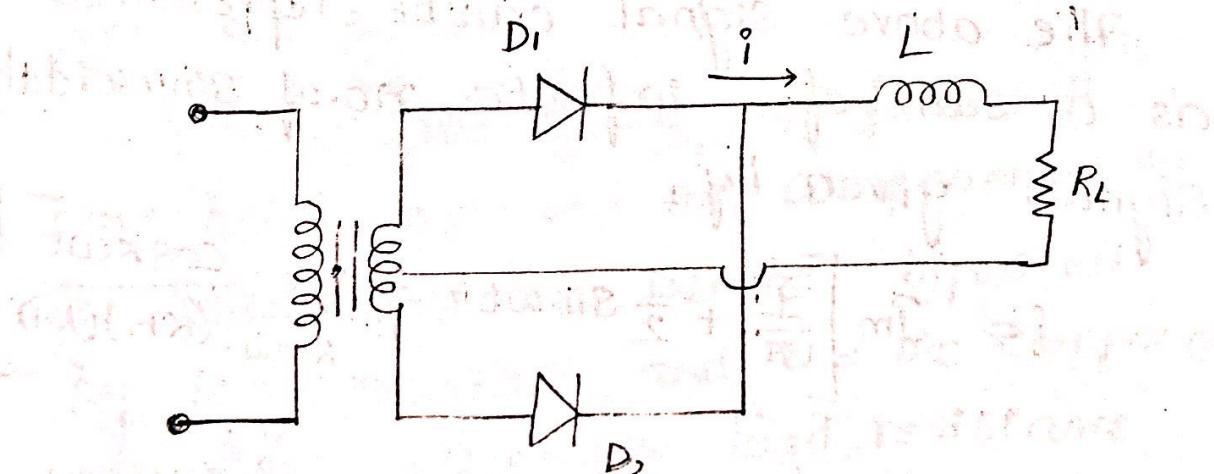
Similarly, the output full-wave of rectifier is as shown in the following figure



The Fourier-Series expansion of above Signal gives,

$$i = I_m \left[\frac{2}{\pi} - \frac{4}{\pi} \sum_{k=2,4,6,\dots} \frac{\cos k\omega t}{(k+1)(k-1)} \right]$$

INDUCTOR FILTER:



Full

Working: [Theoretical explanation]

As shown in the above figure, the inductor is added to the full-wave rectifier in series to the load resistance. The impedance of the inductor is

$$X_L = j\omega L$$

The output current contains both AC and DC components. For DC signals,

- $X_L = 0$ and inductor acts as a short circuit and allows DC signals to pass through the load resistance.

For AC signals, X_L will be large. Therefore, most of the AC signal will be dropped across inductor. Thus, inductor blocks the AC signal.

Derivation of ripple factor for Full-wave rectifier with inductor filter:

$$i = \text{Im} \left[\frac{2}{\pi} - \frac{4}{\pi} \sum_{k=2,4,6, \dots} \frac{\cos k\omega t}{(k+1)(k-1)} \right]$$

The above equation represents the current components in a full-wave rectifier. Expanding the above equation, we get

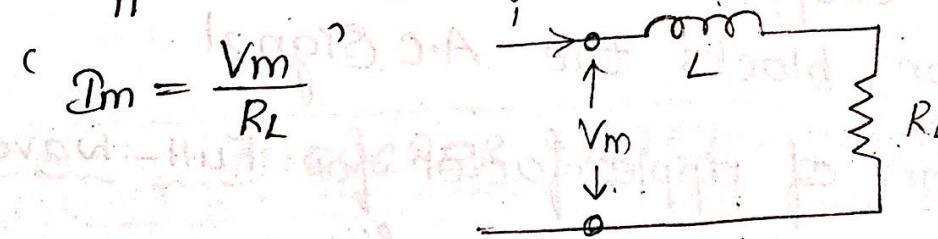
$$i = \left[\frac{2\bar{I}_m}{\pi} - \frac{4\bar{I}_m}{3\pi} \cos 2\omega t - \frac{4\bar{I}_m}{15\pi} \cos 4\omega t \right. \\ \left. - \frac{4\bar{I}_m}{35\pi} \cos 6\omega t - \dots \right]$$

All the higher harmonic components will be easily blocked by the inductor therefore, we can neglect the higher components.

$$\therefore i = \left[\frac{2\bar{I}_m}{\pi} - \frac{4\bar{I}_m}{3\pi} \cos 2\omega t \right]$$

Consider the first component,

i.e $\frac{2\bar{I}_m}{\pi}$ in this component,



for the A.C component,

$$\bar{I}_m = \frac{V_m}{(R_L + j\omega_2 L)}$$

\therefore The total current,

$$i = \frac{2V_m}{\pi R_L} - \frac{4V_m}{3\pi(R_L + 2j\omega L)} \cos 2\omega t$$

$$\Rightarrow i = \frac{2V_m}{\pi R_L} - \frac{4}{3\pi} \frac{V_m}{\sqrt{R_L^2 + 4\omega^2 L^2}} \cos(2\omega t - \phi)$$

$$\text{where, } \phi = \tan^{-1}\left(\frac{2\omega L}{R_L}\right)$$

The RMS value of the A.C component present in the output

$$(i_{ac})_{rms} = \frac{4V_m}{3\pi \cdot \sqrt{2} \cdot \sqrt{(R_L^2 + \omega^2 L^2)^2}}$$

$$\gamma = \frac{(i_{ac})_{rms}}{i_{dc}} = \frac{(i_{ac})_{rms}}{\left(\frac{2V_m}{\pi R_L}\right)}$$

$$\Rightarrow \gamma = \frac{2R_L}{3\sqrt{2} \left(\sqrt{R_L^2 + 4\omega^2 L^2} \right)}$$

For better performance, 'L' should be larger than 'R_L'

$$\text{i.e., } \omega L \gg R_L$$

$$\Rightarrow 4\omega^2 L^2 \gg R_L^2$$

$$\Rightarrow \gamma = \frac{2R_L}{3\sqrt{2} \left(\sqrt{4\omega^2 L^2} \right)} = \frac{R_L}{3\sqrt{2} (\omega L)}$$

$$\therefore \gamma = \frac{R_L}{3\sqrt{2} \omega L}$$

L-C Filter (or) L-section filter (or)

choke-input filter:

The ripple factor of a full-wave rectifier when using capacitor filter is given by

$$\gamma = \frac{1}{4\sqrt{3}fR_L C}$$

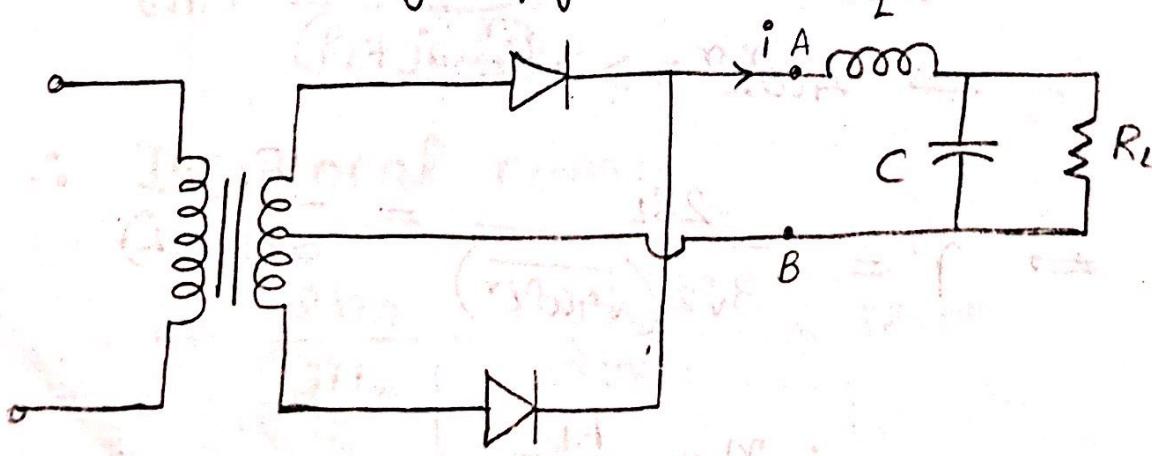
When using inductor filter,

$$\gamma = \frac{R_L}{3\sqrt{2}CWL}$$

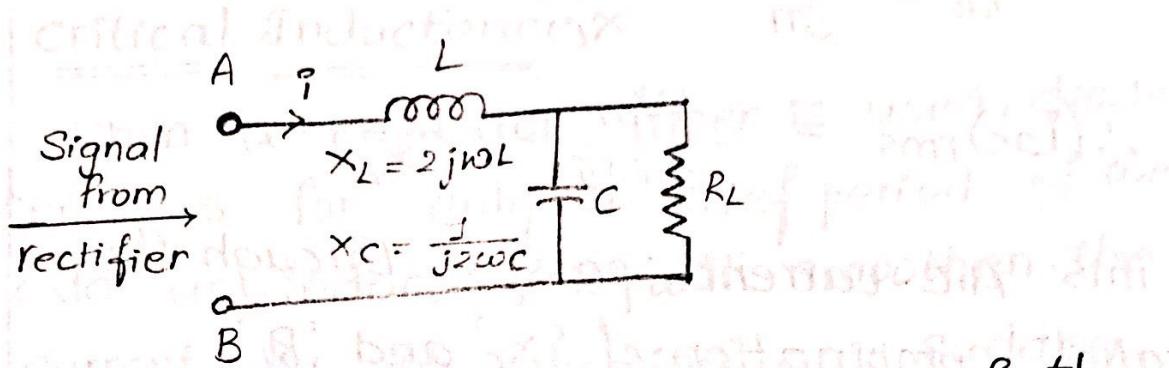
In case of capacitor filter, $\gamma \propto \frac{1}{R_L}$

In case of inductor filter, $\gamma \propto R_L$

∴ By combining an 'L' filter with 'C' filter, we can make ' γ ' independent of ' R_L '. Such a filter is known as an 'L-C filter' and is shown in the following figure.



The above circuit is a full-wave rectifier with an L-C filter. The output of the rectifier is applied to the L-C filter between the terminals A and B as shown in the following figure



The Fourier series expansion of the output current is given by

$$i = \frac{2I_m}{\pi} - \frac{4I_m}{3\pi} \cos 2\omega t - \frac{4I_m}{15\pi} \cos 4\omega t - \dots$$

Similarly, the output voltage of the rectifier is given by,

$$V_o = \frac{2V_m}{\pi} - \frac{4V_m}{3\pi} \cos 2\omega t - \frac{4V_m}{15\pi} \cos 4\omega t - \dots$$

Consider, the A.C component of the output voltage; it is given by

$$(V_{A.C})_{O.P} = \frac{4V_m}{3\pi} \cos 2\omega t$$

For better performance, ' X_L ' should be larger than the parallel combination of X_C and R_L

under these conditions, all the A.C voltage will be dropped across X_L

\therefore The a.c current is given by,

$$i_{ac} = \frac{4Vm}{3\pi} \frac{\cos 2\omega t}{X_L}$$

$$\therefore (i_{ac})_{rms} = \frac{4Vm}{3\pi\sqrt{2}} \cdot \frac{1}{X_L}$$

This A.C current passes through the parallel combination of ' X_C ' and ' R_L '.

To bypass the A.C component ' X_C ' should be smaller than ' R_L ' i.e. $X_C \ll R_L$

Then, A.C current will pass through the ' X_C '. Therefore, the output A.C, rms voltage is

$$(V_{AC})_{rms} = [i_{ac} \text{ rms}] \times X_C$$

$$\Rightarrow (V_{AC})_{rms} = \frac{4Vm}{3\pi\sqrt{2}} \cdot \frac{X_C}{X_L}$$
$$= \frac{2}{3} \left(\frac{2Vm}{\pi} \right) \frac{1}{\sqrt{2}} \frac{X_C}{X_L}$$

$$= \frac{\sqrt{2}}{3} V_{dc} \frac{X_C}{X_L}$$

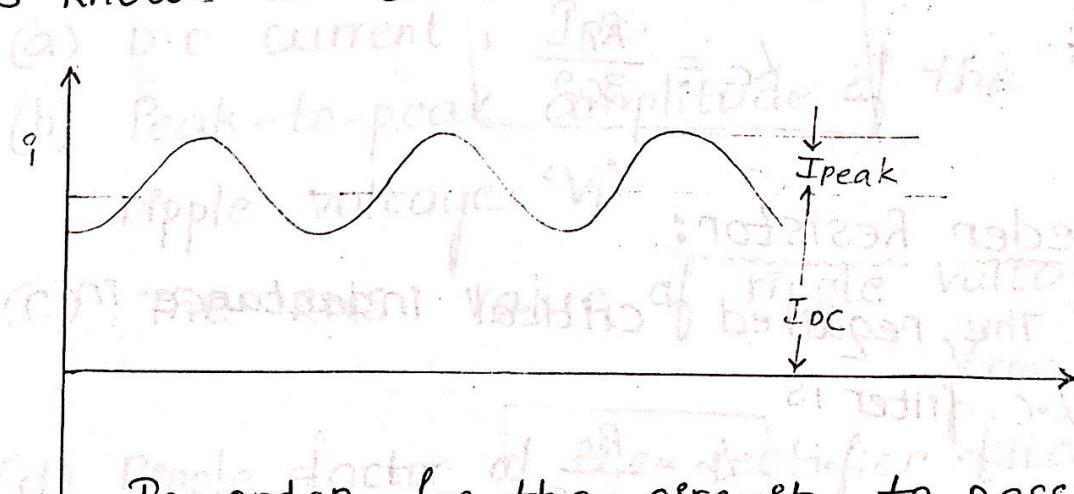
$$\therefore \text{ripple factor } \gamma = \frac{(V_{AC})_{rms}}{V_{dc}} = \frac{\sqrt{2}}{3} \frac{X_C}{X_L}$$

$$\therefore r = \frac{\sqrt{2}}{3} \left[\frac{1}{2\omega C} \right] \left[\frac{1}{2\omega L} \right]$$

\therefore By combining ' L ' and ' C ' ripple factor has become independent of ' R_L '.

Critical Inductance:

When a capacitor filter is used, diode conducts for only a brief period. If we add an inductor, it will smoothen the current by not allowing any sudden changes. As the value of inductance is increased, a value will be reached where current flows continuously in the circuit. This value of the inductance is known as critical inductance.



In order for the circuit, to pass the current continuously, the following condition must be satisfied i.e.

$$I_{DC} > I_{peak} \Rightarrow I_{DC} > \sqrt{2} i_{ac(rms)}$$

$$\Rightarrow \frac{V_{DC}}{R_L} > \sqrt{2} \cdot \frac{1}{3\pi} \cdot \frac{V_m}{X_L} \left[\frac{1}{\sqrt{2}} \right]$$

$$\Rightarrow \frac{V_{DC}}{R_L} > \frac{1}{3} \cdot \frac{1}{X_L} \cdot 2 \left[\frac{2V_m}{\pi} \right]$$

$$\Rightarrow \frac{V_{DC}}{R_L} > \frac{1}{3X_L} \cdot 2 V_{DC}$$

$$\Rightarrow \frac{1}{R_L} > \frac{2}{3X_L}$$

$$\Rightarrow \left| \frac{1}{R_L} \right| > \left| \frac{\omega L}{3\pi wL} \right| \Rightarrow \left| \frac{1}{R_L} \right| > \frac{1}{3wL}$$

The minimum value of the required inductance is given by ' L_C '

$$L_C = \frac{R_L}{3w}$$

*Bleeder Resistor:

The required critical inductance in a $L-C$ filter is

$$L_C = \frac{R_L}{3w}$$

under, no load conditions, $R_L = \infty$
 $\Rightarrow L_C = \infty$

In order to reduce the inductance, under no-load conditions, a small

resistance is connected across the output terminals of the (rectifier) filter. This resistance is called "Bleeder resistance".

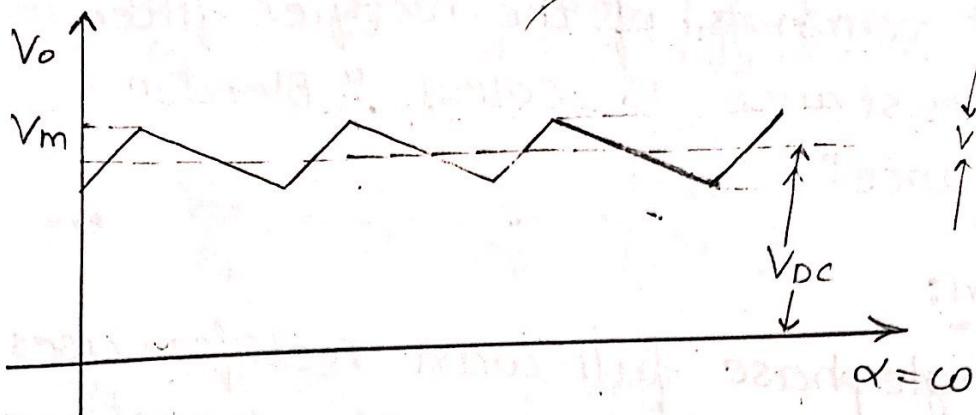
Problem:

* A single phase full-wave rectifier uses semi-conductor diodes. The transformer voltage is 35V(rms) to centre tap. The load consists of $40\mu F$ capacitor in parallel with a 250Ω resistor, the diode and transformer resistances and leakage reactance can be neglected. Assume that the power line frequency is 50Hz, calculate

- (a) D.C current, I_{DC} .
- (b) Peak-to-peak amplitude of the ripple voltage ' V_r '.
- (c) The RMS value of ripple voltage ' V_{rms} '
- (d) Ripple factor of the rectifier filter

Output

A) The Output voltage of a full wave rectifier with capacitor filter can be drawn approximately as



From the above figure, we can write,

$$V_{DC} = \frac{V_m - V_r}{2} \quad \text{--- (1)}$$

But,

$$I_{DC} = \frac{CV_r}{T} = CV_r 2f$$

$$\Rightarrow V_r = \frac{I_{DC}}{2fC} \quad \text{--- (2)}$$

Sub (2) in (1),

$$\Rightarrow V_{DC} = V_m - \frac{I_{DC}}{4fC}$$

$$\Rightarrow I_{DC} R_L = V_m - \frac{I_{DC}}{4fC}$$

$$\Rightarrow I_{DC} = \frac{V_m}{R_L + \frac{1}{4fC}}$$

Given that,

$$(V_s)_{rms} = 35V$$

now,

$$V_m = \sqrt{2} [(V_s)_{rms}]$$

$$\Rightarrow V_m = \sqrt{2}(35) = 49.5V.$$

Given,

$$R_L = 250\Omega$$

$$C = 40\mu F$$

$$f = 50Hz$$

$$(a) \Rightarrow I_{DC} = \frac{49.5}{250 + \frac{1}{4(50)(40)10^6}}$$

$$\Rightarrow I_{DC} = \frac{49.5}{250 + 125}$$

$$\Rightarrow I_{DC} = \frac{49.5}{375}$$

$$\Rightarrow I_{DC} = 0.132A$$

$$(b) V_r = \frac{I_{DC}}{2fC}$$

$$\Rightarrow V_r = \frac{0.132}{2(50)(40)10^{-6}}$$

$$\Rightarrow V_r = 33V.$$

(c)

$$V_{rms}' = \frac{V_r}{2\sqrt{3}}$$

RMS value of ripple voltage

$$\Rightarrow V_{rms}' = \frac{33}{2\sqrt{3}} = 9.52 V.$$

(d) The ripple factor

$$\gamma = \frac{1}{4\sqrt{3} f R L C}$$

$$\Rightarrow \gamma = \frac{1}{4\sqrt{3}(50) 40 \times 10^{-6}(250)}$$

$$\Rightarrow \gamma = 0.28$$

- * An λ -section filter is used in the output of a full-wave rectifier i.e fed from a 40-0-40 transform. The load current is 0.2 A. The filter consists of a 40 μF capacitor and a 2-Henry choke @ Determine, the [fr = 50 Hz] critical inductance (b) calculate 100 Hz ripple voltage [when the filter consists of the same elements].

A) Given that,

$$(V_s)_{rms} = 40 V.$$

$$\Rightarrow V_m = \sqrt{2}(40) = 56.56 \text{ V.}$$

Load current is I_{DC}

\therefore DC current flows through load

$$\therefore I_{DC} = 0.2 \text{ A.}$$

$$V_{DC} = \frac{2V_m}{\pi} = \frac{2(56.56)}{\pi}$$

$$\Rightarrow V_{DC} = 36 \text{ V.}$$

$$\text{now; } R_L = \frac{V_{DC}}{I_{DC}} = \frac{36}{0.2} = 180 \Omega.$$

now

$$L_C = \frac{R_L}{3\omega} = \frac{180}{3(2\pi f)}$$

$$\therefore L_C = \frac{60}{2\pi(50)} = \frac{30}{\pi(50)}$$

$$\Rightarrow L_C = 0.19 \text{ H.}$$

(b) We have to find $(V_{AC})_{rms}$

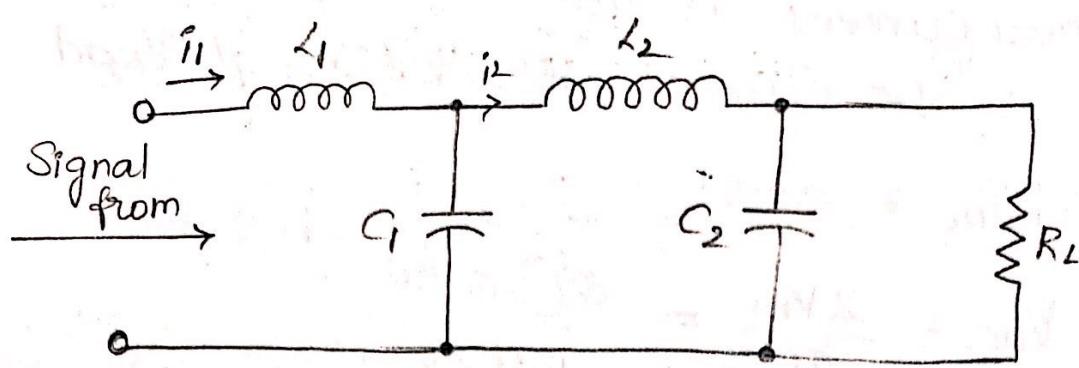
$$(V_{AC})_{rms} = \frac{\sqrt{2}}{3} (V_{DC}) \left(\frac{X_C}{X_L} \right)$$

in an L.C filter,

$$\therefore (V_{AC})_{rms} = \frac{\sqrt{2}}{3} (36) \left[\frac{1}{(2\omega C)(2\omega L)} \right]$$

$$= 0.134 \text{ V.}$$

* Multiple L-C Section filters:



The above figure shows a two stage L-C Filter. Between the terminals A and B, the Voltage is coming from the rectifier and is given by

$$V_o = \frac{2V_m}{\pi} - \left[\frac{4V_m}{3\pi} \cos 2\omega t \right]$$

[Higher Harmonics are neglected]

The a.c component is given by,

$$V_{a.c.} = \frac{4V_m}{3\pi} \cos 2\omega t$$

If X_{L1} is large, the A.C current through L_1 is given by,

$$I_{a.c.} = \frac{4V_m}{3\pi} \frac{\cos 2\omega t}{X_L}$$

This current passes through the capacitor C_1 , developing an A.C voltage

$$V_{a.c.} = \frac{4V_m}{3\pi} \frac{\cos 2\omega t}{X_L} \cdot X_C$$

The RMS value of the above voltage

∴ $V_{AC_2 \text{ rms}} = \frac{4V_m}{3\pi} \cdot \frac{X_C}{X_L} \left(\frac{1}{\sqrt{2}} \right)$

$$\Rightarrow V_{AC_2 \text{ rms}} = \frac{\sqrt{2}}{3} V_m \left(\frac{X_C}{X_L} \right)$$

If X_{L_2} is large, then, A.C current through L_2 is given by $\frac{\sqrt{2}}{3} V_{DC} \frac{X_{C_1}}{X_{L_1}} \frac{X_{C_2}}{X_{L_2}}$ (rms)

This A.C current passes through C_2 ,

∴ The A.C voltage across C_2 is,

$$V_{AC_2 \text{ rms}} = \frac{\sqrt{2}}{3} V_{DC} \frac{X_{C_1}}{X_{L_1}} \frac{X_{C_2}}{X_{L_2}}$$

∴ The ripple factor,

$$\circ \quad \gamma = \frac{\sqrt{2}}{3} \frac{X_{C_1}}{X_{L_1}} \frac{X_{C_2}}{X_{L_2}}$$

For an 'n' stage L-C filter,
with $C_1 = C_2 = C_3 = \dots = C_n$ and

$$L_1 = L_2 = \dots = L_n$$

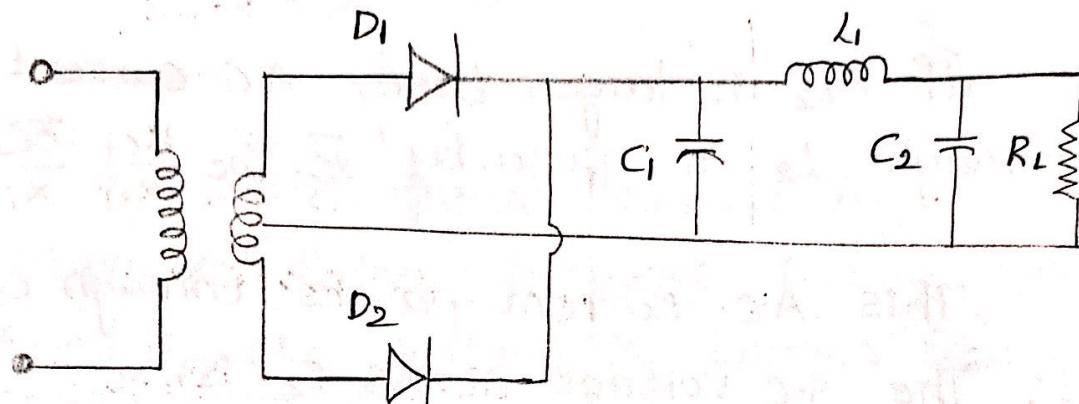
$$\boxed{\gamma = \frac{\sqrt{2}}{3} \left(\frac{X_C}{X_L} \right)^n}$$

This A.C current will pass through the capacitors and will be given by

The delivered power is given by $V_{AC} \cdot I \cdot \text{Sin}^2(\omega t) \cdot Z_{eq}$

II- Section Filter:

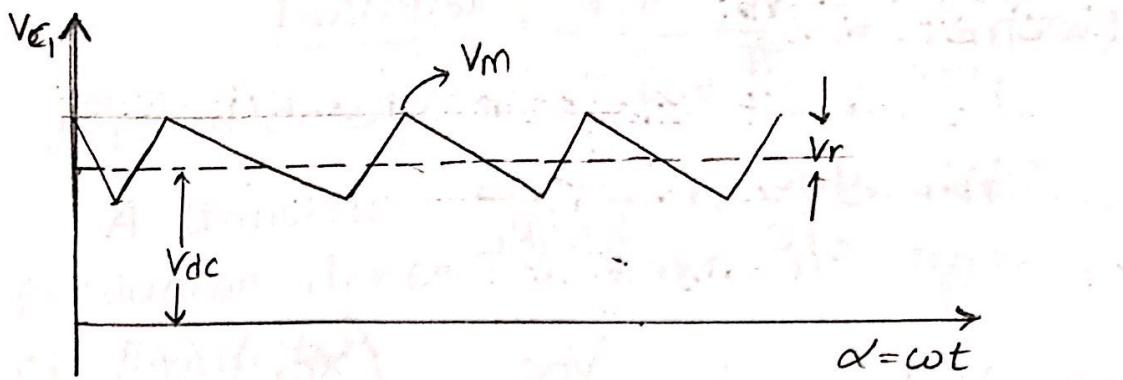
The circuit diagram of a full-wave rectifier using a C-L-C filter is as shown in the following figure



A very smooth output can be obtained by using a filter that consists of two capacitors, separated by an inductor.

This filter is known as a "II section filter".

The behaviour of the circuit can be best understood by assuming the inductor and the 2nd capacitor as an L-Section filter that is acting on the Output of the first capacitor filter is approximately a sine wave



The above wave-form acts as an input to the L-C filter. The Fourier Series expansion of this waveform gives

$$V_{C1} = \frac{2Vm}{\pi} - \frac{Vr}{\pi} \left[\frac{\sin 2\omega t - \frac{\sin 4\omega t}{2}}{2} + \frac{\sin 6\omega t}{3} - \dots \right]$$

(neglecting the higher harmonic components)

$$V_{C1} = \frac{2Vm}{\pi} - \frac{Vr}{\pi} \sin 2\omega t$$

$$\text{The a.c component} = \frac{Vr}{\pi} \sin 2\omega t$$

If L_1 is large, this voltage drops across L_1 .

\therefore The A.C current through L_1 is

$$\frac{Vr}{\pi} \frac{\sin 2\omega t}{X_{L1}}$$

This A.C current will pass through the capacitor C_{21} , if $X_{C2} < R_L$

\therefore The A.C Voltage across C_2 is given by

$$V_{a.c} = \frac{Vr}{\pi} \sin 2\omega t \left(\frac{1}{X_{L1}} \right) X_{C2}$$

$$(V_{ac})_{rms} = \frac{V_r}{\pi} \frac{x_{C_2}}{x_{L_1}} \left(\frac{1}{\sqrt{2}} \right)$$

$$V_r = \frac{I_{dc}}{2fC} = \frac{V_{DC}}{2fC_1 R_L}$$

$$\Rightarrow (V_{ac})_{rms} = \frac{V_{DC}}{\pi 2 f C_1 R_L} \left(\frac{x_{C_2}}{x_{L_1}} \right) \left(\frac{1}{\sqrt{2}} \right)$$

$$\Rightarrow r = \frac{1}{2\pi f C_1} \cdot \frac{1}{R_L} \frac{x_{C_2}}{x_{L_1}} \left(\frac{1}{\sqrt{2}} \right)$$

$$\Rightarrow r = \frac{1}{\sqrt{2} \omega C_1} \frac{1}{R_L} \left[\frac{x_{C_2}}{x_{L_1}} \right]$$

$$\Rightarrow r = \frac{\sqrt{2}}{2\omega C_1} \frac{1}{R_L} \frac{x_{C_2}}{x_{L_1}}$$

$$\Rightarrow r = \boxed{\sqrt{2} \frac{x_{C_1}}{R_L} \frac{x_{C_2}}{x_{L_1}}}$$

wed

TRANSISTORS:

physical description of the Transistor:

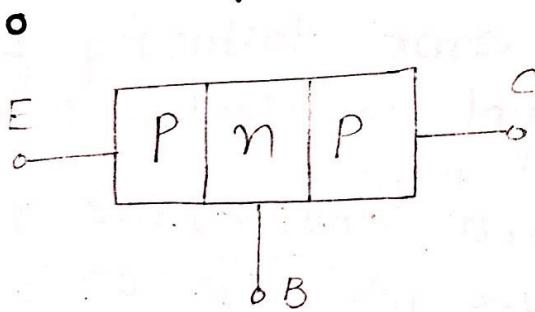
A transistor is a 3-terminal Semiconductor device we have two types of Transistors

1) P-n-p transistor

2) n-p-n transistor

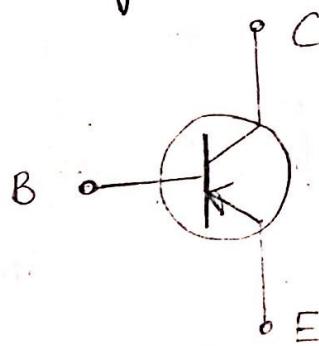
P-n-P transistor:

It consists of an n-type silicon layer sandwiched between two p-type Silicon layers.



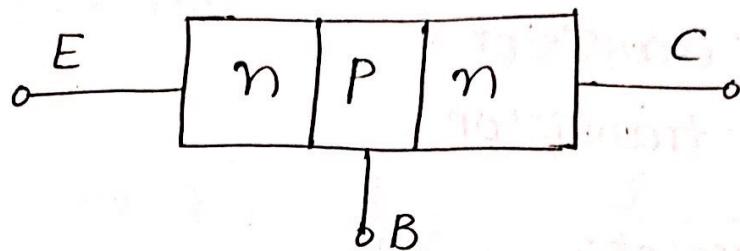
The transistor has 3-portions called Emitter, Base and Collector

circuit Symbol of P-n-P transistor:

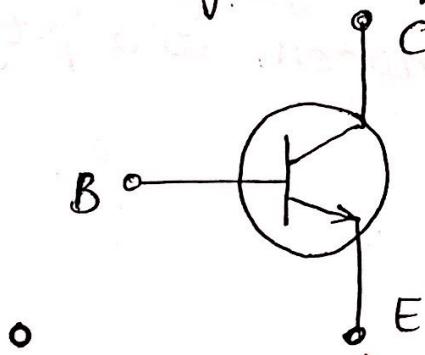


2) n-p-n transistor:

An, n-p-n transistor consists of a P-type silicon layer sandwiched between two n-type silicon layers.



Circuit Symbol of n-p-n transistor



In the above two symbols, the arrowhead indicates the direction of the conventional flow of the current (Opposite to the flow of electrons) when emitter junction is forward biased.

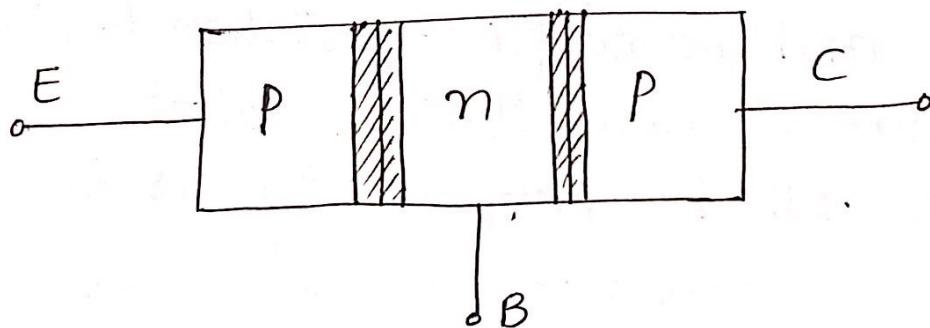
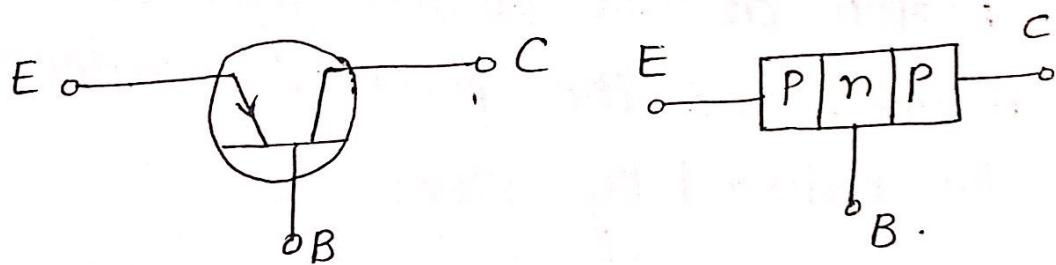
The base region of the transistor is very lightly doped and the physical area of the base is also small.

The emitter region is very heavily doped. The physical dimension of the collector region is highest of the three.

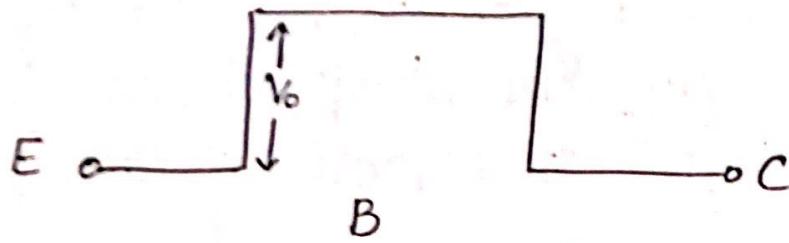
Open-circuited transistor: transistor:

When a transistor is open-circuited, there exists two p-n junctions, the emitter base p-n junction is called the "emitter junction" represented by ' J_e ' and the collector base p-n junction is called the "collector junction" represented by ' J_c '

There exists a contact difference of potential across the two junctions and a depletion layer exists at the two junctions. Consider, an open circuited P-n-p transistor

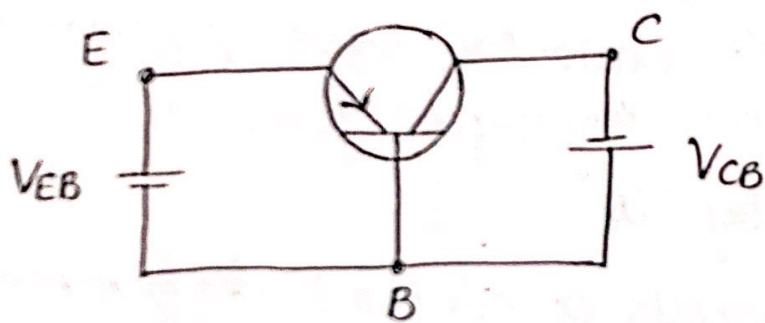


Depletion region at the two junctions.



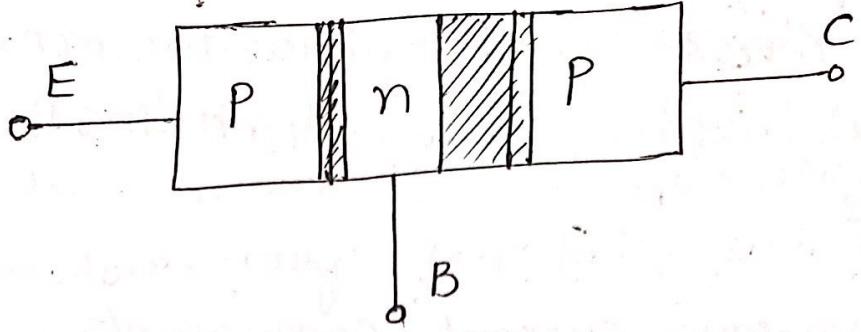
contact potential Barrier at the two junctions

Consider the following diagram,

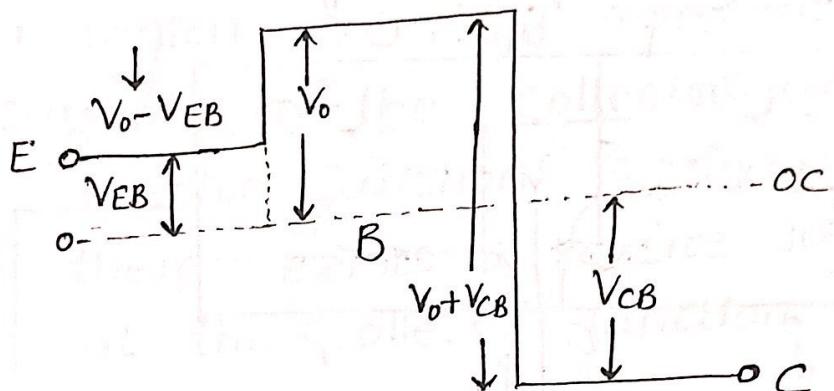


In this figure, the emitter junction is forward biased and the collector junction is reverse biased. The depletion region at the emitter junction will be reduced and the potential barrier will be reduced by $|V_{EB}|$

The collector junction is reverse biased and hence the depletion region will increase and the potential barrier will be increased by $|V_{CB}|$



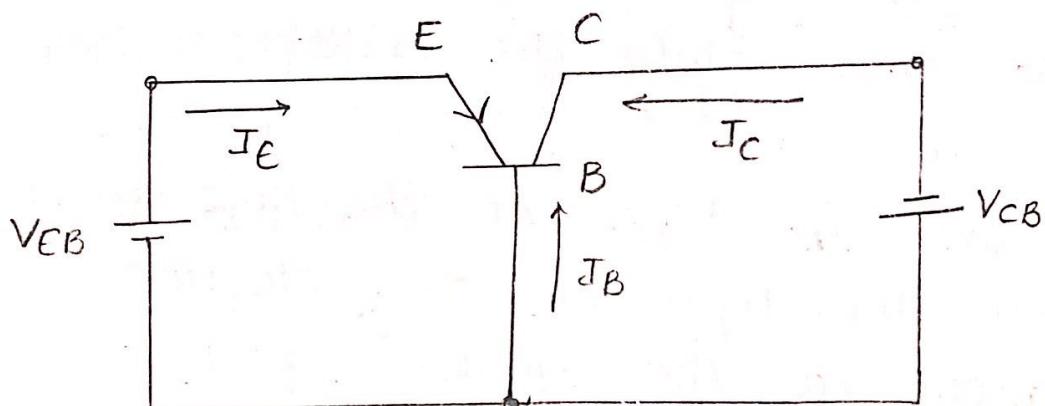
Depletion region at the two junctions



contact potential Barrier at the two junctions

29/9/11
Thursday

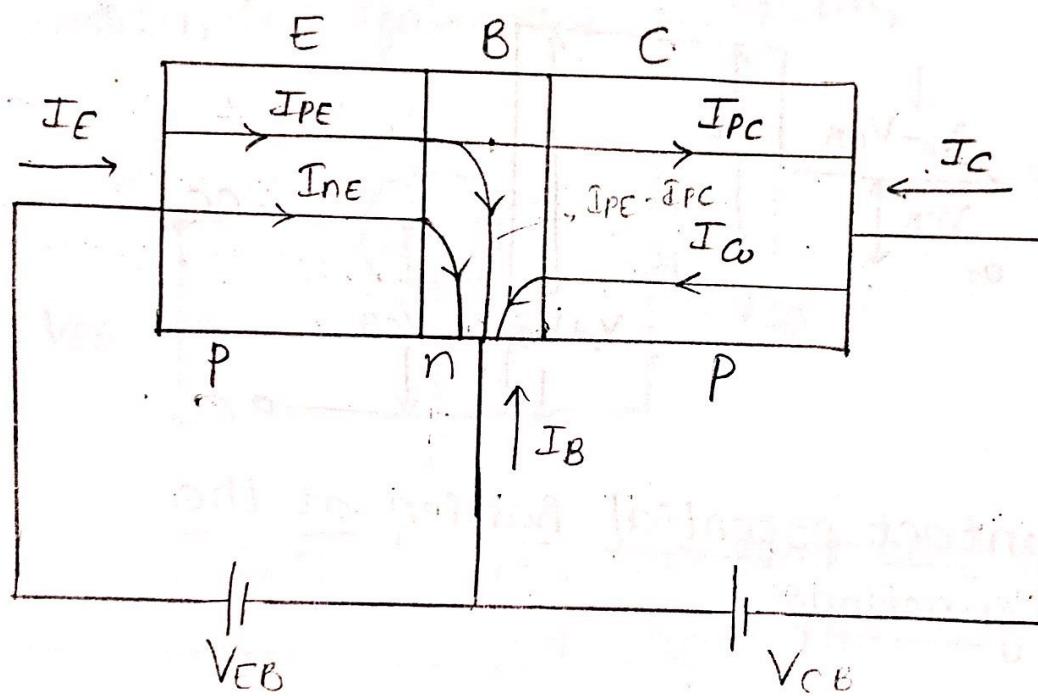
* CURRENT COMPONENTS IN A TRANSISTOR:



The above figure represents a common base transistor with emitter

junction forward biased and collector junction reverse biased". The directions of various currents are shown in the figure

The various current components are indicated in the following figure



Since, Emitter junction is forward Biased, holes from emitter enter into the base region and electrons from the Base enter into the emitter region.

Let I_{PE} represent the hole current and I_{nE} represent the electron current at the emitter region

$$\text{The emitter current, } I_E = I_{PE} + I_{nE}$$

Some holes will be lost in the base region due to recombination. Since, the width of the base region is very small, there is less chance for recombination. Therefore, only few holes will be lost in the base.

The remaining holes will enter the collector region. Let, ' I_{pc} ' represent the hole current at the collector junction. Since, collector junction is reverse biased, there exists a reverse saturation current at the collector junction.

The total collector current is therefore given by,

$$I_c = -I_{pc} + I_{co} \quad \text{--- } ①$$

Emitter Efficiency (γ):

It is defined as the ratio of the current injected by the emitter at the emitter junction to the total emitter current.

$$\gamma = \frac{I_{pe}}{I_e}$$

Transport Factor (β^*)

It is defined as the ratio of injected carrier current, reaching the collector junction to the injected carrier current at the emitter junction.

$$\boxed{\beta^* = \frac{I_{PC}}{I_{PE}}}$$

Large Signal current gain (α):

It is defined as the ratio of injected carrier current at the collector junction to the total emitter current

$$\boxed{\alpha = \frac{I_{PC}}{I_E}}$$

The ratio is always ' < 1 '
But it is almost
Equal to one

$$\Rightarrow \alpha = \frac{I_{PC}}{I_{PE}} \cdot \frac{I_{PE}}{I_E}$$

$$\Rightarrow \alpha = \beta^* r_i$$

We know that,

$$I_C = -I_{PC} + I_{CO}$$

from Equation ①

$$\Rightarrow I_C = -\alpha I_E + I_{CO}$$

$$\therefore \alpha = \frac{I_c - I_{co}}{I_E}$$

$$\Rightarrow \alpha = - \left[\frac{I_c - I_{co}}{I_E - 0} \right]$$

' α ' is the ratio of incremental collector current to the incremental emitter current

Hence, ' α ' is called as "large signal current gain" [here, large signal means DC Signal]

Consider, the equation

$$I_c = -\alpha I_E + I_{co}$$

Here, I_{co} represents the reverse saturation current at the collector junction.

The general equation for the collector current for any bias is

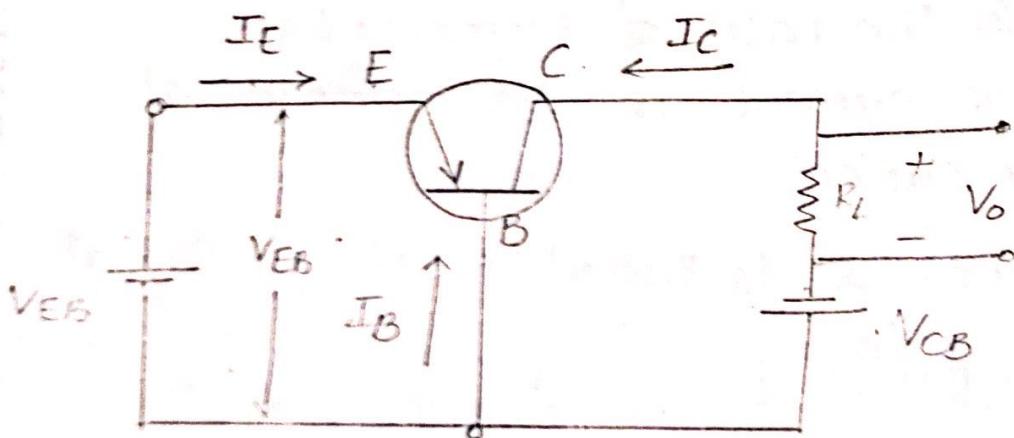
$$I_{co} [1 - e^{\frac{V_{CB}}{nV_T}}]$$

$$\therefore I_c = -\alpha I_E + I_{co} [1 - e^{\frac{V_{CB}}{nV_T}}]$$

This Equation is called "Transistor current Equation".

The large signal current gain ' α ' is always less than 1 but close to one.

* Transistor as an amplifier:



In this circuit diagram, a load resistance ' R_L ' is connected in series to the collector terminal. The transistor is connected in common base configuration. The emitter junction is forward biased and the collector junction is reverse biased.

- The various (input & output) voltages and currents are as shown in the figure

Assume, there is a small change in the input voltage ΔV_{EB} . Corresponding to this change, the emitter current

changes by ΔI_E , the change in the collector current will be

$$\Delta I_C = -\alpha \Delta I_E$$

\therefore The change in the output voltage

is $\Delta V_o = -\Delta I_C [R_L]$

$$\implies \Delta V_o = R_L (\alpha \Delta I_E)$$

$$\Delta V_{EB} = r_e [\Delta I_E]$$

Where, r_e - Diode forward resistance at the emitter junction

[Here, Emitter-Base part can be considered as a diode]

$$\frac{\Delta V_o}{\Delta V_{EB}} = \frac{R_L (\alpha \Delta I_E)}{\Delta I_E r_e} = \frac{R_L \alpha}{r_e}$$

If $R_L = 10k$, $r_e = 100\Omega$ and $\alpha = 0.9$,

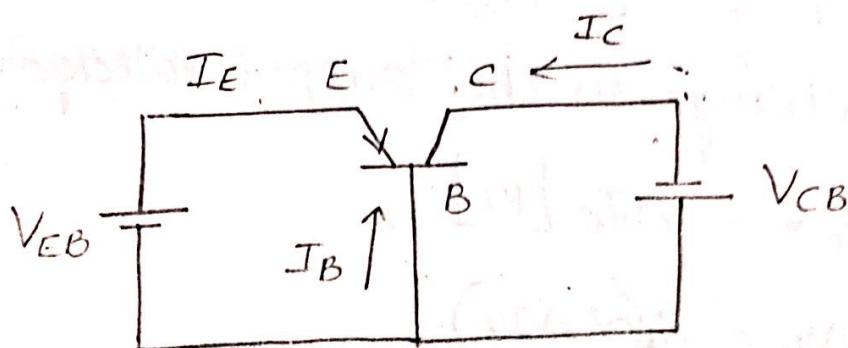
then,

$$\frac{\Delta V_o}{\Delta V_{EB}} = 90 > 1$$

Therefore, the small change at the input voltage, results in a large change at the Output.

\therefore The transistor acts as an amplifier.

Early Effect: [Base width modulation] or
[reach through] or [Punch through]

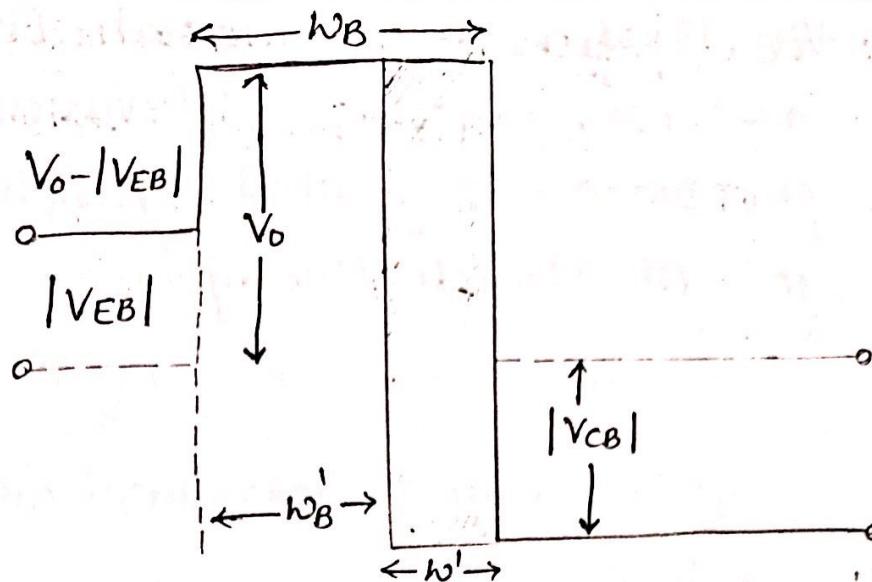


The above figure shows a P-n-P transistor with emitter junction forward bias and collector junction reverse bias.

When, a junction is reverse biased, the depletion region across that junction will increase.

The depletion region will spread more into the region where the concentration is less. Since, collector base junction is reverse biased, depletion region width will be more in the base region because the concentration in the base region is low.

The potential distribution and the depletion region is as shown in the following figure.



As shown in the above figure, the effective width of the base decreases when, V_{CB} increases. This effect is known as "Base-width modulation" or "Early effect".

This has three consequences,

- 1) Since, the effective base width is decreased, there is less chance for recombination. Therefore, the fraction of emitter-current reaching the collector $\left[\alpha = \frac{I_C}{I_E} \right]$ increases and the base current decreases.
- 2) The concentration gradient at the emitter junction $\left[\frac{dp}{dx} \right]$ will increase. Therefore, the emitter current will increase $\therefore J = -q D_p \frac{dp}{dx}$
 $\text{If } \frac{dp}{dx} \propto \propto \Rightarrow J \propto J_E$

③ If V_{CB} is further increased, the Collector-Base junction will break-down. This phenomena is called "Punch through" or "reach through".

[\because Collector-Base junction is reverse biased, the V_{CB} will be reverse voltage so, it causes break-down]

④ Since, the recombination is less in the base, the base current " I_B " will decrease.

30/9/11 (friday)

* COMMON BASE TRANSISTOR CHARACTERISTICS:

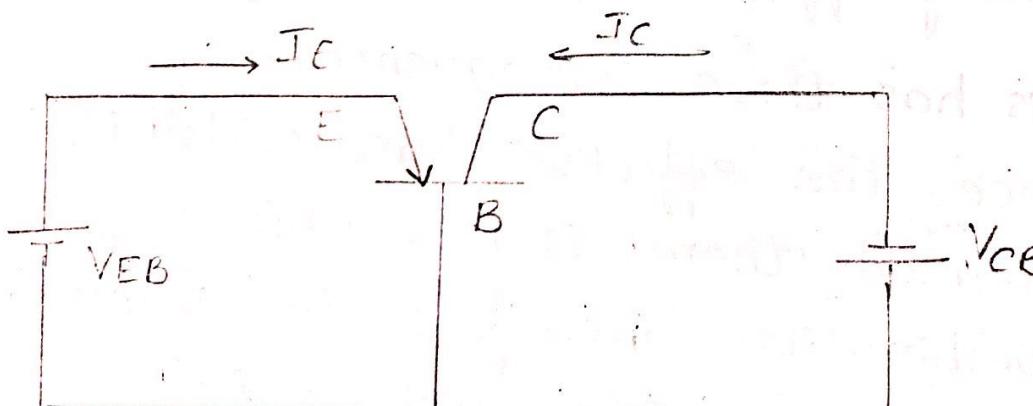


Figure shows a transistor connected in common base configuration.

I_E → Input current

I_C → Output current

V_{EB} → Input voltage

V_{CB} → Output voltage

since, the transistor is p-n-p, for the given polarities, I_E is positive, and I_C is negative. For a forward biased emitter junction, V_{EB} is positive and V_{CB} is negative.

The collector current is given by

$$I_C = -\alpha I_E + I_{C0} \left[1 - e^{\frac{V_{CB}}{nV_T}} \right]$$

The collector current is a function of Emitter current I_E and V_{CB} .

$$I_C = f_2(I_E, V_{CB}) \quad \text{--- (1)}$$

Similarly, the input voltage V_{EB} , can be represented as

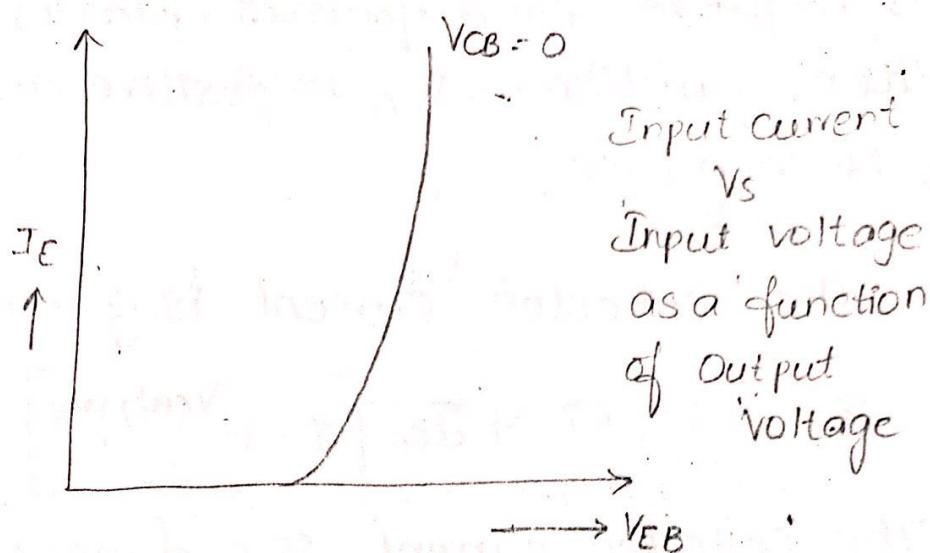
$$V_{EB} = f_1(I_E, V_{CB}) \quad \text{--- (2)}$$

The plot of Equation (2) gives the input characteristics and the plot of Equation (1) gives Output characteristics

* Input characteristics:

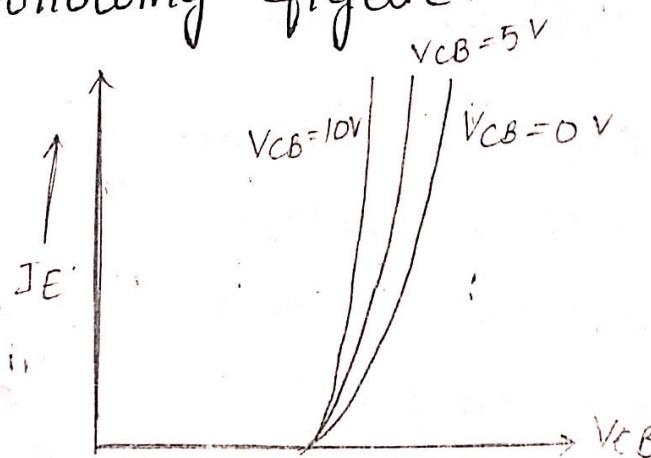
Consider the case when $V_{CB} = 0$, If V_{EB} is positive, Emitter junction will be forward biased and acts as a forward biased p-n junction diode.

The Emitter current I_E increases as per the diode current Equation



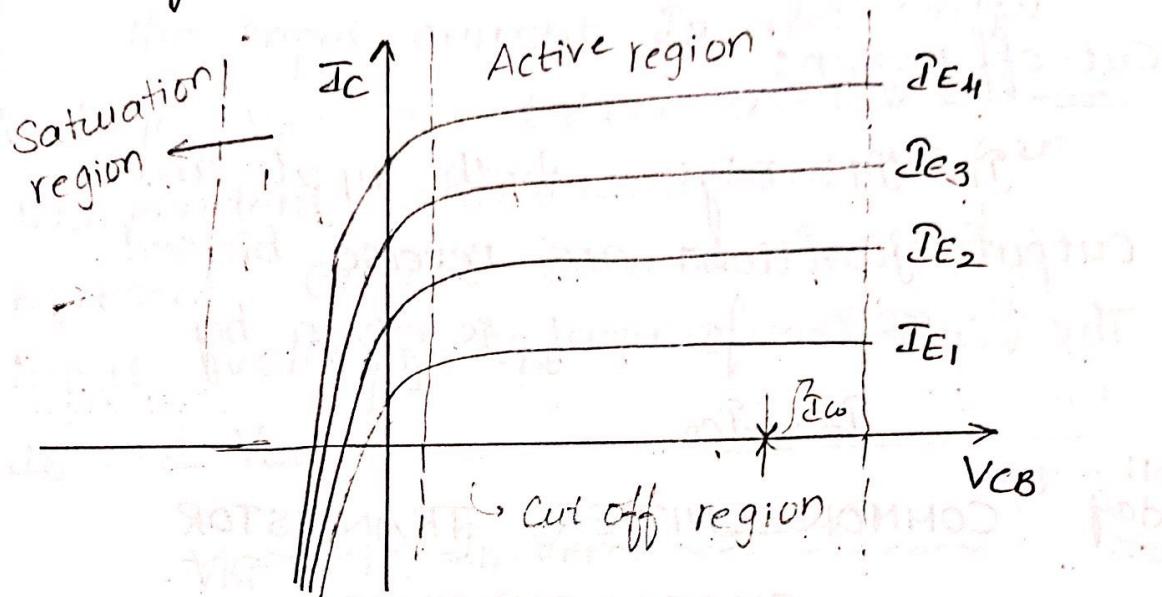
Now, if V_{CB} is applied at the collector junction in reverse bias, then base width modulation will take place i.e. the width of the base decreases and the concentration gradient $(\frac{dP}{dx})$ in the base increases. Therefore, emitter current will increase

\therefore The input characteristic curves will move inwards as shown in the following figure



* Output characteristics:

The plot of Equation ② gives the output characteristics. This function gives the plot of Output current Vs Output voltage as a function of input current



The Output characteristics are divided into three regions (i) active region (ii) saturation region (iii) cutoff region

Active region:

In this region, input junction is forward biased and output junction is reverse biased. The collector current is given by,

$$I_c \approx -\alpha I_E + I_{C0}$$

$$\Rightarrow I_c \approx -\alpha I_E \quad \left[\begin{array}{l} \text{Independent} \\ \text{of } V_{CB} \end{array} \right]$$

$$\Rightarrow I_c \approx -\alpha I_E \quad (\because \alpha < 1)$$

$$\Rightarrow I_c \approx -I_E$$

Saturation region:

In this region, both input and output junctions are forward biased.

In this region, collector current varies exponentially with 'V_{CB}'.

Cut-off region:

In this region, both input and output junctions are reverse biased.

The collector current is given by

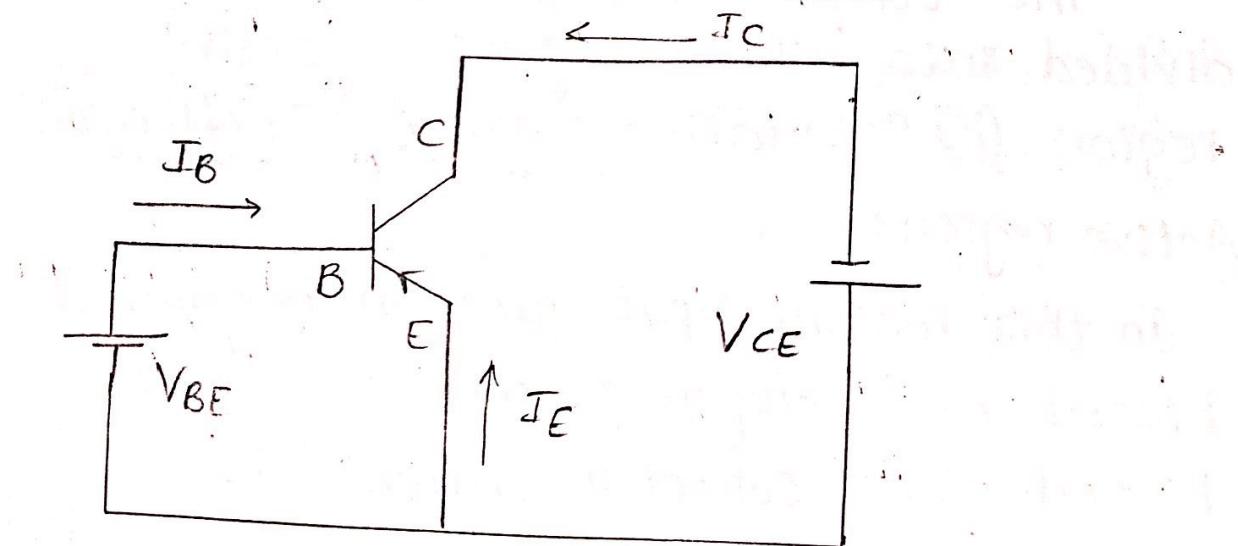
$$I_C = I_{C0}$$

1/10/2011
Saturday

8ml

COMMON-EMITTER TRANSISTOR

CHARACTERISTICS:



The above figure shows a transistor in common emitter configuration.

$I_B \rightarrow$ Input current

$I_C \rightarrow$ Output current

$V_{BE} \rightarrow$ Input voltage

$V_{CE} \rightarrow$ Output voltage

The input current I_B and output voltage V_{CE} are taken as the independent variables. Then, we can represent output current I_C and input voltage V_{BE} as functions of I_B and V_{CE} .

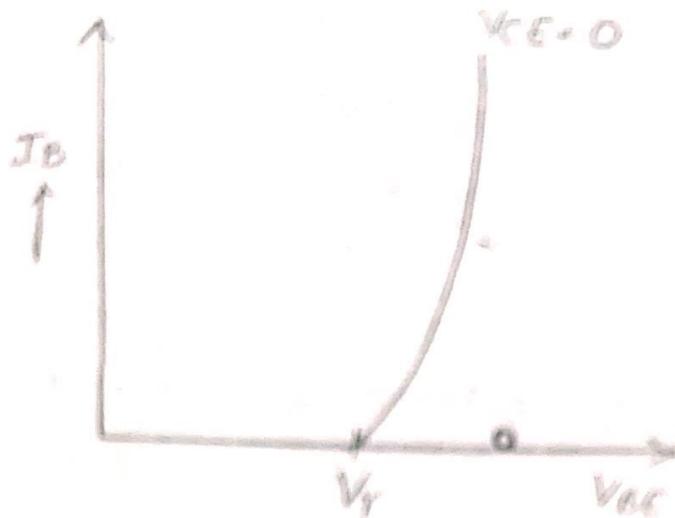
$$V_{BE} = f_1(I_B, V_{CE}) \quad \text{--- } ①$$

$$I_C = f_2(I_B, V_{CE}) \quad \text{--- } ②$$

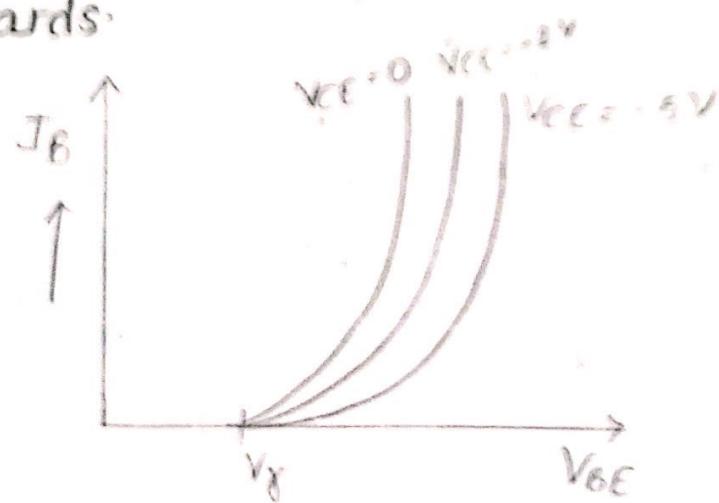
The plot of Eqn ① gives the input characteristics and the plot of Eqn ② gives the output characteristics.

Input characteristics:

Consider, $V_{CE} = 0$, and V_{BE} is increased. The input junction is a forward biased p-n-junction and hence, the current I_B increases just like in a forward biased p-n-junction diode.



If V_{CE} is increased, Base width modulation will takes place and the base current I_B will decrease. Therefore, the input curves moves outwards.



Output characteristics:

According to the given circuit,

$$I_B + I_C + I_E = 0$$

$$\Rightarrow I_C = -I_B - \delta I$$

but

$$I_C = -\alpha I_E + I_{C0}$$

$$\Rightarrow I_E = \frac{I_{Co} - I_C}{\alpha}$$

$$\Rightarrow \therefore I_C = -I_B - \frac{(I_{Co} - I_C)}{\alpha}$$

$$\alpha I_C = -\alpha I_B - I_{Co} + I_C$$

$$\Rightarrow I_C(1-\alpha) = -\alpha I_B - I_{Co}$$

$$I_C = \frac{\alpha}{1-\alpha} I_B + \frac{I_{Co}}{1-\alpha}$$

$$\text{Let } \frac{\alpha}{1-\alpha} = \beta \Rightarrow 1+\beta = \frac{1}{1-\alpha}$$

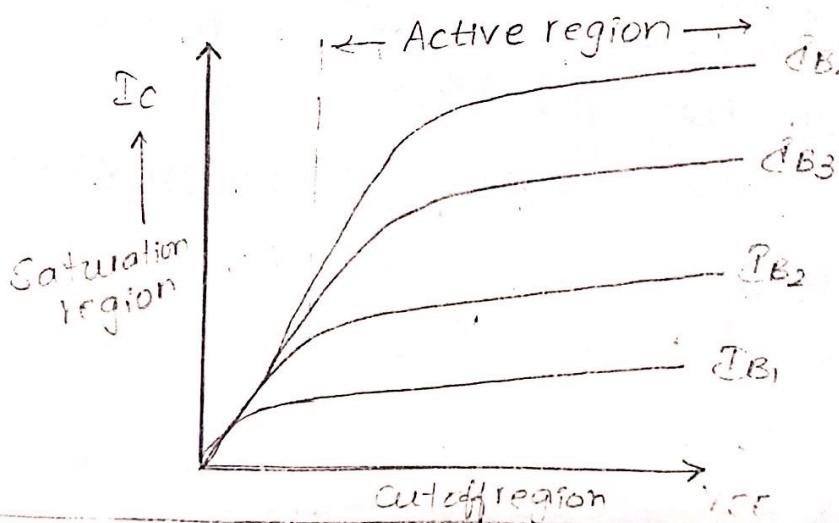
$$\therefore I_C = \beta I_B + \frac{I_{Co}}{(1+\beta)}$$

$$\Rightarrow I_C = \beta I_B + (1+\beta) I_{Co}$$

$$I_B \gg I_{Co}$$

$$\therefore I_C \approx \beta I_B$$

$\beta = \frac{I_C}{I_B}$; ' β ' is called
"DC current gain"



I_{CEO}

I_{CEO} is the collector current, when

$$I_B = 0, \quad I_C = \beta I_B + (1+\beta) I_{CO}$$

If $I_B = 0$

$$\Rightarrow I_C = (1+\beta) I_{CO} = I_{CEO}.$$

I_{CBO}

I_{CBO} is the collector current when Emitter current $I_E = 0$ and the collector junction is reverse biased.

$$I_C + I_B + I_E = 0$$

If $I_E = 0$

$$\Rightarrow I_C = -I_B = I_{CBO}$$

Theoretically, the reverse saturation current should be I_{CO} . But, practically it will be I_{CBO} .

$I_{CBO} > I_{CO}$ for two reasons,

- ① Due to leakage current across the collector junction
- ② Due to the avalanche multiplication of minority carriers at the collector junction.

Note:

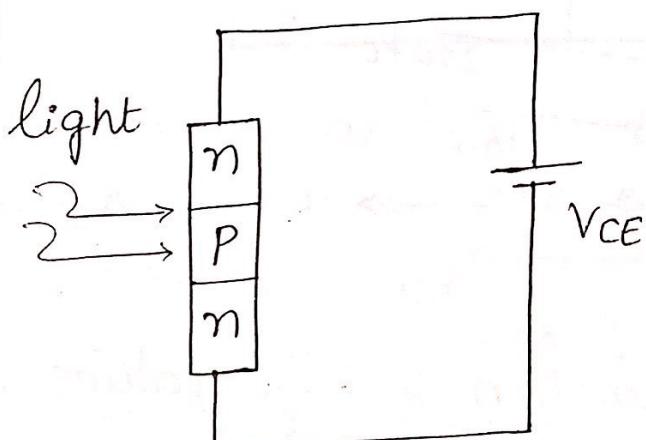
If they asked to derive Transistor current equation, derive upto.

$$I_C = \beta I_B + (1+\beta) I_{Co}$$

110111
Monday

Photo Transistor:

Photo transistor is usually connected in a common Emitter configuration with the base terminal open and the radiation is concentrated near the collector junction.



The emitter junction is forward biased and the collector junction is reverse biased. When there is no light, collector reverse saturation current is equal to I_{Co} and

$$I_C = \beta I_B + (1+\beta) I_{Co}$$

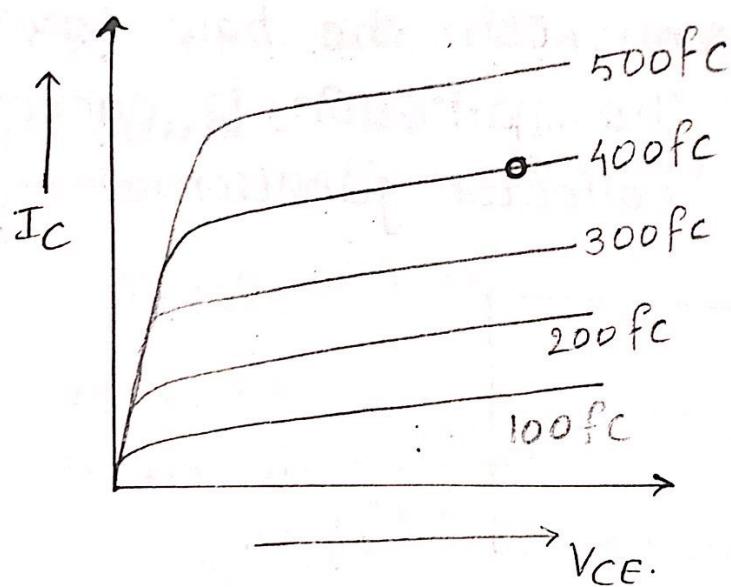
$$\text{and } I_B = 0 \implies I_C = (1+\beta) I_{Co}$$

When the light is turned on, additional minority carriers are generated at the collector junction.

Let, I_L represent the additional current due to radiation

$$\therefore I_C = (1+\beta) I_{C0} + I_L$$

* V-I characteristics of photo transistor:



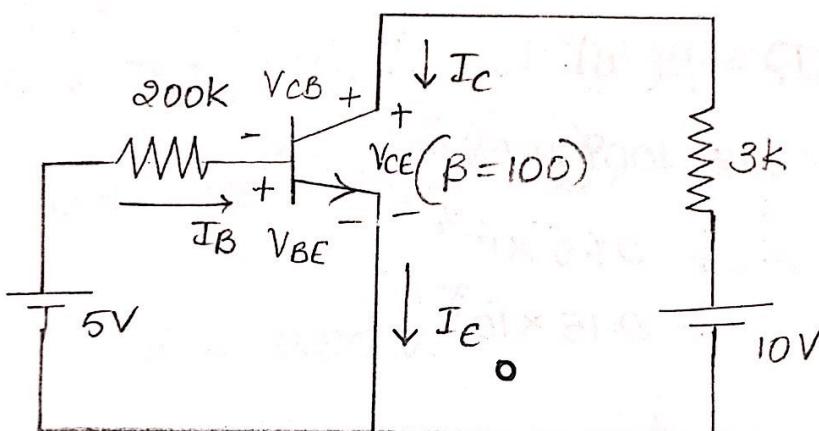
* Typical Transistor junction voltage values for an n-p-n transistor at room temperature (25°C)

	Saturation				
	V_{CE} (sat)	V_{BE} (sat)	V_{BE} (active)	V_{BE} (cut in)	V_{BE} (cutoff)
Si	0.2	0.8	0.7	0.5	0
Ge	0.1	0.3	0.2	0.1	-0.1

If transistor enters into saturation region, V_{CE} becomes constant

Problems:

- * Find transistor currents in the following circuit
- (a) Assume $\beta = 100$ and $I_{CO} = 20nA$
- (b) Repeat Part 'a' if a $2\text{kilo}\Omega$ resistor is added to the emitter terminal.



This is an n-p-n transistor, at '5V'
 (Base) P-terminal is connected to +ve and (Emitter) n-terminal is connected to -ve.

\therefore Input base-emitter junction is forward biased

\therefore It is not in cut-off region.

It should be in active or saturation region

Assume, it is in active region.

With the given polarities, we can assume that the transistor is in active region.

$$\therefore I_C = \beta I_B + (1+\beta) I_{CO}$$

neglecting I_{CO}

$$\Rightarrow I_C = \beta I_B \quad \text{--- (1)}$$

Applying KVL to the input loop,

$$-5 + (200k) I_B + V_{BE} = 0.$$

$V_{BE} = 0.7V$ for silicon.

$$I_B = \frac{5 - V_{BE}}{200k} = \frac{5 - 0.7}{200k} = 21.5 \mu A$$

$$I_C = \beta(I_B)$$

$$= 100(21.5) \times 10^{-6}$$

$$= 21.5 \times 10^{-4}$$

$$= 21.5 \times 10^{-5}$$

$$\Rightarrow I_C = 21.5 \mu A.$$

From the current directions,

I_E → leaving current

I_B, I_C → entering currents

$$\Rightarrow I_E = I_B + I_C$$

$$= 21.5 \mu A + 21.5 \mu A$$

$$\Rightarrow I_E = 43 \mu A.$$

{ The collector-base junction should
be reverse biased for the transistor
to be in active region }

{ So, we need to know the Collector-Base junction voltage }

{ I_C should be positive, ' V_B ' should be negative and totally V_{CB} should be positive Then only our assumption is correct }

Applying KVL,

$$\begin{aligned} -10 + 3KI_C + V_{CB} - 200KIB + 5 &= 0 \\ \Rightarrow -10 + 3 \times 10^3 (2.15) I_C + V_{CB} - 200 \times 10^3 \frac{2.15}{10^6} \\ &\quad + 5 = 0 \\ \Rightarrow V_{CB} &= 2.85 \text{ V.} \end{aligned}$$

$\therefore V_{CB}$ is positive and hence, the transistor is in active region.

\therefore Our assumption is correct

$$\text{and } \therefore I_B = 2.15 \mu\text{A}$$

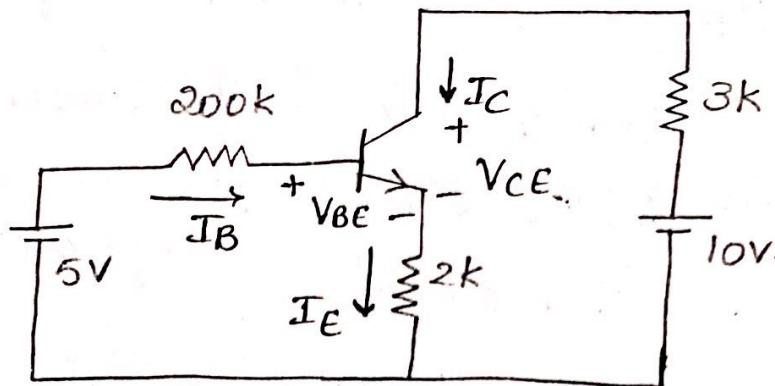
$$I_C = 2.15 \text{ mA}$$

$$I_E = 2.1715 \text{ mA.}$$

$$[I_C = -\alpha I_E]$$

Here, we didn't get '-'ve sign because we had taken reverse direction of I_E (i.e. away from the junction)

b) Now, the circuit becomes,



As given in the previous case,
Assume the transistor is in active region.

Applying KVL,

$$-5 + 200k [I_B] + V_{BE} + 2k I_E = 0.$$

$$\Rightarrow -5 + 200k (I_B) + V_{BE} + 2k [I_B + I_C] = 0.$$

$$\Rightarrow -5 + 0.7 + (202k) I_B + 2k (I_C) = 0.$$

Here, $I_C \approx \beta I_B$ [\because Active region is assumed]

$$\Rightarrow -4.3 + (202k) I_B + 2k (\beta I_B) = 0.$$

$$\Rightarrow -4.3 + (202k) I_B + 200k I_B = 0$$

$$\Rightarrow -4.3 + 402k I_B = 0$$

$$\Rightarrow I_B = \frac{4.3}{402 \times 10^3}$$

$$\Rightarrow I_B = 10.7 \mu A$$

$$I_C = \beta I_B = 10.4 \times 10^6 (100) = 1.04 \text{ mA}$$

$$\begin{aligned} I_E &= I_C + I_B \\ &= 10.4 \mu\text{A} + 1.04 \text{ mA} \\ &= 1.0804 \text{ mA} \end{aligned}$$

now, we have to check our assumption.

as it is n-p-n transistor, we should check whether V_{CB} is +ve

Applying KVL to the Output loop,

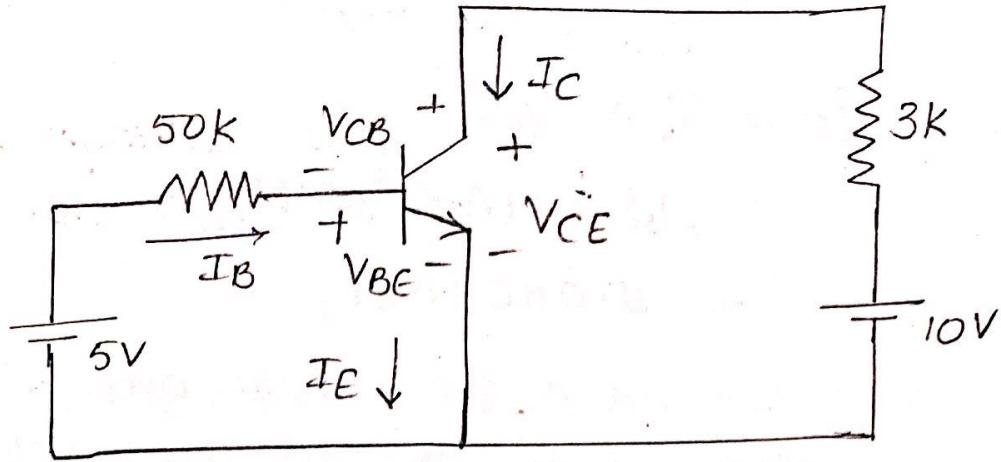
$$\begin{aligned} -10 + 3k I_C + V_{CB} - 200k I_B + 5 &= 0 \\ \Rightarrow -10 + 3k [1.04] 10^{-3} + V_{CB} - 200k (10.4) 10^{-6} \\ &\quad + 5 = 0 \\ \Rightarrow -10 + 3.21 + V_{CB} - 0.2 (10.4) + 5 &= 0 \\ \Rightarrow V_{CB} &= 3.93 \text{ V.} \end{aligned}$$

$\therefore V_{CB}$ is positive

\therefore The device is in active region

* For the following circuit (a) determine the transistor currents if $\beta = 100$ and the transistor is Silicon transistor

(b) repeat part 'a' by inserting a $2k$ resistor in series to the emitter lead.



- A) (a) Assume that the transistor is in active region. $\therefore V_{BE} = 0.7V$
 and $\therefore I_C = \beta I_B$.

Applying KVL to the input loop,

$$-5 + 50k[I_B] + V_{BE} = 0.$$

$V_{BE} = 0.7V$. for silicon

$$I_B = \frac{5 - V_{BE}}{50k} = \frac{5 - 0.7}{50k} = 86 \mu A.$$

$$I_C = \beta I_B = 86 \times 10^6 [100] = 8.6 \text{ mA}$$

$$I_E = I_B + I_C = 8.6 \text{ mA} + 86 \mu A$$

$$\Rightarrow I_E = 8.686 \text{ mA.}$$

verifying our assumption,

Applying KVL,

$$-10 + 3kI_C + V_{CB} - 50kI_B + 5 = 0.$$

$$V_{CB} = -16.5V.$$

$\therefore V_{CB}$ is negative, our assumption is wrong and the device is not in active region.

Assume, the device is in Saturation region.

$$\therefore \text{for silicon, } V_{CE} = 0.2V.$$

$$\text{and } V_{BE} = 0.8V.$$

Applying KVL to the input loop,

$$-5 + 50k(I_B) + V_{BE} = 0.$$

$$I_B = \frac{5 - 0.8}{(50k)} = 84 \mu A.$$

$$\text{here, } I_C = ?$$

we take KVL for outer loop.

$$\left\{ \begin{array}{l} \text{Saturation region or } I_C = \beta I_B \\ I_C = \beta I_B \text{ ദാരുംകുറവിൽ } V_{CE} \text{ തുല്യ} \\ \text{or active region or } I_C = \beta I_B \\ \text{തുല്യമാണ് } I_C = \beta I_B \text{ ദാരുംകുറവിൽ.} \end{array} \right\}$$

$$-10 + (3k)I_C + V_{CE} = 0$$

$$\Rightarrow I_C = \frac{10 - V_{CE}}{3k} = 3.26 \text{ mA.}$$

$$I_E = I_B + I_C = 3.34 \text{ mA}$$

$$(I_B)_{\min} = \frac{I_C}{\beta} = \frac{3.26 \text{ mA}}{100}$$

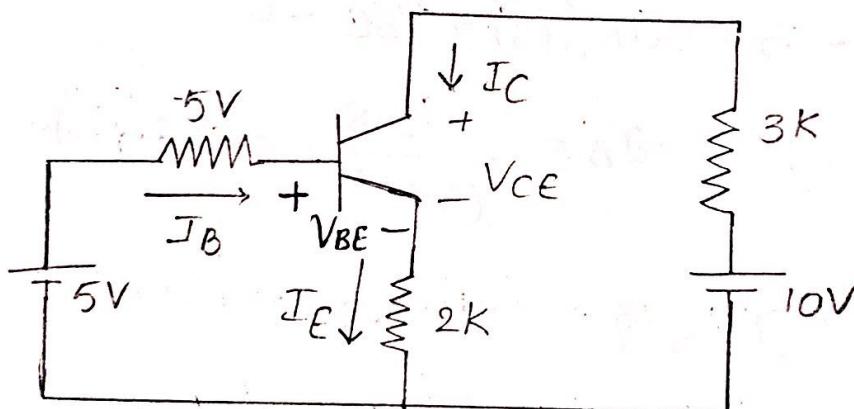
$$\Rightarrow (I_B)_{\min} = 32.6 \mu\text{A}$$

$$I_B = 84 \mu\text{A}$$

$$I_B > (I_B)_{\min}$$

\therefore Device is in Saturation region.

(b) now the circuit becomes,



assume, the transistor is in Saturation region.

$$\Rightarrow V_{CE} = 0.2 \text{ V}$$

$$V_{BE} = 0.8 \text{ V}$$

Applying KVL to input loop,

$$-5 + (50k) I_B + V_{BE} + 2k(I_B + I_C) = 0$$

$$\Rightarrow 52k I_B + 2k I_C = 4.2 \text{ mA} \quad \underline{\text{V}} \quad \textcircled{1}$$

As we cannot solve,

Applying KVL to the Output loop,

$$-10 + 3k I_C + V_{CE} + 2k(I_B + I_C) = 0$$

$$\Rightarrow 2k I_B + 5k I_C = 9.8 \text{ mA} \quad \underline{\text{V}} \quad \textcircled{2}$$

$\Rightarrow \therefore$ now solving $\textcircled{1}$ & $\textcircled{2}$ Eqn's
we get,

$$I_B = 5.46 \mu\text{A}$$

$$I_C = 1.95 \text{ mA}$$

$$(I_B)_{\min} = \frac{I_C}{\beta} = \frac{1.95 \text{ mA}}{100}$$

$$\Rightarrow (I_B)_{\min} = 19.5 \mu\text{A}$$

$$I_B < (I_B)_{\min}$$

\therefore our assumption is wrong

\therefore The device is not in Saturated region.

now assume, the device is in active region,

Applying KVL to input loop.

$$-5 + 50k(\bar{I}_B) + V_{BE} + 2k(\bar{I}_B + \bar{I}_C) = 0$$

here, $\bar{I}_C = \beta \bar{I}_B$ (\because active region)

and $\bar{I}_C = 100 \bar{I}_B$; $V_{BE} = 0.7$

$$\Rightarrow -5 + (50k) \bar{I}_B + 0.7 + 2k(101 \bar{I}_B) = 0$$

$$\Rightarrow -4.3 + 252k\bar{I}_B = 0$$

$$\Rightarrow \bar{I}_B = \frac{4.3}{252k} = 17 \mu A$$

$$\therefore \bar{I}_C = 1.706 \text{ mA}$$

$$\Rightarrow \bar{I}_E = \bar{I}_C + \bar{I}_B = 1.723 \text{ mA}$$

now, we have to find V_{CB} .

Applying KVL to Outer loop,

$$-10 + 3k\bar{I}_E + V_{CB} - 50k\bar{I}_B + 5 = 0$$

$$\Rightarrow V_{CB} = 10 - 5 + 50k\bar{I}_B - 3k\bar{I}_C$$

$$\Rightarrow V_{CB} = 5 + (50 \times 10^{-3}) - 3(1.7)$$

$$\Rightarrow V_{CB} = 0.73 \text{ mA}$$

$\therefore V_{CB}$ is +ve

\therefore Device is in active region

Our assumption is correct

14/10/11
Friday

unit-6

FIELD EFFECT TRANSISTOR [FET]

Types of FET's:

There are three major types of FET's

- (i) JFET : Junction Field Effect Transistor
- (ii) MOSFET: Metal oxide Semiconductor
Field effect transistor

There are two types of JFET's

- (i) n-channel JFET
- (ii) P-channel JFET

There are two types of MOSFET's

- (i) Enhancement MOSFET → ① n-channel MOSFET
- (ii) Depletion MOSFET. ② P-channel MOSFET

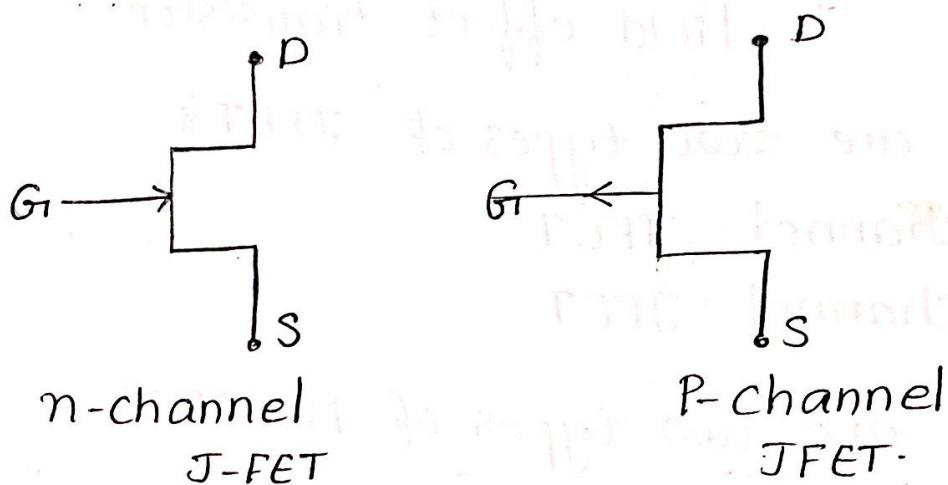
* JFET:

* Advantages of JFET over BJT
Bipolar Junction
transistor

- 1) The operation of the FET depends upon the flow of majority carriers only.
∴ FET is uni-polar device
- 2) It is simpler to fabricate and occupies less space in integrated form

- 3) It exhibits a high input resistance typically many mega ohms.
- 4) It is less noisy than BJT.
- 5) It does not exhibit offset voltage at zero drain current and hence makes an excellent signal chopper.

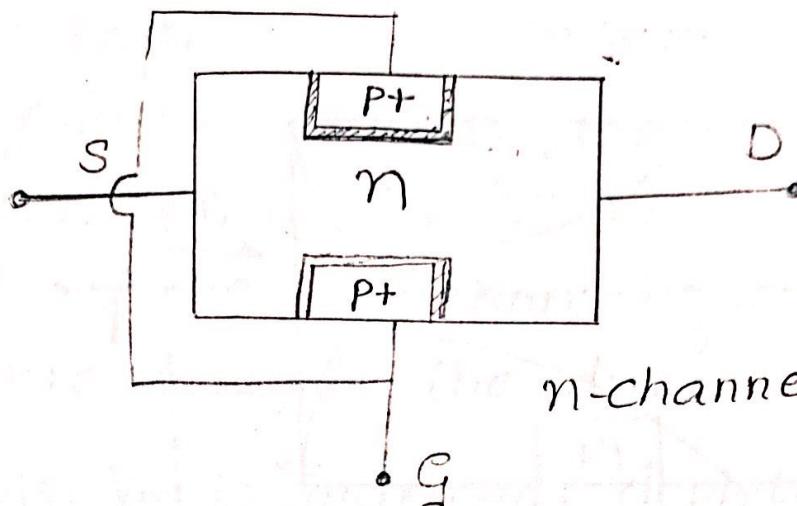
Symbol



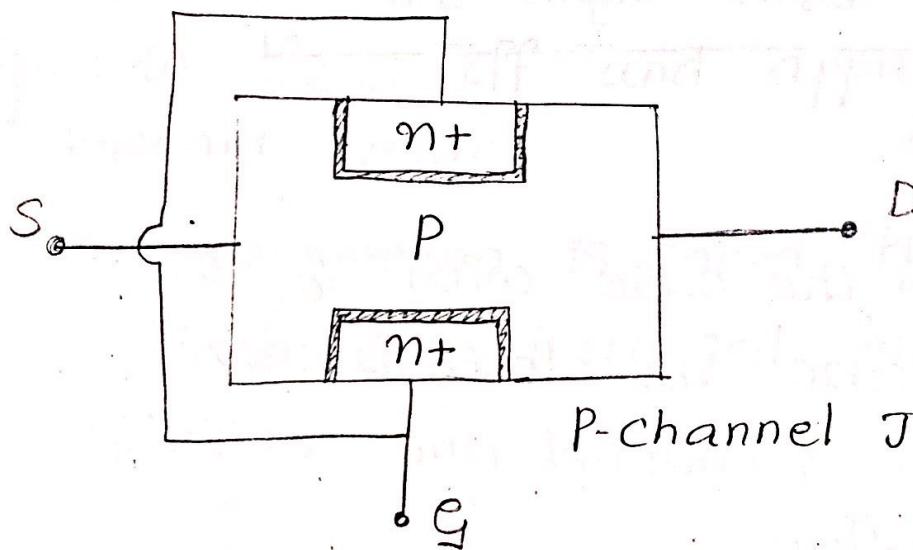
For an n-channel JFET or a p-channel JFET "Source" is the terminal through which majority carriers enter the channel. "Drain" is the terminal through which majority carriers leave the channel.

For n-channel ~~H~~^JFET heavily doped P-regions will be there on either side of the channel. These two regions are called "Gate".

For P-channel JFET heavily doped n-regions exists on either side of the channel. These regions are called "Gate"



n-channel JFET

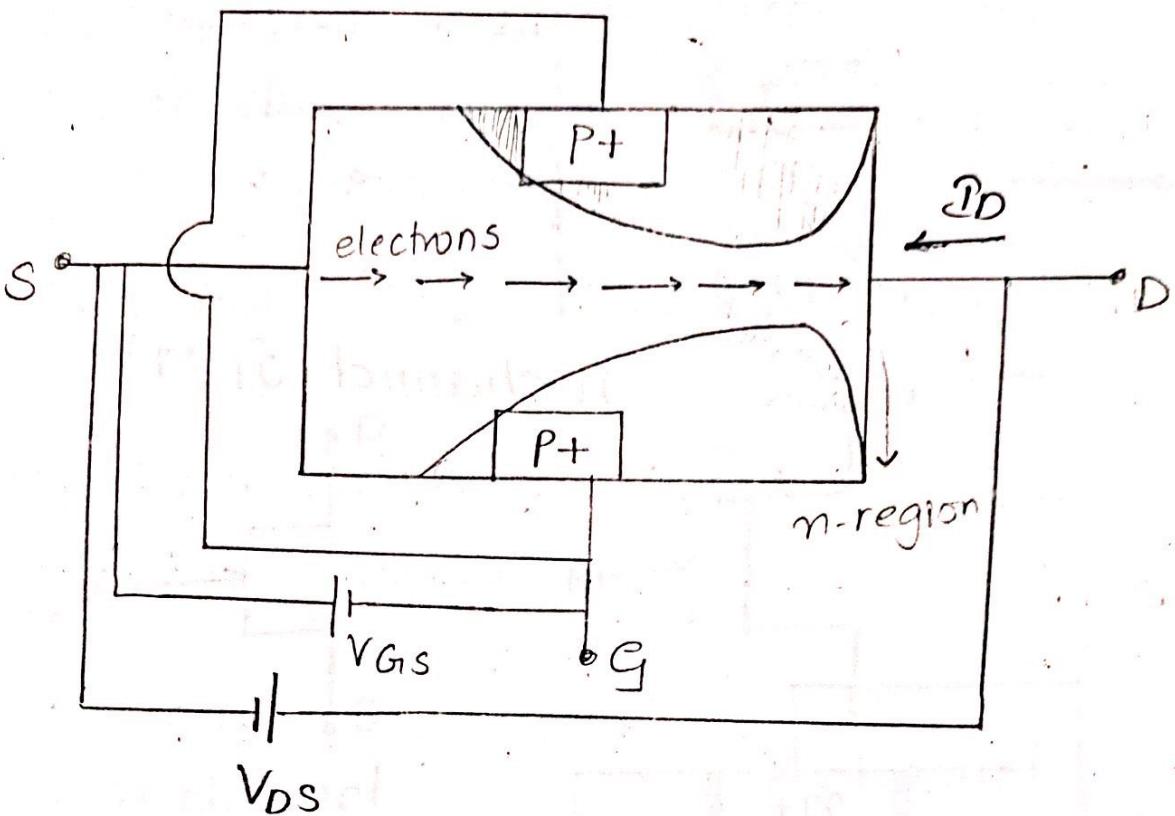


P-channel JFET:

Static characteristics = $D \cdot C = V \cdot I =$ Volt-ampere
= Input

= Drain characteristics.

* Drain characteristics:



Consider the case with $V_{GS} = 0$, if we increase V_{DS} electrons move through the n-channel and current begins to flow.

Electrons enter through the source terminal and leave through the Drain terminal.

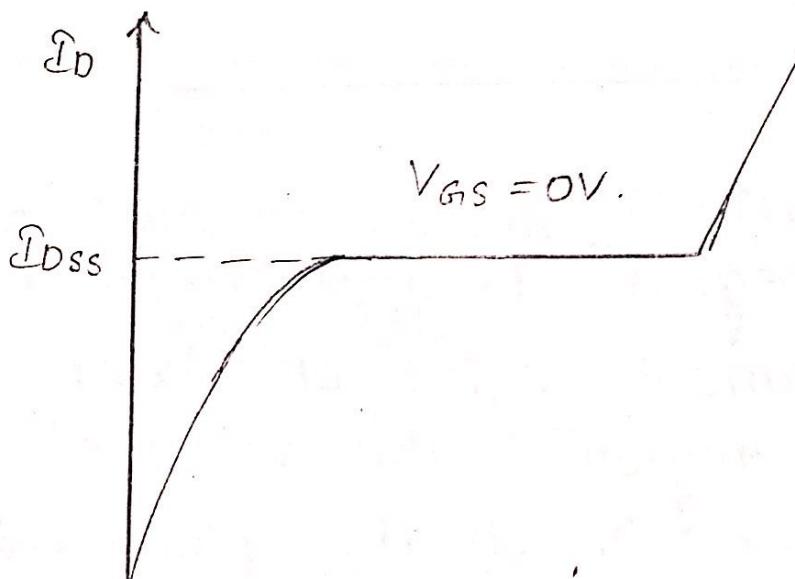
The drain current ' I_D ' is shown in the figure. If we increase V_{DS} , the current increases linearly with V_{DS} and FET acts as a simple resistor.

If V_{DS} is further increased, the ohmic voltage drop along the length of the channel will increase.

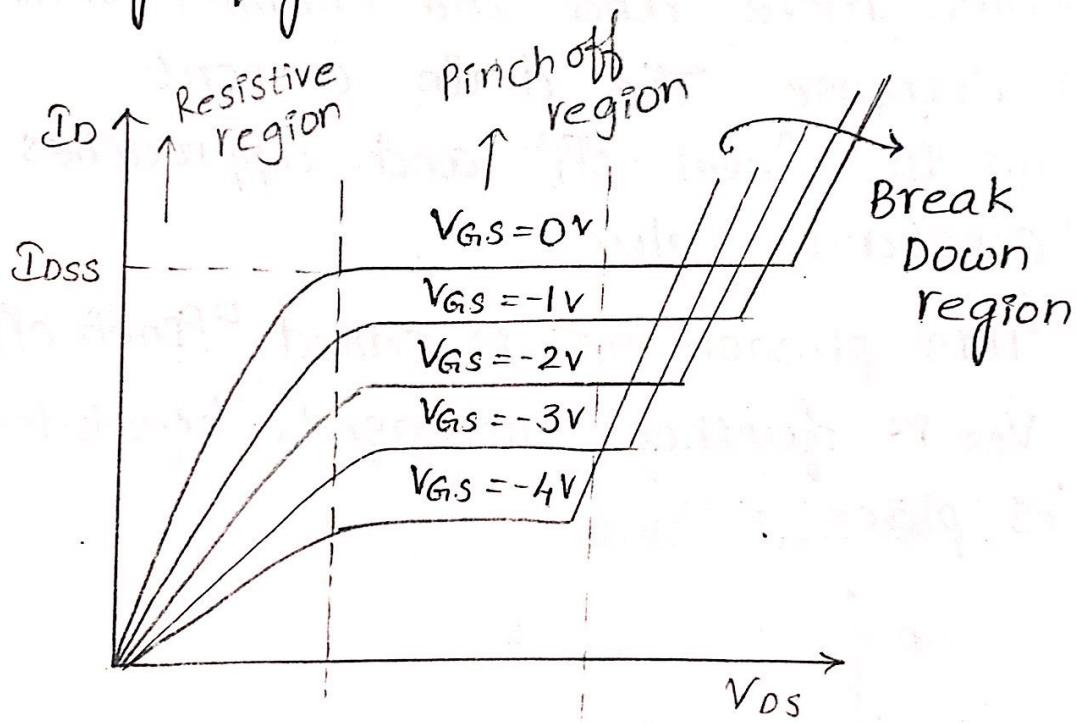
\therefore Drain Voltage is positive, the p-n junction towards the drain end is reverse biased. As a result, the width of the depletion region will be more towards the drain.

As, V_{DS} is increased, depletion region spreads more and the channel width will decrease. The drain current begins to level off and approaches a constant value.

This phenomena is called "Pinch off". If V_{DS} is further increased, breakdown takes place.



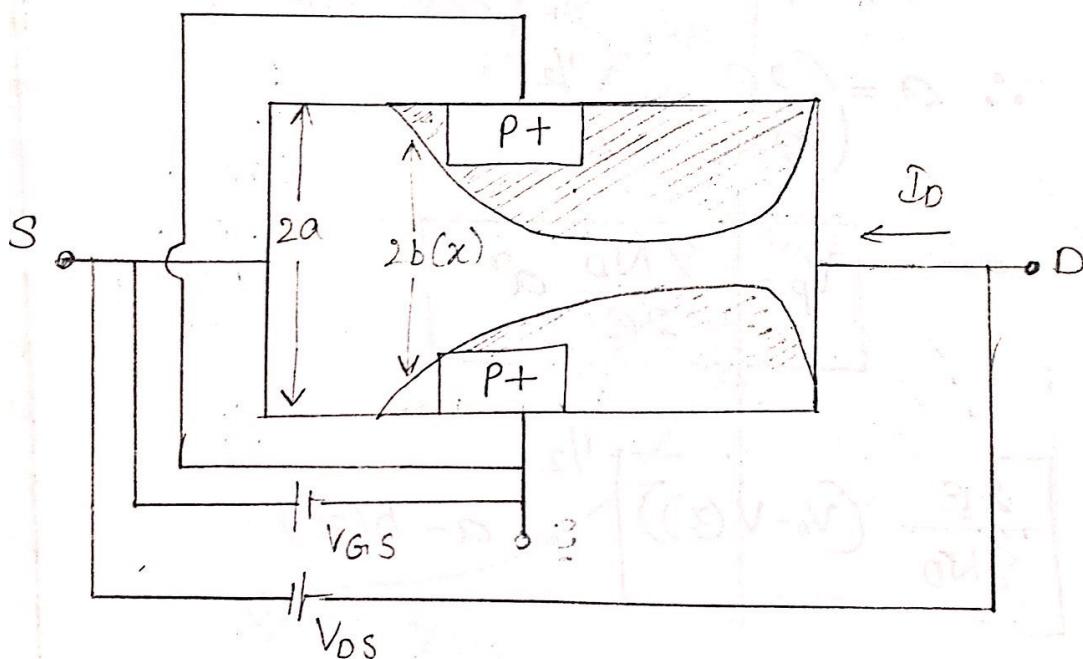
now, consider the case, with $V_{GS} = -1V$. the negative voltage at the Gate reverse biases the pn-junction and hence the depletion region width will be more even before V_{DS} is applied. If we apply V_{DS} now, the resulting drain current will be less than the current when $V_{GS}=0$. The drain characteristics are shown in the following figure.



"Pinch-off region" is also called as "constant current region" or "current saturation region". The value of the drain current I_D in the pinch-off region is called "The Drain-Saturation current" I_{DS} . The value of I_{DS} for

$V_{DS} = 0$ is called "maximum drain saturation current" (I_{DSS}).

If we increase V_{GS} , depletion region spreads into the channel and the channel narrows down. The value of V_{GS} where the channel completely closes and results in zero drain current is called "Pinch-off voltage" and is represented with ' V_p '.



The junction voltage is given by

$$V_j = \frac{2ND}{2E} \omega(\bar{x})$$

where

$$\omega(\bar{x}) = a - b(\bar{x}),$$

↳ width of depletion region

$$V_j = V_0 - V(x)$$

where,

$V(x)$ is negative for a reverse bias

$$V_0 - V(x) = \frac{2ND}{2\epsilon} \omega^r(x)$$

$$\omega(x) = \left[\frac{2\epsilon}{2ND} (V_0 - V(x)) \right]^{1/2} = a - b(x)$$

At pinch-off, $V(x) = -V_p$

and $|V_0| < |V_p|$ and $b(x) = 0$

$$\therefore a = \left(\frac{2\epsilon}{2ND} V_p \right)^{1/2}$$

$$\Rightarrow V_p = \frac{2ND}{2\epsilon} a^r$$

$$\left[\frac{2\epsilon}{2ND} (V_0 - V(x)) \right]^{1/2} = a - b(x)$$

$$V(x) = -V_{GS}$$

and $|V_0| < |V_{GS}|$

$$\Rightarrow \left[\frac{2\epsilon}{2ND} V_{GS} \right]^{1/2} = a - b.$$

$$\Rightarrow V_{GS} = \frac{2ND}{2\epsilon} (a - b)^r$$

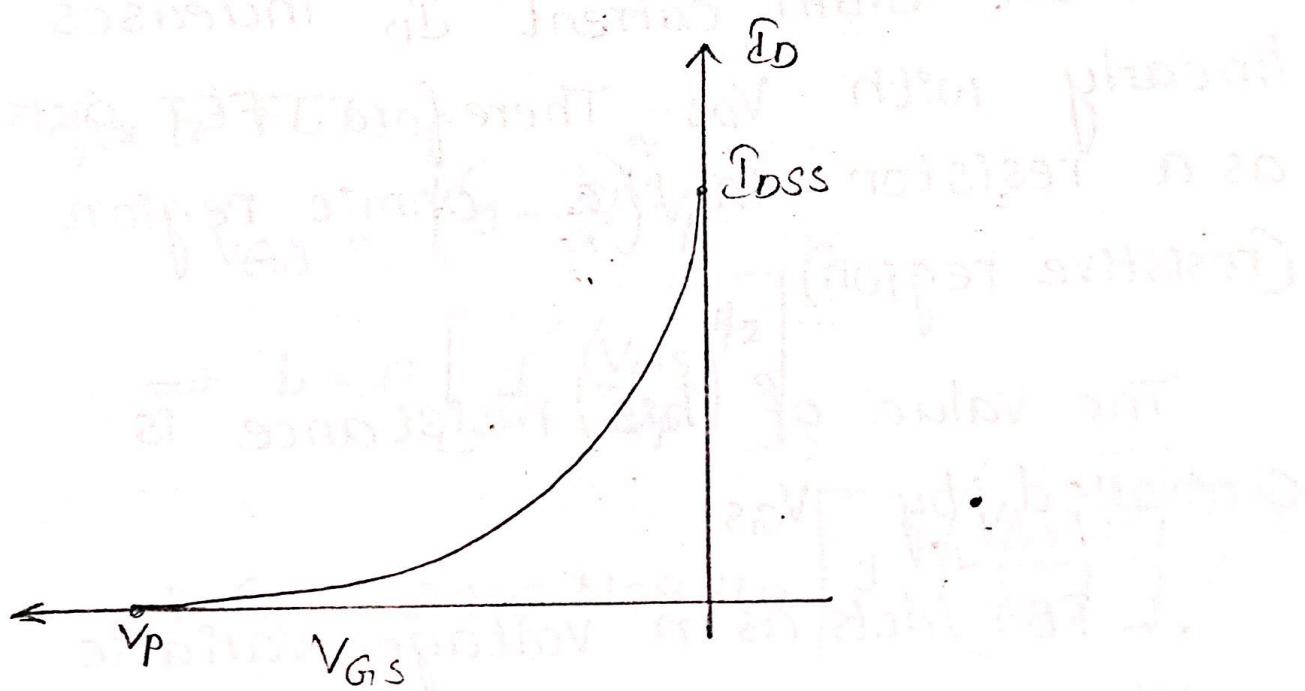
$$V_{GS} = a^r \left(1 - \frac{b}{a}\right)^r \frac{2ND}{2E}$$

$$= V_p \left(1 - \frac{b}{a}\right)^r$$

* Transfer characteristics:

Transfer characteristics is a plot between the drain current I_D and V_{GS} for constant V_{DS} . The Drain current equation is given by

$$I_D = I_{DSS} \left[1 - \frac{V_{GS}}{V_p} \right]^r$$



MOSFET [IGFET]

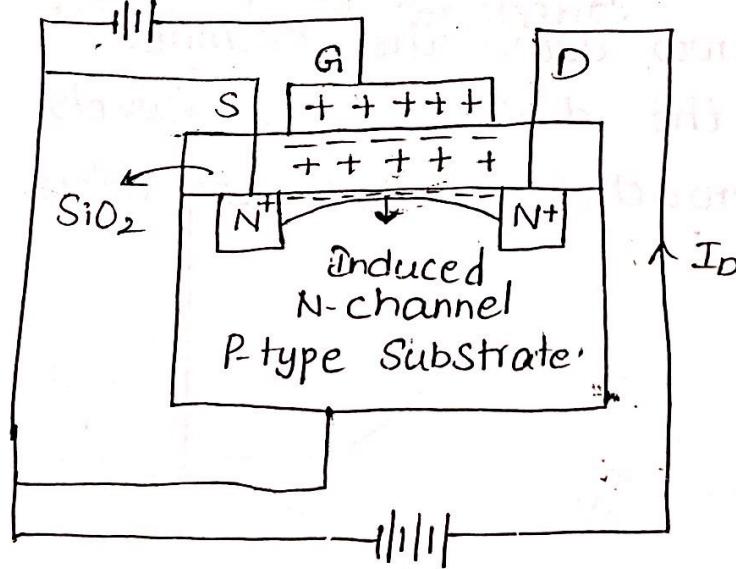
↳ Insulated gate

MOSFET's are of two types.

- (i) Enhancement MOSFET.
- (ii) Depletion MOSFET.

* Enhancement MOSFET:

An n-channel enhancement MOSFET consists of a p-substrate into which two heavily doped n+ regions are formed. The surface of the MOSFET is covered with silicon dioxide layer. Metallic contacts are provided to the n+ regions by cutting holes into the SiO_2 layer. One of the n+ regions by cutting holes into the SiO_2 layer. One of the n+ regions is called "source" and the other as "drain". The oxide layer between source and drain is covered with a metallic layer and is called "gate".



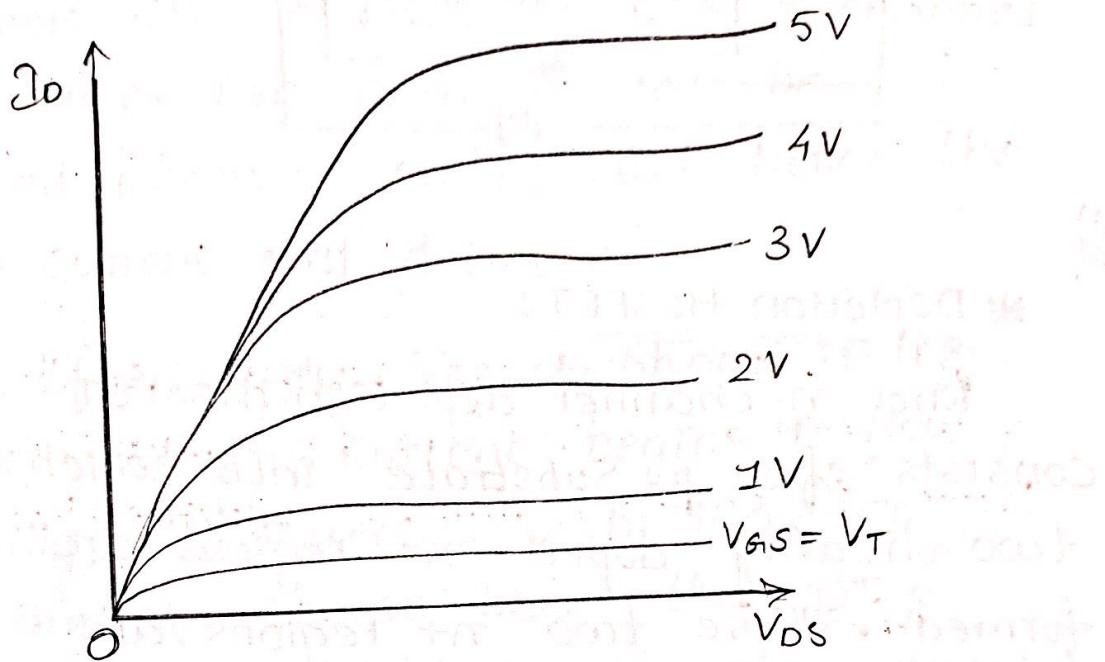
Drain Characteristics:

When we apply positive voltage to the gate, the electrons from 'P' Substrate are attracted towards the gate. If we increase V_{GS} more electrons will accumulate under the gate. These electrons will form an n-channel under the gate, connecting the source and the drain. This n-channel is also called as "Inversion layer". The minimum voltage at the gate required to form the inversion layer is called "Threshold Voltage (V_T)".

Assume $V_{GS} > V_T$. If we apply V_{DS} as shown in the figure the electrons in the nt pulled towards the drain and current I_D begins to flow.

If we increase V_{DS} , the current I_D increases initially. V_{DS} reverse biases the nt-p junction at the drain. Therefore, depletion region spreads into the channel. This will narrow down the channel and hence the drain current levels off and approaches a constant value.

If V_{GS} increases, more electrons are accumulated in the channel and hence, the drain current I_D will be more.

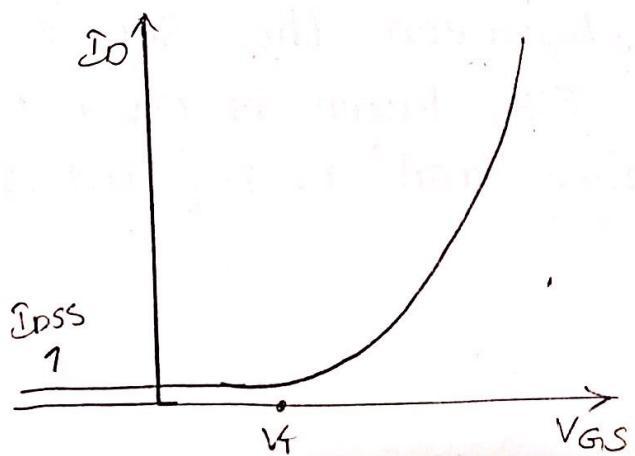


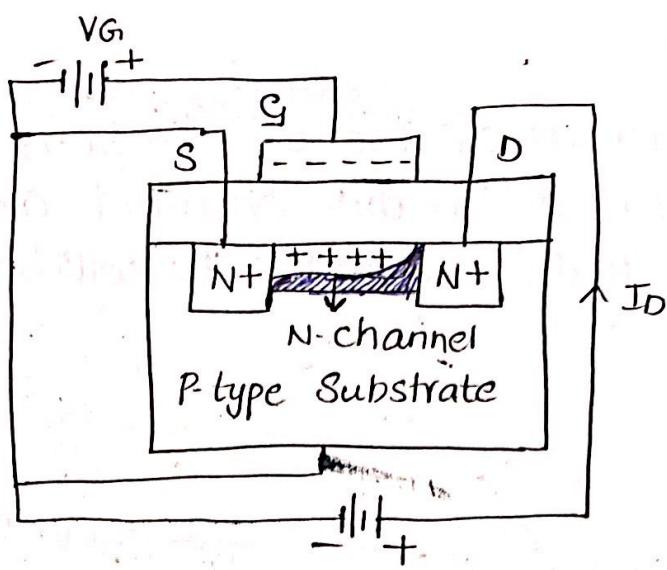
Transfer characteristics:

As long as $V_{GS} < V_T$, $I_D = 0$. Once, if V_{GS} is greater than V_T for large values of V_{DS} , I_D is given by

$$I_D = K [V_{GS} - V_T]^n;$$

where, 'K' is constant.





19/10/11

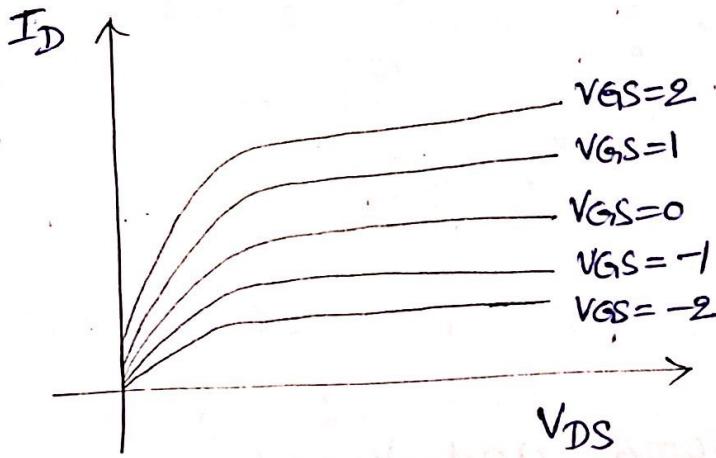
* Depletion MOSFET:

When n-channel depletion MOSFET consists of a p-Substrate into which two heavily doped n⁺ regions are formed. These two n⁺ regions are connected by an n-channel. The Surface of the FET is covered by SiO₂ layer. Metal contacts are made with the two n⁺ regions by cutting holes into SiO₂ layer.

One of the n⁺ regions is referred to as source and the other one as drain. The area between the source and drain above SiO₂ layer is covered with a metal layer and is referred as gate.

If $V_{GS} > 0$, electrons in the P-substrate are attracted into the n-channel and the channel is strengthened. This will increase the drain current. If $V_{GS} < 0$, it repels the electrons in the n-channel and hence, the channel will be depleted (becomes weak) and hence, the drain current will decrease.

If we apply V_{DS} as shown in the figure, drain current begins to flow. Initially, I_D increases with increasing V_{DS} . The V_{DS} reverse biases the n^+ -p junction at the drain. Therefore, the depletion region spreads near the drain and the channel narrows down. The drain current levels off and approaches a constant value with increase in V_{DS} . The Drain characteristics are shown in the figure.

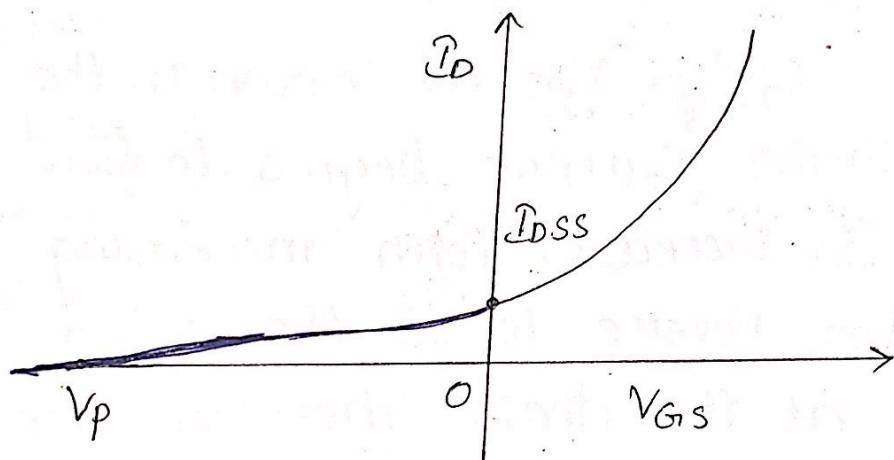


Transfer characteristics:

The Drain current in a depletion MOSFET is given by.

$$I_D = I_{DSS} \left(1 - \frac{V_{GS}}{V_p} \right)^n$$

The transfer characteristics are shown in the following figure



Transistor Biasing & Thermal Stabilization

Biasing:

[Application of direct potentials and currents using external sources to establish certain currents and voltages is known as biasing.]

The established current voltage and current is called D.C. operating point or quiescent point or

Q -point: The operating point must be stable for proper operation of the transistor. However, the operating point (Q -point) shifts with changes in transistor parameters such as I_{CO} , β and V_{BE} . These parameters are temperature dependent, so the operating point is also varies with changes in temperature.

Need for Biasing: We know that the transistor functions most linearly when it is constrained to operate in active region. In order to produce distortion free output in the amplifier circuit, the transistor must be operated in active region. This can be accomplished by biasing the transistor where a set of voltage V_{CEQ} and current I_{CQ} are established and is called Q -point (V_{CEQ}, I_{CQ}).

Usually the Q -point is chosen in the middle of the active region to avoid signal clipping.

How to choose operating point?

By drawing a D.C load line on the output characteristics of common emitter circuit and choosing a point exactly in the middle of the D.C load line, gives the operating point for that circuit.

How to draw D.C. load line?

Consider a common emitter amplifier circuit shown in fig ①. The CE output characteristics are shown in fig ②.

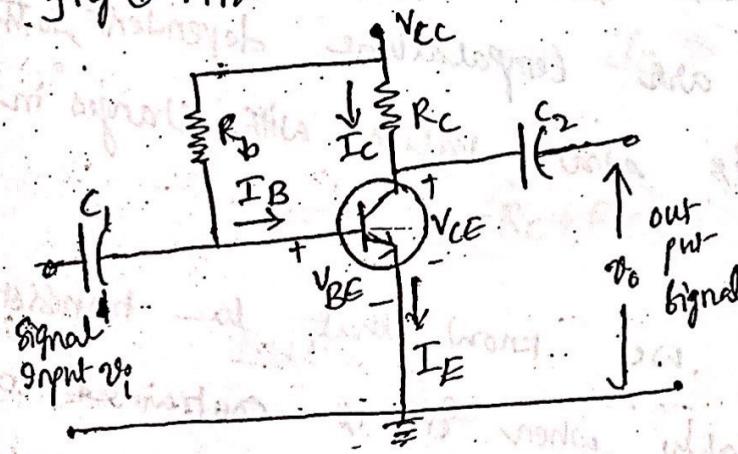


fig ①. ab fixed bias circuit

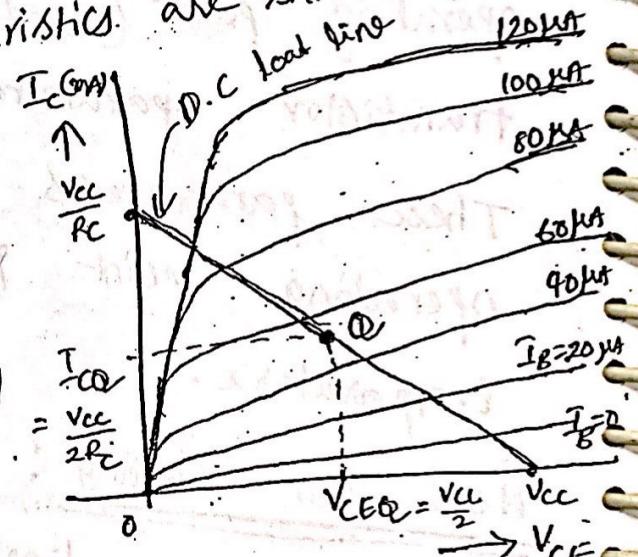


fig ②. CE collector characteristics

For D.C analysis the capacitors C_1 & C_2 act as open ~~circuits~~ circuits i.e. $X_C = \frac{1}{j\omega C}$, for D.C $\omega = 0$.

Then $X_C = \infty$ which indicates an open circuit.

Now applying Kirchoff's Voltage Law for

the output circuit,

$$V_{CC} - I_C R_C - V_{CE} = 0 \quad \text{--- (1)}$$

$$\Rightarrow I_C = \frac{V_{CC}}{R_C} - \frac{1}{R_C} V_{CE} + \frac{V_{CC}}{R_C} \quad \text{--- (2)}$$

Eqn ② indicate a line equation of slope $-1/R_C$

Substituting $I_C = 0$ in eqn ①

$$V_{CE} = V_{CC} \quad \text{--- (3)}$$

Substituting $V_{CE} = 0$ in eqn ①

$$I_C = \frac{V_{CC}}{R_C} \quad \text{--- (4)}$$

By considering the above intercept a load line can be drawn on the characteristics and it is shown in fig ②: The Q-point is chosen in the middle of the line

i.e. $(V_{CEQ}, I_{CQ}) = \left(\frac{V_{CC}}{2}, \frac{V_{CC}}{2R_C}\right)$

Stability factors: Since the collector current (I_C)

is dependent on I_{CO} , V_{BE} and β , the operating point is no longer stable. The extent to which the collector current (I_C) is stabilized with respect to the parameters is given by stability factors.

The stability factor 'S' is defined as the rate of change of collector current I_C with respect to collector base leakage current I_{CO} , keeping both V_{BE} and β constants.

$$S = \frac{\partial I_C}{\partial I_{CO}} \approx \frac{dI_C}{dI_{CO}} \approx \frac{\Delta I_C}{\Delta I_{CO}} \quad \text{--- (5)}$$

The collector current in CE configuration is $I_C = \beta I_B + (1+\beta) I_{CO}$

Differentiating eqn: ⑥

$$\frac{\partial I_C}{\partial I_C} = \frac{\partial}{\partial I_C} \left[\beta I_B + (1+\beta) I_{C0} \right]$$

$$= \beta \left(\frac{\partial I_B}{\partial I_C} \right) + (1+\beta) \cdot \frac{\partial I_{C0}}{\partial I_C}$$

$$= \beta \left(\frac{\partial I_B}{\partial I_C} \right) + (1+\beta) \cdot \gamma_s$$

$$(1+\beta) \cdot \gamma_s = 1 - \beta \left(\frac{\partial I_B}{\partial I_C} \right)$$

$$s^* = \frac{1+\beta}{1 - \beta \left(\frac{\partial I_B}{\partial I_C} \right)}$$

⑦

The stability factor s^* is defined as the rate of change of I_C with respect to V_{BE} , keeping I_{C0} and β constants.

$$s^* = \frac{\partial I_C}{\partial V_{BE}} \approx \frac{\Delta I_C}{\Delta V_{BE}} \quad | I_{C0} \text{ & } \beta = \text{const}$$

The stability factor s^{II} is defined as the rate of change of I_C with respect to β , keeping I_{C0} , V_{BE} constant

$$s^{II} = \frac{\partial I_C}{\partial \beta} \approx \frac{\Delta I_C}{\Delta \beta} \quad | I_{C0}, V_{BE} = \text{const}$$

→ The stability factors are used to compare the biasing circuit. The larger the value of s , the circuit exhibits more thermal instability

Methods of Transistor Biasing:

In order to keep the operating point and to stabilize it, we have different types of biasing circuits 'or' biasing techniques 'or' biasing methods.

1. Fixed bias

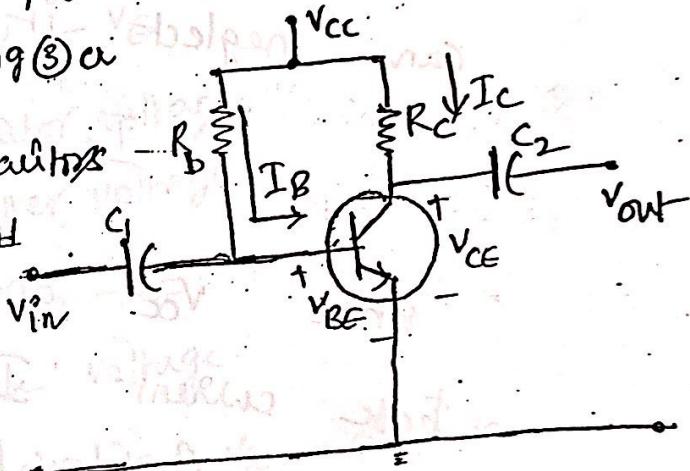
2. collector to base bias

3. self bias.

1. Fixed bias (or) Base resistor bias:

The common emitter amplifier with fixed bias circuit is shown in fig (3)a

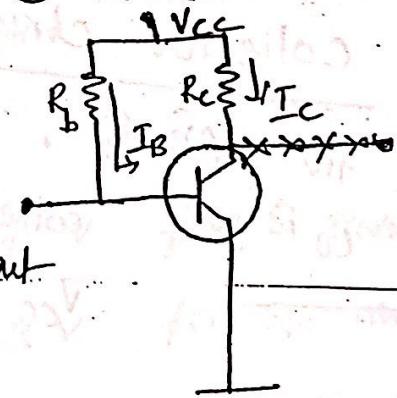
For D.C analysis the capacitors would be open circuited and the equivalent circuit is shown in fig (3)b.



Circuit analysis:

D.C equivalent circuit is divided into two portions, the base circuit or input circuit and the collector circuit or output circuit.

3 (a) fixed bias circuit



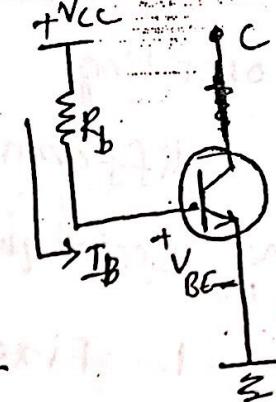
3 (b) D.C equivalent circuit of fixed bias circuit

Base circuit: The base circuit of fixed bias circuit is shown in fig(4).

Applying Kirchoff's voltage law to the input circuit

$$V_{CC} - I_B \cdot R_b - V_{BE} = 0$$

$$I_B = \frac{V_{CC} - V_{BE}}{R_b}$$



fig(4): Base circuit of fixed bias
— (10)

Since V_{BE} is very small and 0.9V for Si transistor and 0.3V for Ge, we

can neglect it.

$$I_B \approx \frac{V_{CC}}{R_b} \quad \text{--- (11)}$$

since V_{CC} and R_b are fixed, the base current I_B also fixed hence the name fixed bias.

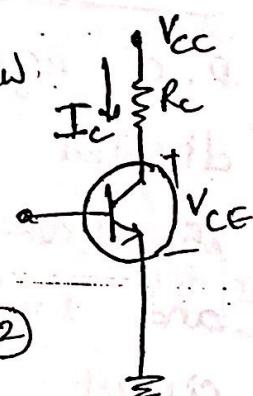
Collector circuit: The collector circuit is shown

in fig(5). Applying Kirchoff's voltage law to the collector circuit,

$$V_{CC} - I_C \cdot R_c - V_{CE} = 0$$

$$V_{CE} = V_{CC} - I_C \cdot R_c. \quad \text{--- (12)}$$

$$\Rightarrow I_C = \frac{V_{CC} - V_{CE}}{R_c} \quad \text{--- (13)}$$



fig(5): Collector circuit of fixed bias

But we know that in active region

$$I_C = \beta I_B \quad (14)$$

i.e., the collector current depends on I_B , where β is constant for a given transistor at a given temperature. The base current in turn depends on R_B from eqn (10). So we can say that the collector current (I_C) is independent of R_C and depends only on I_B . i.e., changing R_C to any level will not affect on I_B and I_C . However, the change in R_C will change the value V_{CE} .

$$V_{CE} = V_C - V_E$$

V_C : Collector voltage

$$V_E : Emitter voltage.$$

$$\text{Similarly } V_{BE} = V_B - V_E$$

V_B : Base voltage.

In fixed bias circuit $V_E = 0$, so

$$V_{CE} = V_C \text{ and}$$

$$V_{BE} = V_B$$

Where $V_{BE} = 0.7 \text{ V}$ for Si Transistor

$V_{BE} = 0.3 \text{ V}$ for Ge Transistor

$$V_{CE(\text{sat})} = 0.2 \text{ V for Si}$$

$$V_{BE(\text{sat})} = 0.8 \text{ V for Si}$$

a. saturation condition $|I_r| < \beta |I_B|$

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Stability factor (S) for fixed bias circuit in order to

find stability factor for any biasing arrangement, it is necessary to find the relation between I_B & I_C . For fixed bias circuit I_B is independent of I_C . From eqn (1). $\therefore \frac{dI_B}{dI_C} = 0$.

$$S = \frac{1 + \beta}{1 - \beta(0)} = 1 + \beta$$

$$S = 1 + \beta \quad \text{for fixed bias}$$

For $\beta = 50$, $S = 51$, which means that I_C increases 51 times as fast as I_{C0} . Due to large value of 'S', a definite possibility of thermal runaway with this circuit. In conclusion,

The stability of Q-point is very poor with fixed bias circuit. In practice, this circuit is not used.

Advantage: Simplicity of circuit.

2. Collector to Base Bias (or) Biasing with feedback

Resistor

The common emitter amplifier circuit with collector to base bias is shown in fig ⑥. This circuit provides some degree of stabilization for the operating point.

The D.C. equivalent circuit is

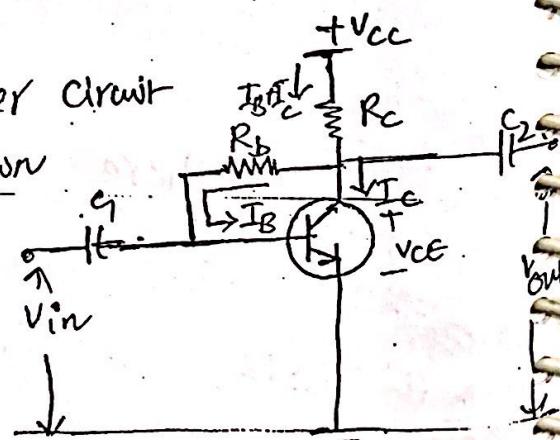


fig ⑥: CE Amplifier with

Circuit Analysis: The D.C equivalent circuit is divided into two portions, the base circuit and the collector circuit.

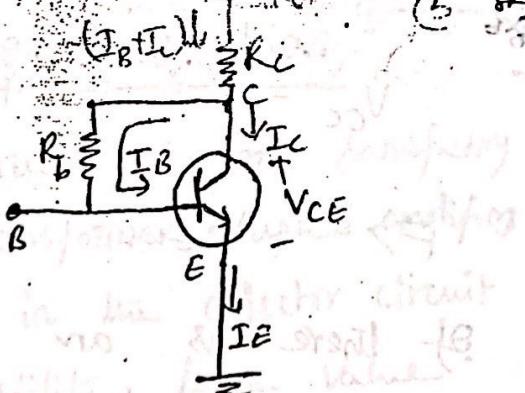


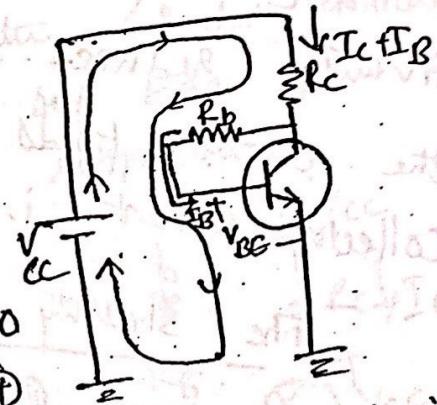
fig 7. D.C equivalent circuit of collector to base bias.

Base circuit: The base circuit or input circuit of

collector-to-base bias circuit is shown in fig 8. Applying

Kirchoff's voltage law to the base circuit

$$V_{CC} - (I_B + I_C)R_C - I_B R_B - V_{BE} = 0 \quad (14)$$



$$\Rightarrow V_{CC} = (R_b + R_c) I_B + \beta I_B R_C + V_{BE} \quad \text{fig 8: Base circuit of collector-to-base bias}$$

$$\Rightarrow I_B = \frac{V_{CC} - V_{BE}}{R_b + (1 + \beta) R_c} \quad (15) \quad (\because I_C = \beta I_B)$$

From eqn(4), we can also write I_B in terms of I_C

$$I_B = \frac{V_{CC} - I_C R_C - V_{BE}}{R_b + R_c} \quad (16)$$

Collector circuit: The collector circuit of collector to

base bias circuit is shown in fig 9. Applying Kirchoff's voltage law (KVL) to the circuit

$$V_{CC} - R_C (I_C + I_B) - V_{CE} = 0$$

$$\Rightarrow V_{CE} = V_{CC} - (I_C + I_B) R_C \quad (1)$$

If there is an increase in collector current due to change in parameters like β and I_{CO} , the base current

decreases since the supply voltage V_{CC} is constant.

As I_C depends on I_B ($I_C = \beta I_B$), the decrease in I_B reduces the original increase in I_C . So the circuit tends to maintain a stable value of collector current i.e., the Q -point is stable.

The Stability factor 'S'

from eqn (1)

$$V_{CC} - I_C R_C - V_{BE}$$

$$I_B = \frac{R_b + R_C}{R_b + R_C}$$

Modes w.r.t. I_C .

Differentiating both sides

$$\frac{dI_B}{dI_C} = \frac{-R_C}{R_b + R_C}$$

The stability factor

$$S = \frac{1 + \beta}{1 - \beta \left(\frac{R_C}{R_b + R_C} \right)}$$

$$S = \frac{1 + \beta}{1 - \beta \left(\frac{R_C}{R_b + R_C} \right)} \quad (18)$$

$$S = \frac{1 + \beta}{1 + \beta \left(\frac{R_C}{R_b + R_C} \right)}$$

If $R_C \gg R_B$ $S \approx 1$. i.e., the stability can be improved by making $R_C \gg R_B$.

If R_b is very small compared to R_C then $S = 1 + \beta$.

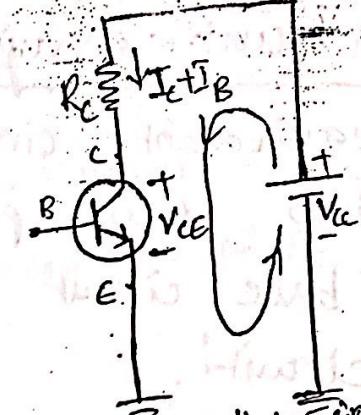
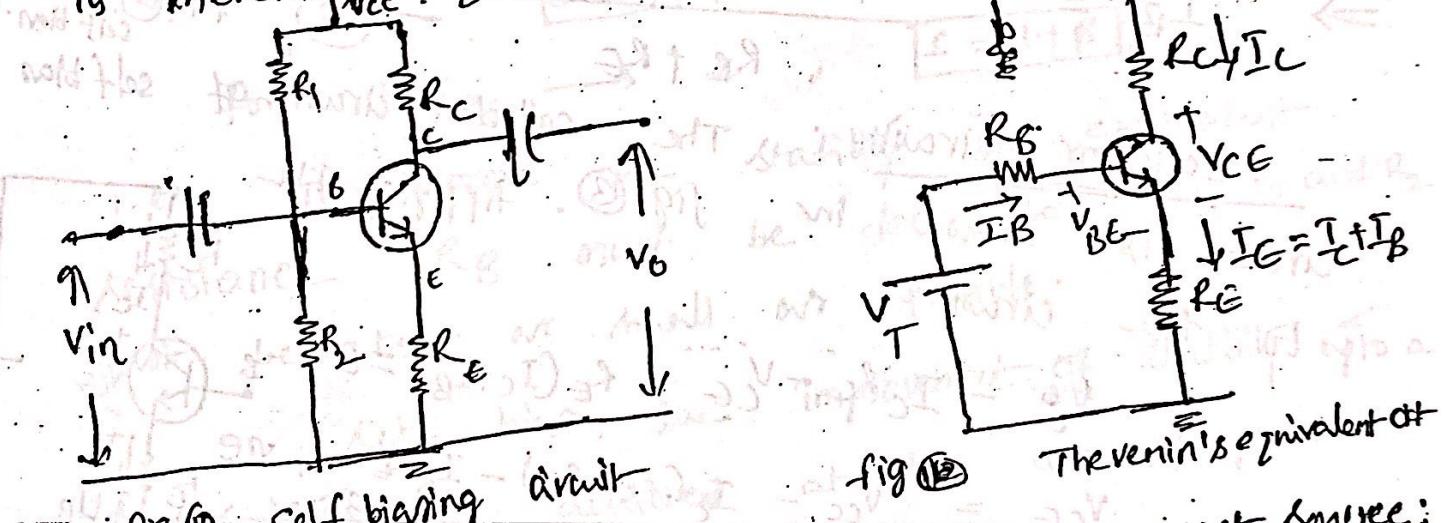


fig (1): collector circuit
 V_{CC} is constant

Self Bias (or) Emitter Bias (or) Voltage Divide Bias

The collector to base bias circuit is not satisfactory for the amplifier circuits like transformer coupled amplifiers where the d.c load resistance in the collector circuit is very small. But for better stability large value of ' R_C ' is required in collector to base bias.

To overcome this problem we use self bias circuit. The self bias circuit can be used if there is zero d.c resistance in series with the collector terminal. fig(10) and fig(11) shows the self bias circuit and its Thevenin's equivalent circuit respectively.



fig(10) self biasing circuit

fig(11)

Thevenin's equivalent of

use of self bias circuit as a constant current source.

If I_C tends to increase, say, due to increase in temperature, the current in R_E increases.

I_{CO} with temperature, the voltage drop across R_E increases thereby decreasing the base current. As a result I_C is maintained almost constant.

Circuit Analysis : Applying Thevenin's theorem for the

circuit in fig ⑩, we will get the circuit in fig ⑪.
where $V_T = \frac{V_{CC} \cdot R_2}{R_1 + R_2}$ and $R_B = \frac{R_1 R_2}{R_1 + R_2}$.

Base circuit : The base circuit of self bias circuit

is shown in fig ⑫. Applying KVL

$$V_T - R_B \cdot I_B - V_{BE} - R_E (I_B + I_C) = 0$$

$$V_T = (R_B + R_E) I_B + R_E I_C + V_{BE}$$

$$\Rightarrow I_B = \frac{V_T - R_E I_C - V_{BE}}{R_B + R_E}$$

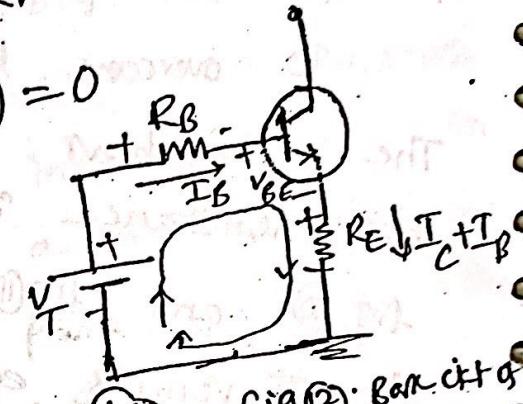


fig ⑫. Base circuit of self bias.

Collector circuit : The collector circuit of self bias

circuit is shown in fig ⑬. Applying KVL

$$V_{CC} - I_C R_C - V_{CE} - R_E (I_C + I_B) = 0$$

$$\Rightarrow V_{CE} = V_{CC} - I_C (R_C + R_E) - I_B R_E$$

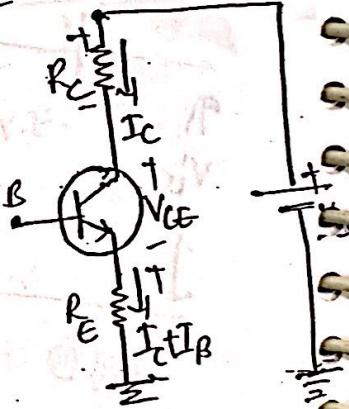


fig ⑬. Collector circuit of self bias.

The stabilization factor 's' :

from eqn ⑯ we know that

$$I_B = \frac{V_T - R_E \cdot I_C - V_{BE}}{R_B + R_E}$$

Differentiating w.r.t I_C both the sides

$$\frac{dI_B}{dI_C} = \frac{-R_E}{R_B + R_E}$$

The stability factor $s = \frac{1+\beta}{1-\beta \left(\frac{dI_C}{dV_B} \right)}$

i.e. For self bias circuit

$$s = \frac{1+\beta}{1-\beta \left(-\frac{R_E}{R_B+R_E} \right)} \quad (22)$$

This can be written as, $\frac{1+\beta R_E}{1+\beta + R_E}$ — (23).

From the above eqn, we can conclude that for small values of R_E/R_B i.e., $\frac{R_E}{R_B} \ll 1$,

$$s \approx 1$$

for $R_E/R_B \rightarrow 0$

$$s = 1+\beta$$

i.e., To improve the stability the equivalent resistance R_E must be decreased i.e., R_1 and R_2 must be kept as small as possible.

In self bias, the improvement of stability upto a factor '1' is achieved at the cost of power dissipation.

The Stability factor 's' for self bias circuit

We know that

$$s = \frac{\partial I_C}{\partial V_{BE}}$$

| I_{CO}, β are constants

From the bias circuit we know that

$$V_T = (R_B+R_E)I_B + R_E I_C + V_{BE} \quad (22)$$

But we know that

$$I_C = \beta I_B + (\text{constant}) \quad (23)$$

$$\Rightarrow I_B = \frac{I_C}{\beta} - (\text{constant}) \quad (24)$$

Substituting eqn (24) in eqn (22)

$$V_T = (R_B + R_E) \frac{I_C}{\beta} + R_E I_C + V_{BE}$$

$$V_T - V_{BE} = \left(R_E + \frac{R_B + R_E}{\beta} \right) I_C$$

$$\Rightarrow I_C = \frac{V_T - V_{BE}}{R_E + \frac{R_B + R_E}{\beta}}$$

Differentiating both the sides w.r.t. V_{BE}

$$\frac{\partial I_C}{\partial V_{BE}} = \frac{1}{R_E + \frac{R_B + R_E}{\beta}}$$

$$s^1 = \frac{-\beta}{R_B + R_E(1+\beta)} \quad (25)$$

from eqn (25) we can write

$$s^1 = -\frac{s}{R_B + R_E} + \frac{\beta}{1+\beta} \quad (26)$$

From the above eqn (26), we can conclude that, as we reduce 's' towards unity (1), s^1 is also reducing, i.e., as 's' is decreased, the change in I_C with respect to I_{CO} and V_{BE} also

The stability factor S^H for self bias circuit.

We know that-

$$S^H = \frac{\partial I_C}{\partial \beta}$$

| I_{CO} , V_{BE} are constant

From the base circuit,

$$I_C = \frac{V_T - V_{BE}}{R_E + \frac{R_B + R_E}{\beta}}$$

$$\beta (V_T - V_{BE})$$

$$R_B + (1+\beta) R_E$$

$$S^H = \frac{\partial I_C}{\partial \beta} = \frac{[R_B + (1+\beta) R_E] (V_T - V_{BE}) - \beta (V_T - V_{BE}) R_E}{(R_B + (1+\beta) R_E)^2}$$

$$S^H = \frac{\partial I_C}{\partial \beta} = \frac{R_B (V_T - V_{BE}) + (V_T - V_{BE}) R_E}{(R_B + (1+\beta) R_E)^2}$$

$$(R_B + R_E) (V_T - V_{BE})$$

$$S^H = \frac{\partial I_C}{\partial \beta} = \frac{(R_B + (1+\beta) R_E)^2}{(R_B + R_E)^2}$$

(29)

BW-

$$I_C \cdot S = \frac{\beta (V_T - V_{BE})}{(R_B + (1+\beta) R_E)} \times \frac{(1+\beta) (R_B + R_E)}{(R_B + (1+\beta) R_E)}$$

$$\Rightarrow \frac{I_c \cdot s}{\beta(1+\beta)} = \frac{(R_B + R_E) (V_T - V_{BE})}{(R_B + (1+\beta) R_E)^2}$$

$$= s'' \quad (\because \text{from eqn } 29)$$

s''	$\frac{I_c \cdot s}{\beta(1+\beta)}$
-------	--------------------------------------

(30)

from eqn (30), we can conclude that, as we reduce 's' towards unity, s'' is also reduced i.e., as s is decreased, the change in I_c with respect to I_{C0} , V_{BE} and β also decreases. i.e., when the ratio R_B/R_E is very small, the stability factors s , s' and s'' also small, which improves the stability of operating point. Self bias circuit is most widely used in amplifier applications.

compensation Techniques

The collector-to-base bias circuit and self bias circuit are used to limit the variations in the operating collector current I_C caused by variations in I_{CO} , V_{BE} and β . These circuits are examples of negative feedback amplifiers where the negative feedback reduces the amplification of the signal. If this loss in signal amplification is intolerable and extremely stable biasing conditions are required, then it is necessary to use compensation techniques.

There are different types of compensation techniques available. They are

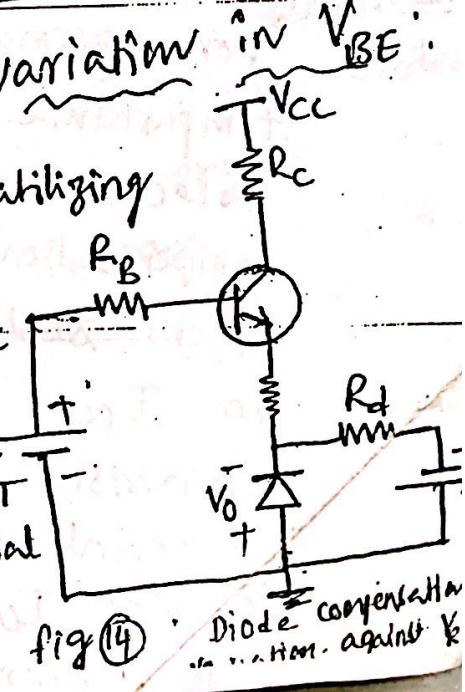
1. Diode compensation techniques
2. Thermistor compensation techniques
3. Sensoristor compensation techniques

1. Diode compensation Techniques

(a) Compensation against variation in V_{BE}

The circuit utilizing self bias stabilizing technique and diode compensation is shown in fig(14). The supply voltage

V_{DD} is used to keep diode in forward biased along with resistance R_d . If the diode is of the same material and type as the transistor,



the voltage V_0 across the diode will have the same temperature coefficient ($-2.5 \text{ mV}/\text{°C}$) as the base to emitter voltage V_{BE} . i.e., when V_{BE} changes by ∂V_{BE} with change in temperature, V_0 changes by ∂V_0 in the opposite direction so that the changes tend to cancel each other.

Applying KVL for the base circuit, we get

$$V_f - R_B I_B - V_{BE} - R_E (I_C + I_B) + V_0 = 0.$$

Bkt- $I_C = \beta I_B \Rightarrow I_B = I_C/\beta$

$$I_C = \frac{\beta [V_f - (V_{BE} - V_0)]}{R_B + (\beta + 1) R_E} \quad (21)$$

Since V_{BE} tracks V_0 with respect to temperature from the above eqn it is clear that I_C is insensitive to variations in V_{BE} .

(b) Compensation against variation in I_{CO}

For germanium transistors, changes in I_{CO} with temperature play the more important role in collector current stability. The diode compensation circuit shown in fig ⑤ offers stabilization against variations in I_{CO} . If the diode and transistor are of same type and material, the reverse saturation current I_0 of the diode will increase with temperature at the same rate as

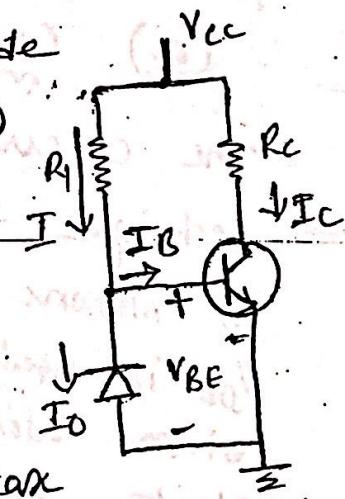


fig ⑤: Diode compensation against variation in I_{CO}

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the transistor collector saturation current I_{CO} .

From fig 15

$$I = \frac{V_{CC} - V_{BE}}{R_1} \approx \frac{V_{CC}}{R_1} = \text{constant}$$

since the diode is reverse biased by the amount $V_{BE} = 0.3V$ for Ge transistors, it follows that the current through D is I_0 .

$$\therefore \text{The base current } I_B = I - I_0 - \text{Eqn 32.}$$

But we know

$$I_C = \beta I_B + (1+\beta) I_{CO}$$

Substituting eqn 32 in the above,

$$I_C = \beta(I - I_0) + (1+\beta) I_{CO}$$

$$I_C = \frac{\beta I - \beta I_0 + I_{CO} + \beta I_{CO}}{\beta I - I_{CO}}$$

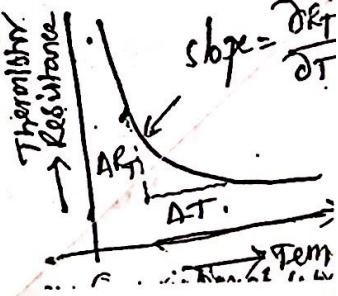
of $\beta \gg 1$, I_C is essentially constant over the desired range of temperature.

② Thermistor compensation Techniques : This method

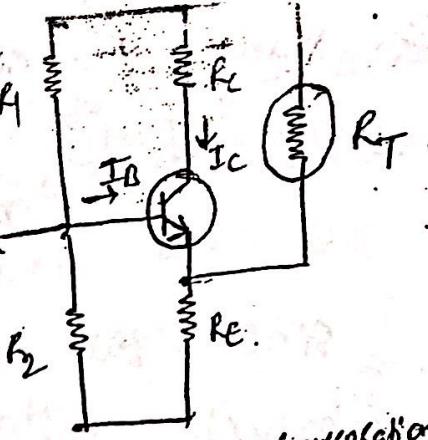
of transistor compensation uses temperature sensitive elements, the Thermistors, rather than diodes or transistors. The Thermistor has a negative temperature coefficient i.e., its resistance decreases exponentially with increasing temperature as shown in fig.

The slope $\frac{\partial R_T}{\partial T}$ is the temperature

Coefficient which is negative.



The circuit of fig (7) uses a thermistor (R_T) to minimize the increase in collector current due to changes in I_{CO} , V_{BE} and β with temperature (T).



As T rises, R_T decreases and

current through R_T increases which fig (7) Thermistor compensation of increase in I_C with flow through resistance R_E . So the voltage drop across R_E also increases which is in the direction to reverse-bias the transistor and hence the base current I_B decreases which stabilizes the collector current I_C ($\because I_C = \beta I_B$)

$$\text{i.e., } I_C = \beta I_B + (1/\beta) I_{CO}$$

As temperature increases I_{CO} increases I_B decreases

so I_C is maintained constant.

An alternative circuit of thermistor compensation technique is shown in fig (8).

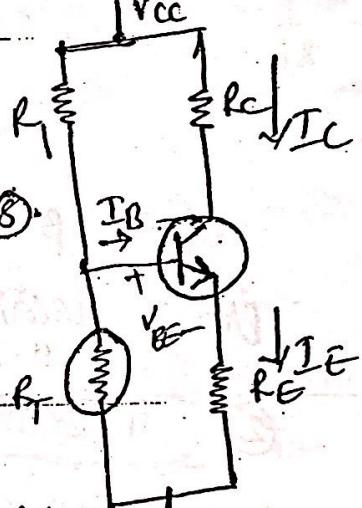
Here the thermistor is connected between base and ground.

When the temperature (T) rises,

the resistance of thermistor (R_T) decreases,

as a result the voltage across fig (8): Thermistor compensation of the thermistor also decreases which increase in I_C due to temperature (T)

causes the base to emitter voltage (V_{BE}) to decrease, hence the base current decreases which stabilizes the collector current.



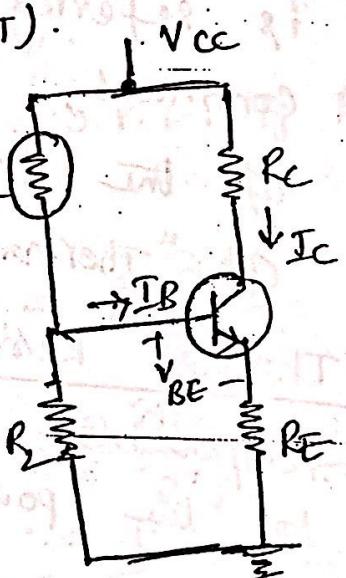
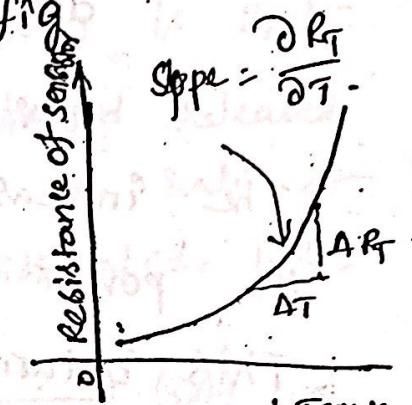
③ Sensor Compensation Technique: This method of transistor compensation also uses temperature sensitive resistive elements "the Sensor". Sensor has a positive temperature coefficient, its resistance increases exponentially with respect to temperature as shown in fig.

The slope $\frac{\partial R_T}{\partial T}$ is the temperature coefficient of the ~~sensor~~ sensor and it is positive.

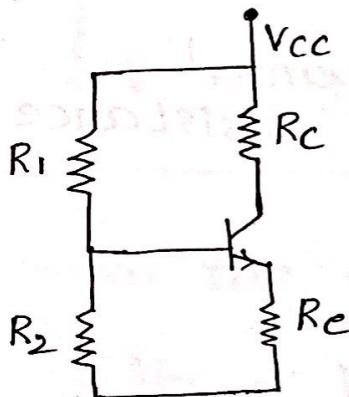
The circuit of fig ② uses a sensor to minimize the increase in collector current due to changes in I_{CO} , V_{BE} and β with temperature (T).

As temperature increases, R_T increases which decreases the current flowing through it. Hence current through R_2 decreases which reduces the voltage drop between base and ground. So V_{BE} also reduces which in turn reduces

the base current I_B . Hence fig ②. sensor compensation of increase in I_C due to T the collector current I_C is maintained constant over a desired range of temperature.



Thermal runaway and the condition to avoid "thermal runaway":



Thermal runaway:

Because of the power dissipation at the collector junction, the junction temperature will increase. This

causes the reverse saturation current (I_{C0}) will increase, which in turn increases (\dot{Q}_c), this will cause more power dissipation and the transistor may be permanently damaged, this phenomena is called "Thermal runaway"

Condition to avoid Thermal runaway

$P_d \rightarrow$ Power dissipated at the collector junction

$P_c \rightarrow$ Power Generated at the collector junction

T_j — junction Temperature

T_A — Ambient (Surrounding) Temperature

$(T_j - T_A)$ — rise in temperature. It is proportional to the power dissipation.

$$\therefore (T_j - T_A) \propto P_D$$

$$T_j - T_A = (\textcircled{H}) P_D$$

[Capital 'H'] \textcircled{H} is called "Thermal resistance"

Differentiate wrt T_j

$$\Rightarrow I - 0 = (\textcircled{H}) \frac{\partial P_D}{\partial T_j}$$

$$\Rightarrow \frac{\partial P_D}{\partial T_j} = \frac{1}{(\textcircled{H})} \quad \textcircled{1}$$

To avoid thermal runaway, the rate of power generated should be less than the rate of power dissipated

$$\therefore \frac{\partial P_c}{\partial T_j} < \frac{\partial P_D}{\partial T_j}$$

\therefore from $\textcircled{1}$

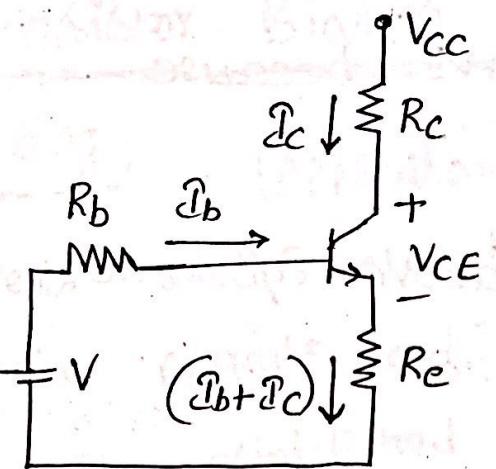
$$\Rightarrow \frac{\partial P_c}{\partial T_j} < \frac{1}{(\textcircled{H})} \quad \textcircled{2}$$

Generated power, $P_c = I_c [V_{CE}]$

$$\approx I_c [V_{EB} + V_{CE}]$$

But, V_{EB} is very small ≈ 0.7

$$\Rightarrow P_c \approx I_c [V_{CE}] \quad \textcircled{3}$$



From the circuits (Outer loop Equation)

$$V_{CE} = V_{CC} - I_c [R_c + R_e]$$

∴ from Eqⁿ ③

$$\Rightarrow P_{CC} = I_c [V_{CC} - I_c (R_c + R_e)]$$

$$\Rightarrow P_{CC} = I_c V_{CC} - I_c^2 (R_c + R_e)$$

Differentiating w.r.t I_c

$$\Rightarrow \frac{\partial P_{CC}}{\partial I_c} = V_{CC} - 2I_c (R_c + R_e) - ④$$

from Eq^m ②

$$\frac{\partial P_C}{\partial T_j} < \frac{1}{H}$$

$$\text{where } \frac{\partial P_C}{\partial I_c} \cdot \frac{\partial I_c}{\partial T_j} < \frac{1}{H}$$

Usually the operating point is chosen at the middle of the active region to avoid oscillations and re-stabilization.

$\frac{\partial I_c}{\partial T_j}$ is always '+ve' because
 I_c increases with T_j

\therefore To satisfy the above Eqⁿ under
all conditions,

$$\frac{\partial P_c}{\partial I_c} < 0$$

from Equation ③,

$$V_{cc} - 2I_c(R_{ct} + R_e) < 0$$

$$\Rightarrow V_{cc} < 2I_c(R_{ct} + R_e)$$

$$\Rightarrow I_c > \frac{V_{cc}}{2(R_{ct} + R_e)}$$

$$\Rightarrow I_c(R_{ct} + R_e) > \frac{V_{cc}}{2} \quad \text{--- } ⑤$$

But,

$$V_{CE} = V_{cc} - I_c(R_{ct} + R_e)$$

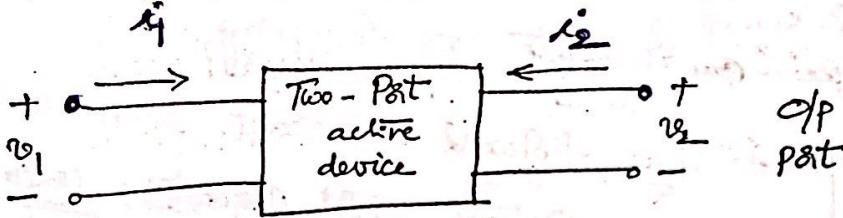
From ⑤,

$$\Rightarrow V_{CE} < V_{cc} - \frac{V_{cc}}{2}$$

$$\Rightarrow V_{CE} < \frac{V_{cc}}{2}$$

TWO PORT NETWORK AND H-PARAMETER MODEL

①



D/P
P&T

The terminal behaviour of a two port device can be specified by two voltages and two currents. The box in the above figure represents a two port network. We may select two parameters as independent variables and express the remaining two as functions of the independent variables.

To use the h-parameter model we select the output current i_2 and output voltage v_2 as independent variables and represent the output current i_2 and input voltage v_1 as functions of i_1, v_2 :

$$v_1 = f_1(i_1, v_2) \rightarrow ① \quad i_2 = f_2(i_1, v_2) \rightarrow ②$$

Equations ① and ②, when expanded using h-parameters gives the following equations:

$$v_1 = h_{11} i_1 + h_{12} v_2 \rightarrow ③ \quad \begin{aligned} &\text{h-parameter equations} \\ &\text{of a two port network,} \\ &\text{eqn ③} \\ &i_2 = h_{21} i_1 + h_{22} v_2 \rightarrow ④ \end{aligned}$$

From eqn ③ we can write the following,

$$h_{11} = \left. \frac{v_1}{i_1} \right|_{v_2=0} = \text{Input Resistance with output short circuited. } \underline{\text{One - ohms.}}$$

$$h_{12} = \frac{v_2}{i_2} \Big|_{i_1=0} = \text{Open circuit; Units: } \text{volt/amp}$$

From eq (4) we can write the following:

$$h_{21} = \frac{i_2}{v_1} \Big|_{v_2=0} = \text{forward current gain with output short circuited; Units: } \text{amp/amp}$$

$$h_{22} = \frac{i_2}{v_2} \Big|_{i_1=0} = \text{output admittance (conductance) with input short circuited; Units: } \text{mho}$$

Abbreviation:

- $h_1 = i = \text{input}$ $z_2 = 0 = \text{output}$
- $h_2 = g = \text{reverse gain}$ $z_1 = f = \text{forward gain}$
- $h_{12} = h_f = \text{forward current gain with output short circuited}$ (forward transfer)

e.g.: $r_{bb} \rightarrow$ Input Resistance in CB with output short circuited

$h_{fe} \rightarrow$ forward current gain with output short circuited

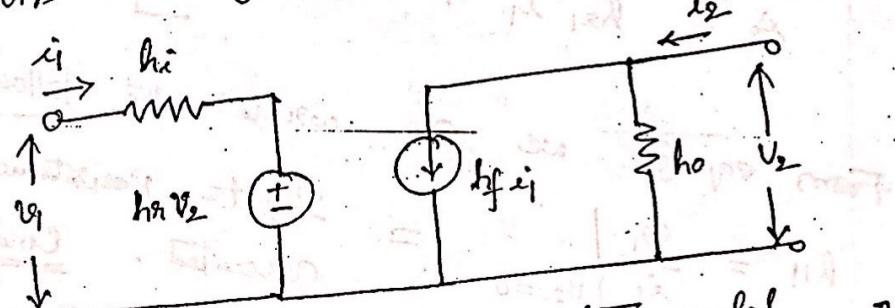
The H-parameter model:

The first equations for any two port network using H-parameters can now be written as,

$$v_1 = h_{11} i_1 + h_{12} v_2$$

$$i_2 = h_{21} i_1 + h_{22} v_2$$

An electrical circuit model which satisfies the given in the following figure.



The H-parameter model

Why the h-parameters are called hybrid parameters? (2)

The dimensions of various h-parameters are,

h_{11} → Open circuit impedance - ohms

h_{12} → Reverse voltage gain - no units

h_{21} → Forward current gain - no units

h_{22} → Open admittance - mhos.

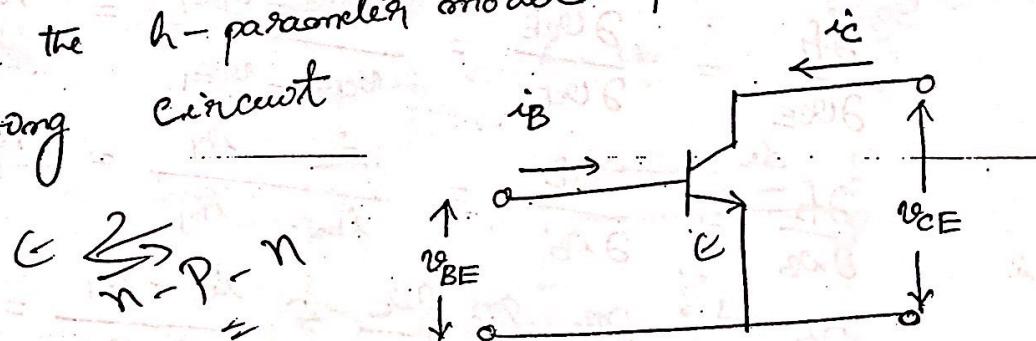
The units of h-parameters are mixed. They are not consistent, hence these parameters are called hybrid parameters.

What are the advantages of hybrid parameters?

- ① h-parameters are real numbers at audio frequencies.
- ② h-parameters are easy to measure.
- ③ h-parameters can be obtained from transistor characteristic curves.
- ④ h-parameters are convenient to use in circuit analysis and design.
- ⑤ h-parameters are specified for many transistors by the manufacturers.

* Transistor h-parameter model (Transistor Hybrid Model)

To derive the h-parameter model for a transistor consider the following circuit



* Derive the h-parameter model for a transistor].

V_{BE} , i_C are functions; i_B , V_{CE} are variables. We can write,
 V_{BE} and i_C as,

$$V_{BE} = f_1(i_B, V_{CE}) \rightarrow ①$$

$$i_C = f_2(i_B, V_{CE}) \rightarrow ②$$

Expanding the above two equations by Taylor's series we get,

$$\Delta V_{BE} = \frac{\partial f_1}{\partial i_B} \Delta i_B + \frac{\partial f_1}{\partial V_{CE}} \Delta V_{CE}$$

$$\Delta V_{BE} = \frac{\partial f_1}{\partial i_B} \cdot \Delta i_B + \frac{\partial f_1}{\partial V_{CE}} \cdot \Delta V_{CE} \rightarrow ③$$

$$\Delta i_C = \frac{\partial f_2}{\partial i_B} \Delta i_B + \frac{\partial f_2}{\partial V_{CE}} \Delta V_{CE} \rightarrow ④$$

The above equations can be modified by considering the following things,

$$\Delta V_{BE} = v_{be},$$

$$\Delta i_B = i_b, \quad \Delta V_{CE} = v_{ce}, \quad \Delta i_C = i_c$$

$$\frac{\partial f_1}{\partial i_B} = \frac{\partial V_{BE}}{\partial i_B} = \frac{v_{BE_2} - v_{BE_1}}{i_{B_2} - i_{B_1}} = h_{ie}$$

$$\frac{\partial f_1}{\partial V_{CE}} = \frac{\partial V_{BE}}{\partial V_{CE}} = \frac{v_{BE_2} - v_{BE_1}}{v_{CE_2} - v_{CE_1}} = h_{re}$$

$$\frac{\partial f_2}{\partial i_B} = \frac{\partial i_C}{\partial i_B} = \frac{i_c - i_{c_1}}{i_{B_2} - i_{B_1}} = h_{fe}$$

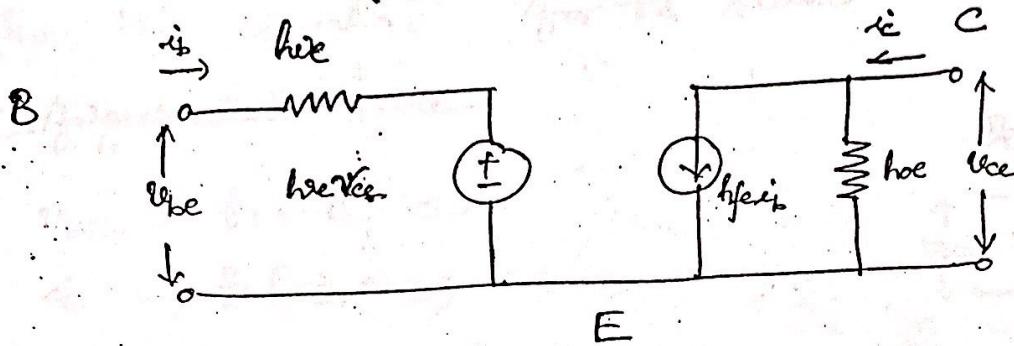
$$\frac{\partial f_2}{\partial V_{CE}} = \frac{\partial i_C}{\partial V_{CE}} = \frac{i_c - i_{c_1}}{v_{CE_2} - v_{CE_1}} = h_{oe}$$

∴ the equations become,

$$\boxed{v_{be} = h_{ie} i_b + h_{re} v_{ce}}$$

$$i_c = h_{fe} i_b + h_{oe} v_{ce}$$

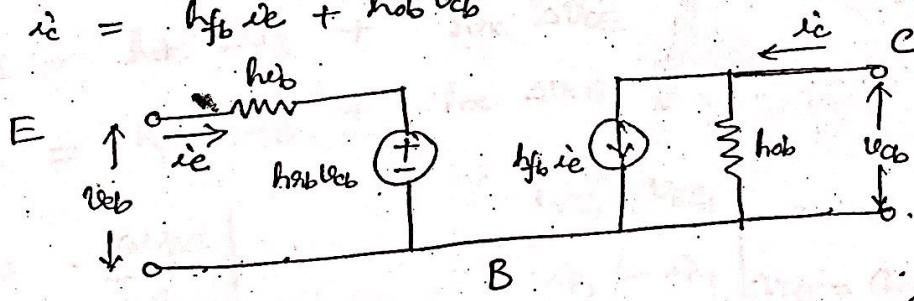
The corresponding h-parameter model is given by,



Similarly the h-parameter model for CB Configuration is,

$$v_{eb} = h_{ab} i_e + h_{bb} v_{cb}$$

$$i_c = h_{fb} i_e + h_{ob} v_{cb}$$

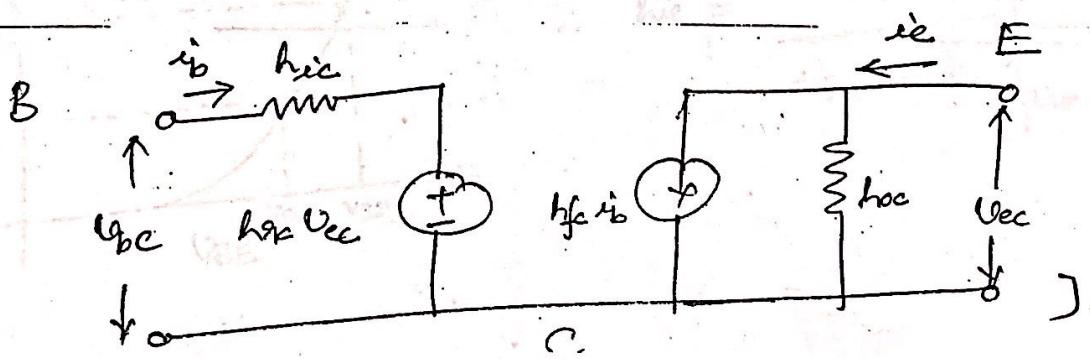


Similarly the h-parameter model for CC Configuration is,

$$v_{bc} = h_{ac} i_b + h_{ec} v_{ec}$$

$$i_c = h_{fc} i_b + h_{oc} v_{ec}$$

emitter = out/Op
base = input



Two to determine the h-parameters from the Transistor static characteristics:

Consider the case of CE Configuration. The four h-parameters are h_{ie} , h_{fe} , h_{re} , h_{oe} .

h_{ie} , h_{fe} are calculated from the I/P characteristics.

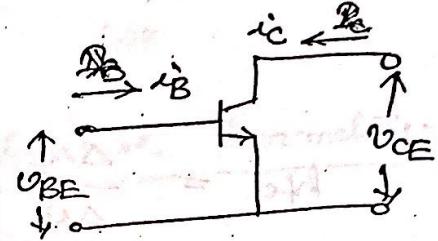
h_{re} , h_{oe} are calculated from the O/P characteristics.

The two equations for the static characteristics of CE

Configuration are

$$V_{BE} = f_1(i_B, V_{CE})$$

$$i_C = f_2(i_B, V_{CE})$$



$$\Delta V_{BE} = \frac{\partial f_1}{\partial i_B} \Delta i_B + \frac{\partial f_1}{\partial V_{CE}} \Delta V_{CE}$$

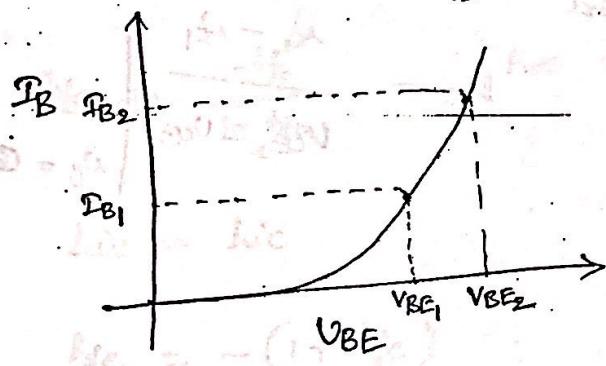
$$\Delta i_C = \frac{\partial f_2}{\partial i_B} \Delta i_B + \frac{\partial f_2}{\partial V_{CE}} \Delta V_{CE}$$

$$\Delta V_{BE} = h_{ie} \Delta i_B + h_{re} \Delta V_{CE}$$

$$\Delta i_C = h_{fe} \Delta i_B + h_{oe} \Delta V_{CE}$$

$$h_{ie} = \frac{\Delta V_{BE}}{\Delta i_B} \Bigg|_{V_{CE}=\text{constant}} = \frac{V_{BE_2} - V_{BE_1}}{i_B_2 - i_B_1} \Bigg|_{V_{CE}=\text{constant}}$$

Consider the I/P characteristics,
 $V_{CE} = \text{constant}$

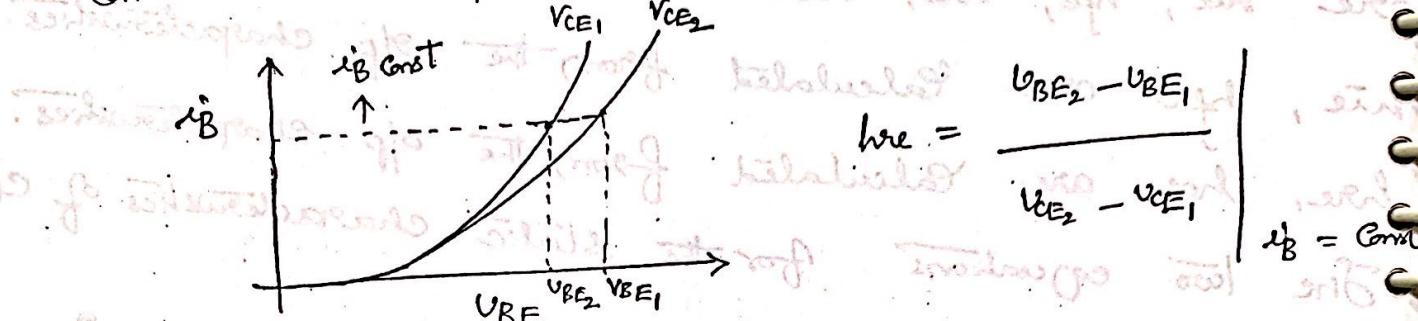


$$\therefore h_{ie} = \frac{V_{BE_2} - V_{BE_1}}{i_B_2 - i_B_1} \Bigg|_{V_{CE}=\text{const.}}$$

$$h_{FE} = \frac{\Delta I_C}{\Delta V_{BE}} \quad |_{V_{CE} = 0} \quad h_{FE} = \frac{V_{CE_2} - V_{CE_1}}{V_B - V_B} \quad |_{I_B = \text{Const}}$$

homogeneous diff. eqn. of AC characteristics for V_{CE} and I_B are

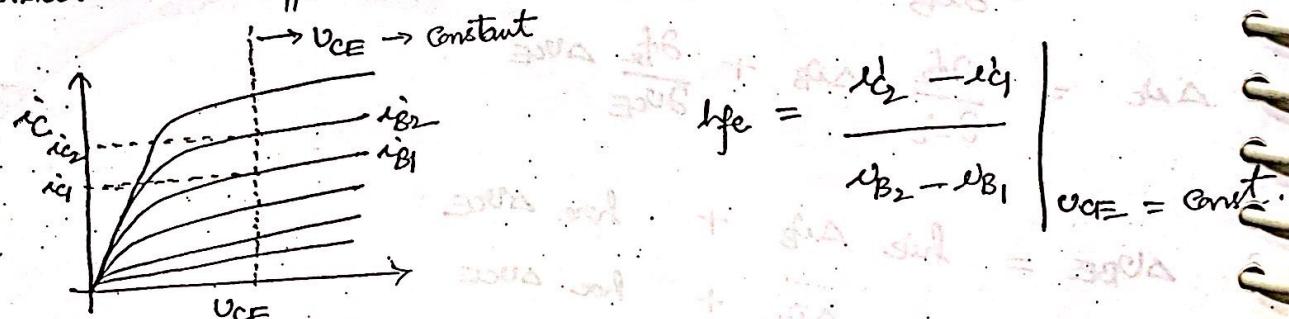
Consider the O/P Characteristics,



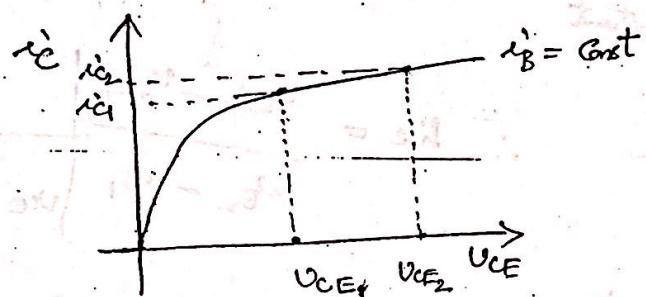
$$h_{FE} = \frac{V_{BE_2} - V_{BE_1}}{V_{CE_2} - V_{CE_1}} \quad |_{I_B = \text{Const}}$$

$$h_{FE} = \frac{\Delta I_C}{\Delta V_B} \quad |_{V_{CE} = 0} \quad = \frac{i_{C2} - i_{C1}}{V_{B2} - V_{B1}} \quad |_{V_{CE} = \text{Const}}$$

Consider the O/P Characteristics,



$$h_{FE} = \frac{\Delta I_C}{\Delta V_{CE}} \quad |_{I_B = 0} \quad = \frac{I_{B2} - I_{B1}}{V_{CE_2} - V_{CE_1}} \quad |_{V_{CE} = \text{Const}} \quad I_B = \text{Constant}$$



$$h_{FE} = \frac{\Delta I_C}{\Delta V_{CE}} \quad |_{I_B = \text{Const}} \quad = \frac{I_{C2} - I_{C1}}{V_{CE_2} - V_{CE_1}} \quad |_{I_B = \text{Const}}$$

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Typical h-parameter Values for a transistor:

Parameter	CE	CB	CC
h_{ie}	$1.1 K\Omega$	21.6Ω	$1.1 K\Omega$
h_{re}	2.5×10^{-4}	2.9×10^{-4}	1
h_{rf}	50	-0.98	-51
h_{oA}	$24 \mu A/V$	$0.49 \mu A/V$	$25 \mu A/V$
Y_{ho}	$40K$	$2.04 M$	$40K$

Approximate Conversion Formulae for hybrid parameters:

$$h_{ic} = h_{ie}$$

$$h_{oc} = 1$$

CE to CC conversion

$$h_{fc} = -(1 + h_{fe})$$

$$h_{oc} = h_{oe}$$

formulae

$$h_{ib} = \frac{h_{ie}}{1 + h_{fe}}$$

$$h_{rb} = \frac{h_{ie} h_{oe}}{1 + h_{fe}} - h_{re}$$

CE to
CB
Conversion
formulae.

$$h_{fb} = \frac{-h_{fe}}{1 + h_{fe}}$$

$$h_{ob} = \frac{h_{oe}}{1 + h_{fe}}$$

$$h_{ie} = \frac{h_{ib}}{1 + h_{fb}}$$

$$h_{re} = \frac{h_{ib} h_{ob}}{1 + h_{fb}} - h_{rb}$$

CB to CE
Conversion formulae

$$h_{fe} = \frac{-h_{fb}}{1 + h_{fb}}$$

$$h_{oe} = \frac{h_{ob}}{1 + h_{fb}}$$

$$h_{ie} = h_{ic}$$

$$h_{re} = 1 - h_{rc}$$

CC to CE
Conversion formulae

$$h_{fe} = -(1 + h_{fc})$$

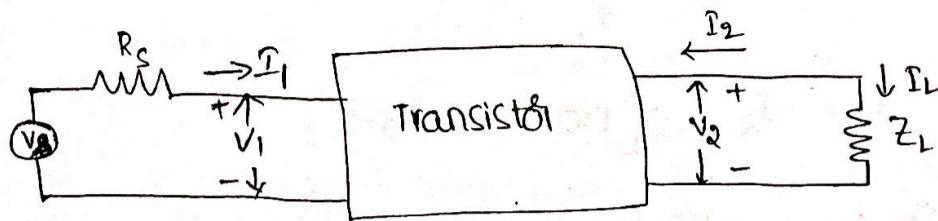
$$h_{oe} = h_{oc}$$

8

Analysis of a general transistor amplifier using h-parameter model (19)

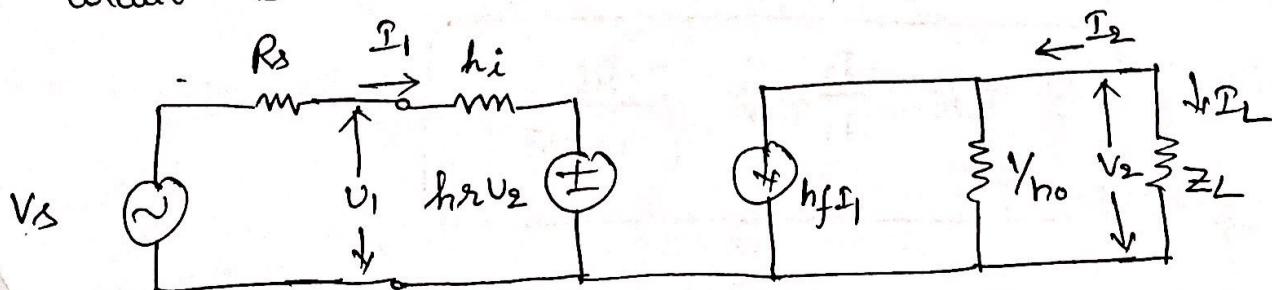
(8)

Derive the expressions for current gain (A_I), input impedance (Z_i), voltage gain (A_v), output Admittance (Y_o) for a general transistor amplifier



The above diagram indicates a transistor to which a signal source V_s is connected at the input, R_s represents the internal Resistance of the signal source. At the output of the transistor a load impedance Z_L connected. Together with V_s and Z_L , the above system acts as an Amplifier.

To analyze the above amplifier, the transistor is replaced with its h-parameter model. The resultant circuit is



current gain (A_I) :-

The h-parameter Equations are,

$$v_1 = h_i I_1 + h_{n1} v_2 \rightarrow ①$$

$$I_2 = h_f I_1 + h_{o1} v_2 \rightarrow ②$$

$$\text{current gain } A_I = \frac{I_L}{I_1}$$

but $I_L = -I_2$ [from the figure]

$$\therefore A_I = -\frac{I_2}{I_1}$$

From Equation ②

$$I_2 = h_f I_1 + h_o v_2 \text{ divide with } I_1$$

$$\frac{I_2}{I_1} = h_f + \frac{h_o v_2}{I_1} \Rightarrow \frac{I_2}{I_1} = h_f + h_o \frac{(I_L Z_L)}{I_1}$$

$$\Rightarrow \frac{I_2}{I_1} = h_f + h_o Z_L \left(-\frac{I_2}{I_1} \right) \Rightarrow \frac{I_2}{I_1} (1 + h_o Z_L) = h_f$$

$$\frac{I_2}{I_1} = \frac{h_f}{1 + h_o Z_L}$$

$$\therefore A_I = -\frac{I_2}{I_1} = -\frac{h_f}{1 + h_o Z_L}$$

2) Input Impedance (z_i) :-

As shown in the figure z_i represents the input impedance seen at the input terminals of the amplifier.

$$z_i = \frac{V_1}{I_1}$$

From equation ①

$$V_1 = h_i I_1 + h_{21} V_2$$

$$\frac{V_1}{I_1} = h_i + h_{21} \frac{V_2}{I_1} \Rightarrow \frac{V_1}{I_1} = h_i + \frac{h_{21} (I_L z_L)}{I_1}$$

$$z_i = h_i + h_{21} A_I z_L$$

3) Voltage Gain (A_v) :-

Voltage Gain excluding R_s is given by

$$A_v = \frac{V_2}{V_1};$$

$$\therefore A_v = \frac{V_2}{V_1} = \frac{I_L z_L}{I_1 z_i} = \frac{A_I z_L}{z_i}$$

$$\therefore A_v = \frac{A_I z_L}{z_i}$$

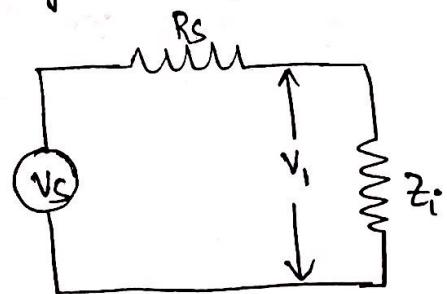
4) Voltage Gain (A_{Vs}) :-

Voltage Gain including R_s is given by

$$A_{Vs} = \frac{V_2}{V_S} = \frac{V_2}{V_1} \cdot \frac{V_1}{V_S}$$

From figure,

$$V_1 = \frac{V_S z_i}{R_s + z_i}$$



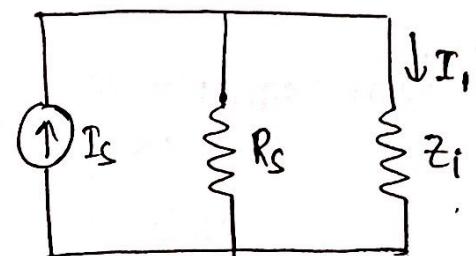
$$\therefore A_{VS} = A_V \cdot \frac{Z_i}{R_S + Z_i}$$

5) Current gain (A_{IS}) :

current gain including the effect of R_S

is given by

$$A_{IS} = \frac{I_L}{I_S} = \frac{I_L}{I_I} \cdot \frac{I_I}{I_S}$$



$$\therefore A_{IS} = A_I \cdot \frac{R_L}{R_S + Z_i}$$

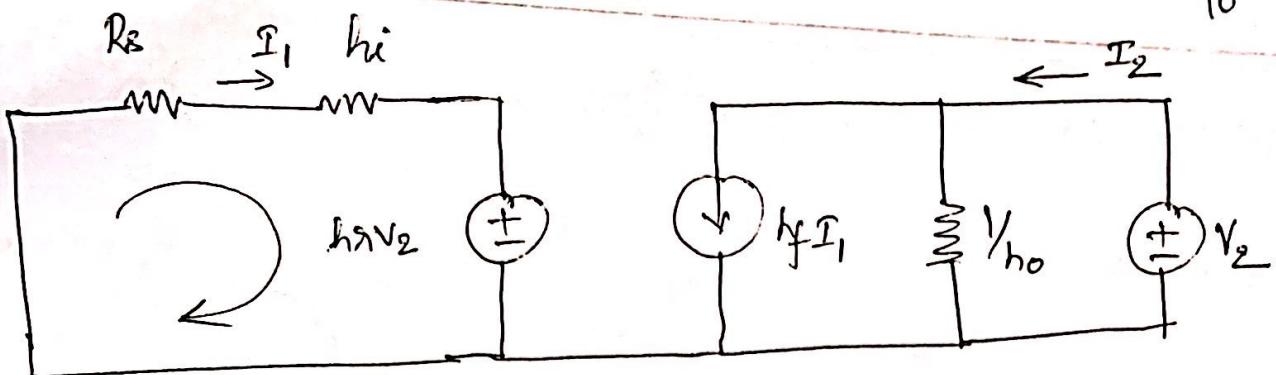
$$I_I = \frac{I_S \cdot R_S}{R_S + Z_i}$$

$$\Rightarrow \frac{I_I}{I_S} = \frac{R_S}{R_S + Z_i}$$

$$\therefore A_{IS} = A_I \cdot \frac{R_S}{R_S + Z_i}$$

6) Output Admittance (γ_0) : (output Impedance $Z_0 = 1/\gamma_0$)

To determine γ_0 , we shall equate the voltage source V_S to zero; Remove the load resistance Z_L and connect an independent voltage source V_2 as shown in the following figure, then $\gamma_0 = I_2/V_2$;



Applying KVL to the Input loop,

$$R_s I_1 + h_i I_1 + h_r V_2 = 0$$

$$\Rightarrow I_1 (R_s + h_i) = -h_r V_2$$

$$\Rightarrow I_1 = \frac{-V_2 h_r}{(R_s + h_i)}$$

$$\Rightarrow \frac{I_1}{V_2} = \frac{-h_r}{R_s + h_i}$$

From Equation ②

$$I_2 = h_f I_1 + h_o V_2$$

$$\frac{I_2}{V_2} = h_f \frac{I_1}{V_2} + h_o$$

$$\therefore h_o = \frac{-h_f h_r}{R_s + h_i} + h_o$$

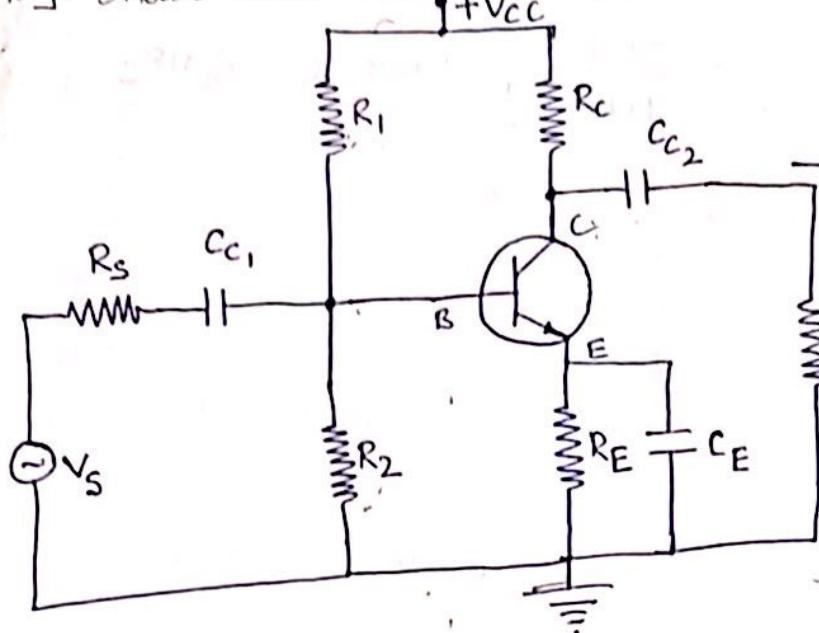
$$h_o = h_o - \frac{h_f h_r}{R_s + h_i}$$

Comparision of various Amplifiers :-

	CE	CB	CC
Voltage Gain	High	High	unity
Current Gain	High	unity	high
Input Impedance	Medium	Low	high
Output Impedance	Medium	High	Low
Power Gain	Very high	Medium	Medium

CE Amplifiers Analysis using (21) h-Parameter model :

→ Fig. shows true circuit diagram of CE amplifiers



$R_1, R_2, R_C \& R_E \Rightarrow$ Biasing Resistors

$+V_{CC} \Rightarrow$ Supply Voltage

$R_s \Rightarrow$ Source Resistance

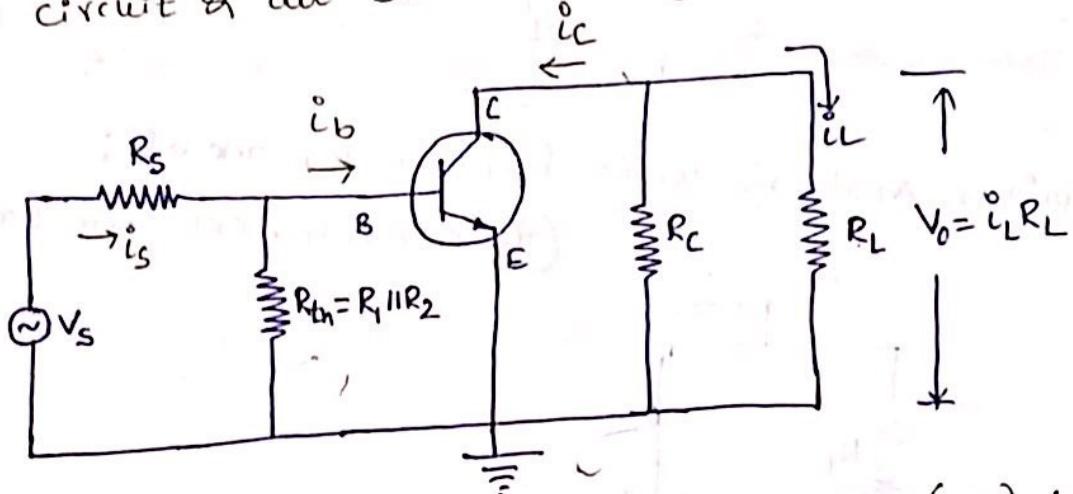
$R_L \Rightarrow$ Load Resistance

$C_{c1} \& C_{c2} \Rightarrow$ Coupling Capacitors

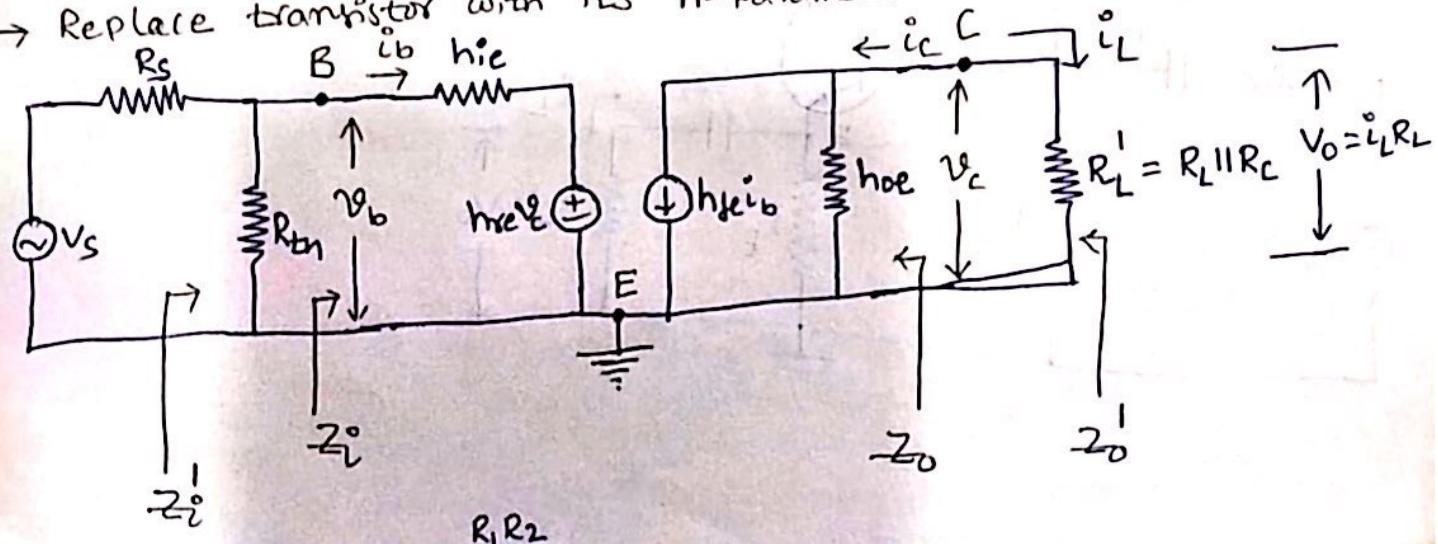
$C_E \Rightarrow$ Emitter bypass capacitor

$V_s \Rightarrow$ I/P ac source

→ Draw ac equivalent circuit by replacing all capacitors by short circuit & all DC sources by short circuit for ac analysis.



→ Replace transistor with its h-Parameter model (CE) for analysis



Note: Procedure for calculating A_I , Z_i , A_v , Z_o are same as the General Analysis (only difference is R_L replaced by R_L' and R_S replaced by R_S').

$$\textcircled{1} \text{ Current Gain } A_I = \frac{\dot{i}_L}{\dot{i}_b} = -\frac{\dot{i}_C}{\dot{i}_b} = \frac{-h_{fe}}{1+h_{fe} R_L'} \quad \text{where } R_L' = R_L || R_C = \frac{R_L R_C}{R_L + R_C}$$

$$\textcircled{2} \text{ i/p impedance } Z_i = \frac{V_b}{\dot{i}_b} = h_{ie} + h_{re} A_I R_L'$$

$$\textcircled{3} \text{ voltage gain } A_v = \frac{A_I R_L'}{Z_i} = \frac{V_o}{V_b}$$

$$\textcircled{4} \text{ o/p admittance } Y_o = h_{oe} - \frac{h_{re} h_{fe}}{h_{ie} + R_S} \quad \text{where } R_S' = R_S || R_{th} = \frac{R_S R_{th}}{R_S + R_{th}}$$

$$\textcircled{5} \text{ over-all voltage gain } A_{vs} = \frac{V_o}{V_s} = \frac{A_v Z_i}{Z_i + R_S} \quad (\text{including } R_S)$$

$$\textcircled{6} \text{ over-all current gain } A_{IS} = \frac{\dot{i}_L}{\dot{i}_S} = \frac{A_I R_S}{Z_i + R_S} \quad (\text{including } R_S)$$

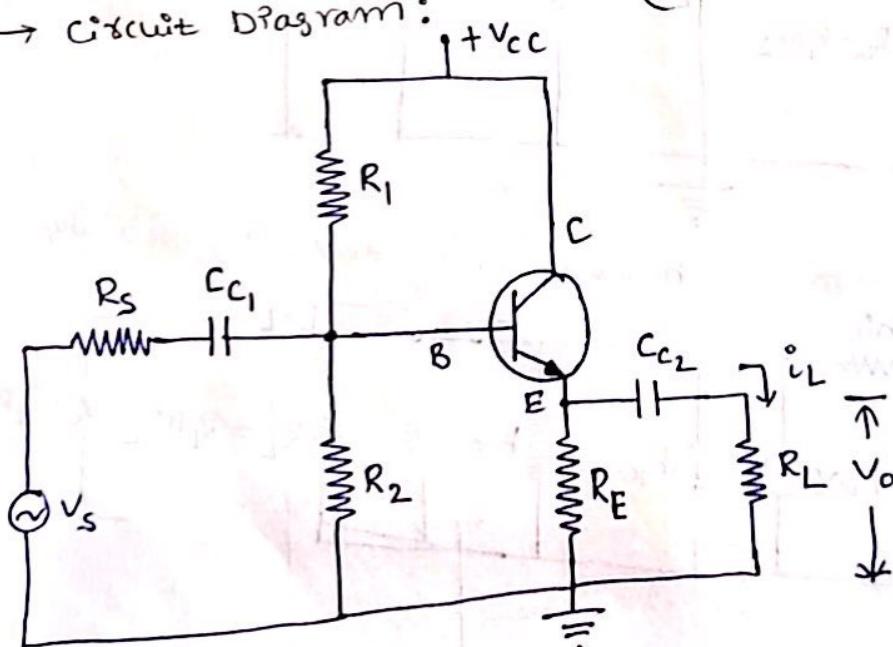
$$\textcircled{7} \quad Z_i' = Z_i || R_{th} \quad \textcircled{8} \quad Z_o' = Z_o || R_L$$

Note: Similar procedure for CC Amplifier & CB Amplifiers.

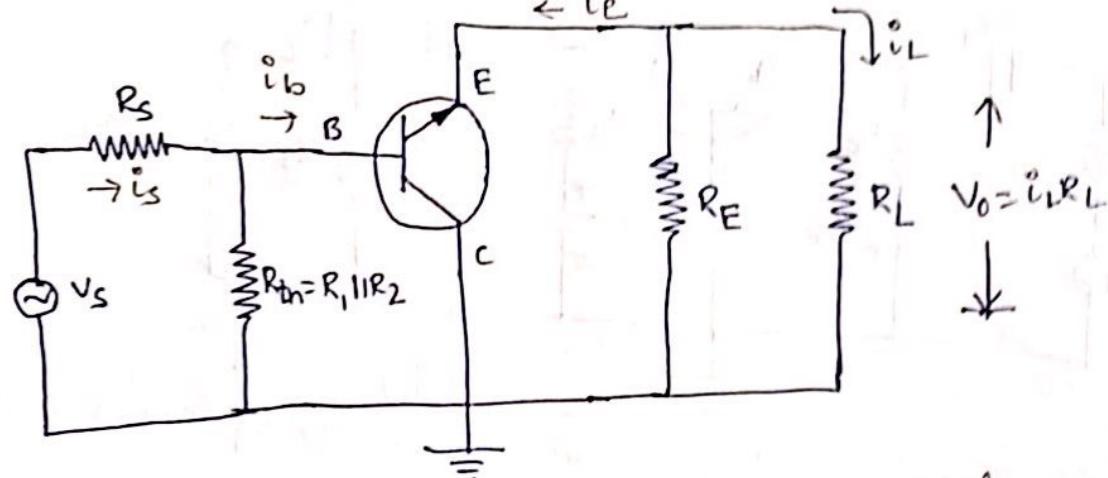
CC Amplifier Analysis using h-parameter model;

(In CC Amplifier ext there is no R_C)

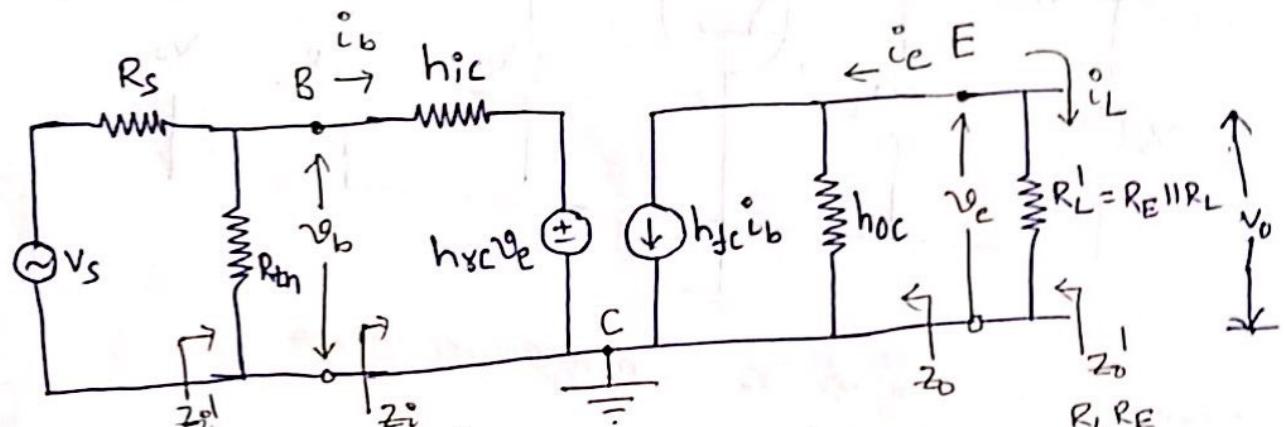
→ Circuit Diagram:



→ AC equivalent circuit (All Capacitors & DC Sources by short circuit) (2A)



→ Replace transistor by its CC h-parameter model



$$\textcircled{1} \quad A_I = \frac{i_L}{i_b} = \frac{-i_e}{i_b} = \frac{-h_{fc}}{1 + h_{oc} R'_L} \quad \text{where } R'_L = R_L \parallel R_E = \frac{R_L R_E}{R_L + R_E}$$

$$\textcircled{2} \quad Z_i = \frac{v_b}{i_b} = h_{ic} + h_{yc} A_I R'_L$$

$$\textcircled{3} \quad A_v = \frac{v_o}{v_b} = \frac{A_I R'_L}{Z_i}$$

$$\textcircled{4} \quad Y_0 = \frac{i_e}{v_c} = h_{oc} - \frac{h_{yc} h_{fc}}{h_{ic} + R'_S}$$

where $R'_S = R_S \parallel R_{th}$.

$$Z_o = \frac{1}{Y_0}$$

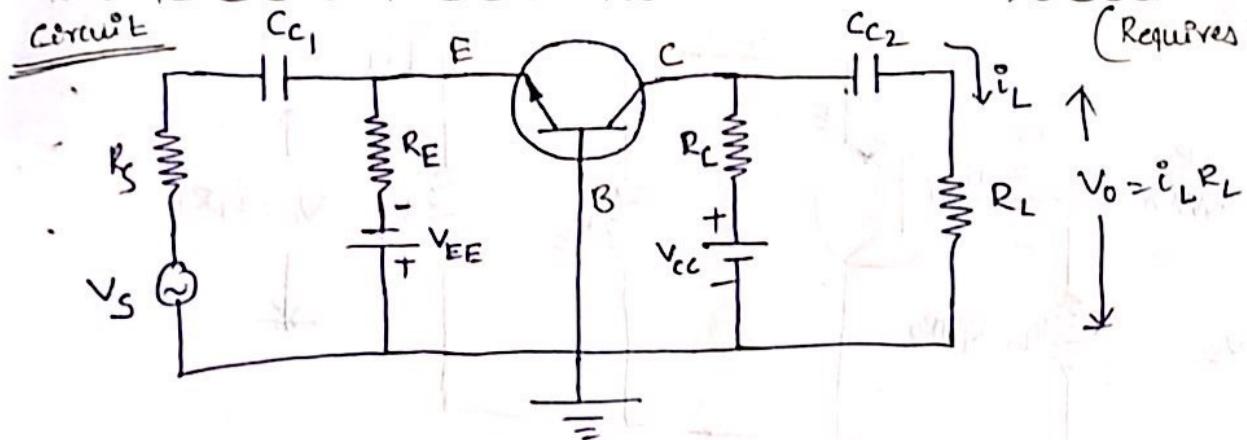
$$\textcircled{5} \quad A_{VS} = \frac{v_o}{v_s} = \frac{A_v Z_i}{Z_i + R_S}$$

$$\textcircled{6} \quad A_{IS} = \frac{i_L}{i_s} = \frac{A_I R_S}{R_S + Z_i}$$

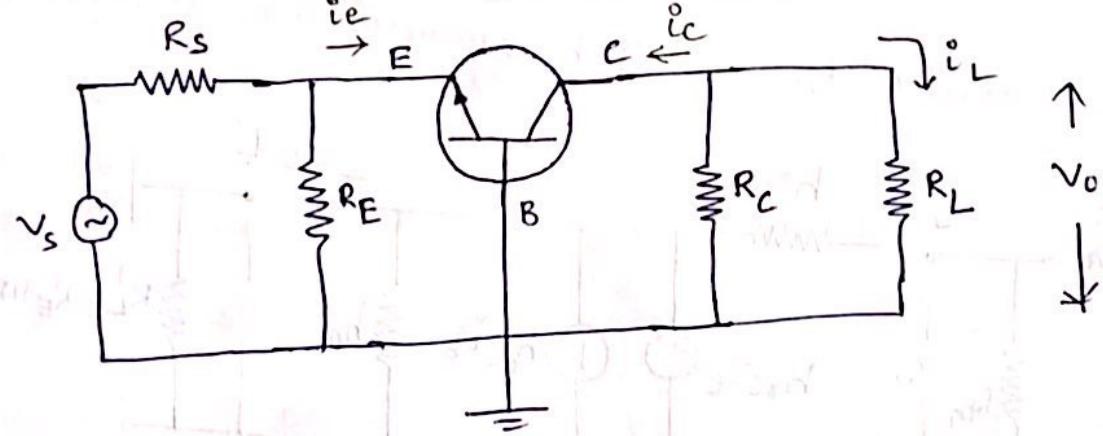
$$\textcircled{7} \quad Z'_i = Z_i \parallel R_{th}$$

$$\textcircled{8} \quad Z'_o = Z_o \parallel R_L$$

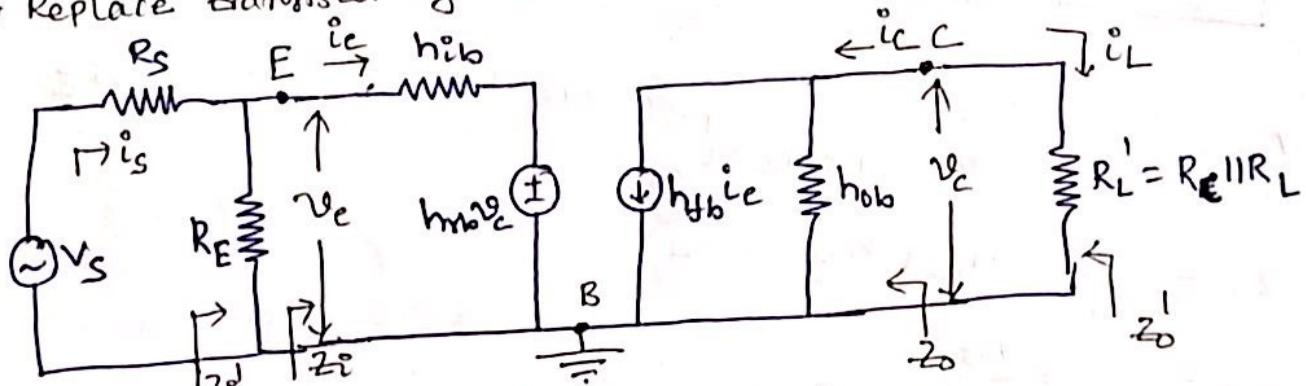
CB Amplifier Analysis using (23) h-parameter model



→ AC equivalent circuit (Capacitors & DC Sources by short circuit)



→ Replace transistor by its CB h-parameter model



$$\textcircled{1} \quad A_I = \frac{i_L}{i_e} = -\frac{i_C}{i_e} = \frac{-h_{fb}}{1 + h_{ob} R_L'} \quad \text{where } R_L' = R_L || R_E$$

$$\textcircled{2} \quad Z_i = \frac{v_e}{i_e} = h_{ie} + h_{re} A_I R_L'$$

$$\textcircled{3} \quad A_V = \frac{A_I R_L'}{Z_i}$$

$$\textcircled{4} \quad Y_0 = h_{ob} - \frac{h_{re} h_{fb}}{h_{ie} + R_s'} \quad \text{where } R_s' = R_s || R_E$$

$$\textcircled{5} \quad A_{VS} = \frac{A_V Z_i}{Z_0 + R_C} \quad \textcircled{6} \quad A_{IS} = \frac{A_I R_S}{R_S + Z_i}$$

$$\textcircled{7} \quad Z_i' = Z_i || R_E$$

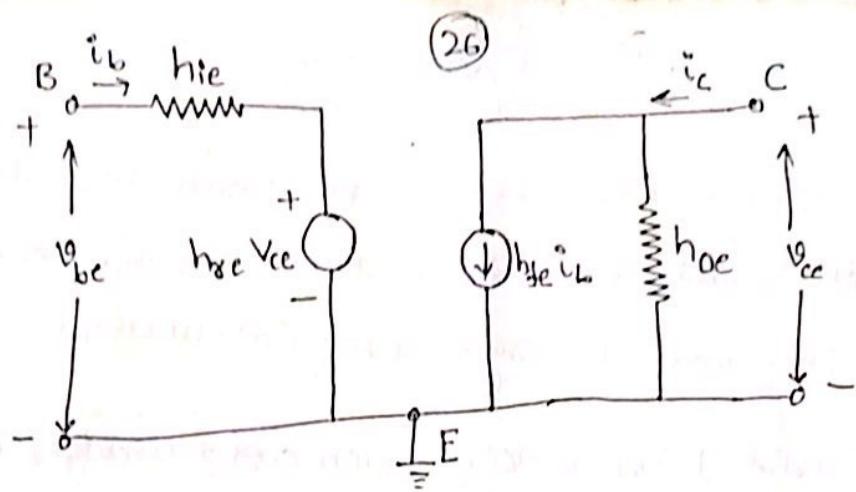
$$\textcircled{8} \quad Z_0' = Z_0 || R_L'$$

(25) Simplified Hybrid Model / Approximate Model :- (14) I

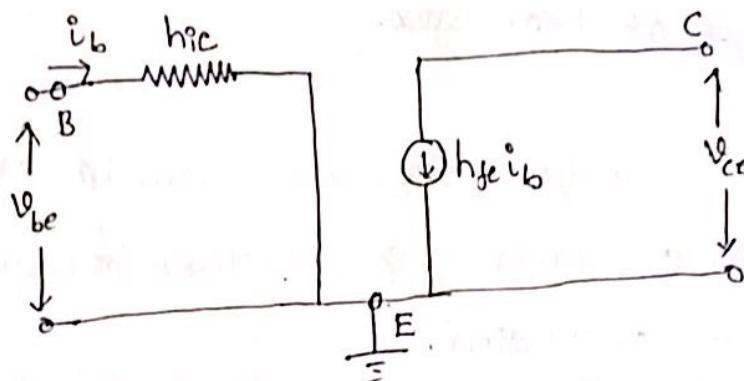
- In most practical cases it is appropriate to obtain approximate values of A_I , A_V , R_i and R_o rather than to carry out the more lengthy exact calculations.
- We are justified in making such approximations because the h-parameters themselves usually vary widely for the same type of transistor.
- The behaviour of a transistor circuit can be obtained from a simple approximate solution than from a more lengthy exact calculation.
- Two of the four h-parameters, h_{ie} & h_{re} are sufficient for the approximate analysis of low frequency transistor circuits, provided that the load resistance is small enough to satisfy the condition

$$h_{re} R_L \ll 0.1$$

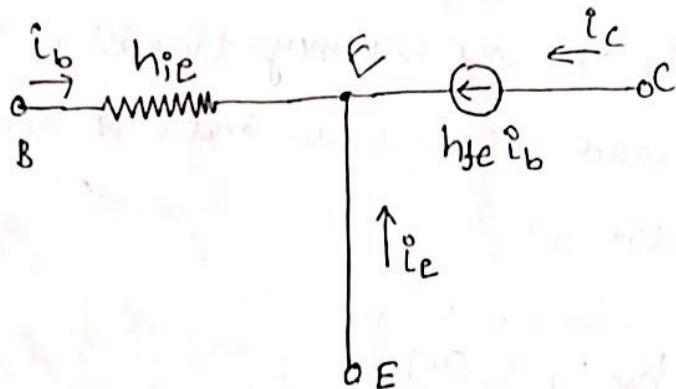
- If the above condition is satisfied, we can neglect h_{ie} & h_{re} .
- The simplified model is shown in fig. The equivalent circuit may be used for any configuration by grounding the appropriate node.



Exact Model



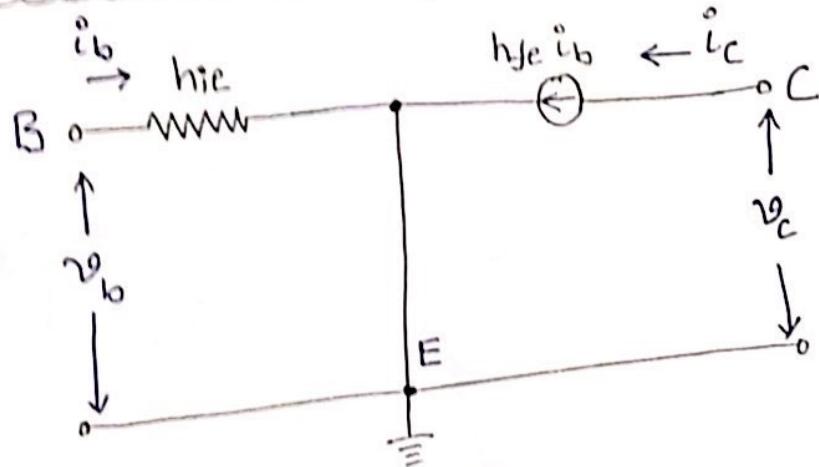
Approximate model / Simplified model



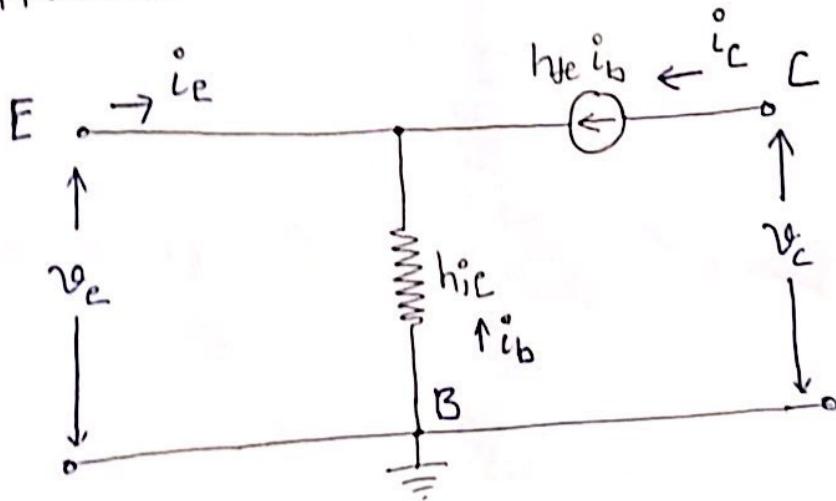
Approximate model which may be used for all three configurations CE, CC and CB.

→ By grounding the appropriate terminal, we can draw approximate or simplified model for any configuration.

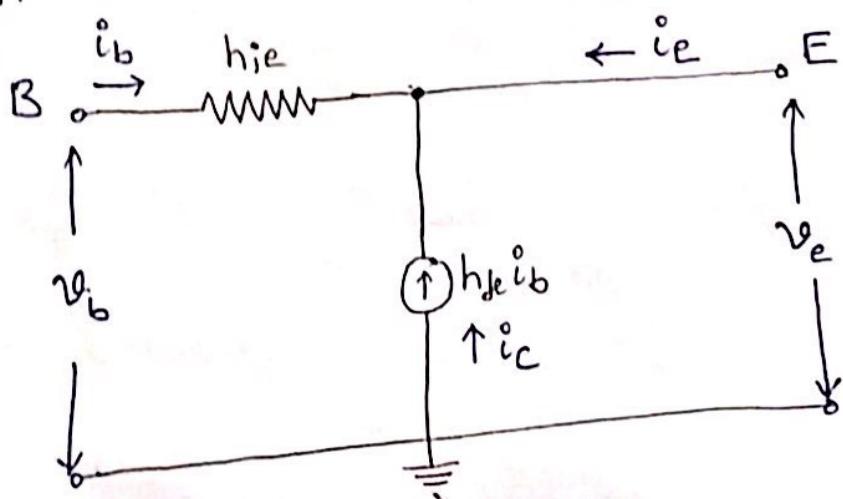
CE Approximate model / Simplified model :



CB approximate model :



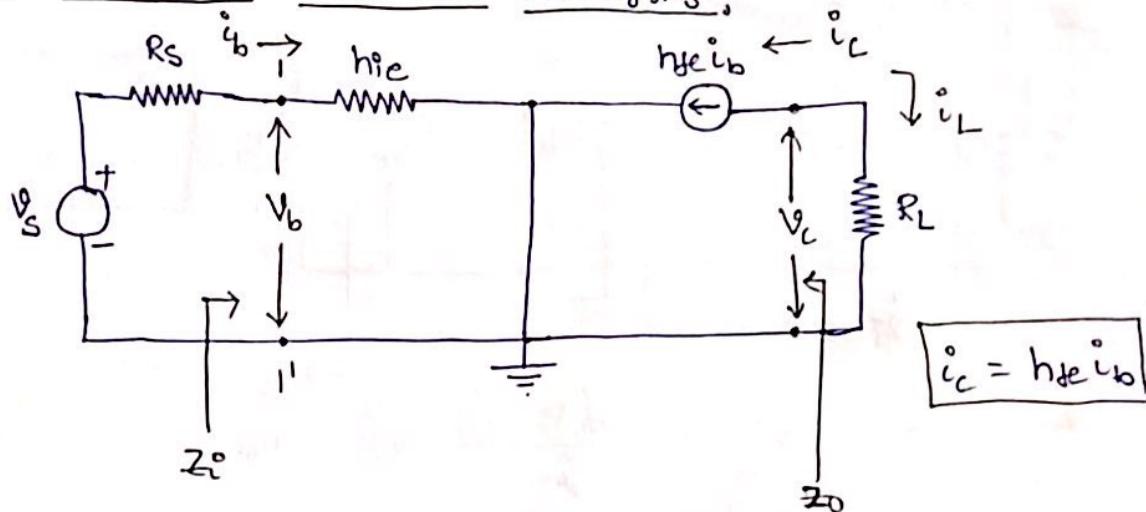
CC approximate model :



(28)

Simplified hybrid model / Approximate model Analysis:

① CE Amplifier simplified Analysis:



$$A_I = \frac{\dot{i}_L}{\dot{i}_b} = -\frac{\dot{i}_c}{\dot{i}_b} = -\frac{h_{fe} \dot{i}_b}{\dot{i}_b} = -h_{fe}$$

$$A_I = -h_{fe}$$

$$Z_i = \frac{V_b}{\dot{i}_b} = \frac{h_{fe} \dot{i}_b}{\dot{i}_b} = h_{fe}$$

$$Z_i = h_{fe}$$

$$A_V = \frac{V_c}{V_b} = \frac{\dot{i}_L R_L}{h_{fe} \dot{i}_b} = \frac{-\dot{i}_c R_L}{\dot{i}_b h_{fe}} = \frac{A_I R_L}{h_{fe}} = \frac{A_I R_L}{Z_i}$$

$$A_V = \frac{A_I R_L}{Z_i}$$

$$Y_o = \frac{\dot{i}_c}{V_c} = \frac{\dot{i}_c}{\dot{i}_L R_L} = \frac{\dot{i}_c}{-\dot{i}_c R_L} = \frac{1}{R_L}$$

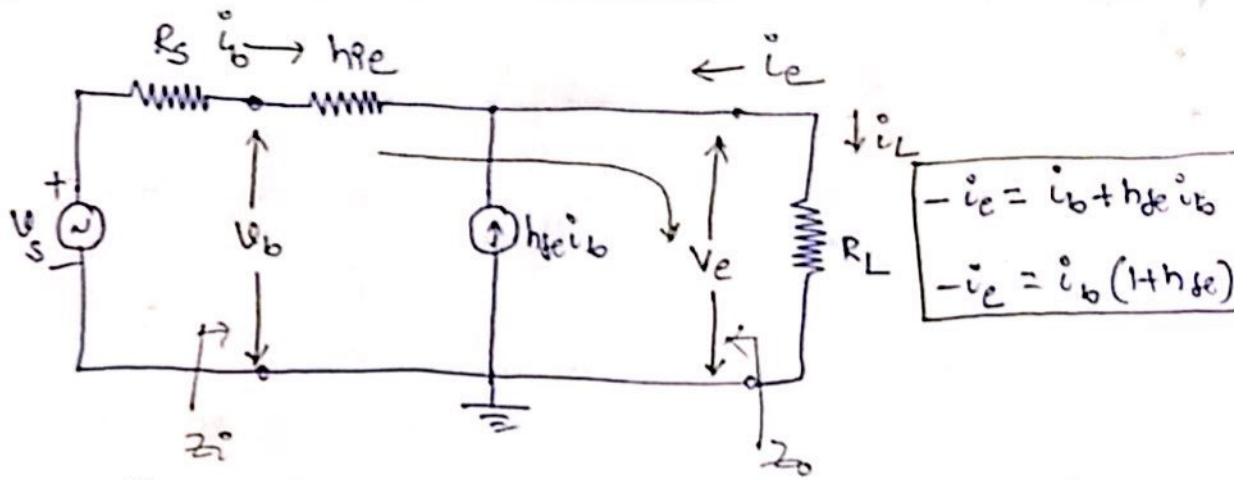
To find o/p admittance setting

~~Assume~~ $V_s = 0$ & $R_L = \infty$

$$Y_o = \frac{1}{\infty} = 0$$

$$Z_i = \frac{1}{Y_o} = \infty$$

CC Amplifiers Simplified Analysis:



$$A_I = \frac{\dot{V}_o}{\dot{V}_b} = -\frac{\dot{i}_e}{\dot{i}_b} = \frac{\dot{i}_b(1+h_{fe})}{\dot{i}_b} = 1 + h_{fe}$$

$$\boxed{A_I = (1 + h_{fe})}$$

$$\begin{aligned} Z_i &= \frac{V_b}{\dot{i}_b} = \frac{h_{ie}\dot{i}_b + V_e}{\dot{i}_b} \\ &= \frac{h_{ie}\dot{i}_b + \dot{i}_L R_L}{\dot{i}_b} \\ &= h_{ie} + \frac{\dot{i}_L}{\dot{i}_b} R_L \\ &= h_{ie} + A_I R_L \end{aligned}$$

$$\boxed{(Z_i)_{CC} > (Z_i)_{CE}}$$

$$A_V = \frac{V_o}{V_b} = \frac{V_e}{h_{ie}\dot{i}_b + V_e} = \frac{\dot{i}_L R_L}{h_{ie}\dot{i}_b + \dot{i}_L R_L}$$

Divide numerator & denominator by \dot{i}_b

$$A_V = \frac{\frac{\dot{i}_L \cdot R_L}{\dot{i}_b}}{h_{ie} + \frac{\dot{i}_L}{\dot{i}_b} R_L} = \frac{A_I R_L}{h_{ie} + A_I R_L}$$

$$\boxed{A_V = \frac{(1 + h_{fe}) R_L}{h_{ie} + (1 + h_{fe}) R_L}}$$

$$(1+h_{fe})R_L \gg h_{ie}, \text{ so } \quad (29) \quad (30)$$

$$A_v = \frac{(1+h_{fe}) R_L}{(1+h_{fe}) R_L} \approx 1$$

$$\therefore Z_0 = \frac{V_e}{i_e}$$

$$V_e = h_{ie}(-i_b) + R_s(-i_b) \quad \text{As } V_s = 0$$

$$V_e = -i_b(h_{ie} + R_s)$$

Divide on both sides by i_e

$$\frac{V_e}{i_b} = -\frac{i_b}{i_e} (h_{ie} + R_s)$$

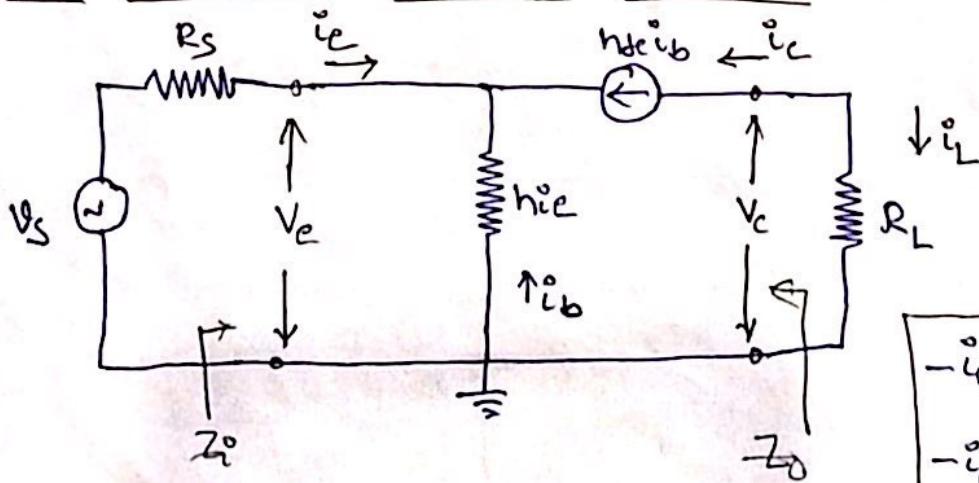
$$Z_0 = \frac{1}{A_v} (h_{ie} + R_s)$$

$$Z_0 = \frac{h_{ie} + R_s}{1 + h_{fe}}$$

$$Y_0 = \frac{1 + h_{fe}}{h_{ie} + R_s}$$

CC OIP resistance is less

CB Amplifier Simplified Analysis:



$$-i_e = h_{de}i_b + i_b$$

$$-i_e = (1 + h_{de})i_b$$

$$A_I = \frac{\dot{i}_L}{\dot{i}_e} = -\frac{\dot{i}_c}{\dot{i}_e} \stackrel{(31)}{=} \frac{+h_{fe}\dot{x}_b}{+(1+h_{fe})\dot{x}_b}$$

$$\boxed{A_I = \frac{h_{fe}}{1+h_{fe}}} \quad A_I < 1$$

$$Z_i^o = \frac{V_e}{\dot{i}_e} = \frac{f h_{ie} \dot{x}_b}{+(1+h_{ie})\dot{x}_b} = \frac{h_{ie}}{1+h_{ie}}$$

$$\boxed{Z_i^o = \frac{h_{ie}}{1+h_{ie}}}$$

$$A_V = \frac{V_c}{V_e} \quad \text{with } \cancel{\frac{i_L R_L}{h_{fe} \dot{x}_b}} \times \cancel{\frac{-\dot{i}_c R_L}{\dot{x}_b h_{ie}}}$$

$$= \frac{i_L R_L}{V_e} = -\frac{\dot{i}_c R_L}{V_e}$$

Divide NV & DV by \dot{i}_e

$$A_V = \frac{-\frac{\dot{i}_c R_L}{\dot{i}_e}}{\frac{V_e}{\dot{i}_e}} = \frac{A_I R_L}{Z_i^o}$$

$$\leq \frac{h_{fe} R_L}{(1+h_{fe})}$$

$$\frac{h_{fe}}{(1+h_{fe})}$$

$$\boxed{A_V = \frac{h_{fe} R_L}{h_{fe}}}$$

$$Z_o = \frac{V_c}{\dot{i}_c} = -\frac{\dot{i}_c R_L}{\dot{i}_c} = R_L$$

To find Z_o set $V_S = 0$ & $R_L = \infty$, so

$$\boxed{Z_o = R_L = \infty}$$

$$\boxed{Y_o = \frac{1}{R_L} = 0}$$

JFET Low Frequency Small Signal Model :-

(General)

- The linear small-signal equivalent circuit for the FET can be obtained in a manner analogous to that used to derive the corresponding model for a transistor.
- we can express the drain current i_D as a function f of the gate voltage v_{GS} and drain voltage v_{DS} by

$$i_D = f(v_{GS}, v_{DS}) \quad \text{--- } ①$$

→ Now, we define the three FET parameters, namely the transconductance g_m , dynamic drain resistance r_d , and amplification factor u .

→ If both the gate and drain voltages are variable, the change in drain current is given approximately by the first two terms in the Taylor's series expansion of eq ①, i.e

$$\Delta \dot{i}_D = \left. \frac{\partial \dot{i}_D}{\partial V_{GS}} \right|_{V_{DS}} \cdot \Delta V_{GS} + \left. \frac{\partial \dot{i}_D}{\partial V_{DS}} \right|_{V_{GS}} \Delta V_{DS}$$

— ②

→ Using the conventional small signal notation, $\Delta \dot{i}_D, \Delta V_{GS}, \Delta V_{DS}$ may be replaced respectively by i_d, v_{gs} and v_{ds} . So eq ② becomes

$$i_d = g_m v_{gs} + \frac{1}{r_d} \cdot v_{ds} \quad — ③$$

where

$$g_m = \left. \frac{\partial \dot{i}_D}{\partial V_{GS}} \right|_{V_{DS}}$$

In BJT, the relation b/w α & i_{HP} is given by β , where α is in FET this is

$$= \left. \frac{\Delta \dot{i}_D}{\Delta V_{GS}} \right|_{V_{DS}}$$

given by transconductance factor g_m .

$$= \left. \frac{i_d}{v_{gs}} \right|_{V_{DS}}$$

- g_m is called mutual conductance or transconductance.
 - It is also often designated by y_{fs} or g_{fs} and called the Common Source forward transadmittance.
 - The second parameter γ_d in eq ③ is the drain or o/p resistance and is defined by
- $$\gamma_d = \left. \frac{\partial V_{DS}}{\partial i_d} \right|_{V_{GS}} = \left. \frac{\Delta V_{DS}}{\Delta i_d} \right|_{V_{GS}} = \left. \frac{V_{DS}}{i_d} \right|_{V_{GS}}$$
- The reciprocal of γ_d is the drain Conductance g_d . It is also designated by y_{os} and g_{os} and called the Common Source o/p Conductance.
 - γ_d determines the o/p impedance Z_o of the JFET amplifier
 - Amplification factor u for an FET is defined as

$$u = - \left. \frac{\partial V_{DS}}{\partial V_{GS}} \right|_{I_D}$$

$$= - \left. \frac{\Delta V_{DS}}{\Delta V_{GS}} \right|_{I_D}$$

$$= - \left. \frac{V_{DS}}{V_{GS}} \right|_{i_d = 0}$$

→ Now, if V_{ds} and V_{gs} are so varied that I_d remains unaltered i.e. $i_d = 0$, then eq ③ becomes

$$0 = g_m V_{gs} + \frac{1}{Y_d} \cdot V_{ds}$$

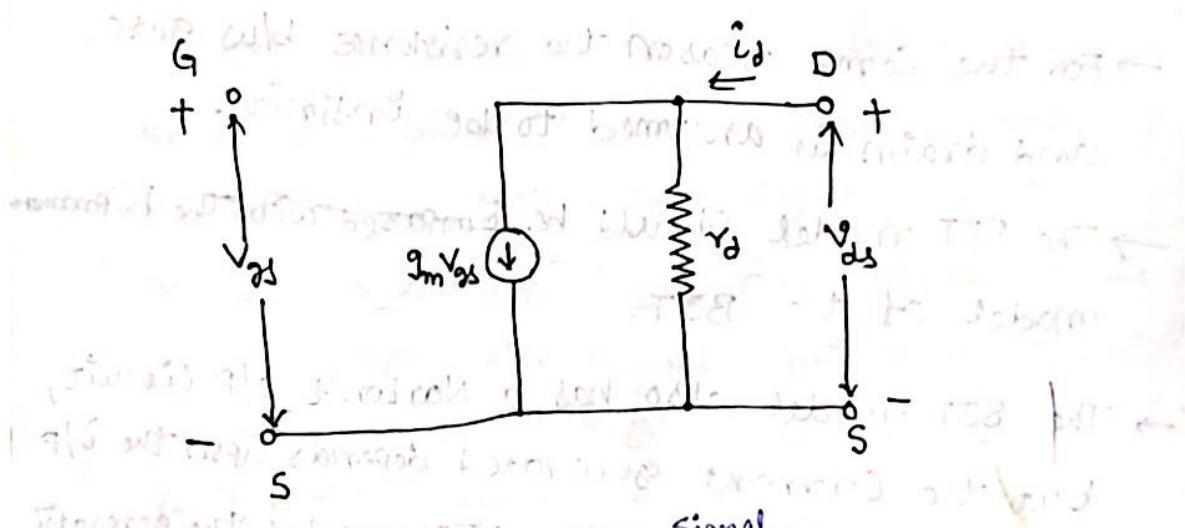
$$g_m V_{gs} = -\frac{V_{ds}}{Y_d}$$

$$g_m \cdot Y_d = -\frac{V_{ds}}{V_{gs}} \quad |_{i_d=0}$$

$$\boxed{g_m \cdot Y_d = \mu}$$

The FET Model :- (ac equivalent circuit)

→ A circuit which satisfies eq ③ is indicated in fig. i.e. the low frequency small signal model.



→ This low frequency small model has a Norton's Op circuit with a dependent current generator whose current is proportional to the gate to source voltage.

→ The proportionality factor is the transconductance g_m , which is consistent with the definition of g_m in below eq.

$$g_m = \frac{i_d}{v_{gs}} \Big| v_{ds}$$

→ The O/P resistance is r_o which is consistent with the definition of eq. below

$$r_o = \frac{v_{ds}}{i_d} \Big| v_{gs}$$

→ The i/p resistance b/w gate and source is infinite, since the reverse biased gate takes no current.

→ For the same reason the resistance b/w gate and drain is assumed to be infinite.

→ The FET model should be compared with the h-parameter model of the BJT.

→ The BJT model also has a Norton's O/P circuit, but the current generated depends upon the i/p current, whereas in the FET model the generated current depends upon the i/p voltage.

→ Note that there is no feedback at low frequencies from O/P to i/p in the FET, whereas such feedback

exists in the bipolar transistor through the parameter β .

- observe that the high (almost infinite) i/p resistance of the FET is replaced by an i/p resistance of about 1k for a CE amplifier.
- In summary, the field-effect transistor is a much more ideal amplifier than the conventional transistor at low frequencies.
- unfortunately, this is not true beyond the audio range.

Approximate FET model :-

- when the value of external drain resistance R_D is very small as compared to the value of o/p impedance represented by r_d , it is possible to replace r_d by open circuit. This gives us approximate ac equivalent circuit of JFET amplifier as shown in fig.

