

Sky130RTLDesignAndSynthesisWorkshop Installation:

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See snap info gh for additional versions.  
harini@harini-VirtualBox:~/VLSI$ git clone https://github.com/kunalg123/sky130RTLDesignAndSynthesisWorkshop.git  
Cloning into 'sky130RTLDesignAndSynthesisWorkshop'...  
remote: Enumerating objects: 417, done.  
remote: Counting objects: 100% (69/69), done.  
remote: Compressing objects: 100% (52/52), done.  
remote: Total 417 (delta 19), reused 47 (delta 12), pack-reused 348 (from 1)  
Receiving objects: 100% (417/417), 7.79 MiB | 3.30 MiB/s, done.  
Resolving deltas: 100% (242/242), done.  
harini@harini-VirtualBox:~/VLSI$ ls  
sky130RTLDesignAndSynthesisWorkshop  vsdflow  
harini@harini-VirtualBox:~/VLSI$ ^C  
harini@harini-VirtualBox:~/VLSI$ cd sky130RTLDesignAndSynthesisWorkshop  
harini@harini-VirtualBox:~/VLSI/sky130RTLDesignAndSynthesisWorkshop$ ls  
DC_WORKSHOP  lib  my_lib  README.md  verilog_files  yosys_run.sh  
harini@harini-VirtualBox:~/VLSI/sky130RTLDesignAndSynthesisWorkshop$
```

Files In the Repo

My_lib : directories => lib ; Verilog_model

Lib : Sky130 standard cell library

Verilog_model : standard cell Verilog models in the lib

Verilog_files : contains lab experiments, Verilog source files, test bench files.