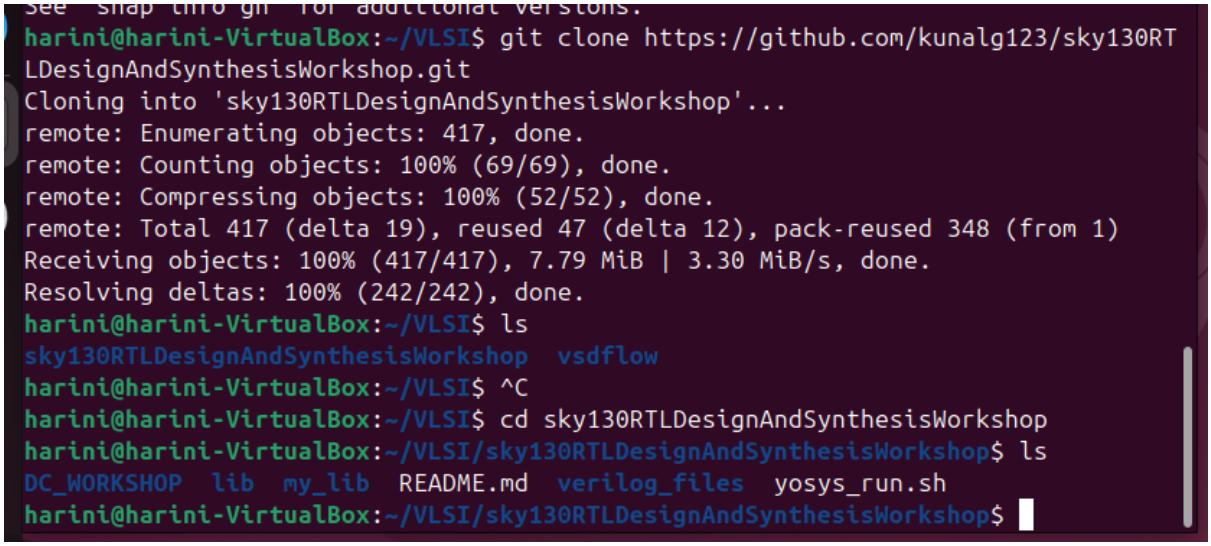
Sky130RTLDesignAndSynthesisWorkshop Installation:



Files In the Repo

My_lib : directories => lib ; Verilog_model

Lib : Sky130 standard cell library

Verilog_model : standard cell Verilog models in the lib

Verilog_files : contains lab experiments, Verilog source files, test bench files.