

LAB 2

Accessing the verilog files:

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harini@harini-VirtualBox: ~/VLSI/sky130RTLDesignAndSynthesisWorkshop/verilog_files
DC_WORKSHOP lib my_lib README.md verilog_files yosys_run.sh
harini@harini-VirtualBox: ~/VLSI/sky130RTLDesignAndSynthesisWorkshop $ cd verilog_files
harini@harini-VirtualBox: ~/VLSI/sky130RTLDesignAndSynthesisWorkshop/verilog_files $ ls
bad_case_net.v      partial_case_assign.v
bad_case.v          pattern_detect_fsm_bad_style.v
bad_counter.v       pattern_detect_fsm.v
bad_latch_2.v       rca.v
bad_latch_net.v     ripple_counter.v
bad_latch.v         tb_bad_case.v
bad_mux_net.v       tb_bad_counter.v
bad_mux.v           tb_bad_latch2.v
bad_shift_reg2.v    tb_bad_latch.v
bad_shift_reg.v      tb_bad_mux.v
blocking_caveat_net.v  tb_bad_shift_reg2.v
blocking_caveat.v    tb_bad_shift_reg.v
comp_case.v          tb_blocking_caveat.v
counter_opt2.v        tb_comp_case.v
counter_opt.v         tb_counter_opt.v
demux_case.v          tb_demux_case.v
demux_generate.v     tb_demux_generate.v
dff_ares.net.v        tb_dff_asyncncs_syncres.v
dff_asyncncs.net.v    tb_dff_asyncncs.v
dff_asyncncs_syncres.v  tb_dff_async_set.v
dff_asyncncs.v        tb_dff_const1.v
dff_async_set.v       tb_dff_const2.v
dff_const1.v         tb_dff_const3.v
dff_const2.v         tb_dff_const4.v
dff_const3.v         tb_dff_const5.v
dff_const4.v         tb_dff_syncncs.v
dff_const5.v         tb_good_counter.v

```

Command for loading the design file and the testbench to the IVerilog:

Iverilog good_mux.v tb_good_mux.v

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    opt_check2.v      upcntr.v
    opt_check3.v      up_dn_cntr.v
    opt_check4.v      up_dn_cntr_with_load.v
    harini@harini-VirtualBox: ~/JLS/sky130RTLDesignAndSynthesisWorkshop/verilog_files$ lverlog good_mux.v tb_good_mux.v
    harini@harini-VirtualBox: ~/JLS/sky130RTLDesignAndSynthesisWorkshop/verilog_files$ ls
a_out      dff_const2.v      partial_case_assign.v      tb_good_latch.v
bad_case_net.v  dff_net.v          pattern_detect_fsm_bad_style.v  tb_good_mux.v
bad_case.v     dff_syncrs.v       pattern_detect_fsm.v         tb_good_shift_reg.v
bad_counter.v  fa.v               rca.v                        tb_incomp_case.v
bad_latch_2.v  good_counter.v     ripple_counter.v            tb_incomp_if2.v
bad_latch_net.v  good_latch.v       tb_bad_case.v               tb_incomp_if.v
bad_latch.v     good_mux_netlist.v  tb_bad_counter.v           tb_multiple_modules.v
bad_mux_net.v   good_mux.v         tb_bad_latch2.v            tb_mux_generate.v
bad_mux.v       good_shift_reg.v   tb_bad_latch.v             tb_opt_check2.v
bad_shift_reg2.v  incmp_case.v       tb_bad_mux.v               tb_opt_check3.v
bad_shift_reg.v  incmp_if2.v        tb_bad_shift_reg2.v        tb_opt_check.v
blocking_caveat.v  incmp_if.v         tb_bad_shift_reg.v         tb_partial_case_assign.v
blocking_caveat.v  mul2_net.v         tb_blocking_caveat.v       tb_pattern_detect_fsm.v
comp_case.v     mult_2.v           tb_comp_case.v             tb_rca.v
counter_opt2.v  mult_8.v           tb_counter_opt.v           tb_ripple_counter.v
counter_opt.v   multiple_module_opt2.v  tb_demux_case.v          tb_ternary_operator_mux.v
demux_case.v   multiple_module_opt.v  tb_mux_generate.v         tb_upcntr.v
mux_generate.v  multiple_modules_flat.v  tb_diff_asyncrs_syncrs.v  tb_up_dn_cntr.v
dff_ares_net.v  multiple_modules_hier.v  tb_diff_asyncrs.v         tb_up_dn_cntr_with_load.v
dff_asyncrs_net.v  multiple_modules.v  tb_diff_asyncr_set.v      tb_up_dn_cntr_with_load_with_start_stop.v
dff_asyncrs_syncrs.v  mux_generate.v      tb_diff_const1.v         ternary_operator_mux_net.v
dff_asyncrs.v   mux_spice.v         tb_diff_const2.v         ternary_operator_mux.v
dff_asyncr_set.v  net.v              tb_diff_const3.v         upcntr.v
dff_const1.v    opt_check2.v        tb_diff_const4.v         up_dn_cntr.v
dff_const2.v    opt_check3.v        tb_diff_const5.v         up_dn_cntr_with_load.v

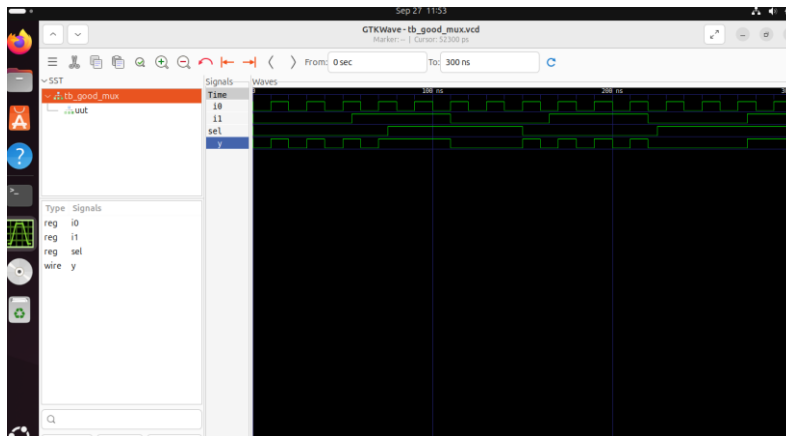
```

The Output file is generated: **a.out**

Dumping the vcd (value change dump) to the testbench tb_good_mux.vcd


[illegible]


Now we need to open the vcd file in the gtkwave to know the waveform generated:



The output that we generated is the 2*1 MUX. The input are dragged and placed in the signals to generate the waves.

The UUT represents the Unit Under Test

The complete waveform needs to be fitted in the screen for which the Zoom Fit  is used.

Using the  we can look for the transitions in any of the desired signal we want. This symbol represents forward but it can be done backward also.