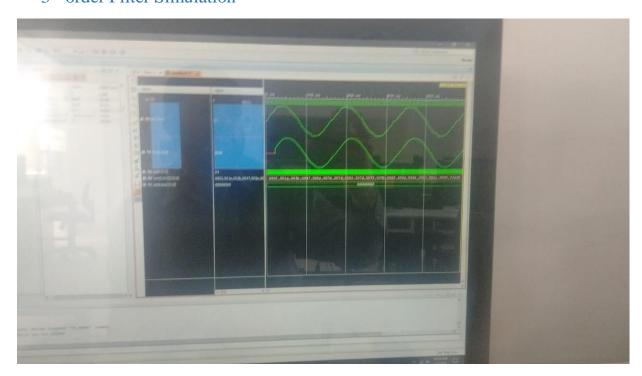
RESULTS

✓ Modular Approach

```
Sources
                                                             ? _ 🗆 🗗 ×
🔍 🔀 🖨 | 📸 🚮 | 🖺 🗷
□··· Design Sources (9)
  in sylin top_level (top_level.sv) (4)
     myrec - recorder (recorder.sv) (3)
       in generator (sine_generator.sv) (1)
       blk_mem_gen_0 - blk_mem_gen_0 (blk_mem_gen_0.xci)
       FIR - FIR_Filter (fir.sv) (31)
      pwm - pwm (pwm.sv)
  . Disabled Sources (3)
  ⊕ • □ Data Files (4)
  .
⊕... ि Text (1)
Hierarchy IP Sources | Libraries | Compile Order
```

✓ 3rd order Filter Simulation



✓ Scaled Filter Simulation

Due to an unknown error the results are not desired one.

