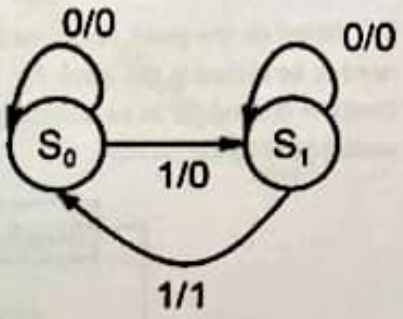
Mid-Sem: Monsoon2023: VLSI Digital (EC2.201)

Max. Time: 90 Mins [4:30 PM to 06:00 PM] Max. Marks: 60 Date: 23/09/2023

Note(s): No query is allowed during exam.

Write your assumptions (if any) for each question.

Q.1. Design the circuit (hardware) for the given State Transition Graph (Finite State Machine) using D-FF and JK-FF separately. Discuss your design (steps) procedure briefly. Also, point out your design observations with D-FF and JK-FF. **[6+4+2=12 Marks]** [CO-5]



Q2. [12 Marks] [CO-6]

In an ice-cream shop four ice-cream flavours are available vanilla, strawberry, chocolate, and butterscotch. A customer can choose flavours by pressing a set of three keys.

1. If no key is pressed, they get vanilla by default
2. If 1 key is pressed they get vanilla+ Some other flavour
3. If 2 keys are pressed, they get vanilla+2 other flavours
4. If 3 keys are pressed, they get all flavours

They are charged according to the extra number of flavours they opt for. Each additional flavour (Except vanilla) costs Rs. 2. Design a system using a full adder and multiplier to calculate the cost. (The costs for all the above four cases will be 0, 2, 4 and 6 respectively).

Hint: Use Full adder to find the number of ones in input, considering input to be a series of 3 bits.

Q3. [10 Marks + 10 Marks = 20 Marks] [CO-3, CO-6]

(a) The block diagram shown in Fig. 3(a) has one input "IN" which is coming serially @ clock, "CLK". It has 4 outputs A, B, C & D. A will be 1 if IN has even number of 1's & even number of 0's. Similarly, B will be 1 for even 1's odd 0's, C for odd 1's even 0's and D for both odd. Give the FSM required to design the block.

(b) Draw the state diagram for a circuit that outputs a "1" if the aggregate serial binary input is divisible by 5. For instance, if the input stream is 1, 0, 1, we output a "1" (since 101 is 5). If we then get a "0", the aggregate total is 10, so we output another "1" (and so on). Refer Fig. 3(b).

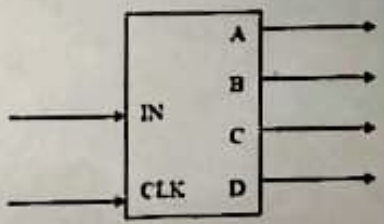


Fig. 3(a)

Input Sequence	Value	Output
1	1	0
10	2	0
101	5	1
1010	10	1
10101	21	0

Fig. 3(b)

Q4. Consider the following JK flipflop in Fig. 4
In the given J-K flipflop, J = Q' and K = 1. Assume that the flip-flop was initially cleared and the clocked for 6 pulses. What is the sequence at the Q output?
[6 Marks] [CO-5]

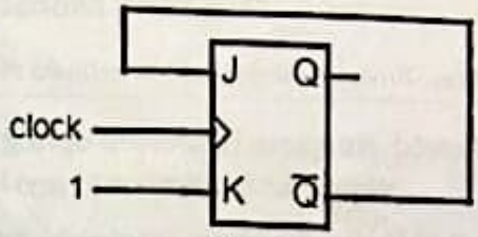


Fig. 4

Q5. Based on the given clock and output find out the necessary combinational blocks (1,2,3) that need to be placed in the given Fig. 5. Explain the output by plotting the Q1, Q2 and output. Consider Q1 and Q2 to be 0 initially. (Hint: Think how positive and negative edge-triggered FF works) **[10 Marks]** [CO-5]

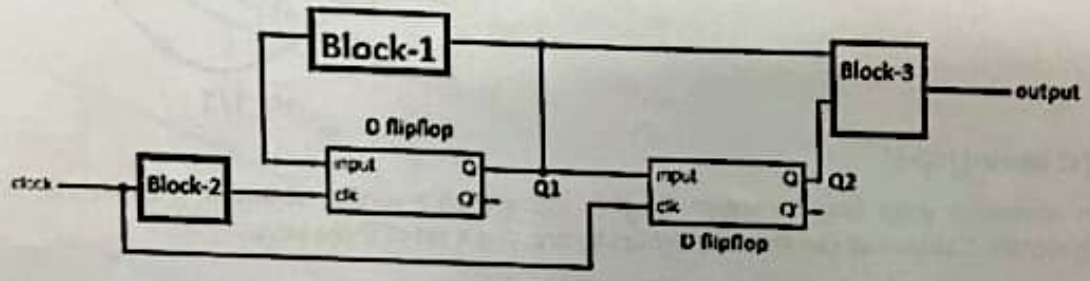


Fig. 5