# End-Sem: Monsoon2023: VLSI Digital (EC2.201)

Max. Time: 180 Mins [9:00 AM to 12:00] Max. Marks: 100 Date: 23/11/2023

**Note(s): Return/Attach the question paper with your sheet.**
**No query is allowed during exam.**
**Write your assumptions (if any) for each question.**

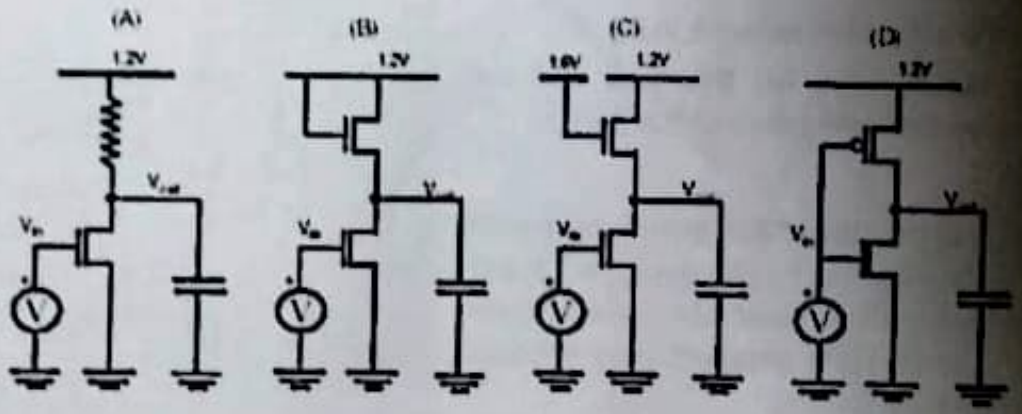
**Q.1.** Design a resistive-load inverter with R=1KΩ, such that $V_{OL}$=0.6V. The enhancement-type NMOS driver transistor has the following parameters: **[15 Marks]**

$V_{DD}$=5.0V, $V_{T0}$=1.0V, γ=0.2V, 1/ λ=0, $\mu_n C_{ox}$=22.0μA/$V^2$

Determine (a) the required aspect ratio, W/L, (b) $V_{IL}$ and $V_{IH}$, (c) Noise Margins $NM_L$ and $NM_H$.

**Q.2.(a).** The circuits below show different implementations of an inverter whose output is connected to a capacitor. **[8 Marks]**

I. Which one of the circuits consumes static power when the input is high?
II. Which one of the below circuits consumes static power when the input is low?
III. $V_{OH}$ of which circuit(s) is 1.2V?
IV. $V_{OL}$ of which circuit(s) is 0V?




**(b).** In a standard CMOS inverter, what happens to its logical functionality if you interchange the connections of the PMOS and NMOS sources, making the PMOS source connected to ground (GND) and the NMOS source connected to the supply voltage ($V_{DD}$)? Explain its voltage transfer characteristics (VTC)? Expecting just the shape of the VTC. **[3 Marks]**

**(c).** If the PMOS transistor in a CMOS inverter is made larger, what changes can be expected in terms of propagation delay and noise margins? **[4 Marks]**

**Q.3. (a):** Draw voltage transfer characteristics (VTC) for resistive load and CMOS inverter. **[2 Marks]**

**(b).** Which of the above two designs have finite largest slope in transition region of VTC? Explain by finding the slope mathematically? **[6 Marks]**
**[Hint: Use the fact that slope of the VTC in this region is voltage gain of the inverter]**

**(c).** Based on the result obtained from Q.3(b), which of the above two designs give better $NM_L$? Explain. **[2 Marks]**

**Q.4.(a).** Shown in Fig. Q.4(a) is the PMOS stack of a logic gate. Identify the logic function being implemented and complete the NMOS stack. **[2.5 Marks]**

**(b).** Sketch a pseudo-nMOS gate that implements the function $F = (A(B + C + D) + EFG)'$ **[2.5 Marks]**

**(c).** What function is implemented by the circuit below in Fig. Q.4(c)? What considerations are necessary when sizing the transistors? **[3 Marks]**

**(d).** An implementation of a D Flip-flop is shown in Fig. Q.4(d). Is this positive edge triggered or negative edge triggered? **[2 Marks]**

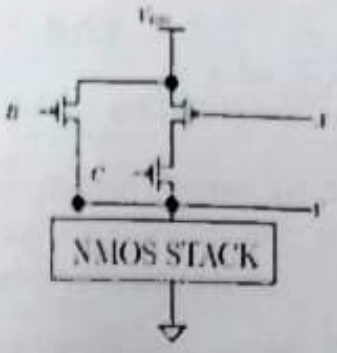



Fig. Q.4(a)

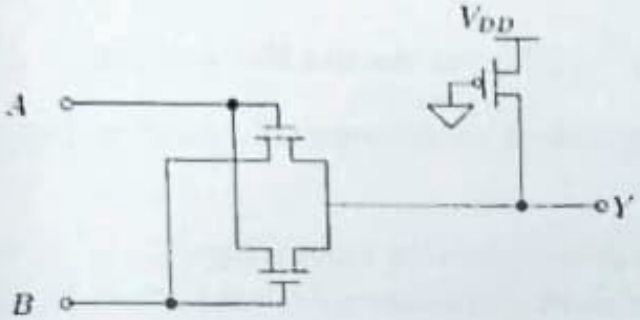



Fig. Q.4(c)

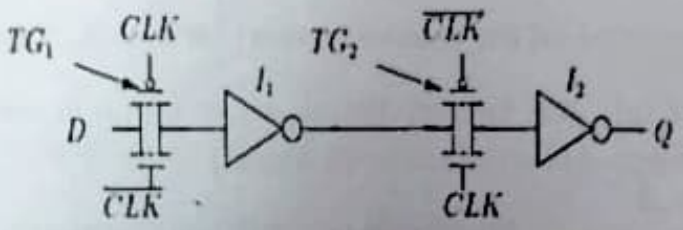



Fig. Q.4(d)

**Q.5.** Consider, the pull-down network in Fig. 5.

**(a).** Draw the pull-up part for this, and find out Boolean expression from the entire CMOS design. **[5 Marks]**

**(b).** Now, it is given that the NMOS in pull-down with input D is faulty. Explain how do you detect this fault? (Hint: Test the circuit with different input combinations with the help of truth table obtained from Boolean expression found earlier) **[5 Marks]**

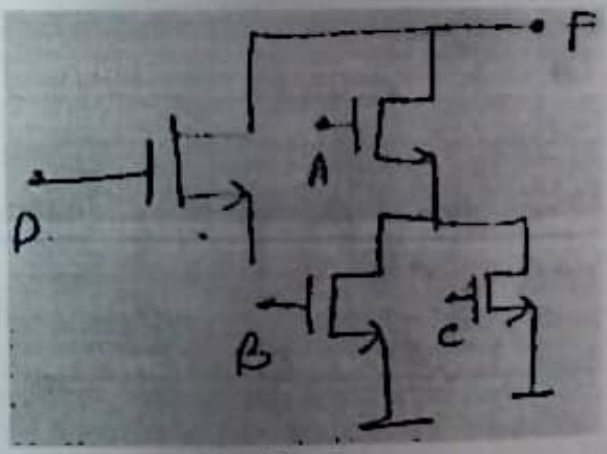



Fig. 5

**Q.6. (a).** Draw the 3D diagram of NMOS and PMOS and label the drain, source gate, and body. **[2 Marks]**

**(b).** In the layout (in MAGIC), we separately put a nwell when putting p-substrate but no pwell is put for n-substrate. What might be the reason for this? **[2 Marks]**

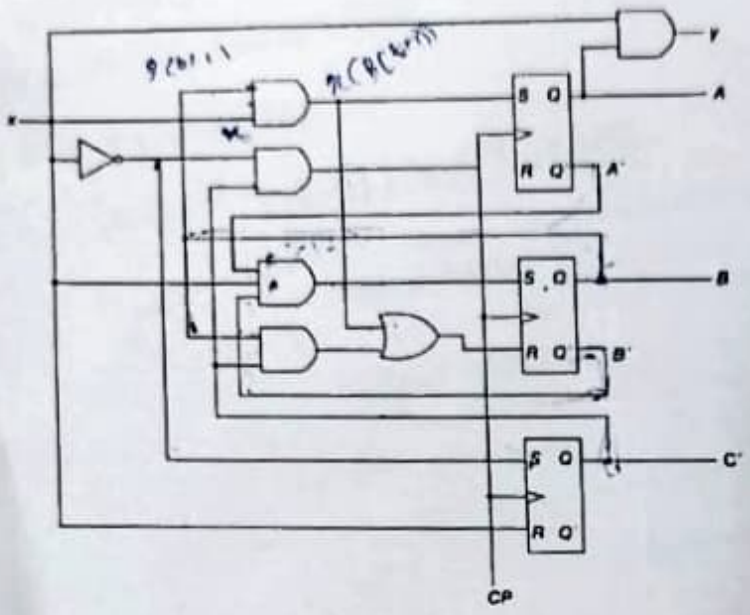
**(c).** When making the layout where are you connecting the body to VDD or GND? If you did not connect, what are the changes that you need to do to make your circuit function the way it is supposed to do ideally? **[2 Marks]**

**(d).** What are AS, AD, PS, and PD when making a netlist for the MOSFET? Define them along with their units. **[2 Marks]**

**(e).** What does lambda stand for in the netlist? **[2 Marks]**

**Q.7.** A certain manufacturer forgot to realize that the machine he was using to fabricate the chip was faulty. He now has only one way to determine if the circuit is working properly or not. He knows the following about the circuit.

(a). Since he made the circuit, he knows the schematic of the circuit and it is as below. Find the outputs Y, A, B, and C as a function of input and time. [4 Marks]




(b). He found out that the defective and non-defective circuits differ by the difference in the maximum clock frequency that can be given. Find the clock frequency that can be given to the circuit assuming $t_{pcq}$ and $t_{Setup}$ are 0. INVERTER has a delay of 100ps, and the AND & OR gate has a delay of 200ps. [6 Marks]

Q. 8. (a). If I am saying, in general propagation delays decreases with increase in supply voltage. Are you agree with this statement? Justify your answer by developing a simple expression for low-to-high ($\tau_{p\_LH}$) and high-to-low ($\tau_{p\_HL}$) delays for CMOS inverter. Consider your CMOS inverter has the similar inverter as load. Also, discuss the parameters impacting propagation delays. [10 Marks]

(b). Will you prefer a CMOS inverter over resistive load and other inverters (e.g., Pseudo NMOS logic, etc.)? Justify your answer in term of propagation delays, power dissipation (static and dynamic), and area. [8 Marks]

(c). A finite state machine is shown in Fig. Q.8(c) where the INVERTER has a delay of 100ps, the AND gate has a delay of 200ps and the XOR has a delay of 300ps. What is the critical path of this system? [2 Marks]

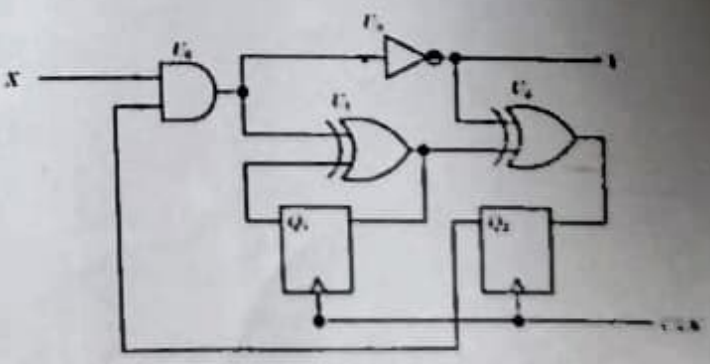



Fig. Q.8(c)

•Good Luck•

**Attach the question paper with your exam sheet**