Mid-Sem: Digital VLSI Design (M24.ECE463)

Max. Time: 90 Mins [8:30 AM to 10:00 AM] Max. Marks: 45 Date: 23/09/2024

NOTE: No query allowed during the exam. Write your assumptions (if any) for each question.

Q 1. Given a PMOS Inverter in Fig. 1. **[3+10+2= 15 Marks]**

(a) Draw the voltage transfer characteristics for the given circuit and mark the regions of operation.

(b) For the given Fig.1 the values of $V_{DD} = 5V$, $Kp = \mu_p C_{ox}(W/L) = 40\ \mu A/V^2$, $|Vt| = 1V$, $R_D = 200\ K\Omega$. Find the values of V_{OL}, V_{IH}, V_{IL}, and V_{OH}. Channel length modulation and body effect can be ignored. Mention clearly if any assumptions are made.

Hint: (Neglect Vsd^2 term for V_{OH}, V_{IL} calculation)

(c) Find the Noise margin (NM_L and NM_H) using the results of Part (b).

Q 2. Consider a PMOS-based resistive load design, driving an inverter (as shown in Fig. 2). Answer the following- **[2.5+2.5+6+4= 15 Marks]**

(a) What is the net capacitance at node V_X?

(b) Consider the abrupt transition of input from V_{DD} to 0. What is the state/region of MOS M_1 before and after the switching?

(c) Develop a simple expression for the calculation of low-to-high propagation delay (τ_{plh}).

(d) Discuss the parameters impacting the τ_{plh}. From the developed expression, how can you improve the operating speed of this resistive-load inverter? Discuss the trade-off. Also, discuss the assumption considered.

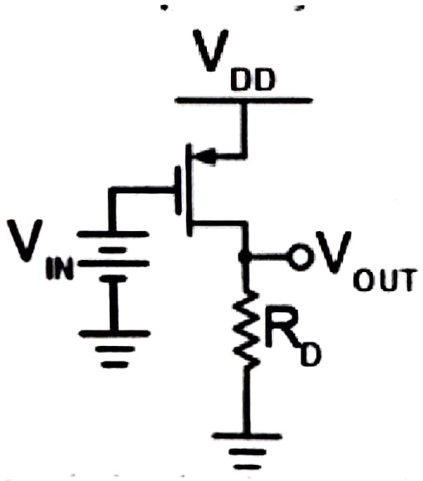


Fig. 1

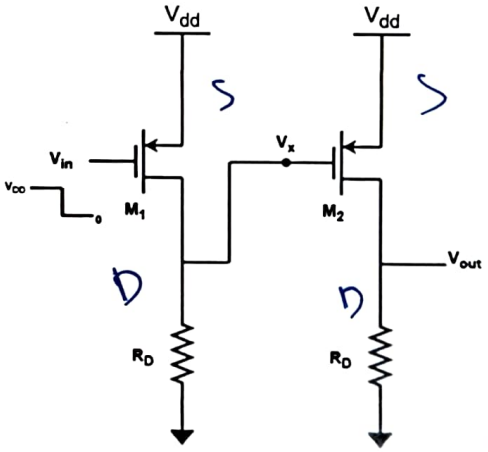
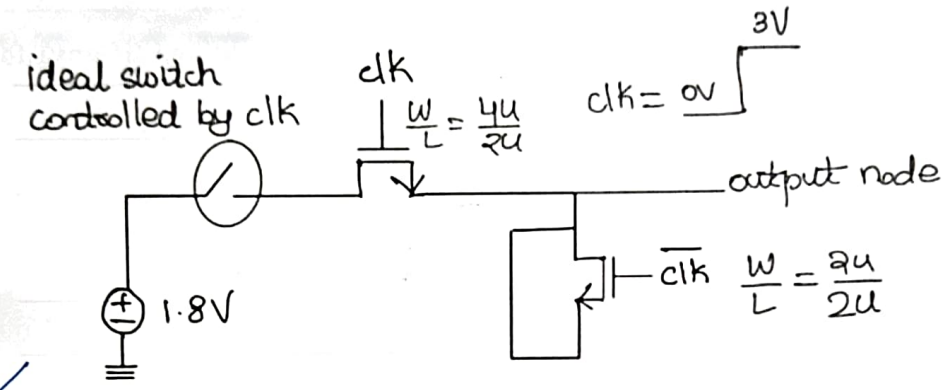


Fig. 2

Q 3. The circuit below consists of 2 NMOS having the same threshold voltage (0.6V) and the same oxide capacitance. The ideal switch is controlled by the 'clk' signal, which means the switch is ON when the 'clk' is 3V and OFF when the 'clk' is 0V. MOS sizes are (4μ/2μ) and (2μ /2μ). Answer the following- **[5+5= 10 Marks]**

(a) Find channel charges in both the MOSFETs and output node voltage when 'clk' is HIGH (3V).

(b) When 'clk' transitions from HIGH (3V) to LOW (0V), find channel charges in both MOSFETs and output node voltage.



Q 4. The drain of an n-channel MOSFET is shorted to the gate so that $V_{GS} = V_{DS}$. The threshold voltage (V_T) of the MOSFET is 1 V. If the drain current I_D is 1 mA for $V_{GS} = 2$ V, then calculate the I_D for $V_{GS} = 3$ V. **[5 Marks]**