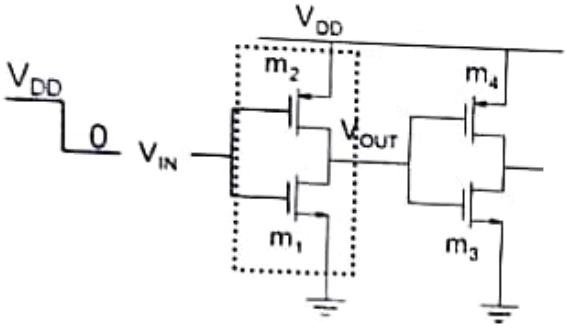
Quiz-2: Digital VLSI Design (M24.ECE408)

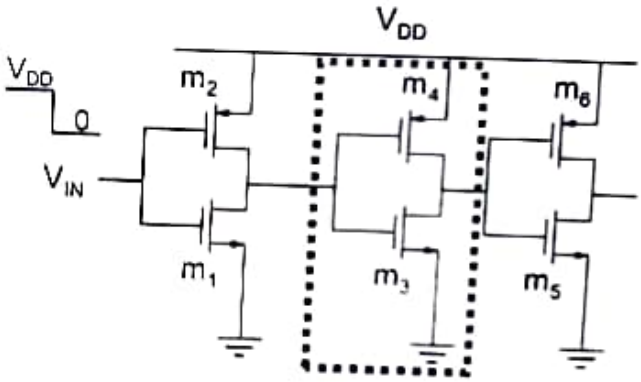
NOTE: No query allowed during the exam. Write your assumptions (if any) for each question.

Q 1(a). Is it good to have an Inverter threshold (V_{INV}) at middle i.e., $V_{DD}/2$? What are the possible advantages of having it at $V_{DD}/2$? Prove it mathematically that it is relatively straight forward to have V_{INV} at middle. Mention the assumption taken. **[5 Marks]**

(b). In the circuits below, all the inverters are same. We are interested in estimating the propagation delays of the inverter highlighted in rectangle. What do you think? (i) delay in both the circuits will be same, (ii) delay in Fig. (a) will be higher or (iii) delay in Fig. (b) will be higher. Justify your answer with proper explanation. **[5 Marks]**



(a)



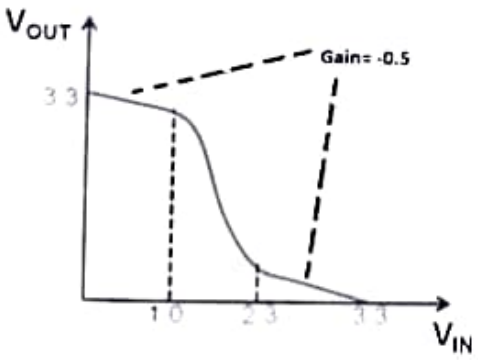
(b)

Q 2(a). What do you understand by 'slow' and 'fast' process corners and how they can impact your circuit? Explain with MOS current equation. **[3 Marks]**

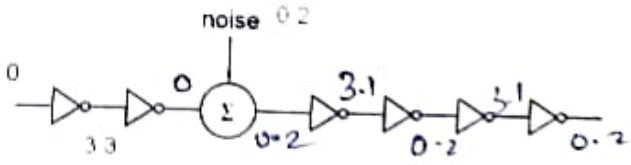
(b). What are the possible ways of improving propagation delays and power in your design? **[2 Marks]**

(c). Are you agree with the statement; the intrinsic delay of the inverter is not dependent on the sizing of the inverter at least with first order approximation? Explain with equations. **[2 Marks]**

(d). The VTC curve for the inverter design is shown in the Fig. x below. Determine the final value of V_{OL} and V_{OH} for the given chain of inverters (in Fig. y) based on the provided VTC curve. **[3 Marks]**



(x)



(y)

Best of Luck

"Attach the question paper with your exam sheet"