

IDLE MODE:

- Upon the IDL bit of the PCON register is set, the microcontroller turns off the greatest power consumer- CPU unit while peripheral units such as serial port, timers and interrupt system continue operating normally consuming 6.5mA.
- In Idle mode, the state of all registers and I/O ports remains unchanged.
- In order to exit the Idle mode and make the microcontroller operate normally, it is necessary to enable and execute any interrupt or reset.
- It will cause the IDL bit to be automatically cleared and the program resumes operation from instruction having set the IDL bit.
- It is recommended that first three instructions

... NOP ...

memory

There's nothing saved in me

8D

HEX 8D
DEC 141
OCT 215
BIN 1000 1101

		QWORD			MS
RoL	RoR	Or	Xor	Not	And
2 nd	Mod	CE	C	☒	÷
A	B	7	8	9	×
C	D	4	5	6	-
E	F	1	2	3	+

4.0 COMPARE/CAPTURE MODULES

Each PCA module has a mode SFR with it. These registers are: CCAPM0 for module 0, CCAPM1 for module 1, etc. Each register contains 7 bits that are used to control the mode in which each module will operate. See Table 4-1.

The ECCF bit (CCAPM_n where $n = 0, 1, 2, 3$, or 4 depending on module) will enable the CCF flag in the CCON SFR to generate an interrupt when a match or compare occurs. PWM (CCAPM_n1) enables the pulse width modulation mode. The MAT_n (CCAPM_n3) bit when set, will cause the CCF_n bit in the CCON register to be set when there is a match between the PCA counter and the module's capture/compare registers. Additionally, the TOG bit (CCAPM_n2) when set, causes the CE_{Xn} output pin associated with that module to toggle when there is a match between the PCA counter and the module's capture/compare registers.



Bits CAPN (CCAPM_n4) and CAPP (CCAPM_n5) determine whether the capture input will be active on a positive edge or negative edge. The CAPN bit enables a capture at the negative edge, and the CAPP bit enables a capture at the positive edge. When both bits are set, both edges will be enabled and a capture will occur for either transition. The last bit in the register ECOM (CCAPM_n) when set, enables the comparator function. Tables 4-2 and 4-3 show the CCAPM_n settings for the various PCA functions.

There are two additional registers associated with each of the PCA modules: CCAPnH and CCAPnL. They are registers that hold the 16-bit count value when a capture occurs or a comparison occurs. When a module is used in PWM mode, these registers are used to control the duty cycle of the output. See Table 4-4.

TABLE 4-1: PCA Compare/Capture Module Mode Register¹ (CCAPM_n)

Location	7	6	5	4	3	2	1	0	Reset Value
DAH	-	ECOM0	CAPP0	CAPN0	MAT0	TOG0	PWM0	ECCF0	00xxx000b
DBH	-	ECOM1	CAPP1	CAPN1	MAT1	TOG1	PWM1	ECCF1	00xxx000b
DCH	-	ECOM2	CAPP2	CAPN2	MAT2	TOG2	PWM2	ECCF2	00xxx000b
DDH	-	ECOM3	CAPP3	CAPN3	MAT3	TOG3	PWM3	ECCF3	00xxx000b
DEH	-	ECOM4	CAPP4	CAPN4	MAT4	TOG4	PWM4	ECCF4	00xxx000b

AT89C51RB2/RC2

Registers

Table 22. CMOD Register

CMOD – PCA Counter Mode Register (D9h)

			7	6	5	4	3	2	1	0
CIDL	WDTE	-	-	-	-	-	CPS1	CPS0	ECF	
Bit Number	Bit Mnemonic	Description								
7	CIDL	Counter Idle Control Cleared to program the PCA Counter to continue functioning during idle Mode. Set to program PCA to be gated off during idle.								
6	WDTE	Watchdog Timer Enable Cleared to disable Watchdog Timer function on PCA Module 4. Set to enable Watchdog Timer function on PCA Module 4.								
5	-	Reserved The value read from this bit is indeterminate. Do not set this bit.								
4	-	Reserved The value read from this bit is indeterminate. Do not set this bit.								
3	-	Reserved The value read from this bit is indeterminate. Do not set this bit.								
2	CPS1	PCA Count Pulse Select CPS1 CPS0 Selected PCA input								
1	CPS0	0 0 Internal clock $F_{CLK\ PERIPH}/6$ 0 1 Internal clock $F_{LK\ PERIPH}/2$ 1 0 Timer 0 Overflow 1 1 External clock at ECI/P1.2 pin (max rate = $f_{CLK\ PERIPH}/4$)								
0	ECF	PCA Enable Counter Overflow Interrupt Cleared to disable CF bit in CCON to inhibit an interrupt. Set to enable CF bit in CCON to generate an interrupt.								

Reset Value = 00XX X000b

Not bit addressable

AT89C51RB2/RC2

Table 44. IEN0 Register

IEN0 - Interrupt Enable Register (A8h)

7	6	5	4	3	2	1	0
EA	EC	ET2	ES	ET1	EX1	ET0	EX0
Bit Number	Bit Mnemonic	Description					
7	EA	Enable All Interrupt Bit Cleared to disable all interrupts. Set to enable all interrupts.					
6	EC	PCA Interrupt Enable Bit Cleared to disable. Set to enable.					
5	ET2	Timer 2 Overflow Interrupt Enable Bit Cleared to disable timer 2 overflow interrupt. Set to enable timer 2 overflow interrupt.					
4	ES	Serial Port Enable Bit Cleared to disable serial port interrupt. Set to enable serial port interrupt.					
3	ET1	Timer 1 Overflow Interrupt Enable Bit Cleared to disable timer 1 overflow interrupt. Set to enable timer 1 overflow interrupt.					
2	EX1	External Interrupt 1 Enable Bit Cleared to disable external interrupt 1. Set to enable external interrupt 1.					
1	ET0	Timer 0 Overflow Interrupt Enable Bit Cleared to disable timer 0 overflow interrupt. Set to enable timer 0 overflow interrupt.					
0	EX0	External Interrupt 0 Enable Bit Cleared to disable external interrupt 0. Set to enable external interrupt 0.					

Reset Value = 0000 0000b

Table 22. CMOD Register

CMOD – PCA Counter Mode Register (D9h)

7	6	5	4	3	2	1	0
CIDL	WDTE	-	-	-	CPS1	CPS0	ECF
Bit Number	Bit Mnemonic	Description					
7	CIDL	Counter Idle Control Cleared to program the PCA Counter to continue functioning during idle Mode. Set to program PCA to be gated off during idle.					
6	WDTE	Watchdog Timer Enable Cleared to disable Watchdog Timer function on PCA Module 4. Set to enable Watchdog Timer function on PCA Module 4.					
5	-	Reserved The value read from this bit is indeterminate. Do not set this bit.					
4	-	Reserved The value read from this bit is indeterminate. Do not set this bit.					
3	-	Reserved The value read from this bit is indeterminate. Do not set this bit.					
2	CPS1	PCA Count Pulse Select CPS1 CPS0 Selected PCA input					
1	CPS0	0 0 Internal clock $F_{CLK\ PERIPH}/6$ 0 1 Internal clock $F_{CLK\ PERIPH}/2$ 1 0 Timer 0 Overflow 1 1 External clock at ECI/P1.2 pin (max rate = $f_{CLK\ PERIPH}/4$)					
0	ECF	PCA Enable Counter Overflow Interrupt Cleared to disable CF bit in CCON to inhibit an interrupt. Set to enable CF bit in CCON to generate an interrupt.					

Reset Value = 00XX X000b

Not bit addressable

The CMOD register includes three additional bits associated with the PCA.

- The CIDL bit which allows the PCA to stop during idle mode.
- The WDTE bit which enables or disables the watchdog function on Module 4.
- The ECF bit which when set causes an interrupt and the PCA overflow flag CF (in the CCON SFR) to be set when the PCA timer overflows.

Table 22-15. ADC14IFGR0 Register Description (continued)

Field	Type	Reset	Description
ADC14IFG2	R	0h	<p>ADC14MEM2 interrupt flag. This bit is set to 1 when ADC14MEM2 is loaded with a conversion result. This bit is reset to 0 when the ADC14MEM2 register is read, or when the corresponding bit in the ADC14CLRIFGR0 register is set to 1.</p> <p>0b = No interrupt pending 1b = Interrupt pending</p>
ADC14IFG1	R	0h	<p>ADC14MEM1 interrupt flag. This bit is set to 1 when ADC14MEM1 is loaded with a conversion result. This bit is reset to 0 when the ADC14MEM1 register is read, or when the corresponding bit in the ADC14CLRIFGR0 register is set to 1.</p> <p>0b = No interrupt pending 1b = Interrupt pending</p>
ADC14IFG0	R	0h	<p>ADC14MEM0 interrupt flag. This bit is set to 1 when ADC14MEM0 is loaded with a conversion result. This bit is reset to 0 when the ADC14MEM0 register is read, or when the corresponding bit in the ADC14CLRIFGR0 register is set to 1.</p> <p>0b = No interrupt pending 1b = Interrupt pending</p>

Figure 6-5. CSKEY Register

31	30	29	28	27	26	25	24
Reserved							
r-0	r-0	r-0	r-0	r-0	r-0	r-0	r-0
23	22	21	20	19	18	17	16
Reserved							
r-0	r-0	r-0	r-0	r-0	r-0	r-0	r-0
15	14	13	12	11	10	9	8
CSKEY							
rw-1	rw-0	rw-1	rw-0	rw-0	rw-1	rw-0	rw-1
7	6	5	4	3	2	1	0
CSKEY							
rw-1	rw-0	rw-0	rw-1	rw-0	rw-1	rw-1	rw-0

Table 6-3 CSKEY Register Description

Figure 6-5. CSKEY Register

31	30	29	28	27	26	25	24
Reserved							
r-0	r-0	r-0	r-0	r-0	r-0	r-0	r-0
23	22	21	20	19	18	17	16
Reserved							
r-0	r-0	r-0	r-0	r-0	r-0	r-0	r-0
15	14	13	12	11	10	9	8
CSKEY							
rw-1	rw-0	rw-1	rw-0	rw-0	rw-1	rw-0	rw-1
7	6	5	4	3	2	1	0
CSKEY							
rw-1	rw-0	rw-0	rw-1	rw-0	rw-1	rw-1	rw-0

Table 6-3. CSKEY Register Description

Bit	Field	Type	Reset	Description
31-16	Reserved	R	0h	Reserved. Always reads as 0.
15- 0	CSKEY	RW	A596h	<p>Write CSKEY = xxxx_695Ah to unlock CS registers. All 16 LSBs need to be written together.</p> <p>Writing CSKEY with any other value causes CS registers to be locked and any writes to these registers are ignored, while reads are still performed. Always reads back A596h.</p>

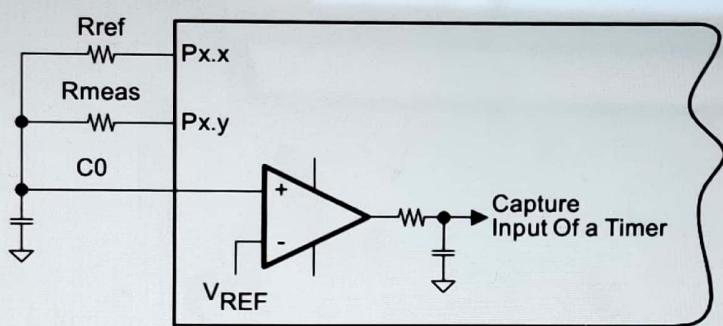


Figure 23-6. Temperature Measurement System

The resources used to calculate the temperature sensed by Rmeas are:

- Two digital I/O pins charge and discharge the capacitor.
- I/O is set to output high (V_{CC}) to charge capacitor, reset to discharge.
- I/O is switched to high-impedance input with CEPDx set when not in use.
- One output charges and discharges the capacitor through Rref.
- One output discharges capacitor through Rmeas.
- The + terminal is connected to the positive terminal of the capacitor.
- The - terminal is connected to a reference level, for example $0.25 \times V_{CC}$.
- The output filter should be used to minimize switching noise.
- CEOUT is used to gate a timer capturing capacitor discharge time.

More than one resistive element can be measured. Additional elements are connected to C0 with available I/O pins and switched to high impedance when not being measured.

				0b = ADC input channel internal 2 is not selected 1b = ADC input channel internal 2 is selected for ADC input channel MAX – 4
25	ADC14CH1MAP	RW	0h	Controls internal channel 1 selection to ADC input channel MAX – 3 0b = ADC input channel internal 1 is not selected 1b = ADC input channel internal 1 is selected for ADC input channel MAX – 3
24	ADC14CH0MAP	RW	0h	Controls internal channel 0 selection to ADC input channel MAX – 2 0b = ADC input channel internal 0 is not selected 1b = ADC input channel internal 0 is selected for ADC input channel MAX – 2
23	ADC14TCMAP	RW	0h	Controls temperature sensor ADC input channel selection 0b = ADC internal temperature sensor channel is not selected for ADC 1b = ADC internal temperature sensor channel is selected for ADC input channel MAX – 1
22	ADC14BATMAP	RW	0h	Controls 1/2 AVCC ADC input channel selection 0b = ADC internal 1/2 x AVCC channel is not selected for ADC 1b = ADC internal 1/2 x AVCC channel is selected for ADC input channel MAX
21	Reserved	R	0h	Reserved. Always reads as 0.
20-16	ADC14CSTARTADDx	RW	0h	ADC14 conversion start address. These bits select which ADC14 conversion memory register is used for a single conversion or for the first conversion in a sequence. The value of CSTARTADDx is 0h to 1Fh, corresponding to ADC14MEM0 to ADC14MEM31
15-6	Reserved	R	0h	Reserved. Always reads as 0.

Figure 24-21. UCAXIE Register

15	14	13	12	11	10	9	8
Reserved							
r-0	r-0	r-0	r-0	r-0	r-0	r-0	r-0
7	6	5	4	3	2	1	0
Reserved				UCTXCPTIE	UCSTTIE	UCTXIE	UCRXIE
r-0	r-0	r-0	r-0	rw-0	rw-0	rw-0	rw-0

Table 24-17. UCAXIE Register Description

Bit	Field	Type	Reset	Description
15-4	Reserved	R	0h	Reserved
3	UCTXCPTIE	RW	0h	Transmit complete interrupt enable 0b = Interrupt disabled 1b = Interrupt enabled
2	UCSTTIE	RW	0h	Start bit interrupt enable 0b = Interrupt disabled 1b = Interrupt enabled
1	UCTXIE	RW	0h	Transmit interrupt enable 0b = Interrupt disabled 1b = Interrupt enabled
0	UCRXIE	RW	0h	Receive interrupt enable 0b = Interrupt disabled 1b = Interrupt enabled

24.4.4 UCAxMCTLW Register

eUSCI_Ax Modulation Control Word Register

Figure 24-15. UCAxMCTLW Register

15	14	13	12	11	10	9	8
UCBRSx							
rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0
7	6	5	4	3	2	1	0
UCBRFx							
rw-0	rw-0	rw-0	rw-0	r0	r0	r0	rw-0
Modify only when UCSWRST = 1							

Table 24-11. UCAxMCTLW Register Description

Bit	Field	Type	Reset	Description
15-8	UCBRSx	RW	0h	Second modulation stage select. These bits hold a free modulation pattern for BITCLK.
7-4	UCBRFx	RW	0h	First modulation stage select. These bits determine the modulation pattern for BITCLK16 when UCOS16 = 1. Ignored with UCOS16 = 0. The "Oversampling Baud-Rate Generation" section shows the modulation pattern.
3-1	Reserved	R	0h	Reserved
0	UCOS16	RW	0h	Oversampling mode enabled 0b = Disabled 1b = Enabled

Table 24-8. UCAxCTLW0 Register Description (continued)

Bit	Field	Type	Reset	Description
3	UCDORM	RW	0h	Dormant. Puts eUSCI_A into sleep mode. 0b = Not dormant. All received characters set UCRXIFG. 1b = Dormant. Only characters that are preceded by an idle-line or with address bit set UCRXIFG. In UART mode with automatic baud-rate detection, only the combination of a break and synch field sets UCRXIFG.
2	UCTXADDR	RW	0h	Transmit address. Next frame to be transmitted is marked as address, depending on the selected multiprocessor mode. 0b = Next frame transmitted is data. 1b = Next frame transmitted is an address.
1	UCTXBRK	RW	0h	Transmit break. Transmits a break with the next write to the transmit buffer. In UART mode with automatic baud-rate detection, 055h must be written into UCAxTXBUF to generate the required break/synch fields. Otherwise, 0h must be written into the transmit buffer. 0b = Next frame transmitted is not a break. 1b = Next frame transmitted is a break or a break/synch.
0	UCSWRST	RW	1h	Software reset enable 0b = Disabled. eUSCI_A reset released for operation. 1b = Enabled. eUSCI_A logic held in reset state.

24.4.2 UCAxCTLW1 Register

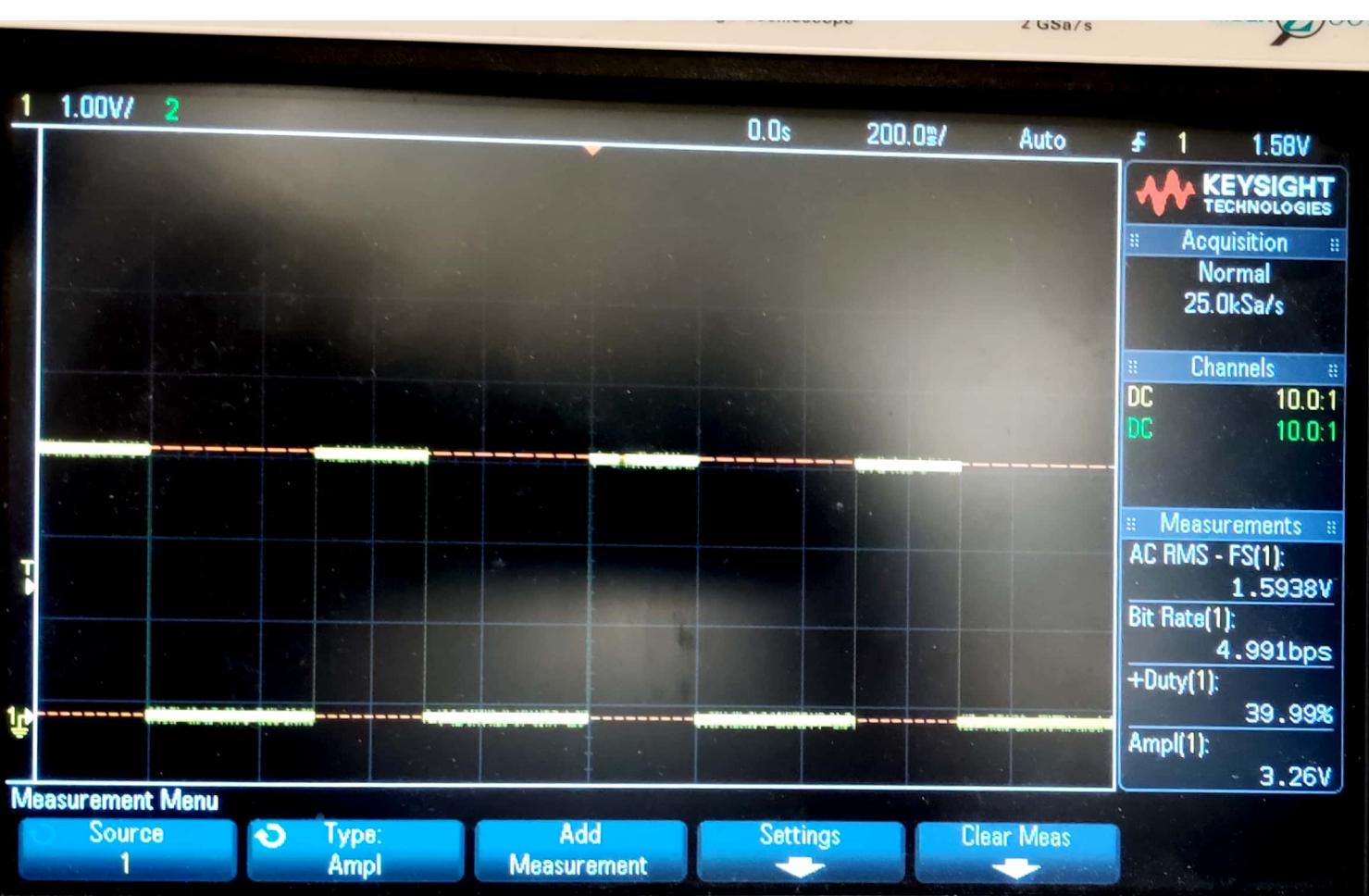
eUSCI_Ax Control Word Register 1

Figure 24-13. UCAxCTLW1 Register

				1b = MSB first
12	UC7BIT	RW	0h	Character length. Selects 7-bit or 8-bit character length. 0b = 8-bit data 1b = 7-bit data
11	UCSPB	RW	0h	Stop bit select. Number of stop bits. 0b = One stop bit 1b = Two stop bits
10-9	UCMODEx	RW	0h	eUSCI_A mode. The UCMODEx bits select the asynchronous mode when UCSYNC = 0. 00b = UART mode 01b = Idle-line multiprocessor mode 10b = Address-bit multiprocessor mode 11b = UART mode with automatic baud-rate detection
8	UCSYNC	RW	0h	Synchronous mode enable 0b = Asynchronous mode 1b = Synchronous mode
7-6	UCSSELx	RW	0h	eUSCI_A clock source select. These bits select the BRCLK source clock. 00b = UCLK 01b = ACLK 10b = SMCLK 11b = SMCLK
5	UCRXIE	RW	0h	Receive erroneous-character interrupt enable 0b = Erroneous characters rejected and UCRXIFG is not set. 1b = Erroneous characters received set UCRXIFG.
4	UCBRKIE	RW	0h	Receive break character interrupt enable 0b = Received break characters do not set UCRXIFG.

Table 24-8. UCAxCTLW0 Register Description (continued)

Bit	Field	Type	Reset	Description
3	UCDORM	RW	0h	Dormant. Puts eUSCI_A into sleep mode. 0b = Not dormant. All received characters set UCRXIFG. 1b = Dormant. Only characters that are preceded by an idle-line or with address bit set UCRXIFG. In UART mode with automatic baud-rate detection, only the combination of a break and synch field sets UCRXIFG.
2	UCTXADDR	RW	0h	Transmit address. Next frame to be transmitted is marked as address, depending on the selected multiprocessor mode. 0b = Next frame transmitted is data. 1b = Next frame transmitted is an address.
1	UCTXBRK	RW	0h	Transmit break. Transmits a break with the next write to the transmit buffer. In UART mode with automatic baud-rate detection, 055h must be written into UCAxTXBUF to generate the required break/synch fields. Otherwise, 0h must be written into the transmit buffer. 0b = Next frame transmitted is not a break. 1b = Next frame transmitted is a break or a break/synch.
0	UCSWRST	RW	1h	Software reset enable 0b = Disabled. eUSCI_A reset released for operation. 1b = Enabled. eUSCI_A logic held in reset state.



19.3.1 TAxCTL Register

Timer_A Control Register

Figure 19-15. TAxCTL Register

15	14	13	12	11	10	9	8
Reserved						TASSEL	
rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0
7	6	5	4	3	2	1	0
ID		MC		Reserved	TACLR	TAIE	TAIFG
rw-0	rw-0	rw-0	rw-0	rw-0	w-0	rw-0	rw-0

Table 19-4. TAxCTL Register Description

Bit	Field	Type	Reset	Description
15-10	Reserved	RW	0h	Reserved
9-8	TASSEL	RW	0h	Timer_A clock source select 00b = TAxCLK 01b = ACLK 10b = SMCLK 11b = INCLK
7-6	ID	RW	0h	Input divider. These bits along with the TAIDEX bits select the divider for the input clock. 00b = /1 01b = /2 10b = /4 11b = /8
5-4	MC	RW	0h	Mode control. Setting MCx = 00h when Timer_A is not in use conserves power. 00b = Stop mode: Timer is halted 01b = Up mode: Timer counts up to TAxCCR0 10b = Continuous mode: Timer counts up to 0FFFFh 11b = Up/down mode: Timer counts up to TAxCCR0 then down to 0000h
3	Reserved	RW	0h	Reserved
2	TACLR	RW	0h	Timer_A clear. Setting this bit resets TAxR, the timer clock divider logic, and the count direction. The TACLR bit is automatically reset and is always read as zero.
1	TAIE	RW	0h	Timer_A interrupt enable. This bit enables the TAIFG interrupt request. 0b = Interrupt disabled 1b = Interrupt enabled
0	TAIFG	RW	0h	Timer_A interrupt flag 0b = No interrupt pending 1b = Interrupt pending

CM	CCIS		SCS	SCCI	Reserved	CAP
rw-0	rw-0	rw-0	rw-0	rw-0	r-0	r-0
7	6	5	4	3	2	1
	OUTMOD		CCIE	CCI	OUT	COV
rw-0	rw-0	rw-0	rw-0	r	rw-0	rw-0

Table 19-6. TAxCCTL0 to TAxCCTL6 Register Description

Bit	Field	Type	Reset	Description
15-14	CM	RW	0h	Capture mode 00b = No capture 01b = Capture on rising edge 10b = Capture on falling edge 11b = Capture on both rising and falling edges
13-12	CCIS	RW	0h	Capture/compare input select. These bits select the TAxCCTL0 input signal. See the device-specific data sheet for specific signal connections. 00b = CCIxA 01b = CCIxB 10b = GND 11b = VCC
11	SCS	RW	0h	Synchronize capture source. This bit is used to synchronize the capture input signal with the timer clock. 0b = Asynchronous capture 1b = Synchronous capture
10	SCCI	RW	0h	Synchronized capture/compare input. The selected CCI input signal is latched with the EQUx signal and can be read via this bit.
9	Reserved	R	0h	Reserved. Reads as 0.
8	CAP	RW	0h	Capture mode 0b = Compare mode 1b = Capture mode
7-5	OUTMOD	RW	0h	Output mode. Modes 2, 3, 6, and 7 are not useful for TAxCCTL0 because EQUx = EQU0. 000b = OUT bit value 001b = Set 010b = Toggle/reset 011b = Set/reset 100b = Toggle 101b = Reset 110b = Toggle/set 111b = Reset/set
4	CCIE	RW	0h	Capture/compare interrupt enable. This bit enables the interrupt request of the corresponding CCIFG flag. 0b = Interrupt disabled 1b = Interrupt enabled
3	CCI	R	0h	Capture/compare input. The selected input signal can be read by this bit.
2	OUT	RW	0h	Output. For output mode 0, this bit directly controls the state of the output. 0b = Output low 1b = Output high

25.4.5 UCAxTXBUF Register

eUSCI_Ax Transmit Buffer Register

Figure 25-9. UCAxTXBUF Register

15	14	13	12	11	10	9	8
Reserved							
r0	r0	r0	r0	r0	r0	r0	r0
7	6	5	4	3	2	1	0
UCTXBUFx							
rw	rw	rw	rw	rw	rw	rw	rw

Table 25-7. UCAxTXBUF Register Description

Bit	Field	Type	Reset	Description
15-8	Reserved	R	0h	Reserved
7-0	UCTXBUFx	RW	0h	The transmit data buffer is user accessible and holds the data waiting to be moved into the transmit shift register and transmitted. Writing to the transmit data buffer clears UCTXIFG. The MSB of UCxTXBUF is not used for 7-bit data and is reset.

24.4.11 UCAXIFG Register

eUSCI_Ax Interrupt Flag Register

Figure 24-22. UCAXIFG Register

15	14	13	12	11	10	9	8
Reserved							
r-0	r-0	r-0	r-0	r-0	r-0	r-0	r-0
7	6	5	4	3	2	1	0
Reserved				UCTXCPTIFG	UCSTTIFG	UCTXIFG	UCRXIFG
r-0	r-0	r-0	r-0	rw-0	rw-0	rw-1	rw-0

Table 24-18. UCAXIFG Register Description

Bit	Field	Type	Reset	Description
15-4	Reserved	R	0h	Reserved
3	UCTXCPTIFG	RW	0h	Transmit complete interrupt flag. UCTXCPTIFG is set when the entire byte in the internal shift register got shifted out and UCAXTXBUF is empty. 0b = No interrupt pending 1b = Interrupt pending
2	UCSTTIFG	RW	0h	Start bit interrupt flag. UCSTTIFG is set after a Start bit was received 0b = No interrupt pending 1b = Interrupt pending
1	UCTXIFG	RW	1h	Transmit interrupt flag. UCTXIFG is set when UCAXTXBUF empty 0b = No interrupt pending 1b = Interrupt pending
0	UCRXIFG	RW	0h	Receive interrupt flag. UCRXIFG is set when UCAXRXBUF has received a complete character. 0b = No interrupt pending 1b = Interrupt pending

eUSCI_A UART Registers**24.4.10 UCAxIE Register**

eUSCI_Ax Interrupt Enable Register

Figure 24-21. UCAxIE Register

15	14	13	12	11	10	9	8
Reserved							
r-0	r-0	r-0	r-0	r-0	r-0	r-0	r-0
7	6	5	4	3	2	1	0
Reserved				UCTXCPTIE	UCSTTIE	UCTXIE	UCRXIE
r-0	r-0	r-0	r-0	rw-0	rw-0	rw-0	rw-0

Table 24-17. UCAxIE Register Description

Bit	Field	Type	Reset	Description
15-4	Reserved	R	0h	Reserved
3	UCTXCPTIE	RW	0h	Transmit complete interrupt enable 0b = Interrupt disabled 1b = Interrupt enabled
2	UCSTTIE	RW	0h	Start bit interrupt enable 0b = Interrupt disabled 1b = Interrupt enabled
1	UCTXIE	RW	0h	Transmit interrupt enable 0b = Interrupt disabled 1b = Interrupt enabled
0	UCRXIE	RW	0h	Receive interrupt enable 0b = Interrupt disabled 1b = Interrupt enabled

Functional Peripherals Registers**2.4.5.5 SCR Register (Offset = D10h) [reset = 00000000h]**

SCR is shown in [Figure 2-55](#) and described in [Table 2-63](#).

System Control Register. Use the System Control Register for power-management functions: signal to the system when the processor can enter a low power state, control how the processor enters and exits low power states.

Figure 2-55. SCR Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-0h							
23	22	21	20	19	18	17	16
RESERVED							
R/W-0h							
15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							
7	6	5	4	3	2	1	0
RESERVED		SEVONPEND		RESERVED		SLEEPDEEP	
R/W-0h		R/W-0h		R/W-0h		R/W-0h	
R/W-0h		R/W-0h		R/W-0h		R/W-0h	

Table 2-63. SCR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-5	RESERVED	R/W	0h	
4	SEVONPEND	R/W	0h	When enabled, this causes WFE to wake up when an interrupt moves from inactive to pended. Otherwise, WFE only wakes up from an event signal, external and SEV instruction generated. The even input, RXEV, is registered even when not waiting for an event, and so effects the next WFE.
3	RESERVED	R/W	0h	
2	SLEEPDEEP	R/W	0h	Sleep deep bit. 0b (R/W) = not OK to turn off system clock 1b (R/W) = Indicates to the system that Cortex-M4 clock can be stopped. Setting this bit causes the SLEEPDEEP port to be asserted when the processor can be stopped.
1	SLEEPONEXIT	R/W	0h	Sleep on exit when returning from Handler mode to Thread mode. Enables interrupt driven applications to avoid returning to empty main application. 0b (R/W) = do not sleep when returning to thread mode 1b (R/W) = sleep on ISR exit
0	RESERVED	R/W	0h	

24.4.4 UCAxMCTLW Register

eUSCI_Ax Modulation Control Word Register

Figure 24-15. UCAxMCTLW Register

15	14	13	12	11	10	9	8
UCBRSx							
rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0
7	6	5	4	3	2	1	0
UCBRFx				Reserved			UCOS16
rw-0	rw-0	rw-0	rw-0	r0	r0	r0	rw-0
Modify only when UCSWRST = 1							

Table 24-11. UCAxMCTLW Register Description

Bit	Field	Type	Reset	Description
15-8	UCBRSx	RW	0h	Second modulation stage select. These bits hold a free modulation pattern for BITCLK.
7-4	UCBRFx	RW	0h	First modulation stage select. These bits determine the modulation pattern for BITCLK16 when UCOS16 = 1. Ignored with UCOS16 = 0. The "Oversampling Baud-Rate Generation" section shows the modulation pattern.
3-1	Reserved	R	0h	Reserved
0	UCOS16	RW	0h	Oversampling mode enabled 0b = Disabled 1b = Enabled

eUSCI_Ax Control Word Register 0

ctlw

Figure 24-12. UCAxCTLW0 Register

15	14	13	12	11	10	9	8
UCPEN	UCPAR	UCMSB	UC7BIT	UCSPB	UCMODEx		UCSYNC
rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0
7	6	5	4	3	2	1	0
UCSSELx	UCRXEIE	UCBRKIE	UCDORM	UCTXADDR	UCTXBRK	UCSWRST	
rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-1
Modify only when UCSWRST = 1							

Table 24-8. UCAxCTLW0 Register Description

Bit	Field	Type	Reset	Description
15	UCPEN	RW	0h	Parity enable 0b = Parity disabled 1b = Parity enabled. Parity bit is generated (UCAxTXD) and expected (UCAxRXD). In address-bit multiprocessor mode, the address bit is included in the parity calculation.
14	UCPAR	RW	0h	Parity select. UCPAR is not used when parity is disabled. 0b = Odd parity 1b = Even parity
13	UCMSB	RW	0h	MSB first select. Controls the direction of the receive and transmit shift register. 0b = LSB first 1b = MSB first
12	UC7BIT	RW	0h	Character length. Selects 7-bit or 8-bit character length. 0b = 8-bit data 1b = 7-bit data
11	UCSPB	RW	0h	Stop bit select. Number of stop bits. 0b = One stop bit 1b = Two stop bits
10-9	UCMODEx	RW	0h	eUSCI_A mode. The UCMODEx bits select the asynchronous mode when UCSYNC = 0. 00b = UART mode 01b = Idle-line multiprocessor mode 10b = Address-bit multiprocessor mode 11b = UART mode with automatic baud-rate detection
8	UCSYNC	RW	0h	Synchronous mode enable 0b = Asynchronous mode 1b = Synchronous mode
7-6	UCSSELx	RW	0h	eUSCI_A clock source select. These bits select the BRCLK source clock. 00b = UCLK 01b = ACLK

uCUnit.h

system.c

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