Verilog Behavioral Modeling Part-IV

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🟢 **Continuous Assignment Statements**

Continuous assignment statements drive nets (wire data type). They represent structural connections.

- They are used for modeling Tri-State buffers.
- They can be used for modeling combinational logic.
- They are outside the procedural blocks (always and initial blocks).
- The continuous assign overrides any procedural assignments.
- The left-hand side of a continuous assignment must be net data type.

syntax : assign (strength, strength) **#(delay)** net = expression;

✦ Example - One bit Adder

```
1  module adder_using_assign ();
2  reg a, b;
3  wire sum, carry;
4
5  assign #5 {carry,sum} = a+b;
6
7  initial begin
8    $monitor (" A = %b  B = %b CARRY = %b SUM = %b",a,b,carry,sum);
9    #10 a = 0;
10   b = 0;
11   #10   a = 1;
12   #10   b = 1;
13   #10   a = 0;
14   #10   b = 0;
15   #10 $finish;
16 end
17
18 endmodule
```

You could download file adder_using_assign.v here

✦ Example - Tri-state buffer

```
1  module tri_buf_using_assign();
2  reg data_in, enable;
3  wire pad;
4
5  assign pad = (enable) ? data_in : 1'bz;
6
7  initial begin
8    $monitor ("TIME = %g ENABLE = %b DATA : %b PAD %b",
9      $time, enable, data_in, pad);
10   #1  enable = 0;
```

```
11   #1   data_in = 1;
12   #1   enable = 1;
13   #1   data_in = 0;
14   #1   enable = 0;
15   #1   $finish;
16   end
17
18   endmodule
```

You could download file tri_buf_using_assign.v here

🟢 Propagation Delay

Continuous Assignments may have a delay specified; only one delay for all transitions may be specified. A minimum:typical:maximum delay range may be specified.

◆ Example - Tri-state buffer

```
1   module tri_buf_using_assign_delays();
2   reg data_in, enable;
3   wire pad;
4
5   assign #(1:2:3) pad = (enable) ? data_in : 1'bz;
6
7   initial begin
8     $monitor ("ENABLE = %b DATA : %b PAD %b",enable, data_in,pad);
9     #10   enable = 0;
10    #10   data_in = 1;
11    #10   enable = 1;
12    #10   data_in = 0;
13    #10   enable = 0;
14    #10   $finish;
15   end
16
17   endmodule
```

You could download file tri_buf_using_assign_delays.v here