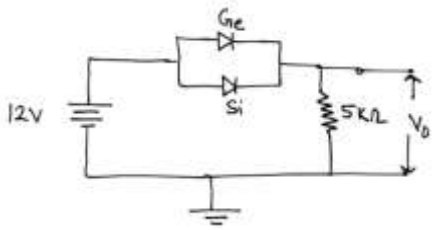
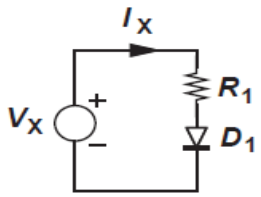
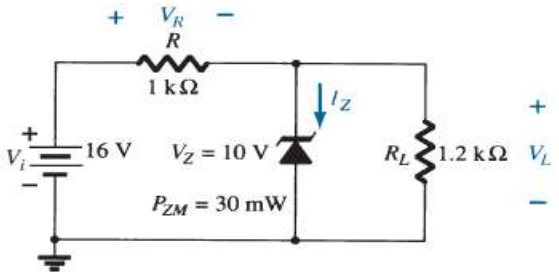
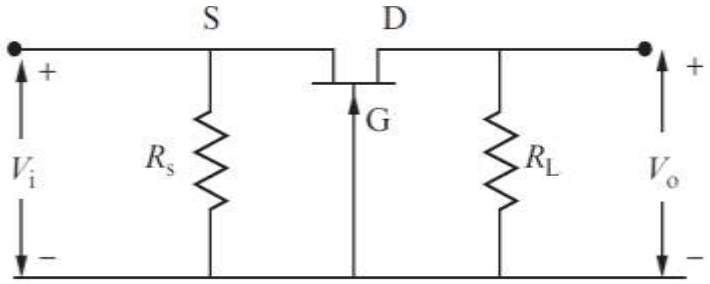
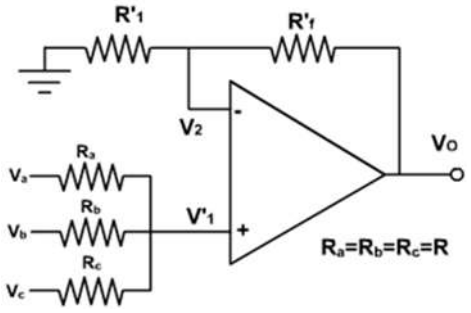
Sub Code: ECT-001 **ROLL NO……..……..**

II SEMESTER EXAMINATION, 2022 – 23
I Year–B. Tech.
BASIC ELECTRONICS ENGINEERING

Duration: 3:00 hrs **Max Marks: 100**

Note: - Attempt all questions. All Questions carry equal marks. In case of any ambiguity or missing data, the same may be assumed and state the assumption made in the answer.

Q 1.	Answer any four parts of the following. a) Calculate the electrons and hole concentrations in an N-type semiconductor with a $10^{17}cm^{-3}$ doping concentration. b) Explain the working of Tunnel diode with suitable energy band diagram and I-V characteristics. c) Why is the biasing done in amplifier circuits? d) Explain the Zener and Avalanche breakdown mechanism with the help of suitable diagram? e) For an n-channel JFET, V_P= −5V, I_{DSS}= 8mA , and VGS= −2.5 V. Determine (i) I_D (ii) and (iii) gm. f) Find the binary equivalent of (17E.F6)16 and the hex equivalent of (1011001110.011011101)2.	5x4=20
Q 2.	Answer any four parts of the following. a) In the following figure, initially, the Ge diode is forward-biased. Suddenly, the Ge diode connection direction is reversed. Find the change in output voltage (Vo). (Assume: Cut-in voltage of the Ge and Si diodes is 0.3V and 0.7V, respectively, and the breakdown voltage of the Ge diode is very high).  Fig.1. b) Consider silicon at T = 300 K doped with arsenic atoms at a concentration of $N_d = 8 \times 10^{15}$ cm^{-3} . Assume mobility values of μ_n = 1350 $cm^2/V–s$ and μ_p = 480 $cm^2/V–s$. Calculate the conductivity of the semiconductor material. c) Plot the I/V characteristic of the circuit shown in Fig.2. Assume the cut-in voltage of diode D1 is 0.7V.  Fig.2. d) An npn transistor is biased in the forward-active mode. The base current is I_B = 5.0μA and the collector current is I_C = 0.62 mA. Determine I_E , β, and α. e) Explain the working of n-channel enhancement -type MOSFETs.	5x4=20

	f) Write the ideal characteristics of an Op-Amp.	
Q 3.	Answer any two parts of the following. a) Explain the operation of Full wave bridge rectifier with neat and clean diagram. Also derive expression of the Ripple Factor for this rectifier. Mention the Advantages of bridge rectifier over centre tapped rectifier. b) For the Zener diode network of Fig. 3, determine V_L, V_R, I_Z, and power dissipated by the Zener diode (P_Z)  Fig.3. c) Draw the common base circuit and sketch the input and output characteristics curves. Also explain different operating regions by indicating them on characteristic curves.	10x2= 20
Q 4.	Answer any two parts of the following. a) Derive the expressions of voltage gain, input impedance, output impedance of an n-channel JFET based comman source amplifier. b) Describe the construction and principle of operation of n-channel JFETs and draw the input and output Characteristic curves for device. c) For the CG amplifier circuit shown in Fig.4, calculate Ri, A, and Ro. The FET has gm =0.0025 mhos, rds = 50 kΩ, R_L = 4 kΩ and Rs=1 kΩ.  Fig.4 : AC circuit of CG amplifier	10x2= 20
Q 5.	Answer any two parts of the following. a) Find the output voltage of non-inverting summer shown in Fig-4. Assume Ra=Rb=Rc=R  Fig.4 b) Draw the circuit of CE amplifier, including biasing network. Obtain its ac circuit. Draw the ac circuit replacing the transistor by its low-frequency h-parameter model. Derive expressions for Current gain (A_I), Input resistance (Ri), Voltage gain (A_V), Overall voltage gain (A_{VS}) and Output impedance(R_O). c) (i) Reduce the Boolean expression $Y = \overline{A}\overline{B}\overline{C}+\overline{A}BC +ABC+A\overline{B}\overline{C}$ using Boolean laws. (ii) For the fig.5, derive the Boolean expression of Y.	10x2= 20

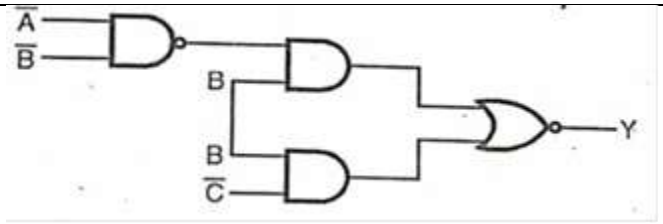


Fig.5

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