Sub Code: TEC-101/201, BECT101 **ROLL NO……..……..**

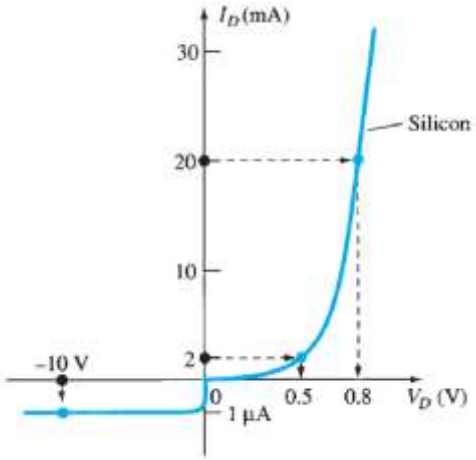
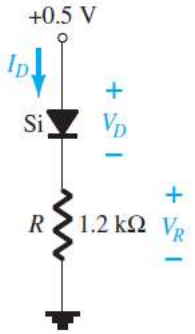
1st /2nd SEMESTER EXAMINATION, 2022 – 23

First Year, B. Tech. – Common to All Branch

FUNDAMENTAL OF ELECTRONICS ENGINEERING

Duration: 3:00 hrs **Max Marks: 100**

Note: - Attempt all questions. All Questions carry equal marks. In case of any ambiguity or missing data, the same may be assumed and state the assumption made in the answer.

Q 1.	Answer any four parts of the following. a) Describe the difference between *n* -type and *p* -type semiconductor materials. Define an intrinsic material, a negative temperature coefficient, and covalent bonding. b) Compare P-N junction diode and zener diode on the basis of: (i) Symbol (ii) Direction of conduction (iii) Reverse breakdown (iv) Application (v) Resistance in reverse biased condition c) What is an LED? Explain its working principle. Write the advantages, and application of LED. d) Draw VI characteristics of PN junction diode and explain it. e) Determine the dc resistance levels for the diode of Fig. 1 at (i) I_D = 2 mA (low level) (ii) I_D = 20 mA (high level) (iii) V_D = —10 V (reverse-biased)  Fig. 1 f) For the series diode configuration of Fig. 2, determine V_D , V_R , and I_D.  Fig. 2	5x4=20

Q 2.	Answer any four parts of the following. a) With help of neat circuit diagrams, explain the working of a full wave bridge rectifier. b) Determine the output waveform for the sinusoidal input of Fig. 3?	5x4=20

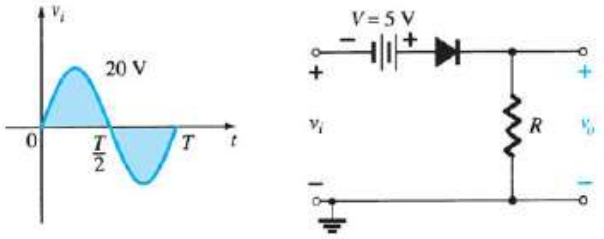


Fig. 3

c) Determine v_o for the network of Fig. 4 for the input indicated.

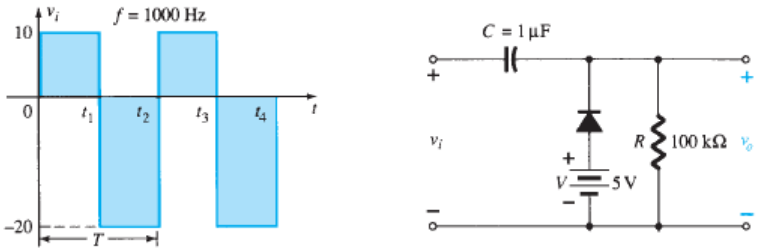


Fig. 4

d) For the Zener diode network with $R_L = 3$ kΩ of Fig. 5, determine V_L, V_R, V_Z, P_Z.

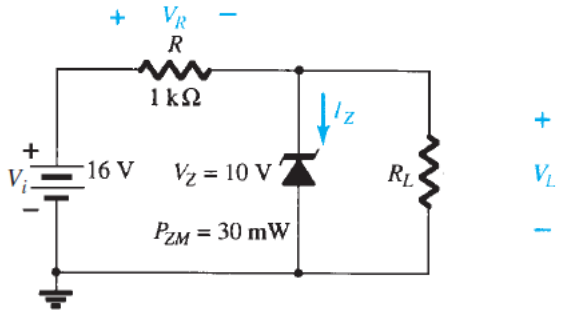


Fig. 5

e) Draw the circuit and explain the working of the voltage Quadrupler circuit.

f) Define the following terms with respect to the rectifier:

(i) Ripple factor (ii) Rectification efficiency (η)

(iii) Transformer Utilization Factor (TUF) (iv) Peak Inverse Voltage (PIV)

Q 3.	Answer any two parts of the following. a) Determine the following for the fixed-bias configuration of Fig. 6 (i) I_{C_Q} and I_{B_Q} (ii) V_{CE_Q} (iii) V_B and V_C (iv) V_{BC}	10x2= 20

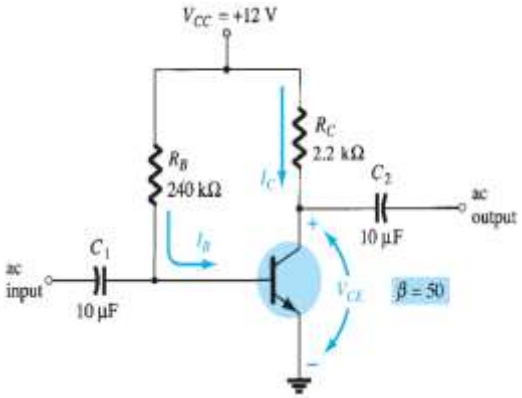
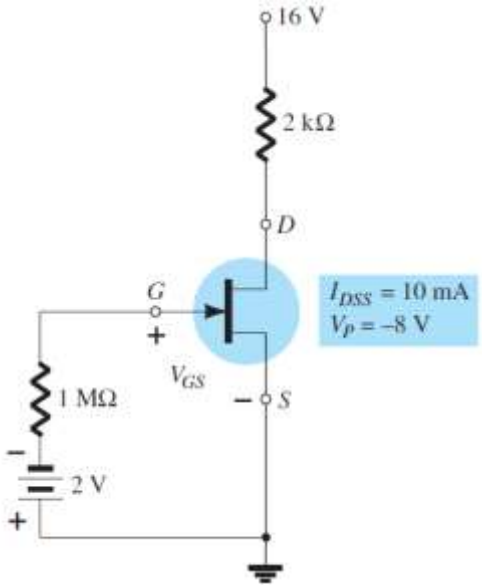


Fig. 6

	b) Define α and β with respect to BJT and derive the relationship between them. A transistor having $\beta = 100$ and reverse saturation current $I_{CEO} = 150\ \mu A$ is operated in CE mode. If the base current is 0.2 mA. Calculate I_E, I_C and α. c) Compare CB, CE and CC configuration on the basis of: (i) Input impedance (ii) Output impedance (iii) Current gain (iv) Voltage gain (v) Phase angle (vi) Power gain (vii) Application	
Q 4.	Answer any two parts of the following. a) Sketch and explain the construction of n-channel JFET and also explain its working. b) Explain working principle of N-channel depletion type MOSFET with construction diagram. Also draw its transfer and drain characteristics. c) Determine the following for the network of Fig. 7 (i) V_{GS_Q} (ii) I_{D_Q} (iii) V_{DS} (iv) V_D (v) V_G (vi) V_S  Fig. 7	10x2= 20
Q 5.	Answer any two parts of the following. a) Minimize using K-map and realize using NOR gates only. $F(A,B,C,D) = \prod(3,4,5,7,9,13,14,15).d(0,2,8)$ b) Draw and explain the working of inverting, non-inverting, and summing amplifier using OP-AMP. c) Perform following operation as indicated: (i) Convert $(25.125)_{10}$ into Haxadecimal number. (ii) Determine the base of following: $(312)_B = (54)_{10}$ (iii) Write the truth table of two input X-OR gate and two input X-NOR gate. (iv) Simplified the boolean equation $X = [(A + \bar{B})(B + C)]B$ (v) Draw the circuit diagram to implement the following equation: $X = [(A + B)(\bar{B} + C)]$	10x2= 20

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