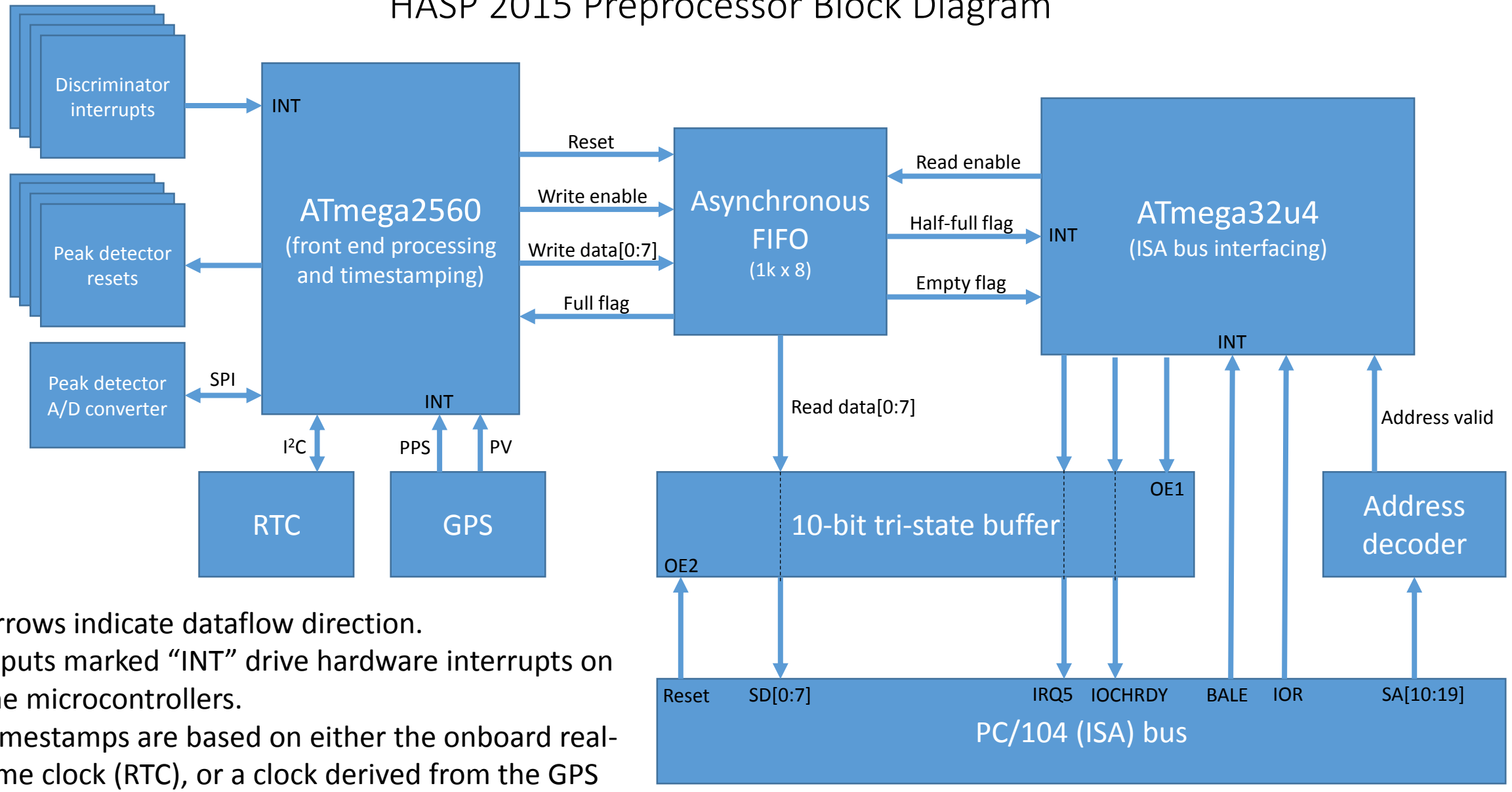
HASP 2015 Preprocessor Block Diagram



- Arrows indicate dataflow direction.
- Inputs marked “INT” drive hardware interrupts on the microcontrollers.
- Timestamps are based on either the onboard real-time clock (RTC), or a clock derived from the GPS pulse-per-second output (PPS). This is selected by user input (selector switch on the board).

Notes

- Operation is as follows: ATmega2560 uses discriminator interrupts to log event data (detector number, timestamp, energy) to the asynchronous first-in first-out (FIFO) memory. When FIFO reaches half-full (512 bytes), the half-full flag interrupts the ATmega32u4. This microcontroller then issues an interrupt request (IRQ) over the ISA bus to request service from the main flight computer. The interrupt handler on the flight computer then initiates an IO port read of either 256 or 512 bytes (TBD) over the ISA bus beginning at the base address 0x800. The BALE line on the ISA bus goes high to signal the start of the cycle, which interrupts the ATmega32u4. The interrupt handler checks the output of the address decoder to determine whether or not data is being requested from this device. The address decoder outputs true if the address is in the range 0x800-0xBFF, and false otherwise. If the address is valid, the ATmega32u4 then checks for the IOR command line, and if it is asserted, continues with the data transfer. The ATmega32u4 completes the data transfer by setting the read enable on the FIFO and the output enable on the tri-state buffer to send one byte of data. If more time is needed than the standard IO cycle allows, then the ATmega32u4 asserts the IOCHRDY line. This process, beginning from the assertion of BALE, repeats for every byte of the transfer.
- The ISA reset line, controlled by the bus master, can tri-state all inputs to the bus on the preprocessor board independently of the ATmega32u4.
- The SRDY (a.k.a. NOWS) line on the ISA bus is not controlled by the ATmega32u4. Thus all ISA transfer cycles will have either “standard” or “ready” timing. “Ready” timing is preferred as it allows the ATmega32u4 to dictate when the data on the bus must be valid.

Notes

Requirements for IO on the microcontrollers:

ATmega2560

- GPS PPS and discriminators (all four channels) all drive interrupts
- A/D converter on SPI bus at 8 MHz
- RTC on I^2C bus (possibly software I^2C)
- GPS position valid (PV) on any digital input pin
- Peak detector resets and SPI chip select must all be on same port (all outputs)
- FIFO write enable and reset must be on same port (output)
- FIFO write data[0:7] must all be on same port (output)
- FIFO full flag on any digital input pin
- Clock source select (RTC/GPS switch) on any digital input pin

ATmega32u4

- FIFO read enable, tri-state buffer output enable (OE1), IOCHRDY, and ISA IRQ must all be on same port (output)
- FIFO half-full flag and ISA BALE drive interrupts
- IOR and address decoder output must be on same port (input)
- FIFO empty flag on any digital input pin