```
1  ------------------------
2  --     D-FlipFlip      --
3  ------------------------
4  entity FF is
5    port(D:    in bit;
6         Q:   out bit;
7         CLK:  in bit);
8  end FF;
9
10 architecture behv of FF is
11 begin
12   process(CLK)
13   begin
14     if CLK = '1' then
15        Q <= D;
16     end if;
17   end process;
18 end behv;
19
20 ------------------------
21 --     CRC decoder     --
22 ------------------------
23 entity CRC6RX is
24   port(ZOUT: out bit;
25        V:    in bit;
26        CLK:  in bit;
27        ERROR: out bit);
28 end CRC6RX;
29
30 architecture behv of CRC6RX is
31
32 component FF
33   port(D:    in bit;
34        Q:   out bit;
35        CLK:  in bit);
36 end component;
37
38 signal H: bit_vector(5 downto 0);
39 signal K: bit_vector(5 downto 0);
40 signal Z: bit;
41
42 begin
43
44 K(0) <= Z XOR V;
45 D0:FF port map (K(0), H(0), CLK);
46 D1:FF port map (H(0), H(1), CLK);
47 K(2) <= Z XOR H(1);
48 D2:FF port map (K(2), H(2), CLK);
49 K(3) <= Z XOR H(2);
50 D3:FF port map (K(3), H(3), CLK);
51 D4:FF port map (H(3), H(4), CLK);
52 K(5) <= Z XOR H(4);
53 D5:FF port map (K(5), H(5), CLK);
54
55 Z <= H(5);
56 ZOUT <= Z;
57 ERROR <= H(0) OR H(1) OR H(2) OR H(3) OR H(4) OR H(5);
58
59 end behv;
```