

```
1  -----
2  --      D-FlipFlip      --
3  -----
4  entity FF is
5      port(D:      in bit;
6            Q:      out bit;
7            CLK:    in bit);
8  end FF;
9
10 architecture behv of FF is
11 begin
12     process(CLK)
13     begin
14         if CLK = '1' then
15             Q <= D;
16         end if;
17     end process;
18 end behv;
19
20 -----
21 --      CRC encoder      --
22 -----
23 entity CRC6TX is
24     port(Z:      in bit;
25           V:      out bit;
26           CLK:    in bit);
27 end CRC6TX;
28
29 architecture behv of CRC6TX is
30
31 component FF
32     port(D:      in bit;
33           Q:      out bit;
34           CLK:    in bit);
35 end component;
36
37 signal H: bit_vector(5 downto 0);
38 signal K: bit_vector(5 downto 0);
39
40 begin
41
42 D0:FF port map (Z,      H(0), CLK);
43 D1:FF port map (H(0), H(1), CLK);
44 K(2) <= Z XOR H(1);
45 D2:FF port map (K(2), H(2), CLK);
46 K(3) <= Z XOR H(2);
47 D3:FF port map (K(3), H(3), CLK);
48 D4:FF port map (H(3), H(4), CLK);
49 K(5) <= Z XOR H(4);
50 D5:FF port map (K(5), H(5), CLK);
51
52 V <= Z XOR H(5);
53
54 end behv;
```