Lab4
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a) Time usage: 8 hours each person
b) Table 1:

Cycle	reset	pc	Instr	branch	srca	srcb	aluresult	zero	pcsrc	Writedata	memwrite	read data
1	1	00	addi $2,$0,5 20020005	0	0	5	5	0	0	0	0	x
2	0	04	addi $3,$0,12 2003000c	0	0	c	c	0	0	0	0	x
3	0	08	addi $7,$3,-9 20067fff7	0	C	-9	3	0	0	0	0	x
4	0	0C	or $4 $7 $2	0	3	5	7	0	0	5	0	X
5	0	10	and $5,$3,$4	0	C	7	4	0	0	7	0	X
6	0	14	add $5,$5,$4	0	4	7	b	0	0	7	0	X
7	0	18	beq $5,$7,end	1	b	3	8	0	0	3	0	X
8	0	1C	slt $4,$3,$4	0	C	7	0	1	0	7	0	X
9	0	20	beq $4,$0,around	1	0	0	0	1	1	0	0	X
10	0	24	slt $4,$7,$2	0	3	5	1	0	0	5	0	X
11	0	28	add $7,$4,$5	0	1	b	c	0	0	b	0	X
12	0	2c	sub $7,$7,$2	0	C	5	7	0	0	5	0	X
13	0	30	sw $7,68($3)	0	C	44	50	0	0	7	1	X
14	0	34	lw $2,80($0)	0	0	50	50	0	0	5	0	7
15	0	38	j end	0	0	0	0	1	0	0	0	X
16	0	3C	sw $2,84($0)	0	0	54	54	0	0	7	1	X

Table 1. First sixteen cycles of executing the test code of Fig. 7.60 in the textbook

c) Simulation waveforms

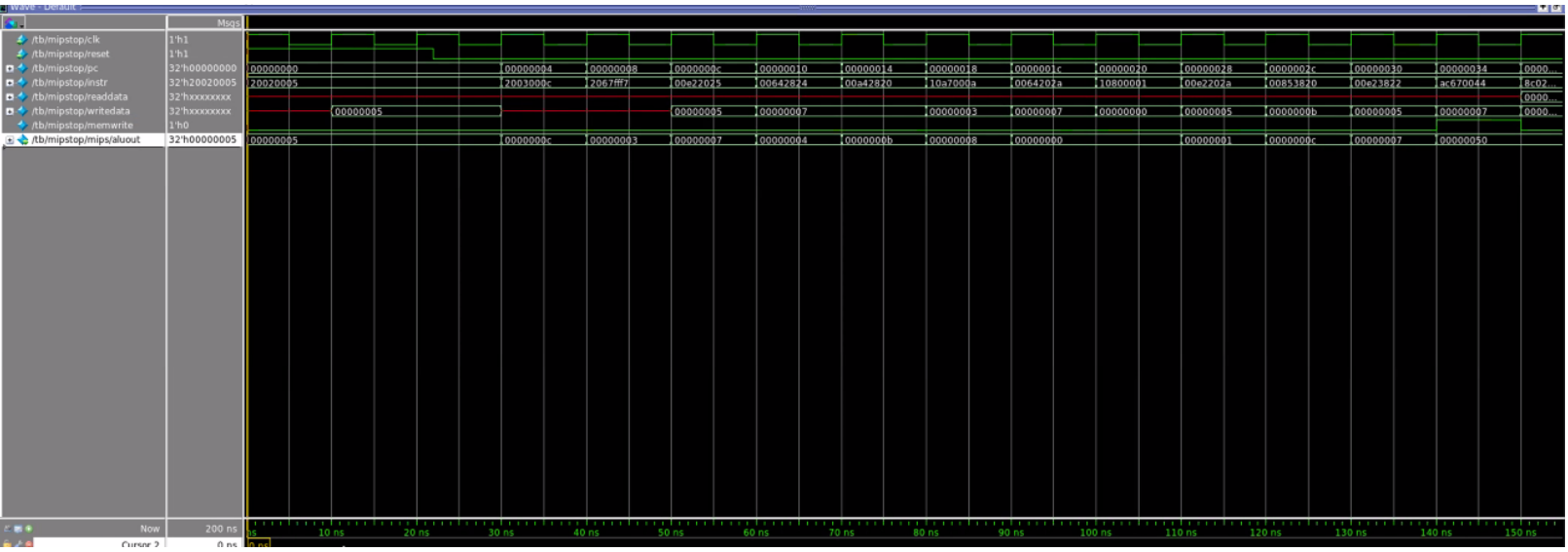
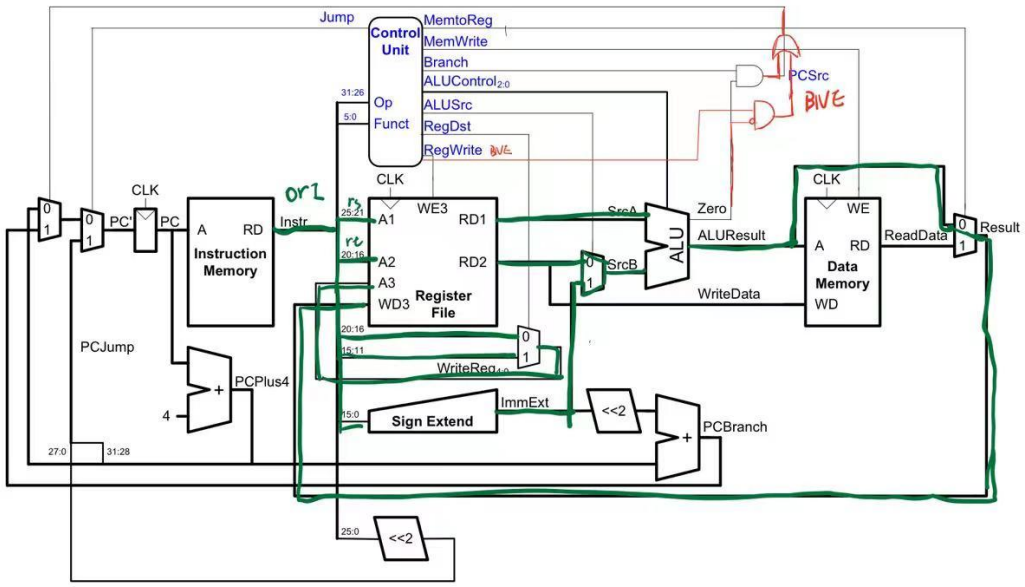


Fig.1 single cycle MIPS processor waveform

Fig.2 single cycle MIPS processor waveform

It writes the correct value to address 84: the value of writedata at the end is 00000007, as expected.

d)



Single-cycle MIPS processor

Fig.3 data path and schematic of BNE and ORI implementation

e) Code: attached in the zip file, also linked at the end

f) Completed table 2 and 3

Table 2. Extended functionality for the main decoder:

Instruction	$Op_{5:0}$	RegWrite	RegDst	AluSrc	Branch	MemWrite	MemtoReg	$ALUOp_{1:0}$	Jump	BNE		
R-type	000000	1	1	0	0	0	0	10	0	0		
lw	100011	1	0	1	0	0	1	00	0	0		
sw	101011	0	X	1	0	1	X	00	0	0		
beq	000100	0	X	0	1	0	X	01	0	0		
addi	001000	1	0	1	0	0	0	00	0	0		
j	000010	0	X	X	X	0	X	XX	1	0		
ori	001101	1	0	1	0	0	0	11	0	0		
bne	000101	0	X	0	1	0	X	01	0	1		

Table 3. Extended functionality for the ALU decoder:

$ALUOp_{1:0}$	Meaning
00	Add
01	Subtract
10	Look at `funct` field
11	or

Fig.4 completed table 2 and 3

g) Memfile2.dat: attached in the zip file

12 lines (12 sloc) | 107 Bytes

```
1   34088000
2   20098000
3   350a8001
4   11090005
5   0128582a
6   15600001
7   08000009
8   01485022
9   350800ff
10  016a5820
11  01484022
12  ad680052
```

h) Image of simulation

Fig5. single cycle MIPS processor waveform with bne and ori

In the final sw instruction, the data value is 0000001 and the address is invalid because there are only 64 lines in the memory file.

Link to git repository: https://github.com/HBzhainan-wzw/ECE154A_Lab4
Link to google doc:
https://docs.google.com/document/d/1h4wzuar8gBNxbDvFiJ4ZiycKzGo-aQtSozugiOzgYK4/edit