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DESCRIPTION OF STATES

S0:

PC \rightarrow MEM_A
MEM_D \rightarrow IR

S1:

IR(11-9) \rightarrow RF_A1
IR(8-6) \rightarrow RF_A2
RF_D1 \rightarrow T1
RF_D2 \rightarrow T2

S1 = ADD, NDV, BEQ

S2:

T1 \rightarrow ALU_A
T2 \rightarrow ALU_B
ALU_C \rightarrow T1

S2 = compute addition (Temp1 \leftarrow Temp1 + Temp2)

S3:

$IR(5-3) \rightarrow RF-A3$

$T1 \rightarrow RF-D3$

modify c f z

S3 = assign to RF-A3 (modify c, z)

S4:

$PC \rightarrow ALU-A$

$T1 \rightarrow ALU-B$

$ALU-C \rightarrow PC$

S4 = next instruction, go to S0

S5:

$IR(11-9) \rightarrow RF-A1$

$RF-D1 \rightarrow T1$

$IR(5-0) \rightarrow T2$

S5 = ADI

S6
 IR(8-6) → RF-A3
 T1 → RF-D3

Assign to RF-A3

S7
 T1 → ALU-A
 T2 → ALU-B
 ALU-C → T1
 NAND

Temp1 ← Temp1 .nand Temp2

S8
 T1 → RF-D3
 IR(5-3) → RF-A3
 MODIFY Z

assign to RF-A3 modify Z

S9
 IR(11-9) → RF-A1
 RF-D1 → T1

LA and SA control

S10
 T1 → MEM-A
 MEM-D → RF-D3
 T3(1-0) → RF-A3
 T1 → ALU-A
 +1 → ALU-B
 ALU-C → T1

LA counter and update for R0 to R7

S11
 T3 → ALU-A
 T1 → ALU-B
 ALU-C → T3

LA counter and update for R0 to R7

S12

$T1 \rightarrow \text{Mem}_A$
 $T3(0) \rightarrow \text{RF_A1}$
 $\text{RF_D1} \rightarrow \text{Mem}_D$
 $T1 \rightarrow \text{Alu}_A$
 $+1 \rightarrow \text{Alu}_B$
 $\text{Alu}_C \rightarrow T1$

S13

$T1 \rightarrow \text{Alu}_A$
 $T2 \rightarrow \text{Alu}_B$
 $\text{IR}(5-0) \rightarrow T2$
 $\text{XOR}(T1) \rightarrow Z$

S14

$\text{PC} \rightarrow \text{Alu}_A$
 $T2 \rightarrow \text{Alu}_B$
 $\text{Alu}_C \rightarrow \text{PC}$

S15

$\text{IR}(11-9) \rightarrow \text{RF_A3}$
 $\text{IR}(8-0) \rightarrow \text{RF_D3}$

S16

$\text{IR}(8-6) \rightarrow \text{RF_A2}$
 $\text{RF_D2} \rightarrow T1$
 $\text{IR}(5-0) \rightarrow T2$

S17

$T1 \rightarrow \text{Mem}_A$
 $\text{Mem}_D \rightarrow \text{RF_D3}$
 $\text{IR}(11-9) \rightarrow \text{RF_A3}$

Description of corresponding states

SA counter & update for R0 to R7

BEQ (Condition if $\text{Temp1} = \text{Temp2}$)

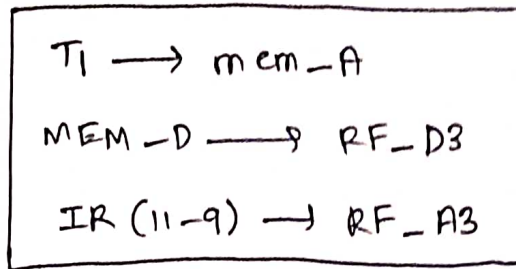
for BEQ, next PC = PC + imm.

LHI (store MSB)

LW & SW

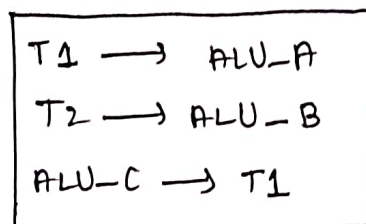
LW (S16 \rightarrow S2 \rightarrow S17) \rightarrow S4 \rightarrow S0.

★ S17 : state 17



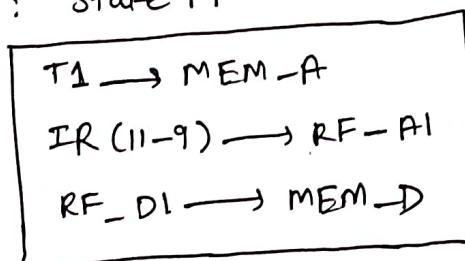
Description: LW ($S16 \rightarrow S2 \rightarrow S17$) $\rightarrow S4 \rightarrow S0$

★ S18 : state 18



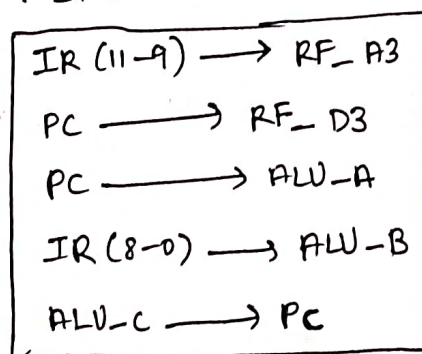
Description: SA counter and update for R0 to R7.

★ S19: state 19



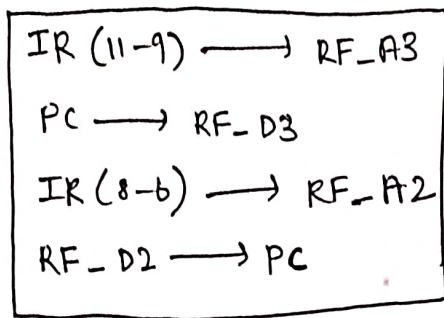
Description: SW ($S16 \rightarrow S2 \rightarrow S19$) $\rightarrow S4 \rightarrow S0$

★ S20 : State 20

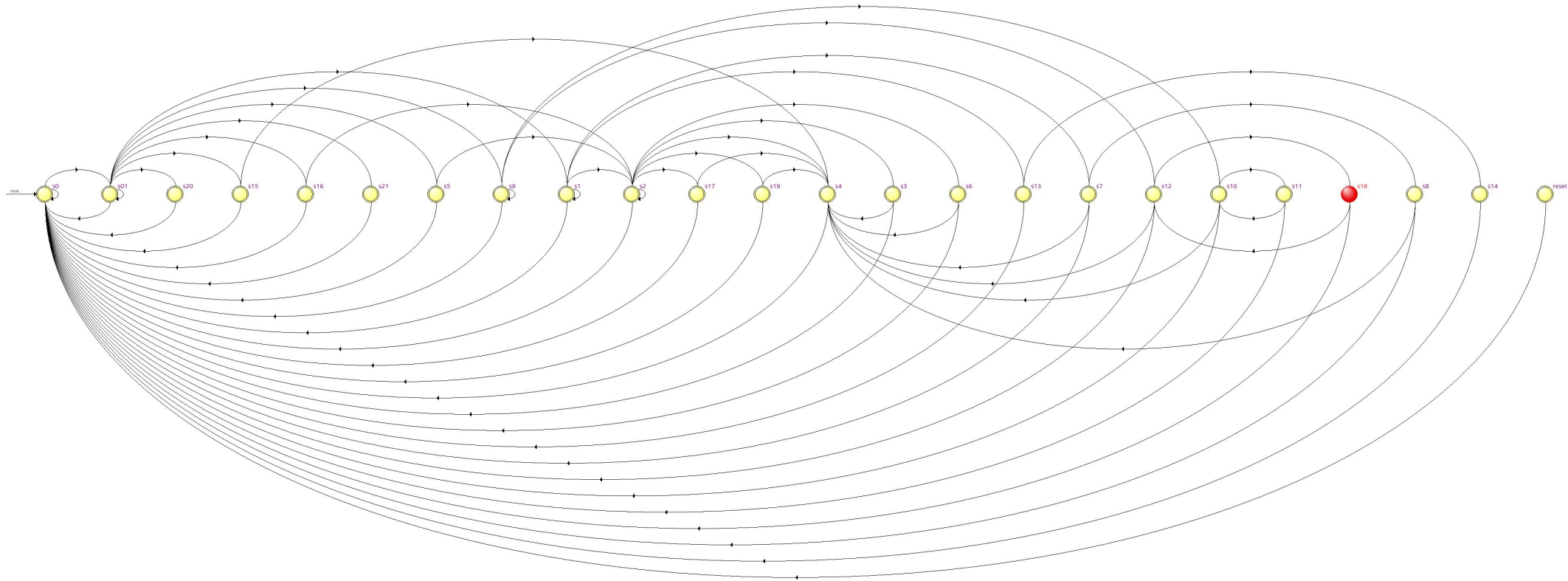


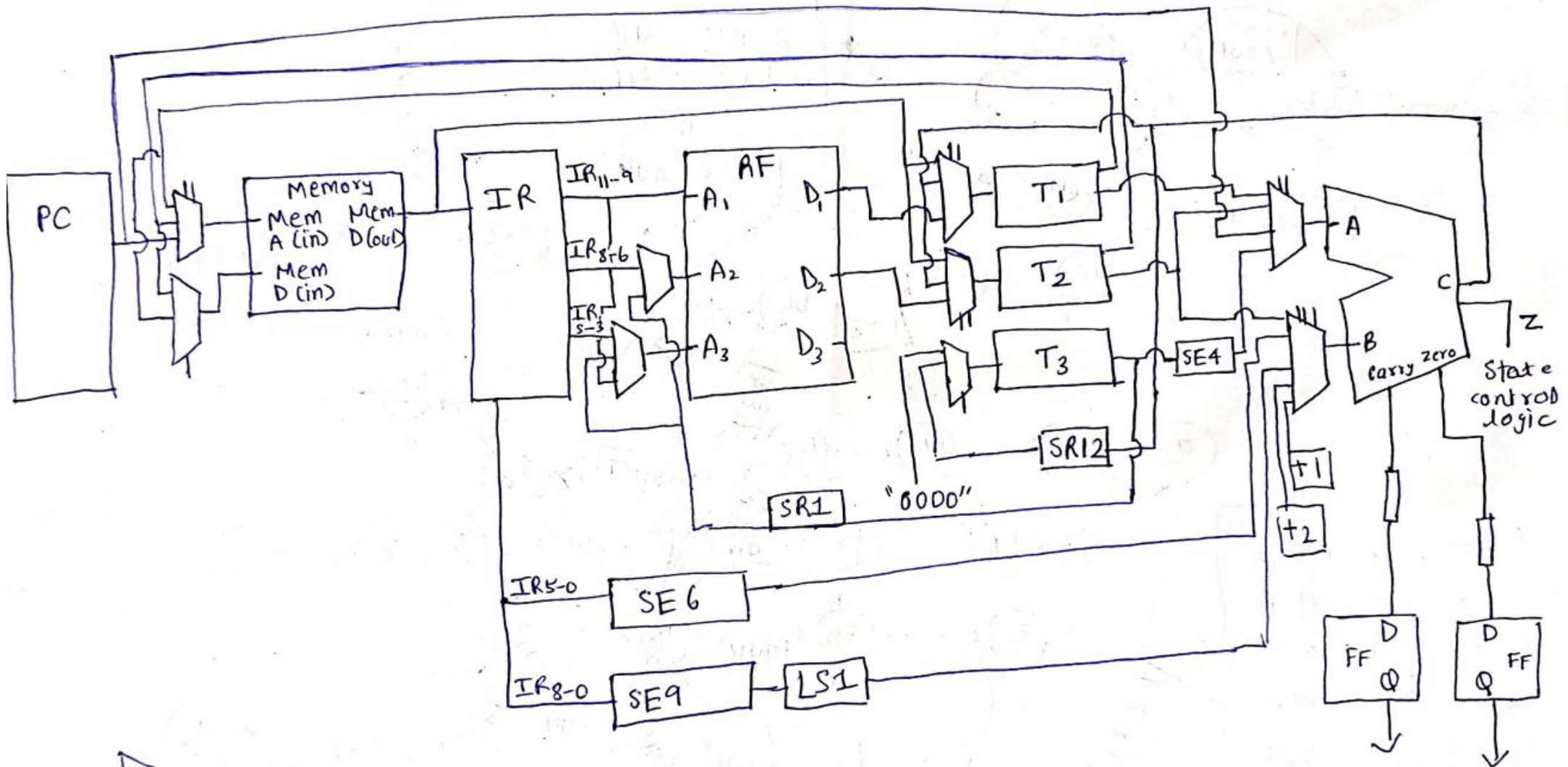
Description: JAL (next PC = PC + immediate)

* 821



description: JLR (next PC = address in reg B)





≡ MUX

≡ ALU

* ALU has been modified to give another outputs: carry and zero flags as well.

To state control logic