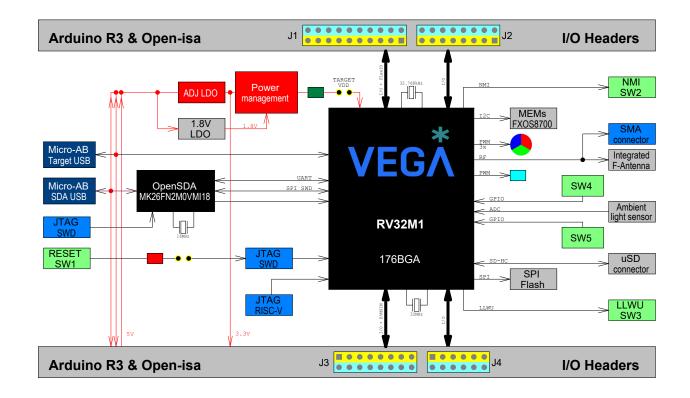
		4	3	2	
Table of Contents					
BLOCK DIAGRAM	Sheet 2				
MCU INTERFACE 1	Sheet 3				
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OPENSDA INTERFACE	Sheet 5				
ARDUINO HEADERS	Sheet 6				
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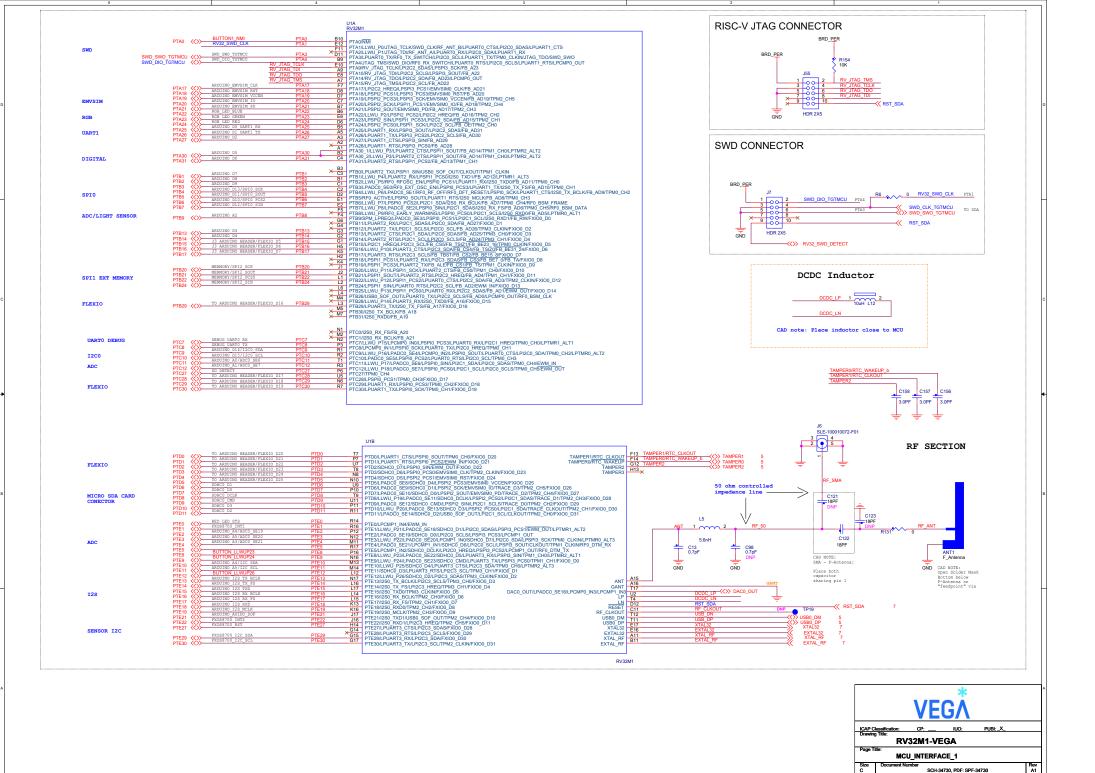
RV32M1-VEGA

VEG [*]			www.open-isa.org							
Designer: Antonio Quiroz	Drawin		ation: CP:	п	JO:	х	PUBI:			
Drawn by: Antonio Quiroz	Page T	Page Title: Table of Contents, Revisions								
Approved: Alistair M.	Size C	Document Number SCH-34730, PDF: SPF-34730						Re A		
	Date:	Wednesday, Nover	mber 21, 2018	Sheet	1	of	-7	_		

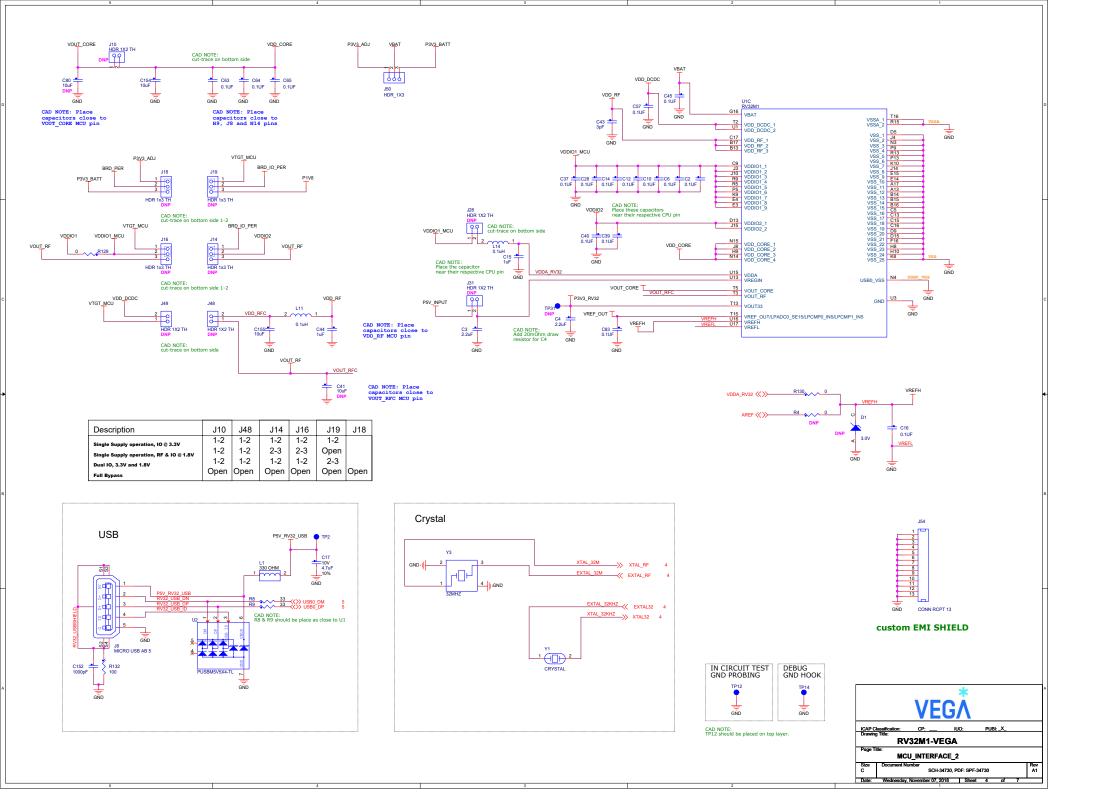
- Unless Otherwise Specified:
 All resistors are in ohms, 5%
 All voltages are DC
 All polarized capacitors are aluminum electrolytic
- Interrupted lines coded with the same letter or letter combinations are electrically connected.
- 3. Device type number is for reference only. The number varies with the manufacturer.
- 4. Special signal usage:
 - _B Denotes Active-Low Signal
 - <> or [] Denotes Vectored Signals
 - Green text Denotes Extra Notes to be considered.
- 5. Interpret diagram in accordance with American National Standards Institute specifications, current revision, with the exception of logic block symbology.

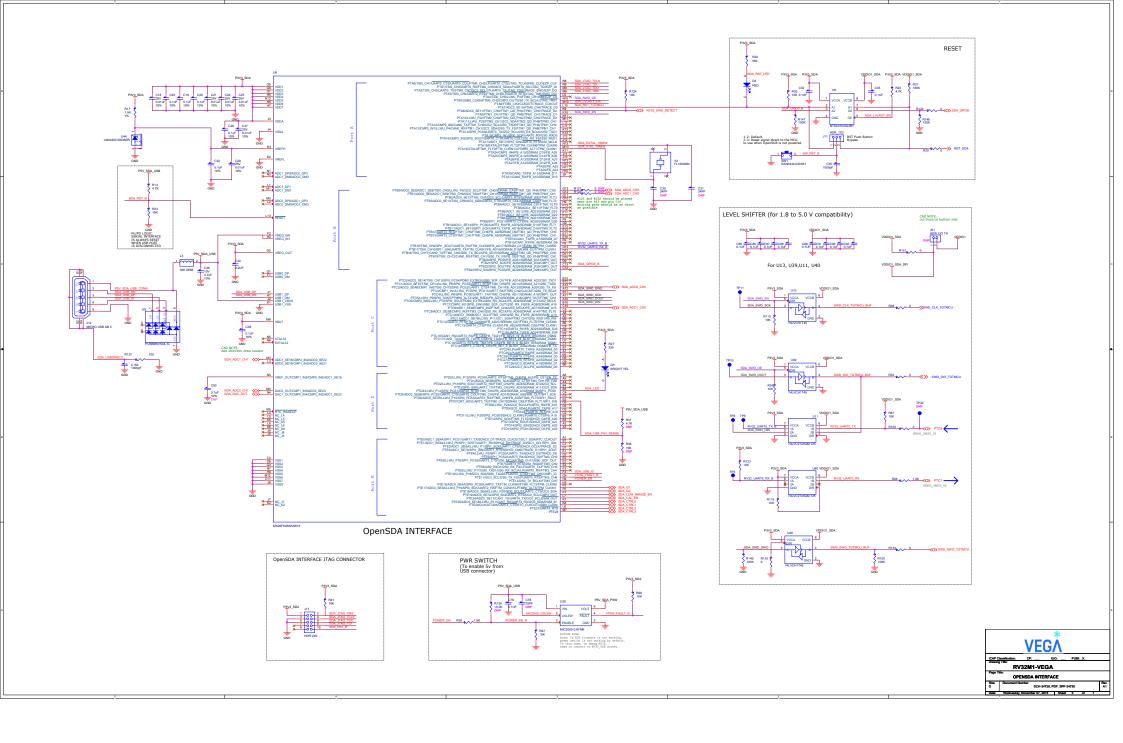


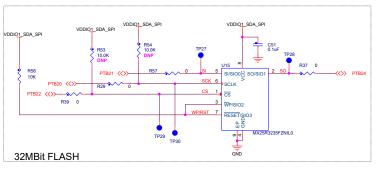


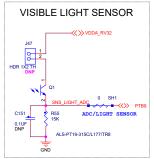


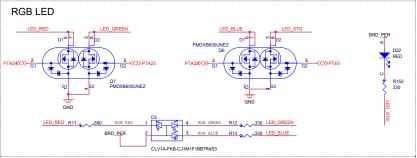
Wednesday, November 07, 2018 Sheet 3

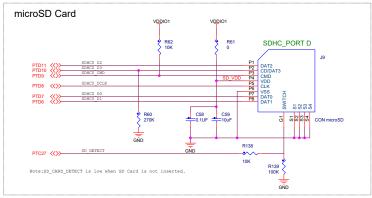


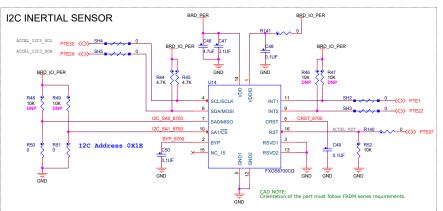


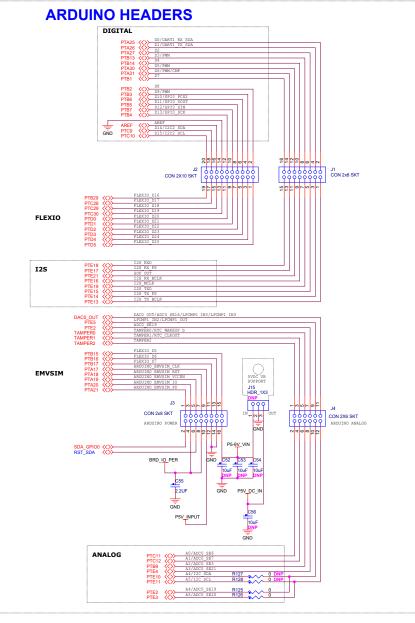


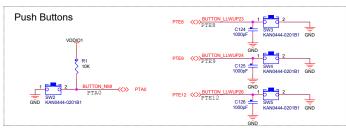




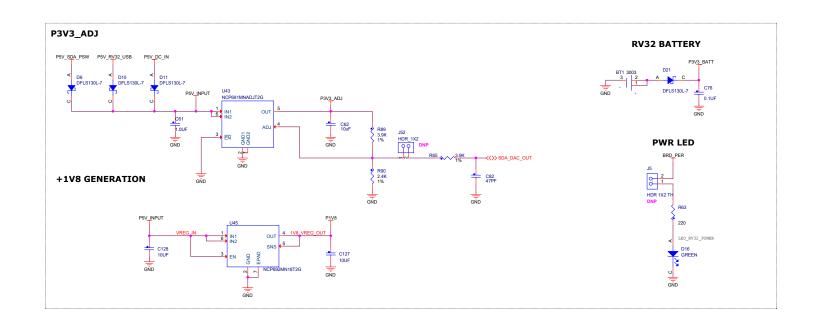












Circuitry for future enhancements

