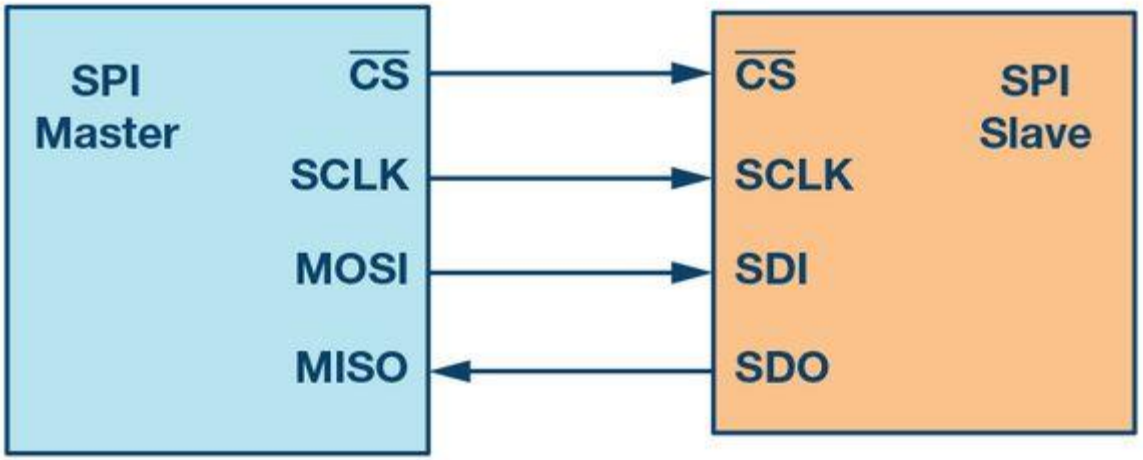
SPI Bus Protocol

SPI bus

- Serial Peripherial Interface (SPI) – developed by Motorola in the mid-1980's
- One of the most widely used interfaces between microcontrollers and peripheral ICs
  - Sensors
  - ADCs
  - DACs
  - Shift registers
  - SRAM
- SPI characteristics
  - Synchronous
  - Full-duplex
  - Master-slave
  - Rising or falling edge
  - 3-wire or 4-wire
  - 8-bit, 16-bit, or larger word sized transfers
  - Operates at SYSCLK/2 up to 12.5MHz

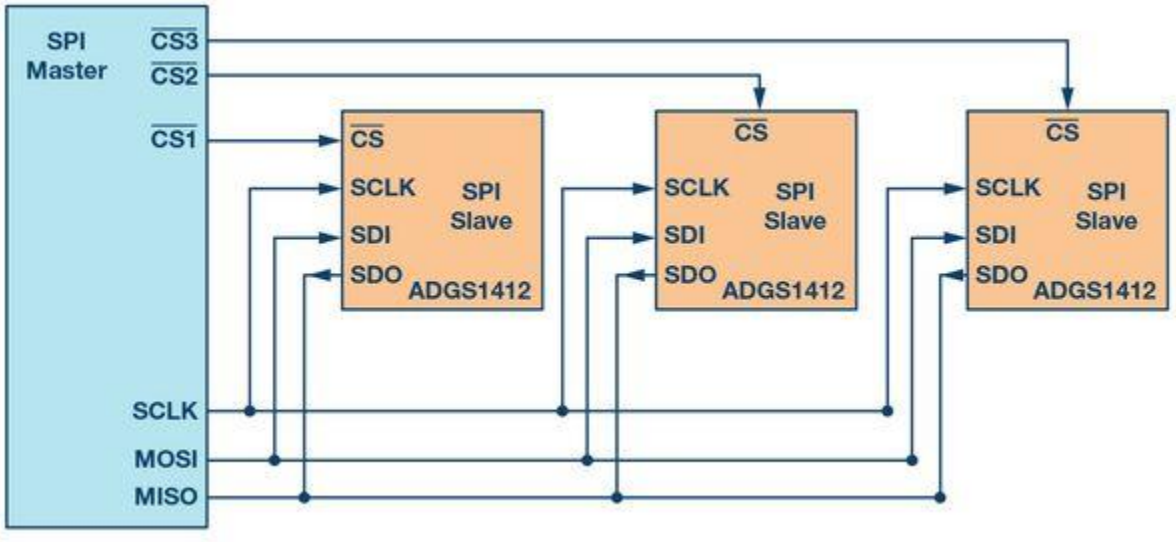
SPI bus

- 4-wire SPI has 4 signals
  - Clock (SCLK)
  - Chip select ($\overline{CS}$)
  - Master out, slave in data (MOSI)
  - Master in, slave out data (MISO)



SPI data transmission

- Master initiates transfer by sending the clock signal and asserting the chip select (usually active low)
- Both master and selected slave can send data at the same time via MISO and MOSI signals
- Serial clock edge synchronizes the shifting and sampling of the data
- Either the rising or falling edge of the clock can be used to sample and/or shift the data



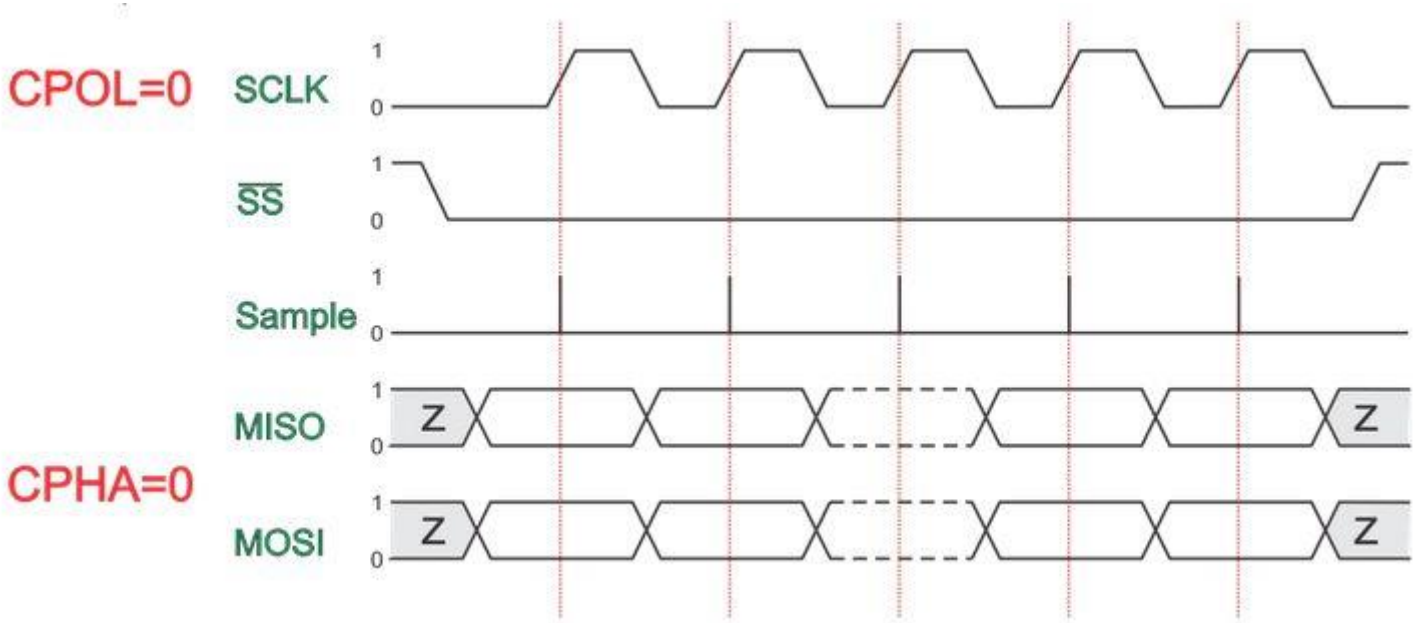
SPI clock polarity and clock phase

- All four combinations of clock polarity and clock phase (SPI modes) can be selected
  - CPOL – clock polarity
    - CPOL=0, clock starts at ‘0’ (non-inverted)
    - CPOL=1, clock starts at ‘1’ (inverted)
  - CPHA – clock phase
    - CPHA=0, data is sampled on the first clock edge
    - CPHA=1, data is sampled on the second edge

Mode	CPOL	CPHA
0	0	0
1	0	1
2	1	0
3	1	1

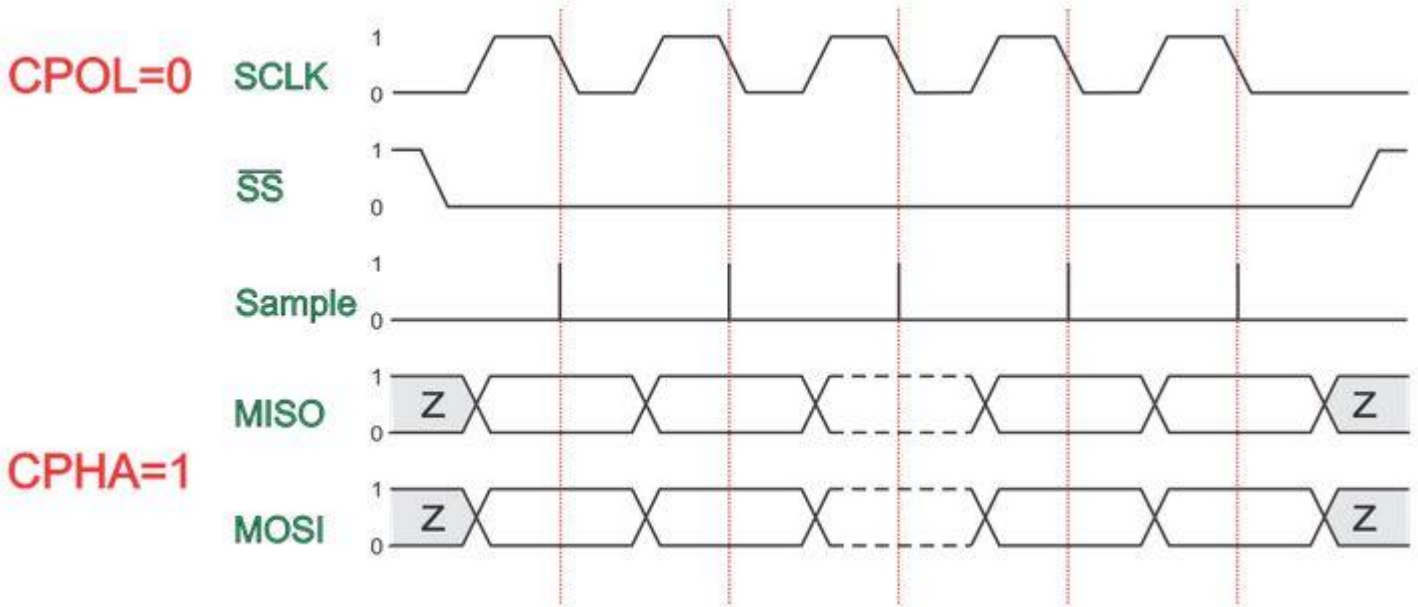
SPI Mode 0

- CPOL = 0, clock is low when CS is asserted
- CPHA = 0, data is sampled on the rising edge, shifted on the falling edge



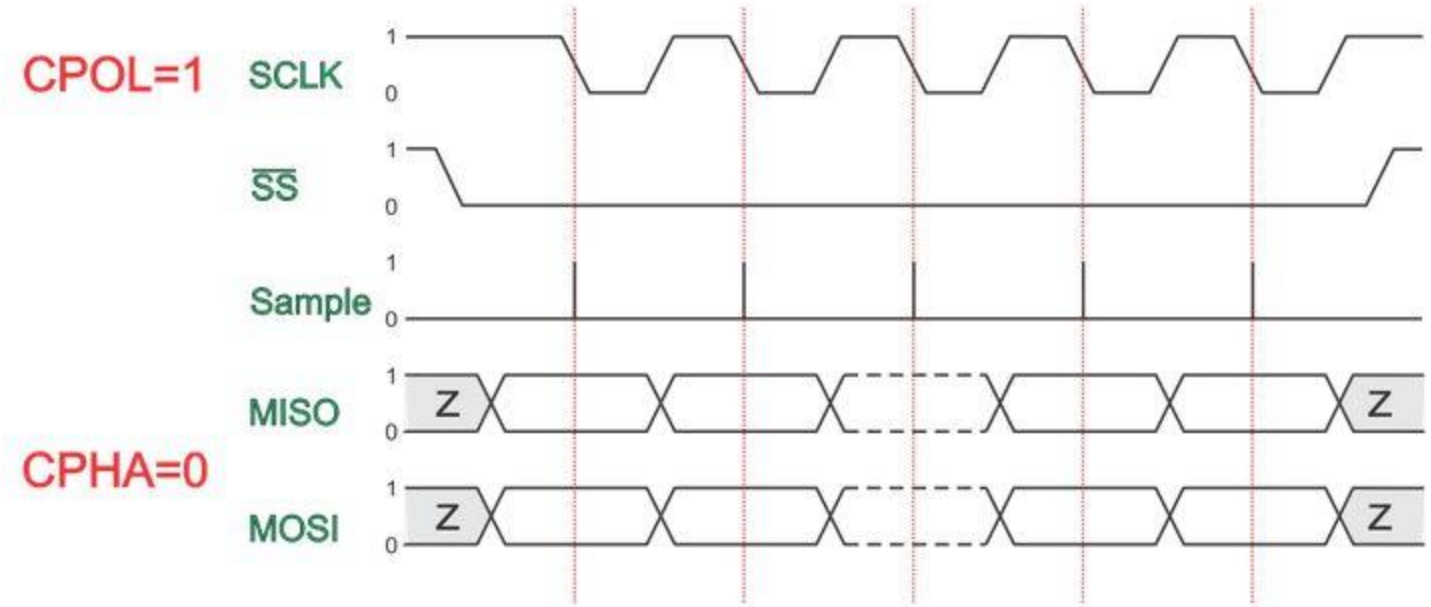
SPI Mode 1

- CPOL = 0, clock is low when CS is asserted
- CPHA = 1, data is shifted on the rising edge, sampled on the falling edge



SPI Mode 2

- CPOL = 1, clock is high when CS is asserted
- CPHA = 0, data is sampled on the falling edge, shifted on the rising edge



SPI Mode 3

- CPOL = 1, clock is high when CS is asserted
- CPHA = 1, data is shifted on the falling edge, sampled on the rising edge