

Lebanese University Faculty of Engineering III Electrical and Electronics Department

12H Adjustable Synchronous Digital Clock Using Logic Circuits On Logisim

Supervised By: Dr. M. Doughan

Presented By: Hussein Kazem(5667)

Abstract: This project depicts a 12 Hours AM/PM digital clock with manually adjustable time using dedicated buttons for each section. The software used was logisim software.

Contents:

- 1. Introduction and Outline
- 2. 7 segment display decoder
- 3. Counters
 - a. 0-9 counter
 - b. 0-5 counter
 - c. 1-12 counter
- 4. 7 segment decoder for hours (H Decoder)
- 5. A/P Indicator
- 6. Clock Circuit
- 7. Main Circuit
- 8. Conclusion

1. Introduction and outline:

As stated, the project depicts a 12 Hours am/pm digital clock making use of various subcircuits for the sake of visual simplicity and tidiness. Also, in the effort of having a very simple design, only <u>D flip flops</u> were used in the making of various subcircuits in need of memory components, mainly counters.

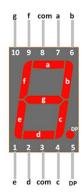
The entire circuit runs on one 2 Hz clock(synchronous circuit) which is used to drive all changes using pauses and reset triggers to make sure the circuit runs as smoothly and accurately as possible.

Now for a closer look at each component and it's uses.

2. 7 Segment display decoder:

Two 7 segment displays were used to show the <u>Hours</u> of the circuit, and one for A/P display indicating AM or PM time.

For the hours displays, a 7 segment display decoder was necessary to translate the output of the 1-12 counter to the display. For that purpose, the **analyse circuit** feature of the <u>logisim</u> software was used in order to facilitate the creation of the decoder simply providing the inputs and outputs and truth table and building the circuit resulting in the circuit found in the "7 segment decoder" file. The decoder uses 4 inputs Q3 Q2 Q1 Q0 (Q3 being the MSB and Q0 the LSB) while having 7 outputs a, b, c, d, e, f and g each driving a segment of the display according to the following configuration(ignoring the none present compins).



3. Counters:

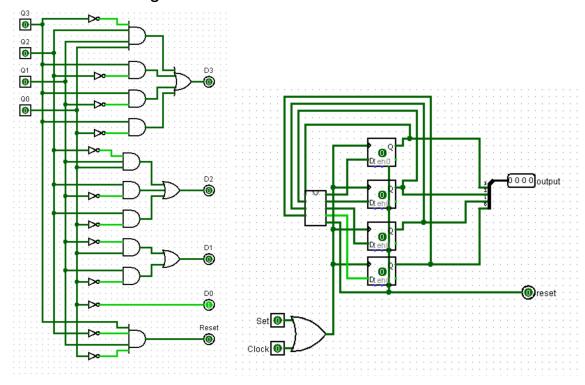
3 types of counters were used in the making of this project all strictly consisting of D flip flops for memory. The counters used a chip "0-9 counter logic" which takes as inputs the current states of the flip flops (Q3, Q2, Q1, Q0) and outputs the next state to be inputted into the flip flops that being the next number in numerical order. All counter logic circuits were made using the analyse circuit feature of the logisim software and all include a "reset" output indicating in each case the return to 0(or 1 in the case of 1 to 12) of each counter. The reset output also plays a role in the "pause" aspect of the circuit to be discussed in the "clock" portion.

The Set input pin is used to increment the value of the counter and is used to set the starting time of the clock.

a. 0-9 Counter:

The two 0-9 counters were used to drive the units output of the seconds and minutes units(denoted "s" and "m" in **main**). The reset output indicates when the next state is 10 (1010) and is connected to the reset pins the flip flops resetting the value of the counter to 0.

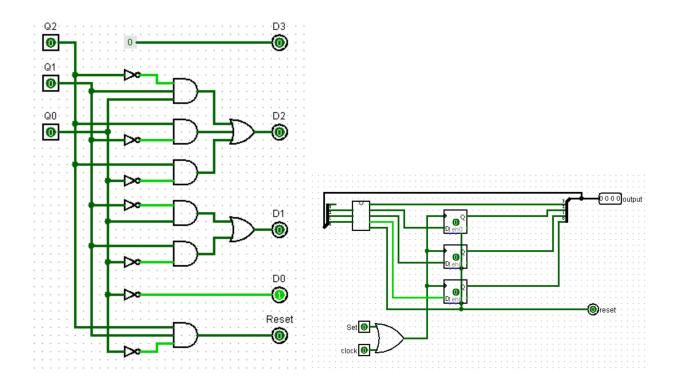
Combinational logic for the 0-9 counters:



b. 0-5 Counter:

The two 0-6 counters were used to drive the tens output of the seconds and minutes units(denoted "S" and "M" in **main**). The reset output indicates when the next state is 6 (0110) and is connected to the reset pins the flip flops resetting the value of the counter to 0.

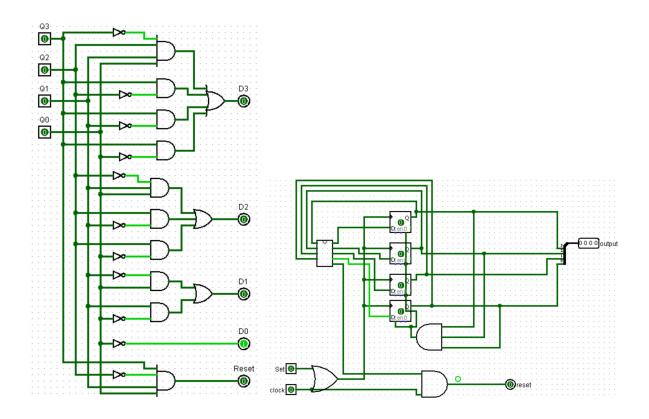
Combinational logic for the 0-5 counters:



c. 1-12 Counter:

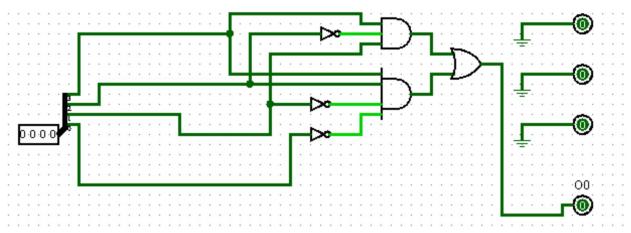
The 1-12 counter(file name: 0-12 counter) was used to drive the units and tens output of the seconds and minutes units(denoted "H" in **main**). The reset output indicates when the next state is 11 (1011) and is connected to the reset output to be used in switching between AM and PM while a separate AND Gate is used to determine the "13" (1101) output and is connected to the Q3, Q2 and Q1 flip flops and the Set pin of the Q0 flip flop resetting the value of the counter to 1.

Combinational logic for the 1-12 counters:



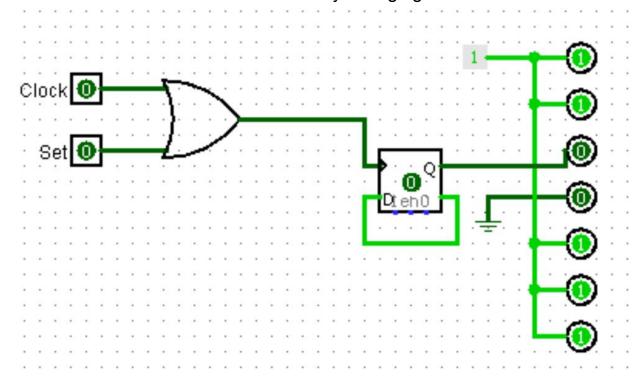
4. 7 segment decoder for hours(H decoder):

This chip was used to drive the 7 segment display representing the tens of hours (0 or 1). Circuit was also made using the analyse feature in logisim, taking 4 inputs Q3, Q2, Q1, Q0 and outputting the necessary outputs for the 7 segment display decoder to output and show 0 if the input is <10 and 1 if the input is >=10.



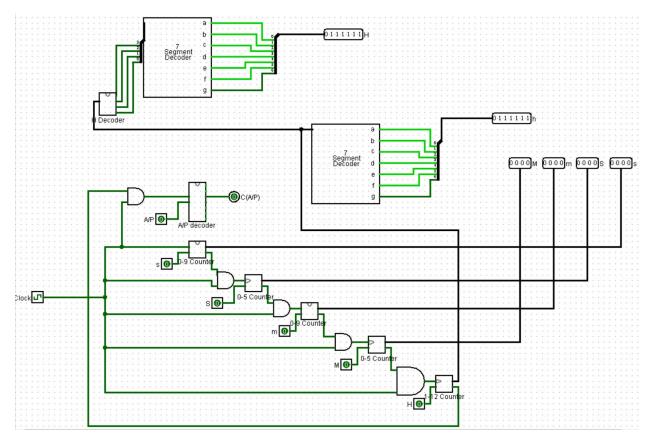
5. A/P indicator:

The A/P indicator is a very simple circuit used to drive the A/P 7 segment display. We notice when displaying A or P that the segments, a, b, e, f and g are always on while d is always off and the differentiating segment is c. This circuit utilizes a single flip flop set to toggle on each clock pulse to switch between c on and c off effectively changing from A to P.



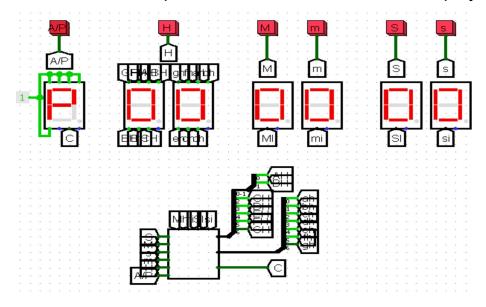
6. Clock Circuit:

The main operational circuit utilizing all the main previously mentioned components to output 4 4-bit M,m,S,s outputs to drive 4 separate hex displays which were used for the sake of simplicity, in addition to 2 8-bit outputs H,h used to drive the 7 segment displays for hours in main and a single bit output to drive the A/P display. Moreover, each counter has its own input on the "set" pin to be connected to a button to drive the adjusting factor of the clock. It can be seen that each reset output for each counter is connected with the main clock using an AND gate and used as the clock for the next circuit effectively causing a pause until the next reset of each counter.



7. Main Circuit:

The main circuit is a very simple circuit consisting of the "clock" chip and making use of many tunnels to drive the displays and button inputs to have the cleanest possible look for the displays and buttons.



8. Conclusion:

All in all, the clock runs as intended and is very accurate. It would be wise to consider other ideas to be added to this project such as stopwatch or alarm features which wouldn't be too difficult only utilising the currently existing components.