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PYNQ Automated System-on-Chip Builder & Remote RISC-V Learning Platform

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GitHub.com/HDLGen-ChatGPT/PYNQ-SoC-Builder

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Project Workflow

Design Specification

Context Diagram
Signal Dictionary
Process Descriptions
Data Flow Diagram
Truth Table etc.

User enters details

HDLGen-ChatGPT

Generates Vivado Project, Captures VHDL/Verilog, Generates Testbench

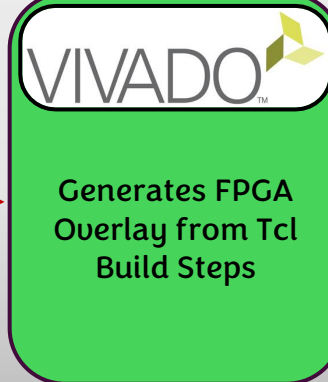
HDLGen XML



PYNQ SoC Builder

Creates Vivado Tcl script with build steps, generates JNB file from HDLGen XML

Export Tcl and JNB



Generates FPGA Overlay from Tcl Build Steps

Upload Binaries to remote/local FPGA

Run Overlay using Python in Jupyter Web Interface



Project Overview and Objectives

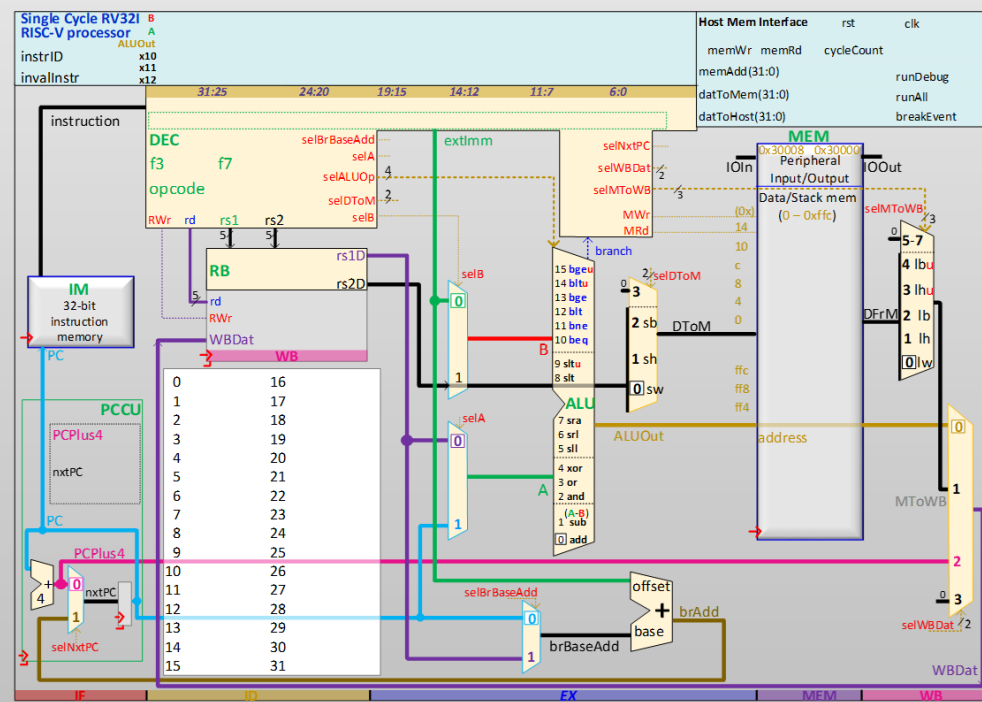
The aim of this project is to:

- Create a remote PYNQ laboratory for students
- Extend the functionality of HDLGen-ChatGPT to automatically deploy projects to PYNQ-Z2 FPGAs
- Develop an interactive challenge-based RISC-V learning tool

Remote PYNQ FPGA Laboratory

The purpose of the remote FPGA laboratory is to make real PYNQ Z2 hardware available to students and enthusiasts.

This is achieved by using a tunnelling service called **ngrok**. This service runs as a background daemon on the PYNQ's ARM processor. Ngrok encrypts all data using HTTPS and authenticates users using OAuth 2.0. OAuth allows users to authenticate using their @universityofgalway.ie Microsoft accounts.



RISC-V Architecture

PYNQ SoC Builder

HDLGen-ChatGPT is an open-source Python tool developed in the University of Galway to enable fast capture of HDL-based SoC capture and implementation, by automated VHDL/Verilog, testbench and waveform generation. PYNQ SoC Builder is a Python application which builds HDLGen-ChatGPT projects.

PYNQ SoC Builder completes the following:

- Generates and imports PYNQ-Z2 constraints and configuration
- Creates and populates a Vivado Block Design
- Configures PYNQ board I/O Connections
- Performs synthesis, implementation and bitstream generation
- Generates a Jupyter Notebook project based on test plan

HDLGen Project XML Data

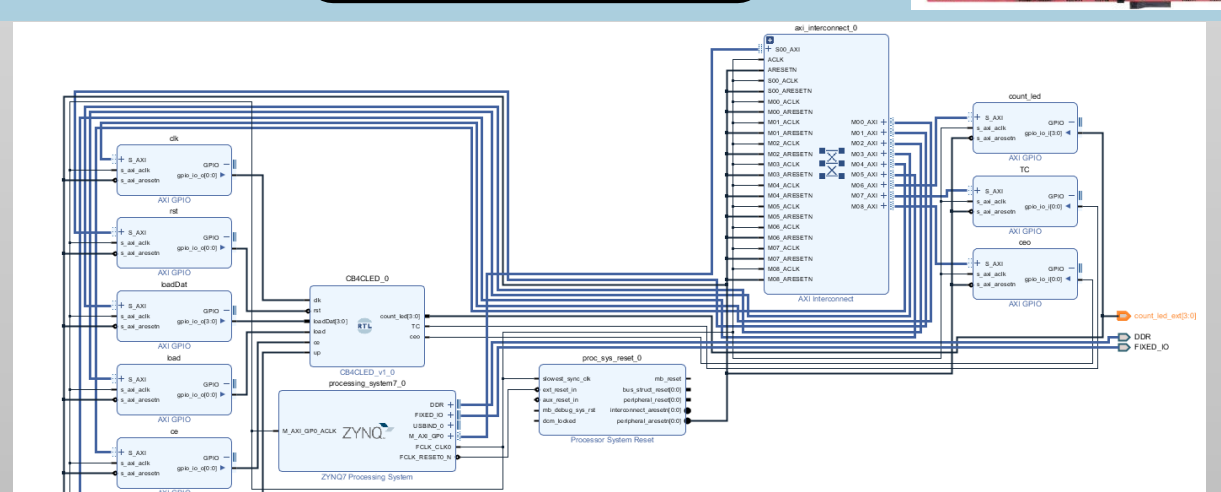
Component Name, Description, Date, Author, Email, Company Sub-Components Signal Type Sub-components Ports Internal Signals Architecture Test Plan

PYNQ SoC Builder

1. Read Data
2. Prepare a Tcl script which applies build steps in Vivado
3. Invoke script in Vivado IDE
4. Vivado exports binaries
5. Generate Jupyter NB based on Test plan
6. Export Binaries and JNB to output folder

Output Binaries

.hwh, .tcl, .bit, .ipynb



Block Diagram generated by SoC Builder for a 4-bit Counter

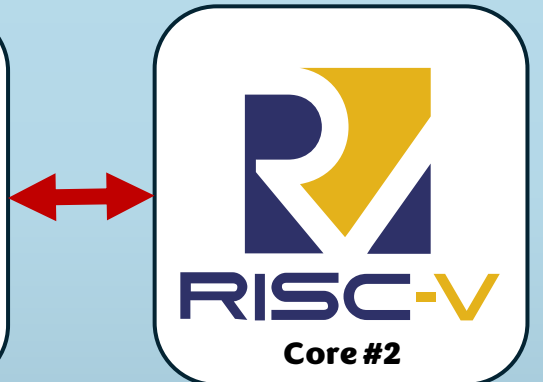
RISC-V Assembly/C Challenge-Based Learning Platform

- The purpose of the RISC-V learning platform through the remote laboratory is to encourage interaction and exploration of RISC-V ISA on real hardware, rather than simulation
- The learning platform will consist of two RISC-V cores. One of which the user will program using assembly or C, The other will remain hidden, only visible to the core #1 by I/O ports. Core #2 will imitate a peripheral device.
- The goal of the user is to interface with the hidden peripheral. The hidden peripheral changes depending on the difficulty level. For example, an interrupt controller or I²C device.

PYNQ Jupyter Notebook Interface



User uploads assembly to Core #1
User may read memory to view results



Core #2 runs hidden program

Future Work

- Automate RISC-V Core Bitstream Creation
- Develop a range of RISC-V challenges of varying difficulty
- Gather feedback from potential users of RV learning platform

Acknowledgements

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