TOSHIBA Field Effect Transistor Silicon P Channel MOS Type

SSM3J01F

High Speed Switching Applications

- Small package
- Low on resistance : Ron = 0.4 Ω (max) (VGS = -4 V) : Ron = 0.6 Ω (max) (VGS = -2.5 V)
- Low gate threshold voltage

Absolute Maximum Ratings (Ta = 25°C)

Characteristics		Symbol	Rating	Unit	
Drain-source voltage		V _{DS}	-30	$(\mathcal{N} \land)$	
Gate-source voltage		V_{GSS}	±10	(V)	
Drain current	DC	I _D	-700	mA	
	Pulse	I _{DP}	-1400		
Drain power dissipation (Ta = 25°C)		PD	200	mW	
Channel temperature		T _{ch}	150	°C	
Storage temperature range		T _{stg}	-55~150	/°C	

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.

Unit: mm

2.5-0.3

+0.25

+0.25

1.5-0.15

1.5-0.15

1.5-0.15

1.5-0.15

2.50URCE
2.50URCE
3. DRAIN

S.MINI

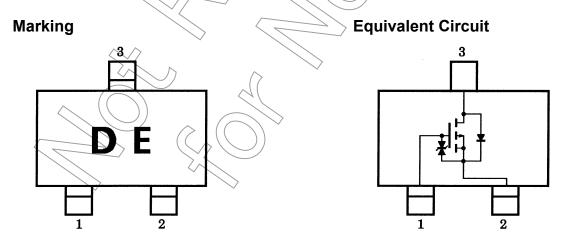
JEDEC TO-236MOD

JEITA SC-59

TOSHIBA 2-3F1F

Weight: 0.012 g (typ.)

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions" ("Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).



Handling Precaution

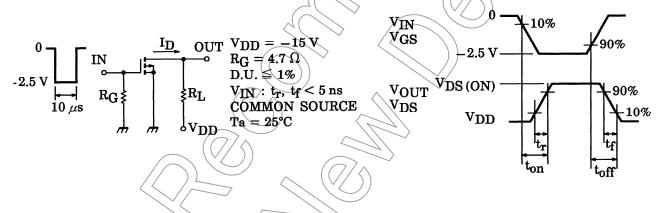
When handling individual devices (which are not yet mounting on a circuit board), be sure that the environment is protected against electrostatic electricity. Operators should wear anti-static clothing, and containers and other objects that come into direct contact with devices should be made of anti-static materials.

Electrical Characteristics (Ta = 25°C)

Chara	acteristics	Symbol	Test Condition	Min	Тур.	Max	Unit
Gate leakage curi	rent	I _{GSS}	$V_{GS} = \pm 10 \text{ V}, V_{DS} = 0$	_	_	±1	μА
Drain-source brea	akdown voltage	V (BR) DSS	$I_D = -1$ mA, $V_{GS} = 0$	-30	_	_	V
Drain cut-off curre	ent	I _{DSS}	$V_{DS} = -30 \text{ V}, V_{GS} = 0$		_	-1	μΑ
Gate threshold vo	ltage	V_{th}	$V_{DS} = -3 \text{ V}, I_D = -0.1 \text{ mA}$	0.6	_	-1.1	V
Forward transfer	admittance	Y _{fs} (Note)	V _{DS} = -3 V, I _D = -0.35 A	1.0)_	_	S
Drain-source ON	resistance	R _{DS} (ON) (Note)	$I_D = -0.35 \text{ A}, V_{GS} = -4 \text{ V}$ $I_D = -0.35 \text{ A}, V_{GS} = -2.5 \text{ V}$		0.3 0.4	0.4 0.6	Ω
Input capacitance	·	C _{iss}	V _{DS} = -10 V, V _{GS} = 0, f = 1 MHz	_	240		pF
Reverse transfer	capacitance	C _{rss}	$V_{DS} = -10 \text{ V}, V_{GS} = 0, f = 1 \text{ MHz}$	_	24	_	pF
Output capacitano	ce	C _{oss}	V _{DS} = -10 V, V _{GS} = 0, f = 1 MHz		94	\rightarrow	pF
Switching time	Turn-on time	t _{on}	$V_{DD} = -15 \text{ V}, I_D = 0.3 \text{ A}, V_{GS} = 0 \sim -2.5 \text{ V}, R_G \neq 4.7 \Omega$	-6	36	> —	no
	Turn-off time	t _{off}			37) —	ns

Note: Pulse test

Switching Time Test Circuit

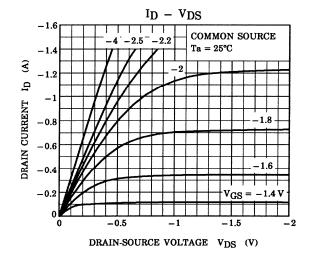


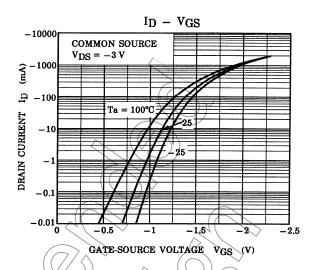
Precaution

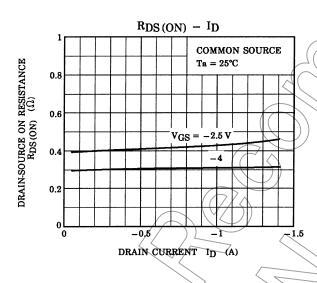
Vth can be expressed as voltage between gate and source when low operating current value is ID = $-100 \,\mu\text{A}$ for this product. For normal switching operation, VGS (ON) requires higher voltage than Vth and VGS (off) requires $\begin{array}{c} {\rm lower \ voltage \ than \ V_{th}.} \\ {\rm (Relationship \ can \ be \ established \ as \ follows \ V_{GS \ (off)} < V_{th} < V_{GS \ (ON)})} \end{array}$

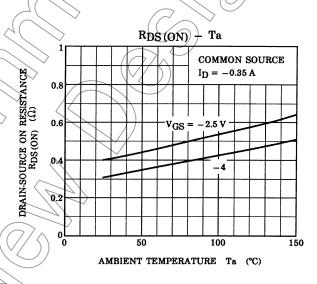
Please take this into consideration for using the device.

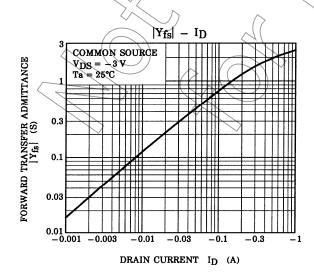
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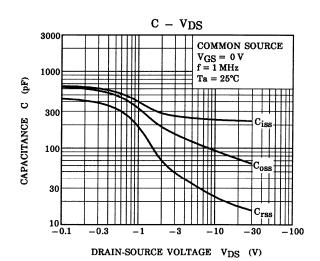












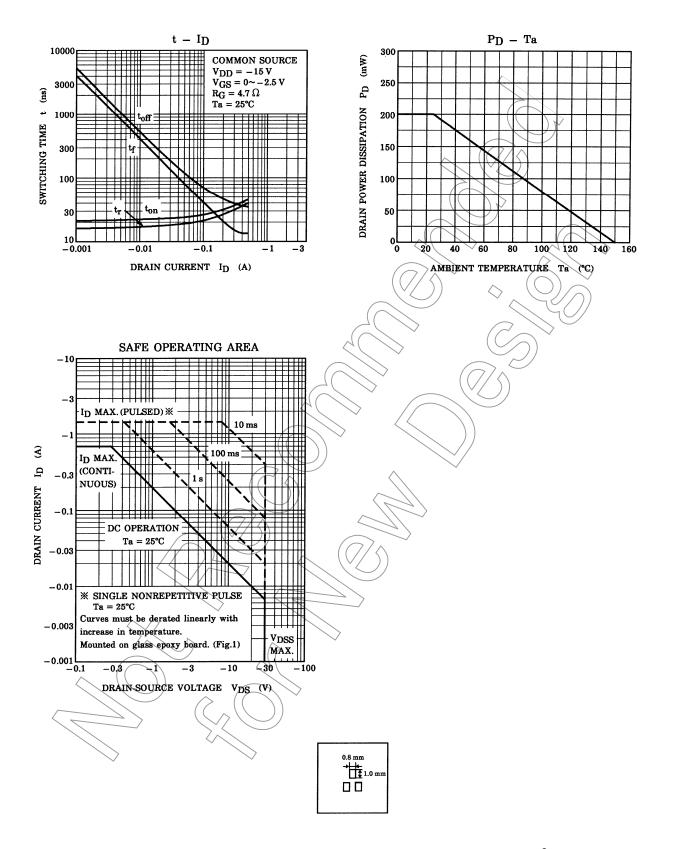


Figure 1 25.4 mm \times 25.4 mm \times 1.6 t (a Cu pad of 0.8 mm² area)

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