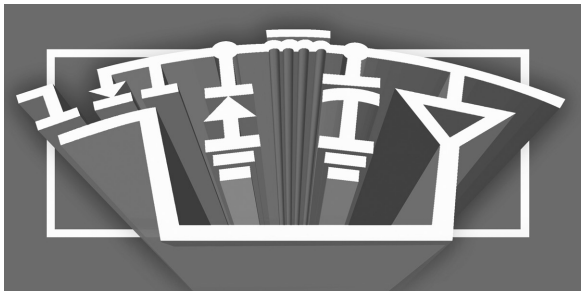

Power Supply Design Seminar

Transformer and Inductor Design for Optimum Circuit Performance

Topic Category:
Magnetic Component Design

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Transformer and Inductor Design for Optimum Circuit Performance

Lloyd H. Dixon

ABSTRACT

The energy absorbed and released by transformer leakage inductances during each switching period usually ends up as loss, thus impairing switching power supply efficiency. Even when much of this energy is recycled and recovered through the use of resonant or active clamping techniques, leakage inductance remains as the main factor in cross-regulation errors among multiple outputs, a problem that cannot be eliminated or reduced with a single control loop. This topic discusses how proper thinking about the causes and effects of leakage inductance can result in optimized transformer design with minimum parasitic inductances and ac winding losses, as well as establishing the winding hierarchy to reduce cross-regulation errors. Also discussed are ways to use reluctance modeling and duality principles to develop the transformer equivalent electrical circuit model which provides provide the best visibility of the effects of parasitic inductances. Examples are presented of forward and flyback transformer applications with multiple outputs.

I. INTRODUCTION

This topic builds upon and applies the procedures presented in the TI/Unitrode Magnetics Design Handbook, presented to attendees of the 2001 Power Supply Design Seminar. To obtain a copy of the Magnetics Design Handbook, see Reference [1].

The word "transformer" is often used in this paper to refer generically to both transformers and inductors.

The process for transformer design and optimization could consist of the following steps:

1. Perform a tentative transformer design, on paper, based on the predefined requirements of the circuit application.
2. Develop the electrical equivalent circuit model based on the physical structure and dimensions of the tentative transformer design. Each element of the physically-based circuit model will correlate with a specific physical region or element of the transformer.
3. Simulate circuit operation in the time domain, using the transformer model operated in its circuit application. Based on the understanding gained from observed effects, make appropriate modifications to the transformer circuit model to obtain improved performance. Even without computer simulation, common-sense evaluation of the physically-based transformer model in its circuit application can provide great insight into ways to manipulate the transformer structure to obtain improved circuit performance.
4. Implement the desired improvements, using the simple relationships between elements of the circuit model (such as leakage inductance) with the underlying physical parameters and dimensions of the transformer structure.
5. Before committing to the planned approach, the designer can explore alternative circuit topologies or operating frequencies, using simulation.
6. The final step is to build a physical prototype of the refined paper design, and evaluate the prototype device in the circuit application.

II. HYPOTHETICAL RESISTIVE SOURCE

Imagine a power distribution hub with a pair of input terminals internally connected to three pairs of output terminals. Each output pair is intended to deliver power to a high-power load. Resistances of the conductors between the terminals are significant, resulting in power loss,

poor load regulation and impaired cross-regulation.

Assuming the circuit configuration within the distribution hub cannot be changed, but circuit *values* can be changed, losses can be minimized and cross regulation improved by:

1. Reducing resistances as much as possible.
2. Selecting the loads attached to each pair of terminals in the most intelligent manner.

In order to achieve this goal, a knowledge of the circuit diagram is essential. In this example, the terminals are connected in a series string as shown in Fig. 1.

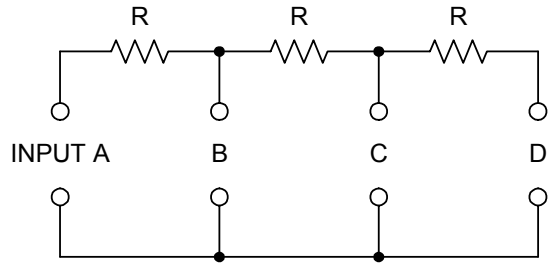


Fig. 1. Resistive source.

The resistance of the conductors between terminal pairs is defined by the following relationship:

$$R = \frac{\ell}{\sigma A}$$

Where A and ℓ are the conductor cross-section area and length, and σ is the conductivity. If the distance between terminal pairs is fixed, conductor length cannot be reduced, but resistances can be minimized by increasing conductor area and by using a material with high conductivity, such as silver or copper.

Taking note of the circuit configuration in Fig. 1, it is obvious that to minimize power loss within the hub, the highest current load should be connected to the "B" terminals, closest to the input, with progressively smaller loads connected to the "C" and "D" terminal pairs. But in order to minimize cross regulation errors, the load with the greatest current *change* should be connected to the "B" terminals. (If the load with the greatest current does not also have the greatest *change*, then these goals conflict and a judicious decision must be made.)

It will be shown that transformer design optimization can follow this same logical pattern. With knowledge of the electrical equivalent circuit and its relationship to the underlying physical parameters of the transformer, parasitic inductances can be minimized and winding sequences arranged for optimum results.

III. Transformer In-Circuit Performance

A. The Effects of Leakage Inductance

Transformer leakage inductances are usually the main factor in poor load regulation and poor cross regulation with multiple outputs. Leakage inductances usually have a much greater effect than all circuit resistances combined: series resistance of transformers and filter inductors, rectifier dynamic resistance, switch R_{DSON}, and circuit wiring. Leakage inductance also seriously impairs power supply efficiency when leakage inductance energy is dumped into dissipative snubbers or clamps.[2]

How does an ideal lossless inductor, with zero resistance, affect DC load regulation, and cause losses? In a linear circuit application, an ideal inductor has no effect on load regulation or cross-regulation. But in a switching power supply, currents in the windings are switched and discontinuous. Leakage inductance is a circuit representation of energy stored physically between the windings of the transformer. When the primary-side power switch turns on, energy must be provided to the leakage inductance field between the windings in order for the transfer of current between windings to take place. When the primary switch turns off, the discharge of this energy results in a large reversal of voltage which appears across the switch. This voltage must be suitably clamped to avoid damaging the switch. The leakage inductance energy is thus dumped into the clamp, resulting in loss.

The time required to provide and remove energy from the leakage inductance field causes a delay in the current transition between primary and secondary. The transition time is directly proportional to load current. It effectively reduces the pulse width on the secondary side as a function of load current, thus impairing load regulation.

It is worth pointing out again that *leakage inductance is usually the main cause of poor load regulation*. Likewise, with multiple outputs, leakage inductance between secondary windings is the main cause of poor cross regulation.

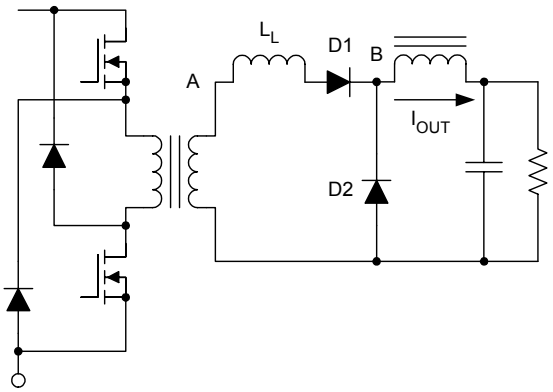


Fig. 2. Forward converter circuit model.

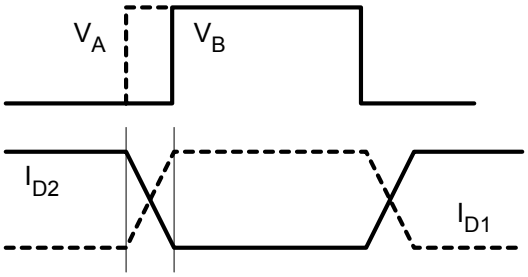


Fig. 2a. Waveforms.

Fig. 2 shows the effect of leakage inductance between primary and secondary in a forward converter with a single output. The leakage inductance could be referred either to the primary or the secondary – it is shown here in series with the secondary. Before the primary side power switch is turned on, the output filter inductor current (which is essentially constant during the switching transition) flows through the freewheeling diode D2, and the current through the series leakage inductance and D1 is zero. When the switch is turned on, current through the leakage inductance L_L cannot change instantaneously, but rises at a rate:

$$di/dt = \frac{V_A}{L_L} = \frac{V_{in}}{nL_L} \qquad (1)$$

Where n is the primary/secondary turns ratio. This rate of current rise determines the transition time for the current to transfer completely from the shunt freewheeling diode to the leakage inductance and to the primary side. *During this entire transition, the freewheeling diode remains in the forward direction,* conducting an ever-decreasing current. This causes the voltage at the input of the filter inductor to remain at zero throughout the transition. Thus, the leading edge of the voltage pulse applied to the output filter inductor is delayed by an amount equal to the transition time, which reduces the average voltage delivered to the output. The turn-on transition delay and the resulting reduction in output voltage are directly proportional to the load current flowing through the filter inductor:

$$t_D = \frac{I_{out} L_L}{V_{secondary}} \qquad (2)$$

When the power switch turns off, current through the leakage inductance falls at a rate:

$$di/dt = \frac{V_{clamp}/n}{L_L} \qquad (3)$$

However, at the very beginning of the turn off transition, the initial reduction of current through the leakage inductance forces the remainder of the output filter inductor current through the free-wheeling diode. *The freewheeling diode immediately conducts, and the voltage at the input of the filter inductor is forced to zero without any transition delay.*

Thus, there is a turn-on delay, but no turn-off delay – the leakage inductance causes a reduction of the pulse width applied to the filter inductor input. The turn-on transition time and corresponding pulse width reduction is proportional to load current. If the duty cycle of the power switch is not changed, the output voltage will drop by an amount proportional to load current. The leakage inductance behaves like a lossless series resistance. However, during the turn off transition, all of the energy stored in the leakage inductance is delivered into the clamp. With a dissipative clamp, this becomes power loss. Thus, loss does not occur in the inductor, but it causes loss by dumping its energy into the

clamp. Even with a non-dissipative clamp, the leakage inductance causes power to be diverted away from the output.

The control loop, sensing the output voltage reduction, increases the duty cycle to provide eventual correction, depending upon the control loop response time. However, the pulse width reduction caused by the turn-on transition reduces the available duty cycle range. In a forward converter, for example, the duty cycle of the voltage waveform applied to the transformer primary is often limited to 50 percent, in order to allow time for transformer core reset. The turn on transition time will then reduce the maximum duty cycle of the pulse applied to the filter inductor input to something less than 50 percent. Peak current values must be correspondingly increased. To obtain the desired averaged output voltage with a shorter pulse width, a higher peak secondary voltage is required. This is achieved by an adjustment of the transformer turns ratio.

B. Multiple Secondary Windings

When there are more than two windings in the transformer, a more serious situation occurs. Fig. 3 shows a simplified equivalent circuit of a forward converter with two outputs, using a transformer with two secondaries.

In order to simplify the equivalent circuit, the assumption is made that the two secondaries have equal number of turns. By eliminating the turns ratio between the secondaries, the two secondaries in the equivalent circuit can be directly interconnected, except for the leakage inductance intervening between the actual windings. (Later, a normalization process will be discussed which enables secondaries with different numbers of turns to be treated in a similar manner.) In Fig. 3, leakage inductance values appear in their proper locations in the equivalent circuit.

To further simplify the equivalent circuit, the output filters and loads have been replaced by equivalent constant-current loads.

L_{P1} represents the leakage inductance energy existing in the field between the primary and adjacent secondary #1. L_{12} represents the additional leakage inductance energy between secondaries 1 and 2. Leakage inductance between the secondaries causes cross-regulation or tracking errors between the outputs that cannot be corrected by the control loop. If the loop is closed on output #1, it will be well regulated, but increased load on output #2 will cause its voltage to decline. Conversely, if the loop is closed on output #2, it will be well regulated, but an increase in load on output #2 will cause the voltage on output #1 to *rise*.

Fig. 3a shows the resulting waveforms. (The validity of the model and resulting waveshapes can be observed in an actual power supply at the filter inductor inputs.

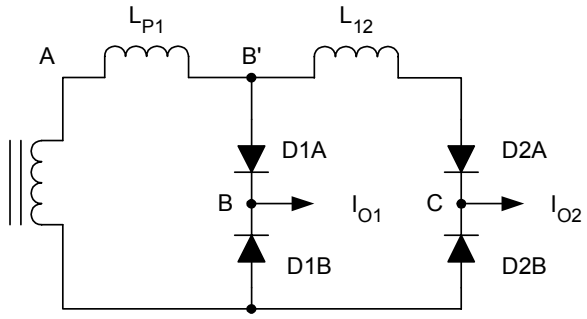


Fig 3. Two-output equivalent circuit.

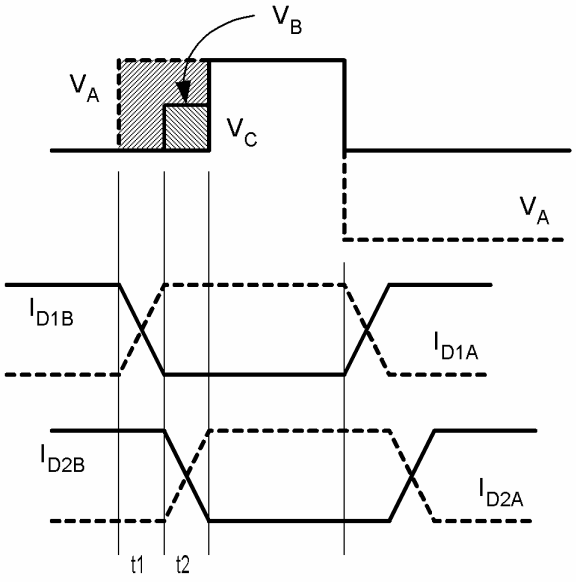


Fig. 3a. Waveforms.

Before the primary-side power switch turns on, free-wheeling diodes $D1_B$ and $D2_B$ are conducting output currents I_{O1} and I_{O2}. When the power switch turns on, voltage is applied across L_{P1}, initiating current transition t_1, just as in the previous example of Fig. 2. Current through $D1_A$

increases, while $D1_B$ current decreases. Since $D1_A$ and $D1_B$ are both conducting throughout transition time t_1, voltages V_B and V_B' are essentially zero. Therefore, the voltage across L_{12} is zero, so that *current through L_{12} and $D2_A$ remain at zero throughout t_1*.

At the end of t_1, when the current through L_{P1} and $D1_A$ has risen to output current I_{O1}, current through $D1_B$ reaches zero. This permits the voltage at B and B' to rise, applying voltage to L_{12}. This begins the second transition, t_2. During t_2, $D2_A$ and $D2_B$ are both conducting, and V_C remains at zero. Note that transition time t_2 is a function of V_A across L_{P1} and L_{12} *in series*.

$$t_2 = \frac{I_{O2}\,(L_{P1} + L_{12})}{V_A} \qquad (4)$$

During t_2, voltage at B' and B cannot rise to equal V_A, because B' is at the mid-point of inductive divider L_{P1} and L_{12}. Thus, full voltage is not applied to Output 1 filter inductor (at point B) until the end of *both* transitions.

As shown in Fig. 3a, the larger-hatched area shows the volt-seconds per switching period that is subtracted from the input pulse applied to Output 1. The smaller hatched area shows the *additional* volt-seconds per switching period subtracted from Output 2, which represents cross-regulation error.

Computer simulation using the equivalent circuit model can provide detailed information regarding circuit performance. However, valuable insight can be gained just by a simple understanding of how the equivalent circuit functions:

The equivalent circuit shows that Output 1 load current results in energy stored only in L_{P1}. A change in Output 1 current does not affect cross-regulation, because L_{12} is not involved. But Output 2 current results in stored energy in both L_{P1} and L_{12}, and affects Output 1 regulation *and* cross-regulation.

This holds true even if the number of turns in the secondary windings are not equal. The highest power load always translates into the greatest Ampere-turns. Therefore, to minimize the total energy stored in the leakage inductances (which usually ends up as loss), the highest power load (greatest Ampere-turns) should always be the closest coupled to the primary, in this case secondary #1.

But – if it is more important to achieve good cross regulation, then the load with the greatest power *variation* should be closest to the primary. If secondary #2 has a constant load, there will be no dynamic cross-regulation error between outputs 1 and 2, even if the load on secondary #1 has large variation, but if the location of the secondaries is interchanged, there will then be significant cross regulation error.

Thus it can be seen that it is not only important to design the transformer with minimum leakage inductance values, the sequence of the windings is also very important, depending upon whether the goal is to achieve minimum loss or minimum cross-regulation error.

IV. Modeling the Transformer

As discussed earlier, a proper electrical equivalent circuit model of a transformer (or inductor) permits circuit simulation of power supply performance, revealing problems and performance limitations attributable to the transformer. In addition, if the electrical parameters of the model can be directly correlated with the physical structure, then simulation results or simple common-sense circuit evaluation can show how to modify the transformer structure to improve circuit performance.

The traditional "black box" method for defining the transformer electrical model involves measuring the impedance of each winding, with other windings open and short-circuited. This method assumes no knowledge of the internal transformer structure, not even the turns ratio. (Much like the blind men attempting to define an elephant by feeling different parts of its anatomy.) Actually, if the measurements are sufficiently accurate, this method can result in a model which will produce the correct simulation results. However, it is unlikely that the electrical parameters of such a model will directly correlate with physical properties of the transformer. Thus a model derived in this manner will provide little

insight, and probably much confusion, regarding transformer improvement.

This is because there are an infinite number of possible circuit models for a specific transformer, all of which are electrically equivalent. Each of these theoretically possible models has different impedance values and correspondingly different turns ratios, and each will produce the same, presumably correct, simulation results. However, only one of these possible models has electrical parameters which correlate directly with physical parameters of the transformer structure. In this physically-based model, the turns ratios are the same as the actual transformer turns ratios. All of the other electrically equivalent models are abstractions.[3]

The Thevenin equivalent circuit of a "black box" circuit source is another example of an abstraction that provides proper results with circuit analysis, but provides little insight into the inner workings of the "black box" which would be necessary if it was desired to improve or modify the source circuitry.

The traditional "black box" method for defining the transformer model assumes a symmetrical bilateral coupling coefficient between each pair of windings, i.e.: k12 = k21 = k. This assumption (which is as reasonable any other if the inner workings are not known) results in a model consisting of a symmetrical tee or pi network, coupled with an ideal transformer whose turns ratio is *unlikely* to equal the actual transformer turns ratio. This is because in the actual transformer, the flux coupling coefficient k12 is unlikely to equal k21, and the corresponding network is therefore unlikely to be symmetrical.

However, If the *actual* turns ratio is known, the physically-based model could then be derived from measured impedance values by using the actual transformer turns ratios in the calculations.

But with high frequency SMPS transformers, it is often difficult to achieve sufficiently accurate measurements. For example, it is difficult to distinguish the short-circuit impedance of a one or two turn secondary from the inductance of the external leads. Even if the measurements are sufficiently accurate, any method based on measurement obviously requires building a prototype transformer in order to obtain the required values.

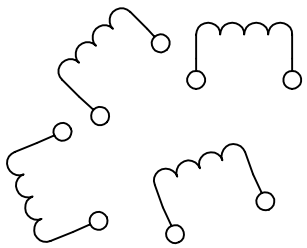


Fig. 4. Four randomly located windings.

The author prefers to develop the electrical equivalent circuit model from simple calculations based upon the physical parameters of the transformer, rather than by impedance measurements. This method, which will be discussed in a later section, permits simulation to be accomplished in the early phase of transformer design, using values calculated from the physical parameters of a proposed design, thus not requiring prototype construction and measurement.

Another serious problem is that in a transformer with more than two windings, the abstract theoretical model becomes much more complex. In Fig. 4, for example, with four windings arranged as shown and with no magnetic core, each winding cross-couples directly and independently to every other winding. The resulting complex and confusing equivalent circuit is usually the result of the "black box" measurement method which assumes no knowledge of the actual physical structure.

Fortunately, in most transformer structures with either helical or planar windings, the physically-based circuit model is quite simple. For example, in the helical transformer structure shown in cross-section in Fig. 5, flux lines cannot independently link primary winding P to secondary 2 without also linking to 1, and flux linking P to 3 must also link to 1 and 2. The circuit model for this configuration is shown in Fig. 5a. All windings are normalized to one turn, in order to eliminate the complexity introduced by turns ratios. (Each winding X would then be connected to its external circuit through an ideal dc-dc transformer with $1:N_X$ turns ratio.)

The three series inductors are leakage inductances, correlating directly with energy stored in the three regions between windings P–1, 1–2, and 2–3. The two shunt inductors are magnetizing inductances, representing the core center leg and the combined outer legs, respectively. Magnetizing inductance represents energy stored in the core, and is shared, or mutual, with all windings. If the magnetizing inductances are much greater than the leakage inductance values (which is usually the case), they can be combined into a single mutual inductance, located across the terminals of any winding (usually the primary as shown in Fig. 5b) without significantly affecting simulation results.

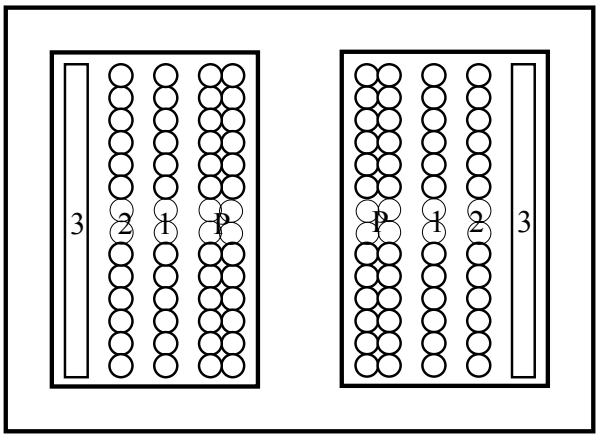


Fig. 5. Four concentric helical windings.

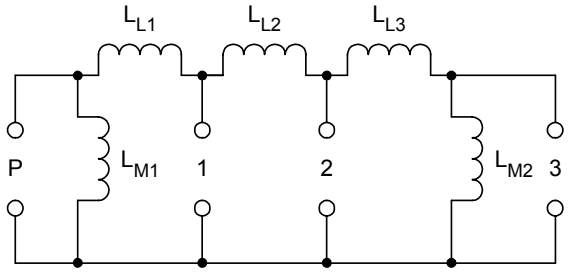


Fig 5a. Electrical equivalent circuit model.

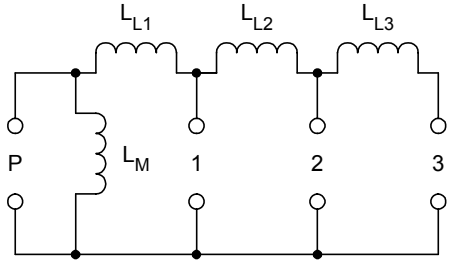


Fig. 5b. Modified electrical model.

V. Defining the Circuit Model

A. Based on Physical Parameters/Dimensions

The first step in defining the electrical circuit model of transformer without making electrical measurements is to define the *magnetic* equivalent circuit, often called a reluctance diagram.[4]

Reluctance, in a magnetic circuit, is the counterpart of resistance in an electrical circuit. When an electrical force (voltage) is applied, current flow is determined by circuit resistance. When a magnetic force (Ampere-turns) is applied to a magnetic element (such as a section of the core, or an air gap), the amount of flux is determined by the reluctance of that magnetic element. However, there the similarity ends – resistance is a power dissipating element, whereas reluctance is an energy storage element.

B. The Reluctance Diagram

Fig. 6 is the reluctance diagram of the transformer structure shown in Fig. 5. Reluctance values can be defined for each element of the transformer structure, according to the length, cross-section area, and permeability of that element, in the SI system of units:

$$\Re = \frac{\ell}{\mu A} \quad \text{A-T/Weber} \tag{5}$$

Where length and area are expressed in meters, and permeability μ equals:

$$\mu = \mu_0 \mu_r = 4\pi \times 10^{-7} \times \mu_r \tag{6}$$

$\mu_0 = 4\pi \cdot 10^{-7}$ (permeability of free space)
$\mu_r =$ relative permeability

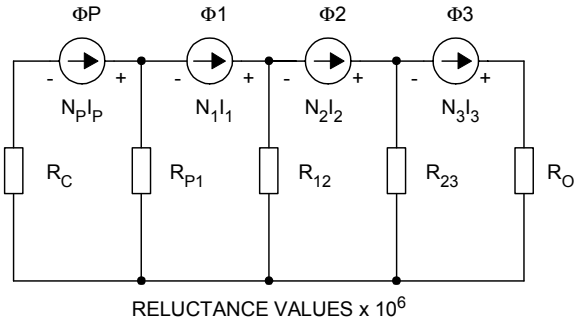


Fig. 6. Reluctance diagram.

The transformer of Fig. 5 has 4 helical windings arranged concentrically around the centerleg of a ferrite magnetic core.

Voltage applied to primary winding P causes the flux to *change* at a precise rate determined by Faraday's Law:

$$d\Phi/dt = E/N \quad (7)$$

Thus the total change in flux within the winding is precisely determined by the applied Volts/turn, integrated over time. Most of this flux passes through the low reluctance outer legs to complete its closed-loop path. Thus, the changing flux links to all of the other windings which will then (according to Faraday's Law) have the same induced Volts/turn as the primary.

The core has a small but finite reluctance, thus requiring a small magnetic force to push the flux dictated by Faraday's Law through the core.

$$F = \Phi\Re = N_P I_m \quad (8)$$

Magnetic force equates directly with Ampere-turns in the SI system of units. Thus a small magnetizing current, I_m, is required in the primary.

Because the reluctance of the outer legs is not zero, and the reluctance of the regions between each of the windings is not infinite, a small amount of the flux generated by the primary will flow through the regions between the windings. This is called leakage flux, one of the components of the leakage inductance field between the windings. Leakage inductance energy is not coupled to all windings – only to those windings linked by the flux lines.

When loads are applied to the secondaries, the resulting secondary Ampere-turns are offset by equal and opposite Ampere-turns in the primary. Thus, along the flux path through the core which encompasses all windings, the magnetic force created by these load-related currents cancels. The magnetic force through the core and its associated magnetizing current are not changed by load current. There is one place where the forces associated with load current do not cancel – that is between the windings. In those locations, the load related currents result in greatly increased leakage inductance energy between the windings.

All of the effects discussed above can be observed and evaluated with the reluctance diagram of Fig. 6.

C. Creating the Reluctance Diagram

The reluctance diagram is created by calculating the reluctance of each significant element in the transformer structure. Each winding appears in the reluctance diagram as a source.

The reluctance diagram should be no more complex than necessary – each element of the reluctance diagram becomes an element in the electrical equivalent circuit. Using equation (5) to calculate the reluctance of the centerleg, the ferrite cross-section area and centerleg length are available from the core datasheet. (Dimensions must be converted to meters for use in the SI system.) Absolute permeability, μ_0, equals $4\pi \bullet 10^{-7}$. Relative permeability, μ_r, for ferrite (typically 3000) is also available from the datasheet. With an E-E core, centerleg flux divides into two equal portions through the outer legs encircling the windings. The two outer legs can be considered as a single reluctance element with an area twice that of one leg, in order to simplify the reluctance diagram.

In a flyback transformer or filter inductor, an air gap would appear as a separate reluctance in the physical location where it occurs, usually in series with the center leg reluctance. The air gap reluctance has great importance in an inductor or flyback transformer, because this is where the required energy is stored.

The reluctance of each of the three regions between the windings is of key importance—the fields in these regions translate into leakage inductance. Relative permeability equals 1.0 in these non-magnetic regions between the windings as well as in the copper conductors. Just as the windings are cylindrical in form, the leakage inductance field regions between the windings are also cylindrical. The length of these cylindrical fields is the distance across the window in the core. (Where the windings emerge from the core, the leakage inductance field must stretch and bend to reach the core, so the length

of the field in these regions is somewhat greater, increasing the reluctance by 5 or 10 percent.) The cross-section area of these cylindrical regions equals the cylindrical wall thickness multiplied by the circumference. The wall thickness corresponds to the separation between adjacent windings, plus approximately one-third of the thickness of the windings themselves. (The field extends into the windings.) The mean length per turn (MLT) taken from the core datasheet can be used as the circumference of these cylindrical regions.

The regions between the primary and the core center leg and between secondary 3 and the outer legs are simply high reluctances in parallel with the low reluctance ferrite, and can be neglected.

Bear in mind that in this process, super accuracy is not very important. The object is to obtain an understanding in order to achieve improvement.

One additional consideration: Magnetic force is *circulatory* in nature, *distributed* around each winding whose Ampere-turns create the force, in the same manner that a paddle-wheel operating horizontally in a liquid provides a distributed force which would cause the liquid to circulate. (Mathematically, this would be described as *curl*.) The circulatory force results in a closed circulatory path for the resulting flux. However, in the reluctance diagram, the magnetic forces associated with each winding are inserted as discrete elements in locations that result in the same circulatory pattern as the actual distributed force. This requires using a little judgment.

D. The Electrical Equivalent Circuit

C. Cherry, in a 1949 paper, showed that the electrical equivalent circuit is the topological dual of the reluctance model. This is described in more detail in the referenced Magnetics Design Handbook.[4] Through this simple process, the reluctance diagram of Fig. 6 is transformed into the electrical equivalent circuit of Fig. 5a and 5b.

In the duality process as described by Cherry, and demonstrated in Fig. 7a and 7b for a simple inductor, each node in the reluctance diagram becomes a loop, or mesh, in the electrical equivalent circuit, while each loop in the reluctance diagram becomes an electrical node.

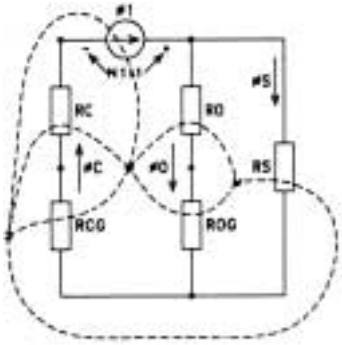


Fig. 7a. Inductor reluctance diagram.

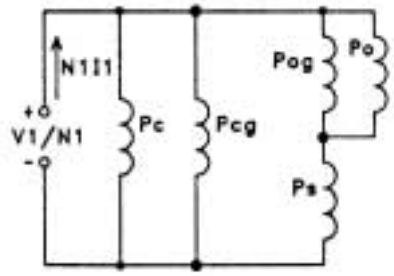


Fig. 7b. Electrical dual.

As shown in Fig. 7a, a node is placed at the center of each loop in the reluctance diagram. (Topologically, the entire outside of the circuit is also considered to be a loop.) Dash lines are drawn from node to node through each intervening element. The dash lines represent the electrical equivalent circuit. All of the series elements in the reluctance diagram become parallel elements in the electrical dual, and all the parallel elements are in series in the dual.

Circuit elements are also transformed. Ampere-turns representing magnetic force in the reluctance diagram are converted into terminal pairs in the electrical equivalent circuit. Reluctances become their reciprocals – permeances. Permeance is actually inductance as seen through a 1-turn winding:

$$P = \frac{1}{\mathfrak{R}} = \frac{\mu A}{\ell} \tag{9}$$

When the electrical equivalent circuit has been established, as in Fig. 7b, all of the actual permeance values are quantified using equation (9), based on the length, area, and permeability of the physical region from which each permeance is derived. The simple equation (9) not only enables quantification of these parasitic elements in the equivalent circuit, it points the way to improve the design to minimize their effects.

Inductance, when referred to any winding, equals permeance times the number of turns in the referenced winding squared:

$$L_N = N^2 P = \frac{N^2}{\Re} = \frac{\mu N^2 A}{\ell} \qquad (10)$$

Note that equation (10) is the inductance formula expressed in the SI system of units. Dimensions are in meters, and $\mu = \mu_0 \cdot \mu_r$.

All of the permeances in the equivalent circuit of Fig. 7b can thus be converted into inductance values as seen from the perspective of the winding terminals, by multiplying by N^2. But in a transformer with multiple windings with different numbers of turns, such as in Fig. 5, this approach becomes very messy and complex because each permeance element takes on different inductance values when seen through different windings with different turns. The transformer equivalent circuit is much simpler and easier to understand if all values are normalized by reference to the same number of turns.

It is best if all values are normalized as if all windings had one turn. Transformers function on the basis of Ampere-turns and Volt-seconds per turn—this is unchanged by normalization. The transformer magnetic fields and their stored energy are the same whether a winding has 10 turns carrying 2 Amperes or 1 turn carrying 20 Amps.) Also, with 1-turn windings, the permeance values obtained through the duality process do not require further conversion—permeances are in fact inductance values as seen through hypothetical one-turn windings. The transformer equivalent circuit remains simple, as shown in Fig. 5b, because all of the elements are on the same basis, and can therefore remain directly connected to each other without intervening turns ratios. This provides better insight and less confusion regarding their relative significance, and best visibility regarding the path to improvement.

With all of the windings normalized to one turn, the transformer equivalent circuit cannot be directly connected to the external circuitry. When it is desired to simulate operation in the actual circuit, each terminal pair must be connected to its external circuit through an ideal dc transformer with $1:N_x$ turns ratio, where N_x is the actual number of turns of that winding.

For example, in the transformer equivalent circuit of Fig. 5b, inductance values are normalized to 1 turn. To connect this equivalent circuit to its external circuit, the primary terminal pair P would be connected through a 1:28 turn ideal transformer, corresponding to the actual number of primary turns. Terminal pairs 1 and 2 would each connect through 1:14 turn ideal transformers. Terminal pair 3 can be directly connected to the external circuit since it actually has 1 turn.

The ideal transformers do nothing more than translate the current, voltage and impedances from the normalized transformer equivalent circuit to their actual values in the external environment. The normalized equivalent circuit of the transformer thus contains the non-ideal elements, properly related to each other.

Currents in each normalized 1-turn winding are proportional to load power. The highest power load translates into the highest current because with all windings 1-turn, the voltages are equal. This makes it more obvious that: *To minimize loss and other leakage inductance effects, the highest power winding should be closest coupled to the primary, and the winding hierarchy should progress from the greatest to the least power.*

The winding with the greatest power *change* translates into the greatest current change and greatest Ampere-turn change. *For best cross-regulation, this winding with the greatest power change should be closest coupled to the primary. The winding hierarchy should progress from greatest power* ***change*** *to least power* ***change****.*

VI. CIRCUIT SIMULATION

A. *Transformer Design Benefits*

Computer simulation of power supply performance is widely used, and is of tremendous benefit in power supply design. Simulation that focuses on the magnetic elements of the power supply can serve as the basis for improved transformer design, and also reveal unexpected problems. With a proper transformer equivalent circuit model, simulation can have the following benefits:

1. Quantify losses from energy stored in leakage and magnetizing inductances, which ends up dumped into snubbers or clamps.
2. Observe limitations on duty cycle due to Volt-second delays caused by leakage inductance. This may result in failure to achieve required output voltage at low line.
3. Measure cross-regulation problems and evaluate winding hierarchy in this regard.
4. Perform Fourier analysis of current waveforms to help deal more effectively with eddy current losses in the transformer windings.
5. Evaluate modified transformer designs.
6. Discover unexpected problems.

B. *Using the Model with Simulation Software*

Using the transformer equivalent circuit normalized to single turn windings, it is necessary to use ideal transformer models with $1{:}N_x$ turns ratio at each set of terminals to properly translate voltages and currents for compatibility with the circuitry external to the transformer. Ideal transformer models are available with most simulation software packages.

Although the currents within the normalized equivalent circuit differ from the currents in the actual windings, this is not a problem. The Ampere-turns are the same, and that is what determines the magnetic force. Leakage inductance *energy* is a function of ampere-turns and permeance, not turns.

When implementing the transformer equivalent circuit in the simulation software net listing, it is best to use discrete inductors to model the leakage inductances and mutual inductances. Avoid using the "coupled inductor" model, which unfortunately assumes a symmetrical bilateral coupling coefficient $k12 = k21$, and usually puts the leakage inductance is in the wrong place.

The effects of transformer parasitic inductances can be observed by simulation only in the time domain. This is because leakage inductances and mutual inductances store and release their energy within the span of each switching period.

Operating a switching power supply in the time domain with closed loop can be difficult. A great deal of time can be wasted attempting to solve convergence problems related to the steep leading edges encountered in switching supplies.

It is much easier to operate open loop in the time domain. Evaluating the closed loop is a separate problem best handled in the frequency domain. However, run times can be very long in the time domain, because time intervals are very short. And if the run is started with zero initial conditions, it can take forever to reach equilibrium operation, especially with control loop open. To avoid this problem, establish initial conditions for power switch pulse width, inductor currents and capacitor voltages that are estimated close to equilibrium values. It may be necessary to make two or three short runs to refine these initial estimates. This can take a lot less time than fighting convergence problems.

Don't worry too much about absolute accuracy - look at *differential changes*. For example, suppose that in checking DC cross regulation error between two outputs, one load is changed. With closed loop operation, the regulated output voltage would remain constant, but the other output would change. With open loop operation, both output voltages will probably change, but that is not important. The *differential* voltage change is the important concern.

C. *Minimizing Leakage Inductance*

The problems associated with leakage inductance are obviously reduced by minimizing the leakage inductance value (although some resonant converter topologies make beneficial use of leakage inductance.) In a conventional

transformer structure with concentric helical windings, the leakage inductance field between any two windings has the form of a thick walled cylinder. The shaded area in Fig. 8 shows the cross-section of the leakage inductance field between the primary and secondary 1. Similar cylindrical leakage inductance fields will occur between secondaries 1 and 2, and between 2 and 3.

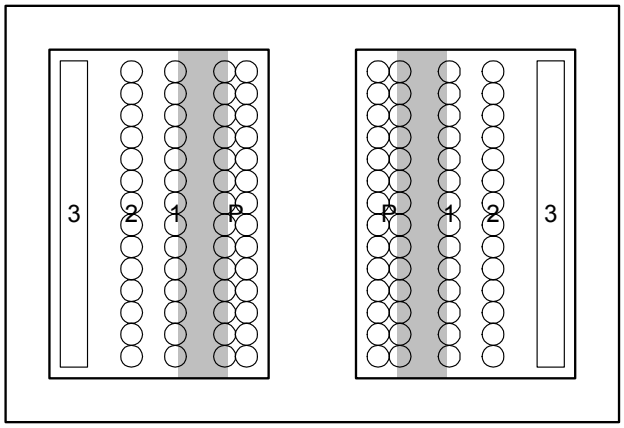


Fig. 8. Leakage inductance field.

The inductance formula of equation (10) shows what can be done to minimize leakage inductance. For $\boldsymbol{A}$ and $\boldsymbol{\ell}$ in equation (10), use the area and length of the cylindrically shaped leakage inductance field between adjacent windings.

Perhaps the best way of minimizing leakage inductance is to increase the length of the field. The same magnetic force (same Ampere-turns) is spread over a greater distance, resulting in lower field intensity, H, thus lower flux density, B, and much lower energy density. This is accomplished by selecting a core with a long narrow window. Thus, the length of the windings (winding breadth) is maximized, while the thickness of the windings and the number of layers is minimized. This has the additional very significant advantage of minimizing AC winding losses.

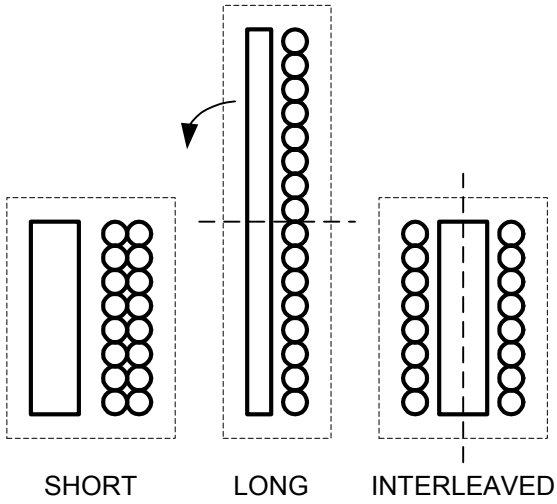


Fig. 9. Reducing leakage L and losses.

Ferrite cores designed for high frequency power applications have long narrow windows. Pot cores and PQ cores, although well shielded, are an example of the other extreme, resulting in high leakage inductance.

Interleaving the windings has the same beneficial result as doubling the winding length. Interleaving effectively uses twice the winding length that would fit the available window, then folds the combined lengthened windings in half to fit the available space. Thus the leakage inductance field is also doubled and folded, as shown in Fig. 9.

The disadvantage of increasing the length or interleaving the windings is that capacitance between the windings is increased.

The cross-section area of the cylindrical leakage inductance field is equal to the separation between the windings multiplied by the field circumference -- the mean length per turn of the windings. The cross-section area of the cylindrical leakage inductance field is minimized by minimizing the separation between the windings. Actually, the field penetrates *into* the windings, as shown in Fig. 8. Accuracy of the calculation is improved by assuming the field thickness equals the separation between the windings plus 1/3 of the thickness of each winding. Ideally, if the windings are wound together (multifilar), leakage inductance is virtually eliminated. However, dielectric isolation requirements or the use of copper foil windings often dictate a separation between the windings.

Even if the physical separation is reduced to zero, the field thickness still includes the penetration into each winding.

The only way to significantly reduce the circumference of the windings would be to use a core with a smaller diameter centerleg, but this would increase flux density, core losses, and perhaps saturate the core

Reducing the number of turns has a powerful effect on minimizing leakage inductance, but it also reduces shunt mutual inductance with a corresponding increase in magnetizing current and related losses. Also, reducing the number of turns increases flux swing in accordance with Faraday's Law. This may result in an unacceptable increase in core losses, or core saturation.

Any or all of the steps above should be taken, up to the point where adverse effects become undesirable. The design approach that will follow attempts to do just that.

Another important point to remember is that windings should conform to each other as much as possible. Windings should have the same length, placed one over the other. Do not place windings side-by-side along the core centerpost. This results in huge leakage inductance values.

VII. Design Strategy

The generalized recommendations in this section will be subsequently illustrated with specific application examples.

A. Designing a Transformer or Inductor for a Specific Application

The circuit designer must first specify the electrical requirements of the application before the magnetic device design can begin.

B. Core Selection

The first step in the design process is to tentatively select a core. this involves selecting the core material, core shape and size.[7]

At the frequencies involved in most switching power supply applications (>100 kHz), ferrite is the almost universal choice because it generally has lower losses than other available materials. High frequency losses in ferrites are mostly caused by eddy currents in the core. Ferrite materials with the highest resistivity have the lowest high frequency core loss, but these materials also have lower permeability, resulting in greater magnetizing current and smaller mutual inductance.

Select a core family with a long, narrow winding window. Maximizing the winding "breadth" minimizes the leakage inductance, minimizes the number of layers in each winding, and minimizes eddy current losses in the windings. Many good choices are possible in the E-E, low profile, and planar families Avoid pot cores and PQ cores, which have short, stubby windows.

The next step in core selection is to tentatively determine the appropriate core size. Experience can be very helpful in making this decision. Area product formulae are also useful in making an approximation of core size. At the conclusion of the design process (on paper), if the calculated temperature rise or calculated losses are too great, repeat the process using the next larger core size. Likewise, if losses and temperature rise are well below the design limits, repeat the design with the next smaller size.

C. Core Utilization

A core can be said to be fully utilized in a given application if it is operated at times at maximum flux density (determined by core loss or core saturation) and at other times, at maximum current density in the windings (determined by winding loss). Above 50 kHz, in applications where large flux swings are encountered, flux density is usually limited by core loss. (In transformers used in buck derived topologies such as forward converter, half bridge, and bridge, and in flyback transformers operated in the discontinuous mode.) But in filter inductors and flyback transformers operated in the continuous mode, flux swings are usually small, resulting in small core losses. Flux density is more likely to be limited by core saturation.

The author recommends a design approach which operates the core near its flux density limit, determined either by core loss or by saturation. By pushing flux density to its limit, the windings will have minimum turns, minimizing leakage inductance and minimizing

winding loss. Because core sizes come in discrete steps, it is most likely that the best choice will be somewhat oversize and thus the winding window may not be fully utilized. This is beneficial because it makes it easier to design the windings to achieve low ac loss.

D. Saturation or Loss Limited?

For a transformer -- changes in flux density, ΔB, are determined solely by the Volt-seconds per turn applied to the windings (Faraday's Law). In a transformer application, use the manufacturer's core loss data to determine the ΔB that can be sustained for normal operation. (As a rough guide, core loss of 100 mW/cm^3 is a good initial goal for a transformer operated with natural convection cooling.) Then calculate worst-case ΔB_{MAX} with maximum Volt-seconds under start-up or transient overload conditions, to determine whether flux density remains within the saturation limit under these abnormal conditions. According to Faraday's Law:

$$\frac{\Delta B_{MAX}}{\Delta B_{NORMAL}} = \frac{\text{max Volt-seconds}}{\text{normal Volt-seconds}} \qquad (11)$$

Magnetizing current in a transformer is unrelated to load. It is in addition to load related currents in the windings, and is usually much smaller. Magnetizing current can be determined from calculated flux density applied to the ferrite non-linear B-H characteristic shown on the core manufacturer's data sheet.

But **for an inductor or flyback transformer** – *all* of the current is *magnetizing* current, and current established by the external circuit, rather than Volt-seconds/turn, determines the points of operation along the B-H characteristic. In order to store the necessary energy in inductors and flyback transformers, non-magnetic gaps are used in series with the core. The gap characteristic is perfectly linear, and it dominates and linearizes the overall characteristic. Thus, although ΔB is always determined strictly by Faraday's Law, the linearized B-H characteristic results in flux density being also linearly related to Ampere-turns in the windings, so that:

$$\frac{\Delta B_{max}}{\Delta I_{max}} = \frac{B_{MAX}}{I_{MAX}} \qquad (12)$$

Since worst case ΔI and max. peak short-circuit current I_{MAX} are known circuit parameters, the above relationship makes it easy to determine whether flux density is limited by loss (ΔB_{max}), or by saturation (B_{MAX}).

E. Determine the Loss Limit

Losses may be limited either indirectly by a temperature rise limit, or by a direct loss limit imposed by efficiency considerations, whichever is smaller. Divide the temperature rise limit by the thermal resistance to calculate the temperature rise loss limit. Thermal resistance, R_T, for natural convection cooling is often stated on the manufacturers data sheet. Otherwise, thermal resistance can be crudely calculated from the following relationship:

$$R_T \approx \frac{36}{A_W} \qquad (13)$$

where A_W is the winding window area in cm^2.

F. Winding Losses

Design of the transformer windings to achieve acceptable AC losses can be both difficult and tedious. Computer software is available which can ease this task. A self –written spreadsheet program can prove helpful.

A detailed discussion of ac winding losses, skin and proximity effects, is beyond the scope of this topic – see references [5] and [6]. However, some important points to remember

When the number of turns in a winding exceeds the available breadth, then the winding must be built up in multiple layers, one on top of the other. However, AC winding losses increase exponentially with the number of layers, unless the conductor thickness is much less than the skin depth at the operating frequency. It is vitally important to minimize the number of layers in each winding. The layers can be minimized by:

1. Minimize the number of turns in the windings by operating the core close to the flux density limit.

2. Use a core shape with a long, narrow window. Greater winding breadth reduces the number of layers required to accommodate a given number of turns.

3. Interleave the windings. Interleaving essentially doubles the winding breadth, then folds the windings to fit the available space. This creates two *winding sections*, with half the total number of layers in each section.

Calculate the high frequency current skin depth (penetration depth, D_{PEN}) at the transformer operating frequency. $\boldsymbol{D_{PEN}}$ equals 0.24 mm at 100 kHz in copper at 100ºC, and varies inversely with the square root of frequency. *Remember that!* Thus, at any frequency:

$$\boldsymbol{D_{PEN}} = \mathbf{0.24}\left(\frac{\mathbf{100}\text{kHz}}{\boldsymbol{f}}\right)^{1/2} \text{ mm} \qquad (14)$$

$\boldsymbol{D_{PEN}}$ equals 0.12 mm at 400 kHz, .06 mm at 1.6 MHz, etc.

AC resistance curves such as in Fig. 10 and reference [5] demonstrate clearly the problem that occurs with multiple layers, requiring conductor thickness to be much less than $\boldsymbol{D_{PEN}}$.

However, a single layer winding which happens to be at the outside or the very inside of a group of windings can be of any thickness without any problem. This is because the magnetic field within the winding structure terminates on these layers at the inner and outer extremities. If these layers are much thicker than $\boldsymbol{D_{PEN}}$, the AC resistance will not benefit, but the DC resistance will be less.

When AC losses would otherwise be excessive because conductor thickness is too great, Litz wire is often used. Litz wire consists of many strands of fine wire interwoven in a unique way. (Simply twisting a bundle of fine wires won't do.) But a single layer of Litz wire must be considered as many layers of fine wires. For example, a Litz wire with 225 strands is roughly equivalent to a square array of 15 by 15 fine wires (15 is the square root of 225), and a single layer of this Litz wire must be considered 15 layers of the fine wire when entering the AC resistance curves.

It is necessary to evaluate the current waveforms in each winding to determine the average DC and RMS AC current values. Using the calculated value of DC resistance and the AC resistance multiplying factor, $\boldsymbol{F_R}$, obtained from the AC resistance curves, power loss in the winding can be calculated:

$$\boldsymbol{P_W = I_{DC}^2 \times R_{DC} + I_{AC}^2 \times R_{DC} \times F_R} \qquad (15)$$

Don't make the conductors any bigger than they need to be. If there is some space available within the winding window, resist the temptation to fill it with copper—this can actually make it more difficult to reduce AC losses.

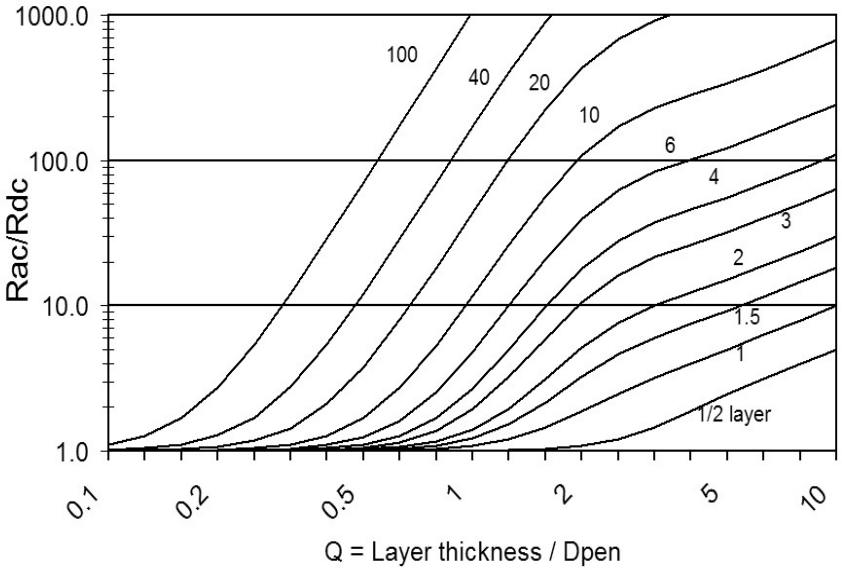


Fig. 10. AC resistance – R_{AC}/R_{DC}.

VIII. Flyback Transformer Design Example

A. Application Parameters:

Operating Mode: Continuous Inductor Current (CCM)
Frequency: 250 kHz
Input Voltage: 100 to 200 VDC
Max. Duty Cycle: 0.45 (@100 V)
Output 1: 3.3 V @ 1.5 A
Output 2: 5 V @ 0.6 A
Primary Inductance: 5 mH
Max. Ambient Temp: 85°C
Max. Temp. Rise: 40°C
Max. Loss: 0.25 W

Calculated Values (see Fig. 11 and Appendix)

Turns Ratio $N = N_P/N_S$: 24
Min. Duty Cycle D_{MIN}: 0.29 (@200 V)
Max Input Power: 8.83 W (@ 90% efficiency)
Max. Primary peak I_{PK}: 0.214 A (@ 100 V)
Max ΔI_{PRI}: .046 A (@ 200 V)
Max RMS Primary I_{FL} : 0.132 A (@ 100 V)
Max DC Primary I_{INdc}: .088 A (@ 100 V)
Max rms AC Primary I_{INac}: .098 A (@ 100 V)

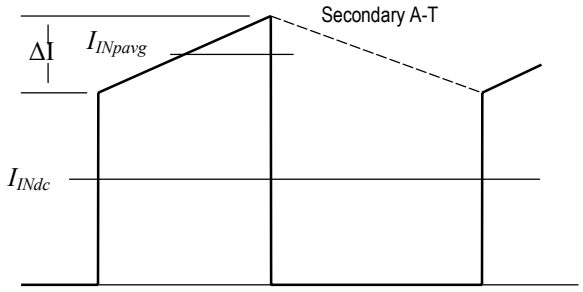


Fig. 11. Primary current waveform.

B. Define Core Material

In the continuous inductor current mode (CCM), the AC flux component is relatively small, so that the flux density swing is usually limited by saturation rather than core loss. ***Magnetics Type P*** material is chosen for this application because it has higher saturation flux density and higher permeability than K material. Lower loss K material would be the better choice for discontinuous mode operation, which has a much greater flux swing.

C. Determine the Maximum Flux Density

With continuous mode operation, start with the assumption that flux density is saturation limited. For P material at 125ºC, a B_{SAT} limit of 0.3 Tesla (3000 Gauss) is assumed. With a gapped core, flux density is linearly related to current, so that equation (12) is used, solving for ΔB_{max}:

$$\Delta B_{max} = \frac{B_{MAX}}{I_{MAX}} \Delta I_{max} \qquad (16)$$

$$\Delta B_{max} = \frac{0.3}{0.214} .046 = .065 \text{ Tesla}$$

Divide ΔB_{max} by 2 to convert from peak-peak to peak (core loss data is based upon peak ac values). Entering the manufacturer's core loss curves at .032T (320 Gauss) and 250 kHz, core loss is **16 mW/cm^3**. This is far below the 100 mW/cm^3 target for core loss limited operation, demonstrating that in this application, the core will definitely be saturation limited and core loss will be very small.

D. Define the Core Size and Configuration

Initial determination of core size can be based on the area product formula (Magnetics Design Handbook, page 5-6). Since the flux swing will be limited by saturation, not by core loss, equation (2a) from the Handbook is used:

$$AP = \left(\frac{LI_{SCpk} I_{FL}}{B_{max} K1} \right)^{4/3} \text{ cm}^4 \qquad (17)$$

The value of K1 for a flyback transformer with primary and secondary isolation is .0085.

$$AP = \left(\frac{5\times10^{-3}\times0.214\times0.132}{0.3\times.0085} \right)^{4/3} = .021 \text{ cm}^4$$

Referring to the core catalog, low profile core set 42110-EC with Area Product=.065 is tentatively chosen. Important measurements are:

Overall Core Dimensions: 2.0 x 2.0 x 0.376 cm
Winding Window Area, A_W: 0.38 cm^2
Window Width / Height: 1.488 / 0.325 cm
Mean Length per Turn MLT: 3.0 cm
Core Area, A_E: 0.171 cm^2
Core Path Length, ℓ_E: 4.61 cm
Core Volume, V_E: 0.79 cm^2

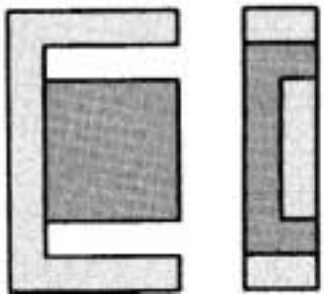


Fig. 12. Core set 42110-EC.

E. Determine the Loss Limit

From equation (13), thermal resistance can be estimated:

$$R_T \approx \frac{36}{A_W} \approx \frac{36}{0.38} \approx \quad 95 \text{ ºC/Watt}$$

Dividing the temperature rise limit, 40ºC, by 95ºC/Watt results in a temperature rise loss limit of 0.42 Watts. Since this is greater than the absolute loss limit of 0.25 W, the 0.25 W limit will apply, and temperature rise will be less than the 40ºC rise allowed in the specification.

F. Calculate the Number of Primary Turns, N_P

Since flux density is saturation limited in this application, B_{max} and corresponding max. peak current are used in equation (18) to calculate the minimum number of primary turns capable of achieving the required inductance value and push core operation to its flux density limit.

$$N_{P\min} = \frac{LI_{pk}}{B_{\max} A_e} = \frac{5\times10^{-3}\times0.214}{0.3\times0.17\times10^{-4}} = 210 \text{ t} \quad (18)$$

Calculate the minimum turns for the 3.3V secondary, and round up to nearest integer. Then recalculate primary turns:

$$N_S = {}^{N_P}\!/_{N} = {}^{210}\!/_{24} = 8.75 \rightarrow 9 \text{ turns}$$

$$N_P = N_S \times N = 9\times24 = 216 \text{ turns}$$

G. Calculate the Gap Length, ℓ_g

The inductance formula, equation (10), is inverted and solved for the air gap length that will satisfy the inductance requirement using the number of turns previously calculated (the 10^4 term modifies SI units to centimeters and micro-Henries):

$$\ell_g = \mu_0 N^2 \frac{A_g}{L}\times10^4$$

$$\ell_g = 4\pi\times10^{-7}\times216^2 \frac{0.171}{5000}\times10^4 = .020 \text{ cm}$$

This formula neglects the fringing field adjacent to the centerleg gap. In this application, the gap length is so small compared to the dimensions of the centerleg that the effect of the fringing field is minimal. Gap correction formulae can reduce inaccuracy due to fringing field.[8] Using the uncorrected gap length calculated above, if the measured inductance is too large, increase the gap length slightly by trial and error. Do not change the number of turns.

H. Define the Primary Winding

Primary Turns, N_P : 216 turns
Turns Ratio (3.3V), N : 24
Secondary Turns (3.3V), N_{S1}:9 turns
Primary lLngth = N_P x MLT = 216 x 3.0 = 648cm

Using wire tables (Reference [10]), AWG32 (0.2 mm) wire is selected for the primary.

Primary Winding AWG32 : 4 layers, 54 turns/layer, 216 t
Primary Resistance : .007 Ω/cm x 648 = 4.5 Ohms
AWG32 Insulated Diameter : 0.24 mm
Primary Breadth / Height : 13mm / 0.96mm
Skin depth @ 250kHz, D_{PEN} : 0.152mm (equation 14)

Referring to the procedure discussed in Reference [5], pages R2-8 to 9, the effective layer thickness equals the conductor diameter multiplied by 0.75, taking into account the conductors are round and spaced apart by the amount of insulation on the wires. Thus, the effective layer thickness equals 0.2 mm x 0.75 = 0.15 mm. Entering the AC resistance curves, Fig. 10:

Layer Thickness/D_{PEN}, Q = 0.15/0.152 = 0.99
AC Resistance Factor, F_R : 2.5 (4 layers)
AC Resistance Factor, F_R : 1.3 (2 layers - interleaved)

With the DC and AC currents defined, equation (15) is used to calculate the winding loss, for 4 and for 2 layers. Interleaving divides the windings into two sections, with 2 primary layers on each side of the secondaries, thus reducing F_R and AC loss substantially.

Non-interleaved:

$$P_W = .088^2 \times 4.5 + .098^2 \times 4.5 \times 2.5 = 0.143 \text{ W}$$

Interleaved:

$$P_W = .088^2 \times 4.5 + .098^2 \times 4.5 \times 1.3 = .091 \text{ W}$$

I. Define the 3.3 Volt Secondary Winding

Calculated Values (see Appendix):

Max DC Secondary I_{DC}: 1.5 A (@ 100 V)
Max rms AC Secondary I_{AC}: 1.35 A (@ 100 V)
Secondary Turns (3.3 V), N_{S1}: 9 turns
Secondary Length = N_{S1} x MLT = 9 x 3.0 = 27 cm

Litz wire consisting of 75 strands AWG40 is selected for the 3.3 V secondary, with 9 turns wound in a single layer. Turns are spaced apart to span 13 mm, conforming to the primary breadth. DC resistance is .000472 Ω/cm.

Secondary Resistance : .000472 Ω/cm x 27 = .0127 **Ω**
Insulated Diameter : 0.89 mm
Secondary Breadth / Height : 13 mm / 0.89 mm
AWG 40 Diameter: .08 mm
Skin depth @ 250 kHz, D_{PEN} : 0.152 mm (equation 14)

The effective layer thickness equals the AWG40 diameter multiplied by 0.75, taking into account the round conductors spaced apart by the amount of insulation on the wires. Thus, the effective layer thickness is .08 mm x 0.75 = .06 mm. The single layer of Litz wire with 75 strands of AWG40 is equivalent to 8.66 layers, 8.66 strands wide ($8.66^2 = 75$). Interleaving halves the effective layers to 4.33. Entering the AC resistance curves, Fig. 10:

Layer Thickness/D_{PEN}, Q = .06 / 0.152 = 0.4
AC Resistance Factor, F_R : 1.2 (8.66 layers)
AC Resistance Factor, F_R : 1.05 (4.33 layers - interleaved)

With the DC and AC currents defined, equation (15) is used to calculate the winding loss, for non-interleaved and for interleaved construction:

Non-interleaved:

$$P_W = 1.5^2 \times .0127 + 1.35^2 \times .0127 \times 1.2 = .056 \text{ W}$$

Interleaved:

$$P_W = 1.5^2 \times .0127 + 1.35^2 \times .0127 \times 1.05 = .053 \text{ W}$$

J. Define the 5 Volt Secondary Winding

Calculated Values (see Appendix):

Max DC Secondary I_{DC}: 0.6 A (@100 V)
Max rms AC Secondary I_{AC}: 0.54 A (@100 V)
Secondary Turns (5 V), N_{S2}: 14 turns
Secondary Length = N_{S1} x MLT = 14 x 3.0 = 42 cm

With 9 turns delivering 3.4 V (including synchronous rectifier drop), 14 turns produces 5.29 V. A Schottky rectifier should be used to reduce the output to a nominal 5 V.

Litz wire consisting of 30 strands AWG40 is selected for the 5-V secondary, with 14 turns wound in a single layer. Turns are spaced apart to span 13mm, conforming to the primary breadth. DC resistance is .00115 Ω/cm.

Secondary Resistance : .00115 Ω/cm x 42=.0483 Ω
Insulated Diameter : 0.56 mm
Secondary Breadth / Height : 13 mm / 0.56mm
AWG 40 diameter: .08 mm
Skin depth @ 250kHz, D_{PEN} : 0.152 mm (equation 14)

The effective layer thickness equals the AWG40 diameter multiplied by 0.75, taking into account the round conductors spaced apart by the amount of insulation on the wires. Thus, the effective layer thickness is .08 mm x 0.75 = .06 mm. The 30 strands of AWG40 are equivalent to 5.5 layers, 5.5 strands wide (5.5^2 = 30). Interleaving halves the effective layers to 2.75. Entering the AC resistance curves, Fig. 10.

Layer Thickness/D_{PEN}, Q = .06 / 0.152 = 0.4
AC Resistance Factor, F_R : 1.1 (5.5 layers)
AC Resistance Factor, F_R : 1.02 (2.75 layers - interleaved)

Equation (15) is used to calculate the winding loss, for non-interleaved and for interleaved construction:

Non-interleaved:

$$P_W = 0.6^2 \times .0483 + 0.54^2 \times .0483 \times 1.1 = .033 \text{ W}$$

Interleaved:

$$P_W = 0.6^2 \times .0483 + 0.54^2 \times .0483 \times 1.02 = .032 \text{ W}$$

K. Total winding losses

Non-interleaved:0.143 + .056 + .033 = **0.232 W**

Interleaved: .091 + .053 + .032 = **0.176 W**

Interleaving is not necessary to achieve loss goal, but can reduce loss by .056 W and reduce leakage inductance, at the expense of additional inter-winding capacitance.

Total winding Height = 2.41 mm

0.96 + 0.89 + 0.56 = 2.41 mm, out of an available 3.25 mm. An additional 2 layers of 1mil mylar insulation is placed between primary and secondaries, .05 mm total for non-interleaved, 0.1 mm total for interleaved windings.

L. Total Losses

Core loss equals 16 mW/cm^3 times core volume of 0.79 cm^3 equals **12.5 mW**. Thus, total loss equals:

Non-interleaved: $P_T = 0.232 + .013 = 0.245$ W

Interleaved: $P_T = 0.176 + .013 = 0.189$ W

M. The Equivalent Circuit Model

Fig. 13 shows the non-interleaved winding structure through the window on one side of the core (not to scale).

The corresponding reluctance model and electrical equivalent circuit are shown in Figs. 13a and 13b.

From equation (5), reluctance = $\ell/\mu A$. *Convert all dimensions to meters!*

For the cylindrical regions between P and S1, and between S1 and S2, Areas include 1/3 the thickness of adjacent windings (plus insulation between P and S1), multiplied by mean length per turn (MLT = 3 cm). The length of these cylindrical regions equals the breadth of the winding window = 1.488 cm.

Reluctance P-S1:

$$A_{P1} = \left(0.96/3 + 0.89/3 + .05\right)10^{-3} \times 3 \cdot 10^{-2}$$

$$= 2.0 \cdot 10^{-5} \quad \text{m}^2$$

$$\Re_{P1} = \frac{\ell}{\mu A} = \frac{1.488 \cdot 10^{-2}}{4\pi \cdot 10^{-7} \times 2 \cdot 10^{-5}} = 590 \cdot 10^6$$

Reluctance S1-S2:

$$A_{P1} = \left(0.89/3 + 0.56/3\right)10^{-3} \times 3 \cdot 10^{-2}$$

$$= 1.45 \cdot 10^{-5} \quad \text{m}^2$$

$$\Re_{12} = \frac{1.488 \cdot 10^{-2}}{4\pi \cdot 10^{-7} \times 1.45 \cdot 10^{-5}} = 816 \cdot 10^6$$

Reluctance of Centerleg Gap

$$\Re_{GAP} = \frac{\ell_g}{\mu A_e} = \frac{.020 \cdot 10^{-2}}{4\pi \cdot 10^{-7} \cdot 0.171 \cdot 10^{-4}} = 9.3 \cdot 10^6$$

Reluctances of the two outer legs are paralleled, and can be combined into a single reluctance. One half of the total ferrite path length is assigned to the combined outer legs, the other half to the centerleg, making these reluctances equal. Relative permeability of the ferrite equals 3000.

Reluctance of Ferrite Centerleg and Outer Legs

$$\Re_L = \frac{\ell_e/2}{\mu_0 \mu_r A_e} = \frac{\left(4.61/2\right) \times 10^{-2}}{4\pi \cdot 10^{-7} \cdot 3000 \cdot 0.171 \cdot 10^{-4}}$$

$$= 0.36 \cdot 10^6$$

Permeance values in Fig. 13b are the reciprocal of the reluctance values in Fig. 13a. Permeance values equal inductance that would be seen through a 1 turn winding, and should be multiplied by N^2 to obtain inductance value seen through a winding of N turns. For example, referred to the 216 turn primary, P_{GAP} = 0.107 µH x 216^2 becomes 5 mH, and leakage inductance P_{P1} = .0017 µH x 216^2 becomes 79 µH.

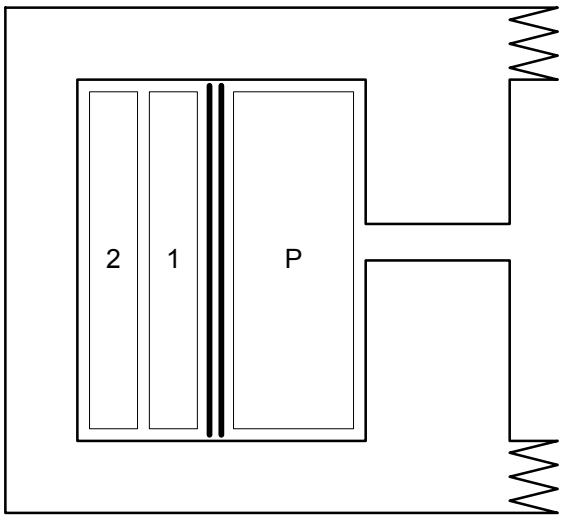


Fig. 13. Flyback transformer structure.

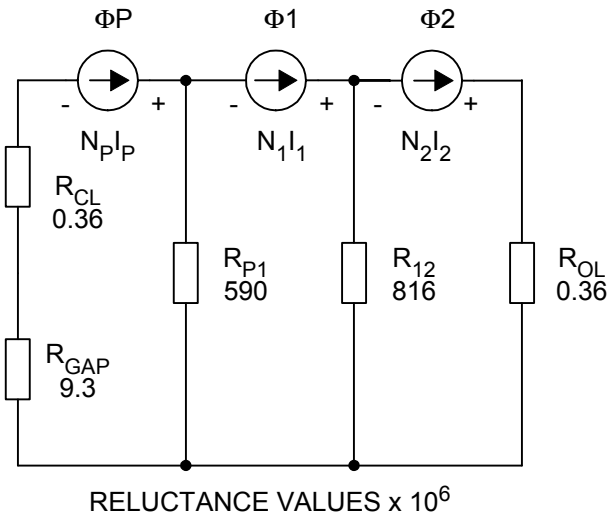


Fig. 13a. Reluctance model.

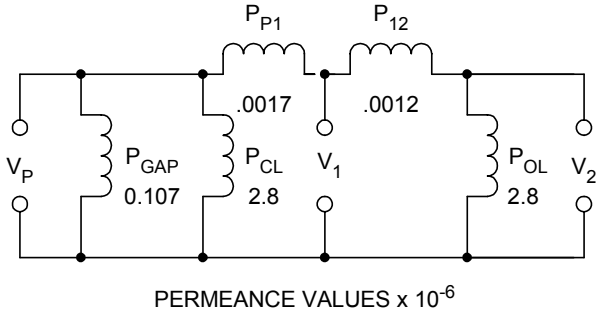


Fig. 13b. Equivalent circuit model.

IX. Transformer Design Example

A. Application Parameters:

Operating Mode:	Forward Converter, 250 W
Frequency:	250 kHz
Input Voltage:	100 to 200 VDC
Max. Duty Cycle:	0.45 (@100 V)
Output 1:	3.3 V @ 60 A
Output 2:	5V @ 10 A
Max. Ambient Temp:	85°C
Max. Temp. Rise:	40°C
Max. Loss:	2.5 W

B. Calculated Values (see Appendix):

Turns Ratio $N = N_P/N_S$: 12

C. Define Core Material

In the continuous current mode, the AC flux component is relatively large, so that the flux density swing is usually limited by core loss rather than saturation. ***Magnetics Type K*** material is chosen for this application because it has lower loss than P material, although it has lower saturation flux density and lower permeability.

D. Determine Maximum Flux Density

Start with the assumption that flux density is core loss limited. Refer to the core manufacturer's loss curves for the K material. Since the transformer will be used with natural convection cooling, the curve is entered at 100 mW/cm^3 and 250 kHz. The corresponding flux density is 700 Gauss, or .07 Tesla. The flux density axis on the core loss curves is based upon peak ac values, so multiply by 2 to convert from peak to ΔB (peak-to-peak). Thus **ΔB = 0.14 Tesla**

The turns ratio is established so that under normal operating conditions, maximum duty cycle, D_{MAX}, occurs only at low V_{IN} = 100 V. However, under abnormal operating conditions, such as during startup or with transient overload, the control circuit may call for D_{MAX} when the V_{IN} may be simultaneously at maximum – 200 V. Thus, the Volt-second pulses and corresponding ΔB applied to the primary for a few cycles will be greater than normal. From equation (11), solving for ΔB_{MAX}:

$$\Delta B_{MAX} = \frac{200\text{ V}}{100\text{ V}} 0.14\text{ T} = \mathbf{0.28}\text{ Tesla}$$

Since this is less than the B_{SAT} limit of 0.3 T (3000 Gauss) for K material, core operation is loss limited.

E. Define Core Size and Configuration

Initial approximation of core size can be based on the area product formula (Magnetics Design Handbook, page 4-8:

The value of K for a forward converter is .014.

$$AP = \left(\frac{P_O}{K\,\Delta B\,f_T} \right)^{4/3} \qquad (19)$$

$$AP = \left(\frac{250}{.014 \times 0.14 \times 250 \square 10^3} \right)^{4/3} = .41\text{ cm}^4$$

Referring to the Magnetics core catalog, from the ETD family, the smallest core set 43434-EC with AP = 1.21 is tentatively chosen.

Overall Core Dimensions: 3.4 x 3.4 x 1.08 cm
Core Area, A_E: 0.98 cm^2
Core Path Length, ℓ_E: 7.91 cm
Core Volume, V_E: 7.80 cm^2

Winding Window Area, A_W: 1.83 cm^2
Bobbin Winding Area, A_W': 1.23 cm^2
Winding Area Width/Height: 2.15 / 0.62 cm
Mean Length per Turn, MLT: 6.1 cm

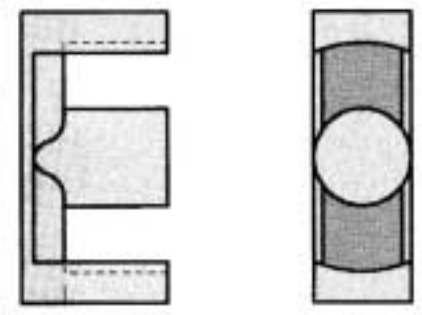


Fig. 14. 43434-EC core set.

Determine Loss Limit

From equation (13), thermal resistance can be estimated:

$$R_T \approx \frac{36}{A_W} \approx \frac{36}{1.83} \approx \mathbf{19.6}\text{ ºC/Watt}$$

Dividing the temperature rise limit, 40 ºC, by 19.6ºC/Watt results in a temperature rise limited loss of 2.04 W. Since this is less than the absolute loss limit of 2.5 W, the 2.04 W temperature rise limit will apply. One Watt will be allocated to core loss, 1 W to winding loss.

F. Recalculate Loss Limited Flux Swing?

With 1 W allocated to core loss divided by core volume of 7.8 cm^3, core loss of 128 mW/cm^3 is permissible. This would allow a slightly greater flux swing, but bring the worst case startup condition closer to saturation. Retaining the original 100 mW/cm^3 limit times 7.8 cm^3 core volume, **core loss will be 0.78 W**.

G. Calculate Max Volt-seconds/Turn

Faraday's Law:

$$\frac{d\phi}{dt} = -\frac{E}{N}$$

$$\max\ {}^{Vdt}\!/_{N} = A_E\,\Delta B = 0.98 \times 0.14$$
$$= \mathbf{13.72}\text{ Volt-}\mu\text{sec/turn}$$

H. Calculate Secondary Turns

Because the number of turns must be an integral number, the winding with the fewest turns poses the greatest difficulty. For example, if the minimum number of secondary turns dictated by max. Volt-seconds per turn equals 1.4, then 2 turns must actually be used. This will make the winding bulkier than optimum, perhaps necessitating a larger core size.

Secondary Volt-µsec:

$$V_O T = {}^{V_O}\!/_{f} = (3.3 + 0.1)/0.25 = \mathbf{13.6}\text{ V-µs}$$

Minimum secondary turns:

$$N_{S\,\min} = \left({}^{13.6\text{V-µs}}\!/_{13.72\text{V-µs/turn}} \right) = \mathbf{0.99}\text{ turns}$$

This is indeed fortunate! With a 1-turn secondary, flux swing will be only 1% less than the previously determined maximum. This will make it unnecessary to recalculate core loss.

But a 1-turn secondary for the 3.4 (3.3) V output results in 6.8 V from a 2 turn winding for the 5-V output. This will require a post-regulator. Cross-regulation problems are thereby eliminated. But a linear post-regulator will dissipate an unacceptable 17 W at 10 A, a 7% loss of efficiency. So a switching post-regulator must be used – at little cost by independent PWM control of the synchronous rectifiers in the 5-V output.

There are 3 alternatives to resolving this issue:

1. Use 1 turn for 3.3 V, 2 turns for 5 V, with switched post-regulation as above.

2. Go to 2 turns for the 3.3-V output, 3 turns for the 5-V output. 3.4 Vx3/2 = 5.1 V, allowing for a 0.1-V synchronous rectifier drop. There is probably room for the bulkier windings, because the core selected was significantly oversize, but cross-regulation becomes critical, and leakage inductance will be 4 times greater (2 turns^2), causing 4 times greater loss in snubbers or clamps. Flux swing will be much less, reducing core loss.

3. Use 1 turn for the 3.3-V output and 1½ turns for the 5-V output. Fractional turns require additional windings on the core, otherwise leakage inductance is totally unacceptable. See Reference [11]. Cross regulation becomes critical.

Because synchronous rectifiers will be used for both outputs, independent PWM of the 5-V output using Option 1, although it adds complexity, has the benefits of efficiency, regulation, and much lower leakage inductance,

I. Define Primary Turns

With a 12:1 turns ratio, the primary will have 12 turns.

J. Define Primary Turns

Calculated Values (see Appendix):

Max DC Primary I_{INdc}: 2.8A (@100V)
Max AC Primary I_{INac}: 3.37A (@100V)
Primary Turns, N_P : 12 turns
Primary Length = N_P x MLT = 12 x 6.1 = 73 cm

The primary is interleaved with 6 turns inside the secondaries, and 6 turns on the outside. The primary winding consists of 3 paralleled Litz wires, each with 100 strands AWG40. The three Litz wires are wound side-by-side in a single layer across the width of the bobbin. Six turns times 3 wires equals 18 Litz wires across the bobbin. Turns are spaced apart to span 20 mm, within the bobbin 21.5 mm winding breadth. DC resistance is .00045/3 = .00015 Ω/cm.

Primary Resistance :.00015 Ω/cm x 73 = .011 Ω
Insulated Diameter : 1.01 mm
Primary Breadth / Height : 20 mm / 1.01 mm x 2
AWG 40 Diameter: .08 mm
Skin Depth @ 250 kHz, D_{PEN} : 0.152 mm (equation 14)

The effective layer thickness equals the AWG40 diameter multiplied by 0.75, taking into account the round conductors spaced apart by the amount of insulation on the wires. Thus, the effective layer thickness is .08mm x 0.75 = .06mm. The single layer of Litz wire with 100 strands of AWG40 is equivalent to 10 layers, 10 strands wide (10 x 10 = 100). Entering the AC resistance curves, Fig. 10:

Layer Thickness/D_{PEN}, Q = .06 / 0.152 = 0.4
AC Resistance Factor, F_R : 1.25 (10 layers)

With the DC and AC currents defined, equation (15) is used to calculate the winding loss:

$$P_P = 2.8^2 \times .011 + 3.37^2 \times .011 \times 1.25 = 0.242 \text{ W}$$

K. Define the 3.3 Volt Secondary Winding

Calculated Values (see Appendix):

Max DC Secondary 1 I_{1dc}: 60 A (@100 V)
Max AC Secondary 1 I_{1ac}: 72 A (@100 V)

Secondary turns (3.3 V), N_{S1}:1 turn
Secondary length = N_{S1} x MLT = 1 x 6.1 = 6.1 cm

Solid copper strip, 1.5 mm thick by 2 cm wide, conforming to the primary breadth. DC resistance is 5.75 x 10^{-6} Ω/cm.

Secondary Resistance : 5.75x10^{-6} Ω/cm x 6.1 = 35 x 10^{-6} Ω
Thickness : 1.5 mm
Secondary Breadth / Height : 20 mm / 1.5 mm
Skin depth @ 250kHz, D_{PEN} : 0.152 mm (equation 14)

The effective layer thickness equals the 1.5 mm thickness of the strip. One turn equals 1 layer. Interleaving halves the effective layers to ½ layer. Entering the AC resistance curves, Fig.10:

Layer Thickness/D_{PEN}, Q = 1.5 / 0.152 = 9.9
AC Resistance Factor, F_R: 4.5 (1/2 layer - interleaved)

With DC and AC currents defined, equation (15) is used to calculate the winding loss, for interleaved construction:

$$P_{S1} = \left(60^2 + 72^2 \times 4.5\right) \times 35 \cdot 10^{-6} = 0.94 \text{ W}$$

This is a difficult situation. The layer thickness results in a DC loss component of only 0.125 W. The AC current, confined to the surfaces, results in a loss of 0.815 W. Without interleaving, only one surface of the copper strip would conduct AC current, doubling the AC loss. A thicker strip would reduce the already small DC loss, but not improve the AC loss.

L. Define the 5 Volt Secondary Winding

Calculated Values (see Appendix):

Max DC Secondary 2 I_{2dc}: 10 A (@100 V)
Max AC Secondary 2 I_{2ac}: 12.1 A (@100 V)

Secondary Turns (6.8 V), N_{S2}: 2 turns
Secondary Length = N_{S2} x MLT = 2 x 6.1 = 12.2 cm

Solid copper strip, 2 turns, 0.3 mm thick by 2 cm width, conforming to the primary breadth. DC resistance is 29 x 10^{-6} Ω/cm.

Secondary resistance : 29x10^{-6} Ω/cm x 12.2 = .00035 Ω
Thickness : 0.3 mm
Secondary Breadth / Height : 20 mm / 0.6 mm
Skin Depth @ 250 kHz, D_{PEN}: 0.152 mm
(equation 14)

The effective layer thickness equals the 0.3 mm thickness of the strip. Two turns equals 2 layers. Interleaving halves the effective layers to 1 layer. Entering the AC resistance curves, Fig. 10:

Layer Thickness/D_{PEN}, Q = 0.3 / 0.152 = 2.0
AC Resistance Factor, F_R: 2.0 (1 layer - interleaved)

With the DC and AC currents defined, equation (15) is used to calculate the winding loss, for non-interleaved and for interleaved construction:

$$P_{S2} = \left(10^2 + 12.1^2 \times 2.0\right) \times .00035 = 0.14 \text{ W}$$

Total winding losses:

$$P_W = 0.24 + 0.94 + 0.14 = 1.32 \text{ Watts}$$

M. Total Losses

Core loss equals **0.78** Watts. Thus, total loss equals:

$$P_T = P_W + P_C = 1.32 + 0.78 = 2.10 \text{ W}$$

This is less than the specified 2.5 Watt absolute limit, but greater than the 2.04 Watt temperature rise limit. With R_T = 19.6 ºC/W, temperature rise of 41ºC results, slightly exceeding the 40ºC limit. This is an acceptable result, especially considering the uncertainty of the R_T value.

N. Total winding Height:

$$1.01(\times 2) + 1.5 + 0.6 = 4.12 \text{ mm}$$

The available height is 6.1 mm. An additional 2 layers of 1mil mylar insulation is placed between primary and secondaries, and one layer between each of the secondary layers, for a total of 0.15 mm additional.

O. The Equivalent Circuit Model

Fig. 15 shows the interleaved winding structure through the window on one side of the core (not to scale).

The corresponding reluctance model and electrical equivalent circuit are shown in Figs. 15a and 15b.

From equation (5), reluctance = ℓ/μA. *Convert all dimensions to meters!*

For the cylindrical regions between P1 and S1, between S1 and S2, and between S2 and P2: Areas include 1/3 the thickness of adjacent windings (or to one skin depth in thick 3.3 A copper strip) plus insulation between windings, multiplied by mean length per turn (MLT=6.1 cm). The length of these cylindrical regions equals the breadth of the winding window = 2.15 cm.

Reluctance P1-S1:

$$A_{P1} = (1.01/3 + 0.15/3 + .05)10^{-3} \times 6.1 \cdot 10^{-2}$$

$$= 2.66 \cdot 10^{-5} \quad \text{m}^2$$

$$\Re_{P1} = \frac{\ell}{\mu A} = \frac{2.15 \cdot 10^{-2}}{4\pi \cdot 10^{-7} \times 2.66 \cdot 10^{-5}} = 643 \cdot 10^{6}$$

Reluctance S1-S2:

$$A_{12} = (0.15/3 + 0.6/3 + .025)10^{-3} \times 6.1 \cdot 10^{-2}$$

$$= 1.67 \cdot 10^{-5} \quad \text{m}^2$$

$$\Re_{12} = \frac{2.15 \cdot 10^{-2}}{4\pi \cdot 10^{-7} \times 1.67 \cdot 10^{-5}} = 1024 \cdot 10^{6}$$

Reluctance S2-P2:

$$A_{2P} = (0.6/3 + 1.01/3 + .05)10^{-3} \times 6.1 \cdot 10^{-2}$$

$$= 3.57 \cdot 10^{-5} \quad \text{m}^2$$

$$\Re_{2P} = \frac{2.15 \cdot 10^{-2}}{4\pi \cdot 10^{-7} \times 3.57 \cdot 10^{-5}} = 479 \cdot 10^{6}$$

Reluctances of the two outer legs are paralleled, and can be combined. One half of the total core path length is assigned to the combined outer legs, the other half to the centerleg, making these reluctances equal. Ferrite μr = 3000.

Reluctance of Ferrite Centerleg and Outer Legs

$$\Re_L = \frac{\ell_e/2}{\mu_0 \mu_r A_e} = \frac{(7.91/2) \times 10^{-2}}{4\pi \cdot 10^{-7} \cdot 3000 \cdot 0.98 \cdot 10^{-4}}$$

$$\Re_{OL} = \Re_{CL} = 0.107 \times 10^{6}$$

Permeance values in Fig. 15b are the reciprocal of the reluctance values in Fig. 15a. Permeance values equal the inductance that would be seen through a 1 turn winding. Permeance multiplied by N^2 gives the inductance value seen through a winding of N turns. For example, referred to the 12 turn primary, leakage inductance P_{P1} = .00156 μH x 12^2 becomes 0.22 μH.

For simulation in an external circuit, S1 is directly connected since it is 1 turn. Use a 1:2 ideal transformer to connect 2-turn S2. Use 1:6 transformers to connect each of the two primaries, with the external side of these transformers connected in series to achieve the actual 12 turns.

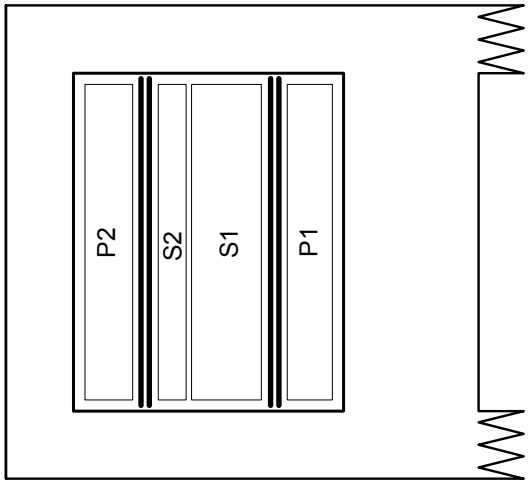


Fig. 15. Interleaved transformer structure.

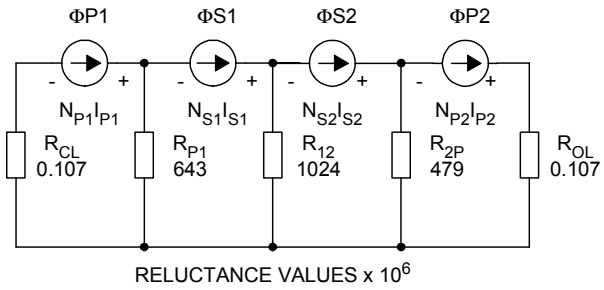


Fig. 15a. Reluctance model.

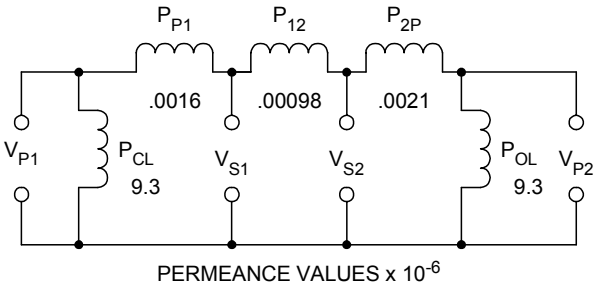


Fig. 15b. Equivalent circuit model.

X. REFERENCES

[1] Unitrode/TI Magnetics Design Handbook, TI Literature No. SLUP132

[2] L.H. Dixon, *The Effects of Leakage Inductance on Switching Power Supply Performance*, Unitrode/TI Magnetics Design Handbook, 2000, Topic R4, TI Literature No. SLUP132

[3] L. H. Dixon, *The 'k' Transformer Model, an Inappropriate Abstraction*, Unitrode/TI Seminar Manual SEM-1400, 2001, pp 3-12, TI Literature No. **SLUP171**

[4] L.H. Dixon, *Deriving the Equivalent Electrical Circuit from the Magnetic Device Physical Properties*, Unitrode/TI Magnetics Design Handbook, 2000, Topic R3, TI Literature No. SLUP132

[5] L.H. Dixon, *Eddy Current Losses in Transformer and Circuit Wiring*, Unitrode/TI Magnetics Design Handbook, 2000, Topic R2, TI Literature No. SLUP132

[6] L.H. Dixon, *Section 3 -- Windings*, Unitrode/TI Magnetics Design Handbook, 2000, Topic 3, TI Literature No. SLUP132

[7] L.H. Dixon, *Section 2 – Magnetic Core Characteristics*, Unitrode/TI Magnetics Design Handbook, 2000, Topic 3, TI Literature No. SLUP132

[8] L.H. Dixon, *Section 5 – Inductor and Flyback Transformer Design*, Unitrode/TI Magnetics Design Handbook, 2000, Topic 3, TI Literature No. SLUP132

[9] L.H. Dixon, *Section 4 – Power Transformer Design*, Unitrode/TI Magnetics Design Handbook, 2000, Topic 3, TI Literature No. SLUP132

[10] L.H. Dixon, *Winding Data*, Unitrode/TI Magnetics Design Handbook, 2000, Topic R7, TI Literature No. SLUP132

[11] L.H. Dixon, *How to Design a Transformer with Fractional Turns*, Unitrode/TI Magnetics Design Handbook, 2000, Topic R6, TI Literature No. SLUP132

The Unitrode/TI Magnetics Design Handbook and other materials referenced above are available on the web site:

power.ti.com/seminars

APPENDIX A

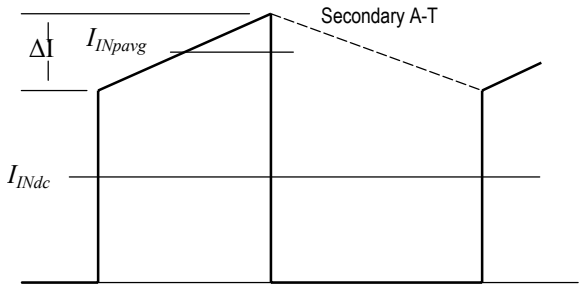
Although not strictly a part of the magnetic design, certain electrical parameters necessary for the design must be calculated:

I. FLYBACK TRANSFORMER, CONTINUOUS MODE

V_{IN}, V_{OUT}, Turns Ratio N = N_P/N_S, and duty cycle D are inter-related as follows. *D* is maximum at low V_{IN}, and minimum at high V_{IN}. (V_O is increased by a 0.1-V synchronous rectifier drop.)

$$N_P/N_S = \frac{V_{IN}D}{V_O(1-D)} = \frac{100\times0.45}{3.4(0.55)} = 24 \qquad D_{MIN} = \frac{V_O}{\left(V_{IN}/N + V_O\right)} = \frac{3.4}{\left(200/24 + 3.4\right)} = 0.29$$

Primary current waveform:



Maximum primary current occurs at low V_{IN}. First, calculate the DC component:

$$I_{INdc} = P_{IN}/V_{IN} = 8.8/100 = .088 \text{ Amps}$$

The primary current pulse average value:

$$I_{INpavg} = I_{INdc}/D = .088/0.45 = 0.196 \text{ A}$$

Maximum total RMS primary current:

$$I_{FL} = \left(I_{INdc}^2/D\right)^{1/2} = \left(.088^2/0.45\right)^{1/2} = 0.132 \text{ A}$$

The AC component:

$$I_{INac} = \left(I_{FL}^2 - I_{INdc}^2\right)^{1/2} = .098 \text{ Amps}$$

Maximum primary ΔI occurs at high V_{IN}, low *D*; minimum ΔI at low V_{IN}, high *D*. t_{ON} = D/f

$$\Delta I_{max} = \frac{V_{IN}D}{L_P f} = \frac{200\times0.29}{.005\times250K} = .046 \text{ Amps} \qquad \Delta I_{min} = \frac{V_{IN}D}{L_P f} = \frac{100\times0.45}{.005\times250K} = .036 \text{ Amps}$$

Maximum instantaneous peak current, I_{pk}, occurs at low V_{IN}:

$$I_{pk} = I_{INpavg} + \Delta I/2 = 0.196 + 0.36/2 = 0.214 \text{ A}$$

A. Calculate currents in 3.3-V secondary:

DC output current, $\mathbf{I_{DC}} = \mathbf{1.5}$ Amps

Maximum total RMS secondary current:

$$I_{FL} = \left({I_{DC}}^2 \Big/ (1 - D) \right)^{1/2} = \left(1.5^2 / 0.55 \right)^{1/2} = 2.02 \text{ A}$$

The AC component:

$$I_{AC} = \left({I_{FL}}^2 - {I_{DC}}^2 \right)^{1/2} = 1.35 \text{ Amps}$$

B. Calculate currents in 5-V secondary:

DC output current, $\mathbf{I_{DC}} = \mathbf{0.6}$ Amps

Maximum total RMS secondary current:

$$I_{FL} = \left({I_{DC}}^2 \Big/ (1 - D) \right)^{1/2} = \left(0.6^2 / 0.55 \right)^{1/2} = 0.81 \text{ A}$$

The AC component:

$$I_{AC} = \left({I_{FL}}^2 - {I_{DC}}^2 \right)^{1/2} = 0.54 \text{ Amps}$$

APPENDIX B

I. FORWARD CONVERTER

V_{IN}, V_{OUT}, Turns Ratio $N = N_P/N_S$, and duty cycle D are inter-related as follows. *D* is maximum at low V_{IN}, and minimum at high V_{IN}. (V_O is increased by 0.1V synchronous rectifier drop.) this calculated value is the *maximum* turns ratio, limited by D_{MAX}.

$$N_{MAX} = \frac{V_{IN\min} D_{\max}}{V_O} = \frac{100 \times 0.45}{3.4} = 13.23$$

A turns ratio of 13:1 will result in *D* at low V_{IN} a little less than the specified D_{max}. However, because the 3.3 V secondary will be quite thick, the winding structure must be interleaved, by dividing the primary into two equal sections, 6 turns each, so that $\boldsymbol{N} = \mathbf{12}$. Recalculating D_{max} with $N = 12$, **Dmax = 0.408.**

A. Calculate Primary Currents:

Once the turns ratios and D_{max} have been established, DC and AC currents in the windings can be calculated.

Maximum primary current occurs at low V_{IN}. First, calculate the DC component. Assuming 90% efficiency, power input is 250/.9 = 278 Watts:

$$I_{INdc} = P_{IN} / V_{IN} = 278 / 100 = 2.8 \text{ Amps}$$

Maximum total RMS primary current:

$$I_{FL} = \left(I_{INdc}^2 / D \right)^{1/2} = \left(2.8^2 / 0.408 \right)^{1/2} = 4.38 \text{ A}$$

The AC component:

$$I_{INac} = \left(I_{FL}^2 - I_{INdc}^2 \right)^{1/2} = 3.37 \text{ Amps}$$

B. Calculate currents in 3.3V secondary:

$$I_{1dc} = 60 \text{ Amps}$$

Maximum total RMS primary current:

$$I_{1FL} = \left(I_{1dc}^2 / D \right)^{1/2} = \left(60^2 / 0.408 \right)^{1/2} = 94 \text{ Amps}$$

The AC component:

$$I_{1ac} = \left(I_{1FL}^2 - I_{1dc}^2 \right)^{1/2} = 72 \text{ Amps}$$

C. Calculate currents in 5V secondary:

$$I_{2dc} = 10 \text{ Amps}$$

Maximum total RMS primary current:

$$I_{2FL} = \left(I_{2dc}^2 / D \right)^{1/2} = \left(10^2 / 0.408 \right)^{1/2} = 15.7 \text{ A}$$

The AC component:

$$I_{2ac} = \left(I_{2FL}^2 - I_{2dc}^2 \right)^{1/2} = 12.1 \text{ Amps}$$

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