Experimental Demonstrator of Full Bridge Modular Multilevel Converter For DC Grid Applications

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***Abstract*—This paper presents the design and control of 12kW medium voltage Modular Multilevel Converter (MMC) prototype, providing a general overview on both the component and system levels. A top level functional overview of the sub-module (SM) converter design including features like semiconductor temperature monitoring and protections for over-voltage, over-current, and over-temperature to enhance reliability. The paper also offers a comprehensive system overview, utilizing OPAL-RT as a high-level controller. To demonstrate the effectiveness of the proposed design, a 12-kW, three-phase MMC prototype was constructed, consisting of four full-bridge (FB) SMs in each converter arm. The paper explains communication management and the integration of analog and digital signals between the physical system and the user interface controller. Finally, the system's output under various operating conditions is analyzed and presented.**

***Index Terms*—Modular Multilevel Converter, Prototype, PCB, Hardware implementation.**

I. Introduction

Modular Multilevel Converters (MMCs) are well-known in academia and industry for their scalability, modularity, high efficiency, and excellent harmonic performance compared to other power electronics converters in comparable fields of implementation. Due to these features, MMCs are widely used in medium- and high-voltage, high-power applications [1]. While extensive literature exists on the control, reliability, and fault tolerance of different MMC sub-module (SM) configurations that feature experimental results focus on down-scaled prototypes in the 1 to 10 kilowatts, typically using two to five SMs per arm to validate their findings [2]–[6]. For medium voltage applications, number of submodules are typically in the range of 4 to 25, depending on the trade-off between efficiency and reliability for the given harmonic performance [7], [8].

This study provides a comprehensive overview of a customized four-level MMC designed to serve as a robust and holistic prototype for various applications, including reliability improvements. The sub-modules are configured as full-bridge (FB) SMs, which can operate as half-bridge (HB) SMs. The prototype includes temperature monitoring of the power modules (in this case, IGBTs) for further analysis. In this prototype, the OPAL-RT is used as the high-level controller-in-the-loop and user interface [9]. This type of demonstrator combines the flexibility of real time simulations with the fidelity of the actual hardware [10].

Fig. 1 presents the circuit configuration of the three-phase MMC, in which each arm consists of four FB SMs. Communication between the SMs and the high-level controller is achieved through digital to optical and vice-versa signals. The prototype includes two levels of protection: local protection at the sub-module level and system-level protection managed by OPAL-RT. The set-up will be used to demonstrate the application of back-to-back fault-tolerant MMCs in medium voltage grids [11]–[14].

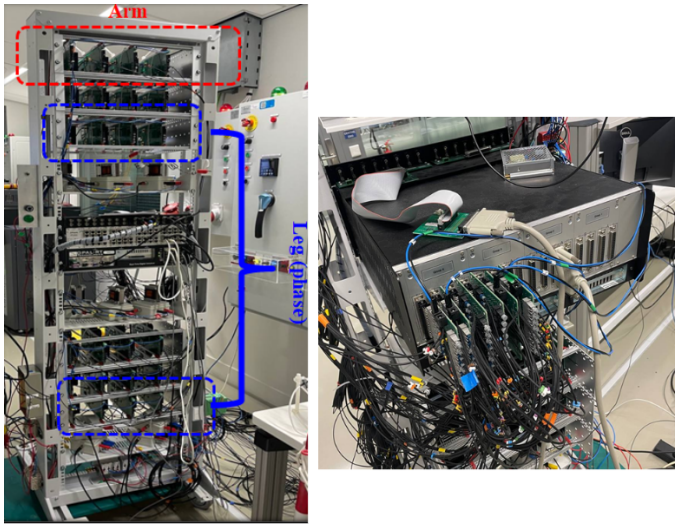


Fig. 1: Assembled lab scale MMC tower (a) front-end, (b) back-end.

This paper outlines the steps required to construct the MMC, which can incorporate features such as fault tolerance, reliability optimization, and scalability. The rest of the paper is organized as follows: II details the design of the MMC from the sub-module level to the system level. Section III elaborates on the controllers and their software interfaces. Section IV presents results from the working model using two different modulation strategies. The paper concludes in Section V.

II. MMC design

The MMC is composed of power electronics SMs connected in series. Each phase of the MMC consists of two identical arms, termed the upper and lower arms. In the configuration described in this paper, each arm includes four SMs, totaling 24 SMs for the entire system. The arms are coupled via inductors acting as filters and utilized for control. Each SM typically consists of a capacitor connected to the DC bus

of either a half-bridge or full-bridge topology, with both configurations supported by the design used in this paper [15].

Each SM has a local controller based on the Xilinx XC95144XL CPLD, programmable via JTAG. The OP5600 real-time simulator from OPAL-RT serves as the central controller for all 24 SMs and can be programmed from a computer. To reduce electromagnetic interference (EMI) and ensure high voltage isolation, communication between the OPAL-RT and CPLDs is via fiber-optic transmitters and receivers, with a custom PCB handling the electrical-optical signal conversion.

For practical system control, key parameters such as the capacitor voltage of each SM, arm current, arm voltage, and DC bus voltage are monitored and transmitted to the OPAL-RT. Capacitor voltages are sent via fiber optics, while LEM sensors measure the arm current, arm voltage, and DC bus voltage. These analog measurements are then relayed to the OPAL-RT. Fig. 1 illustrates the practical implementation of the lab-scale MMC prototype.

A. Interconnection of system

A top-level overview of the MMC tower shown in Fig. 1 is demonstrated in Fig. 2. Each SM receives three fiber-optic signals from the OPAL-RT: an enable signal to activate the specific SM, the HB1 gate signal, and the HB2 gate signal, which correspond to the transmitted PWM signals to the OPAL-RT. A DIP switch on the PCB allows the CPLD to be configured for operation in either half-bridge or full-bridge mode.

Each SM sends two fiber-optic signals to the OPAL-RT: one for IGBT module temperature and one for capacitor voltage using PWM. An analog-to-digital circuit converts these measurements into digital signals, which are transmitted via an optical transmitter. The SM uses frequency modulation for both signals, and the OPAL-RT converts the PWM frequency back to voltage using an internal lookup table.

A custom inductor is used to control the arm current delivered to the load, with each arm current measured by an S-6NP sensor. The LEM LV 25-P voltage transmitter is employed for phase and DC bus voltage measurements, sending the analog measurement signals to the OPAL-RT through the OP8211 interface.

The OPAL-RT serves as the central controller, enabling the user to implement custom control schemes, tune parameters in real-time, and monitor measured values to achieve the desired voltage and current.

This communication is established via an Ethernet port between the user's PC and the OPAL-RT. Commercially available isolated converters power all components at various DC voltage levels, ensuring safety and ease of use. Circuit breakers are installed in series with the power outlets for additional protection.

B. SM Design

The MMC FB can be configured using either a FB or two HBs. To reduce complexity and cost and improve reliability, the PS219B4-S power module was selected, featuring

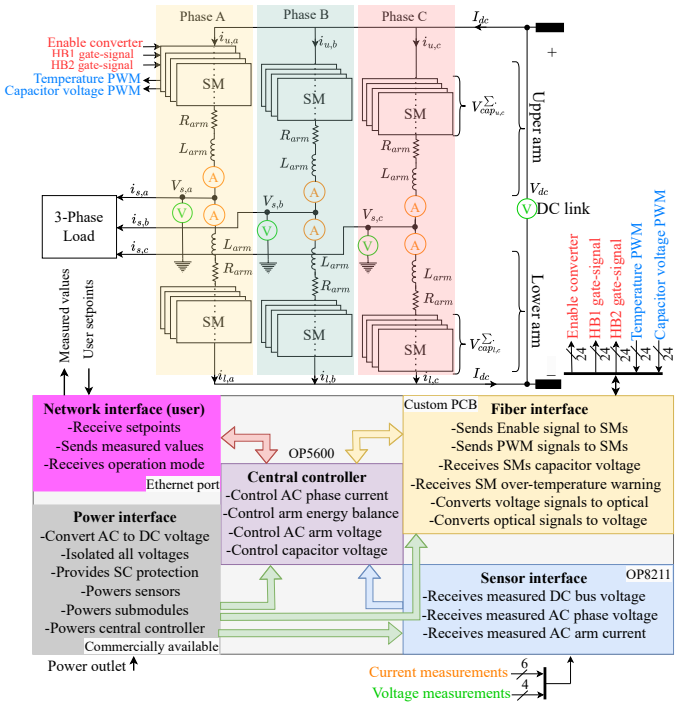


Fig. 2: Top level interconnection of MMC tower

three built-in IGBT HBs with integrated gate drivers and a temperature-sensing pin. For FB configuration, two HBs are used, and if HB configuration is desired, it can be achieved by disabling two gate signals from the CPLD.

Capacitor sizing is crucial due to its typically large size. To address this, each SM is divided into two separate PCBs—one for the IGBTs and one for the capacitors, as shown in Fig. 4. The IGBT board receives two PWM and an enable signals from the OPAL-RT via fiber-optic receivers, while the DC capacitor voltage and module temperature are returned to the OPAL-RT. Fig. 3 shows the top-level schematic of each SM.

A supplementary circuit protects against over-current, over-voltage, and over-temperature by comparing the signals to hardware-implemented thresholds. Although the power module includes built-in gate drivers, it does not feature dead-time control. The SM swiftly disables PWM signals through the CPLD in over-temperature or over-voltage conditions. The SM bypasses the CPLD for over-current conditions and directly shuts off the power module via the control pin for a faster response. A debug connector with the necessary signals facilitates troubleshooting, and isolated power supplies ensure proper isolation between SMs.

III. Software and Controls

This study conducts the experiment by considering the characteristics listed in Table I, which shows the maximum values the prototype can handle [15]. Since, in this prototype, the capacitor bank is detachable from the main SM PCB board, it can be redesigned without any changes to the central system for any research or industry purposes. Also, arm resistance is a parasitic value that can be affected by multiple factors,

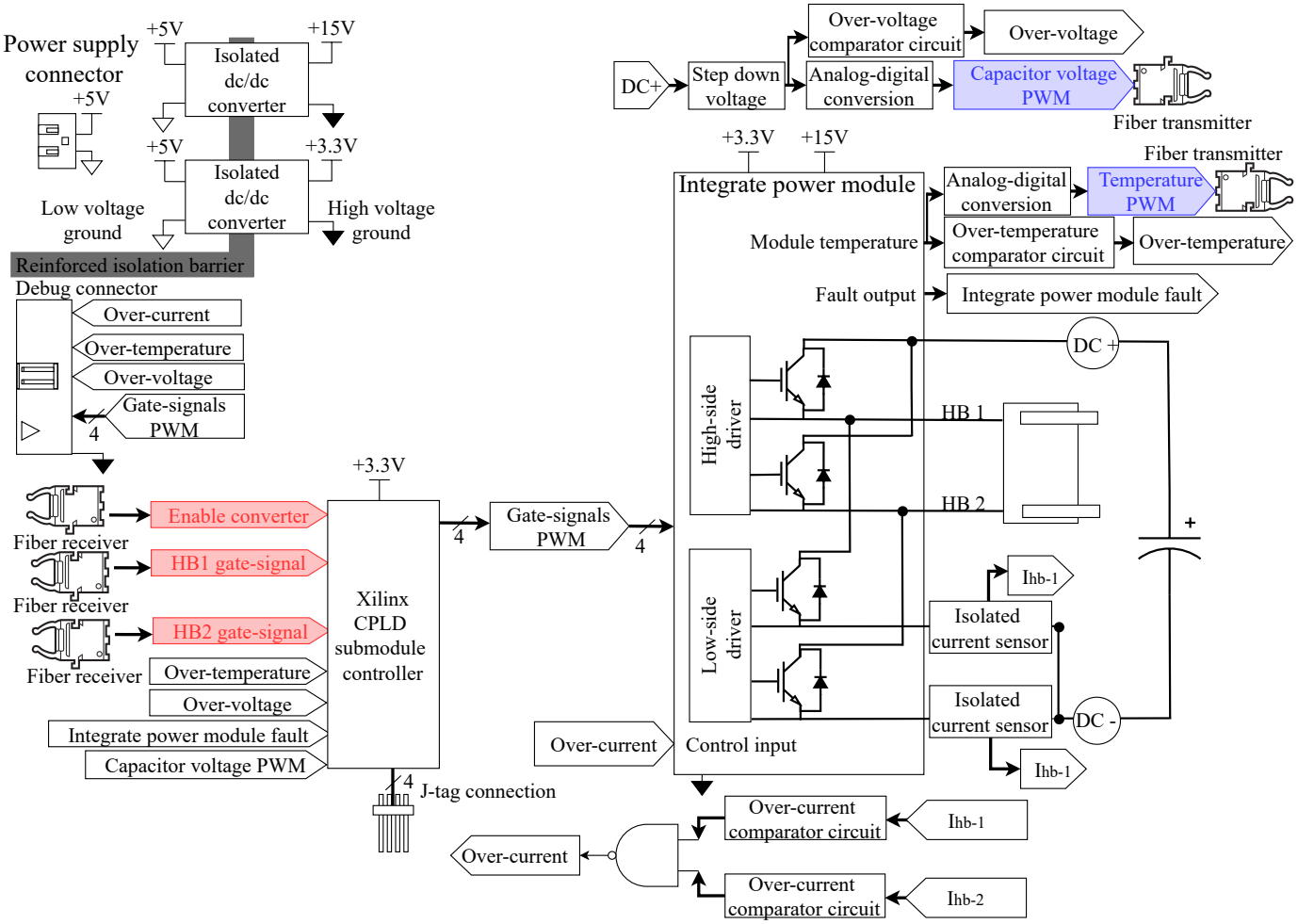


Fig. 3: Top level schematic of the SM circuit

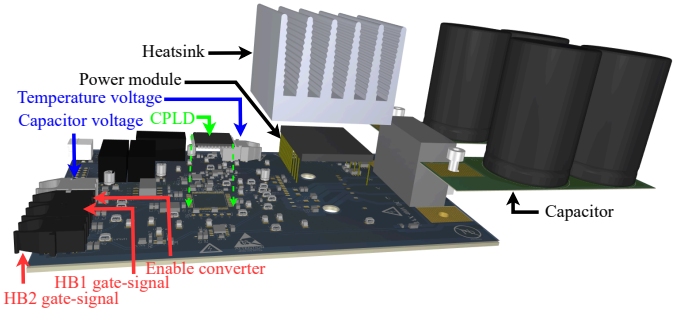


Fig. 4: CAD rendering of the submodule.

TABLE I: MMC Operational Characteristics

Symbols	Item	Value	Max§
N	Number of SMs	4	-
V_{dc}	Pole-to-pole DC voltage	100 V	800 V
V_{SM}	Applied IGBT Voltage	25 V	200 V
C_{SM}	SM capacitance	4 mF*	-
L_{arm}	Arm Inductance	4.3 mH	-
$R_{arm}(R)$	Arm resistance	0.178 Ω‡	-
f_{sw} (PSC)	Switching frequency	1000 Hz	100 kHz
$f_{Control}$ (NLM)	Transition rate of controller	1500 Hz	100 kHz

§ Maximum rated value of the prototype
* it can be redesigned as it is a separate PCB attachable to the main SM board
‡ Estimated resistance of the arm inductor at 50 Hz and rated operating condition

such as SM PCB, wiring connecting the system, and inductor. However, the arm inductor also has resistance, calculated at 50 Hz and rated power. Hence, at different working conditions, this value can change [16]–[18].

As explained in this prototype, the physical MMC is controlled by an independent central system, which runs a Simulink-based controller in OPAL-RT.

As shown in Fig. 2, communication between the SMs and the central controller is facilitated through digital HP1 gate signals, HP2 gate signals, enable signals, and analog current and voltage measurements. In this prototype, the controller, illustrated in Fig. 5, reads the data, interfaces with the user, and then sends output signals—primarily de-gating signals and enabling signals for user-defined protection—to the SMs. It's important to note that digital inputs are converted into actual values using lookup tables; for example, specific received frequencies are translated into corresponding actual values for automation purposes.

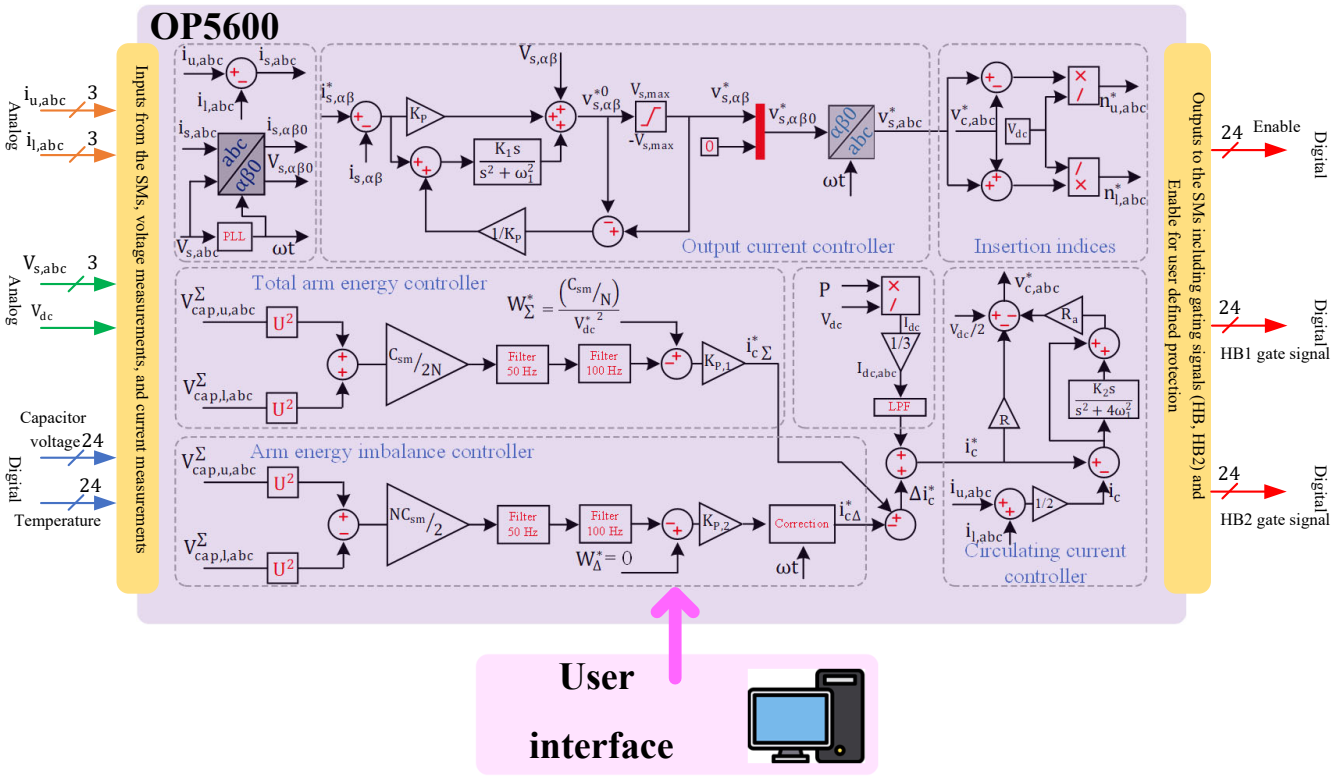


Fig. 5: Central controller of the MMC user-interfaced through the OPAL-RT.

The general control block diagram of the MMC [19] is shown in Fig. 5. It includes an output current controller that manages the output active and reactive powers, a total energy controller, and an imbalance controller that balances the energy storage within each SM and between the upper and lower arms. A circulating current controller is employed to suppress the circulating current. The outputs of the circulating current controller and the outer current controller are combined to generate the insertion indices. These indices produce the digital gating signals by applying various modulation strategies.

The enable signal serves as a user-defined protection mechanism. Specific values are compared with their thresholds, and if necessary, the system is protected by sending the enabling signals to the SMs.

IV. Results

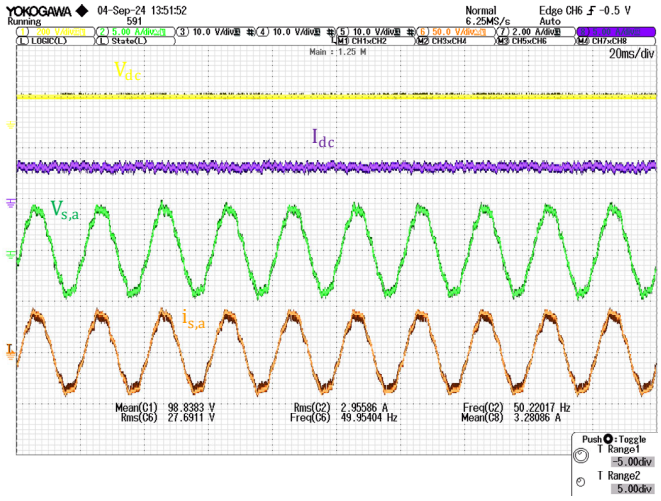
As a demonstration, the prototype was tested and validated under the conditions outlined in Table I. The prototype operates in inverter mode (DC to AC) and is connected to a resistive load, as shown in Fig 2. The results are presented for the FB configuration, where two modulation strategies—Phase Shift Carrier (PSC) and Nearest Level Mode (NLM)—were tested.

One of the key advantages of using OPAL-RT as the controller-in-the-loop system is its user-friendly interface, allowing real-time tuning of control parameters while the system is in operation. It lets the user switch between operating conditions, such as changing modulation strategies. Fig. 6 and Fig. 7 display the AC and DC side voltage and current waveforms for NLM and PSC modulation, respectively. It is worth noting that NLM is typically applied in MMCs with more than 12 SMs per arm in real-world applications. However, in this case, the outputs are shown to validate the prototype's functionality under different modulation strategies.

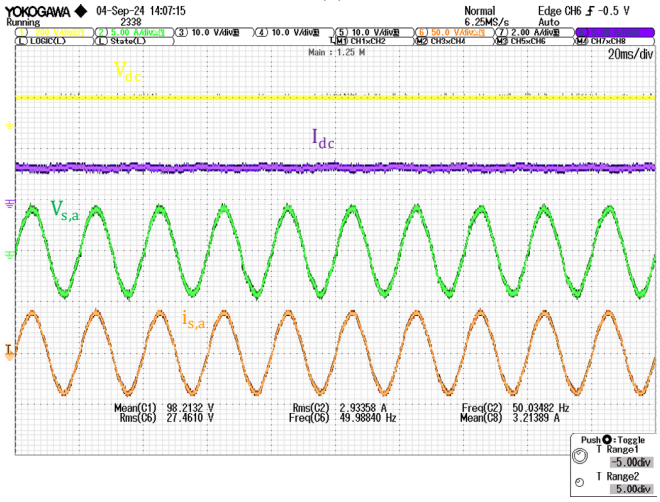
Further experimental results are presented in Fig. 7 (a), (b) for NLM and PSC, respectively. The arm current of For the upper and lower arm of phase A, the currents $(i_{u,a}, i_{l,a})$, a single SM's capacitor voltage $(V_{cap,u,1}, V_{cap,l,1})$, the summation of capacitors voltage $(V^{\Sigma}_{cap,u,a}, V^{\Sigma}_{cap,l,a})$ and the difference between them are presented. As it can be understood, the NLM modulation strategy is performing better when balancing the energy between all the SMs and the upper and lower arms. However, for the number of SM levels in this prototype, the AC voltage and current are quite sinusoidal, which is the advantage of PSC for an MMC with a low number of levels.

V. Conclusion

In this paper, we developed and implemented an MMC prototype using OPAL-RT for hardware-in-the-loop simulation. The design included FB SMs, which were configured to operate in inverter mode (DC to AC) and tested with a resistive load. Two modulation strategies, PSC and NLC, were evaluated, and their performance was compared. The prototype demonstrated reliable operation, with PSC showing better performance in systems with fewer levels and NLC

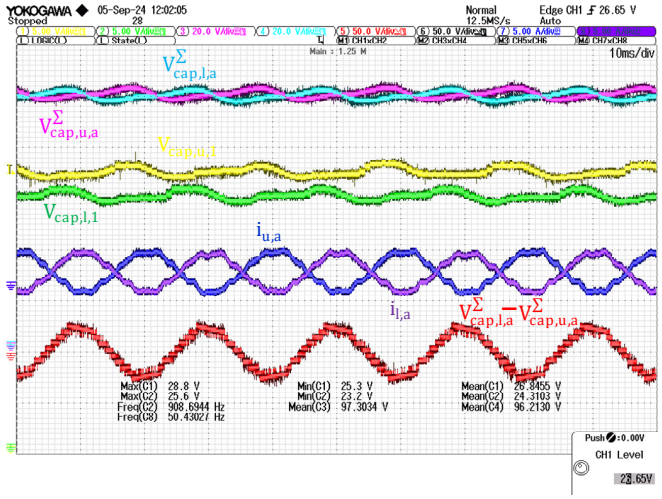


(a)

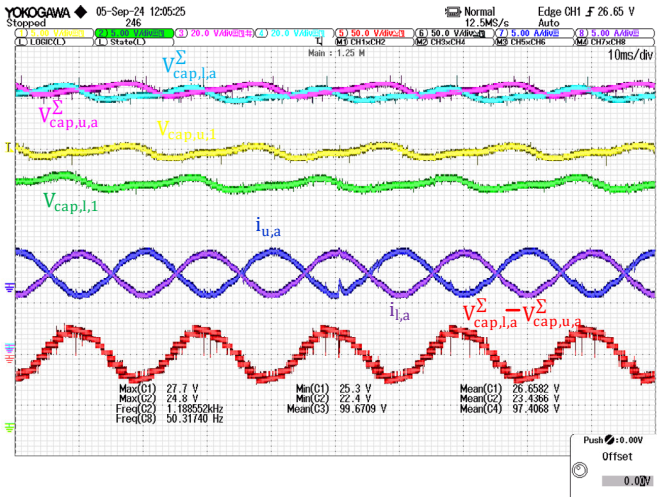


(b)

Fig. 6: DC side (DC-link current and voltage) and AC side (phase A current and voltage) waveforms of the MMC under (a) NLM (b) PSC modulation strategy.



(a)



(b)

Fig. 7: The MMC's waveform for the upper and lower arm of phase A for capacitor voltage, arm current, sum of each arm capacitors voltage, and the difference between lower and upper arm capacitors voltage under (a) NLM (b) PSC modulation strategy.

being more suitable for applications with a higher number of SMs.

The OPAL-RT platform provided an efficient and flexible interface for real-time control, allowing for easy tuning of control parameters and switching between modulation strategies during operation. The system's communication between the SMs and the central controller was successfully managed using digital and analog signals, ensuring proper monitoring and protection.

Overall, this MMC prototype offers a comprehensive and scalable solution for future research, with applications in improving system reliability, fault tolerance, and control strategies. The design also supports further experimentation and development in medium and high-power systems.

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