

Familiarisation avec les étapes d'un projet VHDL

Départements : TIC

Unité d'enseignement

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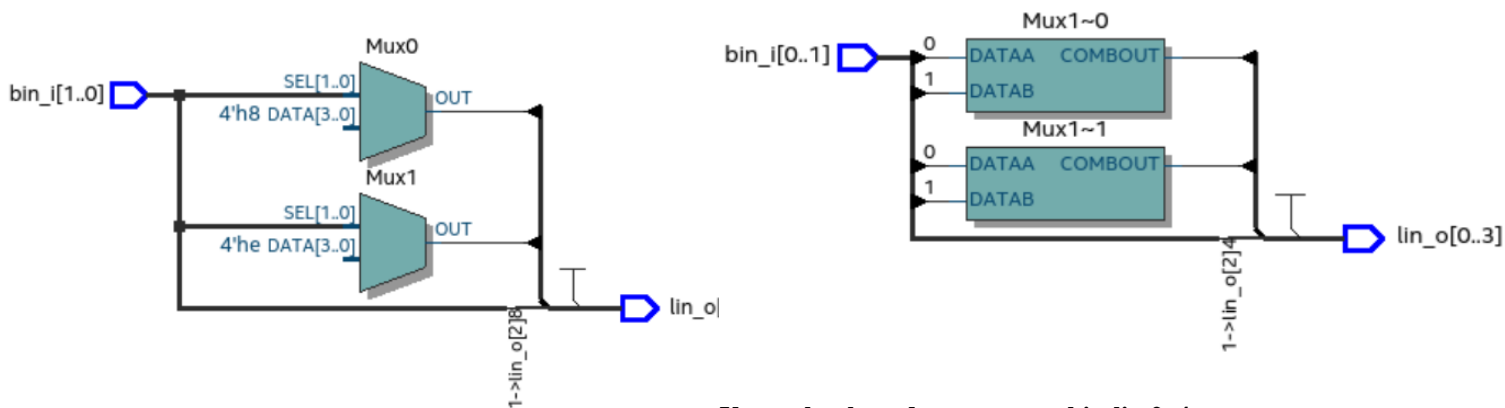
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Classe : **CSN A**
Salle de labo : **A09**

Date : **06.03.2024**

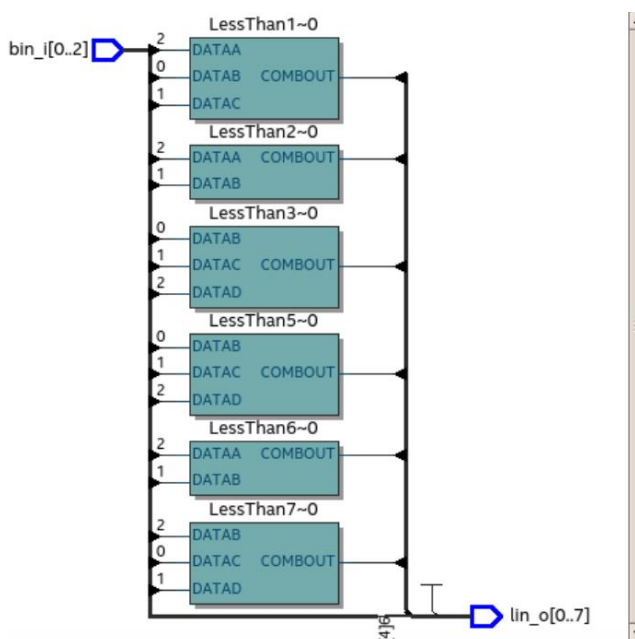
Screenshots

Pour ce labo de découverte, il a fallu implémenter un fichier vhd 3to8

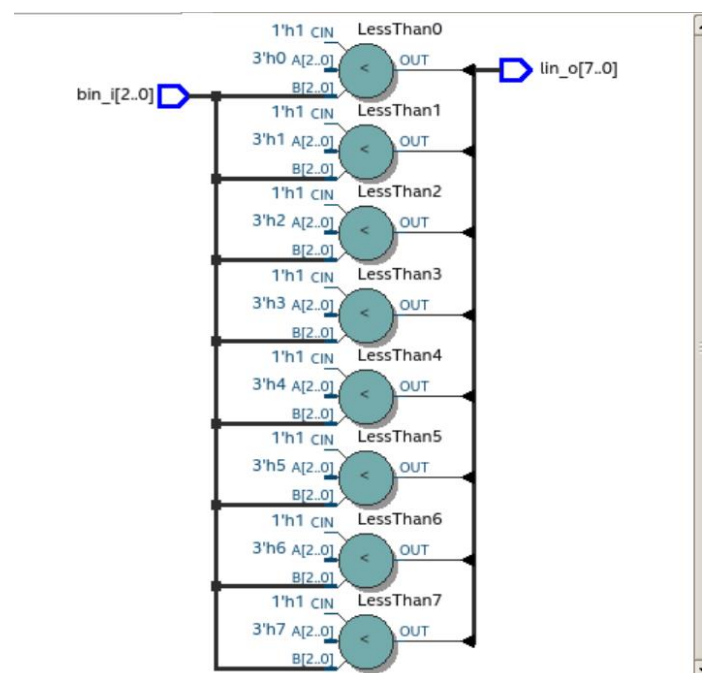


Vue technology du composant bin-lin 2a4

Vue RTL du composant bin-lin 2a4



Vue RTL du composant bin-lin 3a8



Vue technology du composant bin-lin 3a8

```
# End time: 18:30:50 on Mar 05,2024, Elapsed time: 0:00:01
# Errors: 0, Warnings: 0
# QuestaSim-64 vcom 2020.1_1 Compiler 2020.03 Mar 4 2020
# Start time: 18:30:50 on Mar 05,2024
# vcom -reportprogress 300 -work work ../src_tb/bin_lin_3to8_tb.vhd
# -- Loading package STANDARD
# -- Loading package TEXTIO
# -- Loading package std_logic_1164
# -- Loading package NUMERIC_STD
# -- Compiling entity bin_lin_3to8_tb
# -- Compiling architecture test_bench of bin_lin_3to8_tb
# -- Loading entity bin_lin_3to8
# ** Warning: ../src_tb/bin_lin_3to8_tb.vhd(46): (vcom-1236) Shared variables must be of a protected type.
# End time: 18:30:50 on Mar 05,2024, Elapsed time: 0:00:00
# Errors: 0, Warnings: 1
# vsim -voptargs="" +acc work.bin_lin_3to8_tb
# Start time: 18:30:50 on Mar 05,2024
# ** Note: (vsim-3812) Design is being optimized...
# Loading std.standard
# Loading std.textio(body)
# Loading ieee.std_logic_1164(body)
# Loading ieee.numeric_std(body)
# Loading work.bin_lin_3to8_tb(test_bench)#1
# Loading work.bin_lin_3to8(flot_don)#1
QuestaSim> run all
# Invalid time value: all
VSIM 3> run -all
# ** Note: debut de simulation
# Time: 0 ns Iteration: 0 Instance: /bin_lin_3to8_tb
# ** Note: *** VOUS ETES LES MEILLEURS ***
# Time: 900 ns Iteration: 0 Instance: /bin_lin_3to8_tb
# ** Note: *** BRAVO, pas d'erreur ***
# Time: 900 ns Iteration: 0 Instance: /bin_lin_3to8_tb
```

Log de Questasim du bin-lin 3a8.