HAUTE ÉCOLE
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Reconfigurable & embedded
Digital Systems

Description d'éléments mémoire

Départements : TIC

Unité d'enseignement CSN

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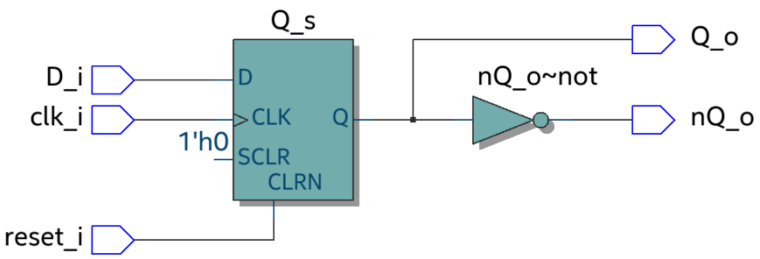
Classe : **CSN**
Salle de labo : **A07 ou A09**

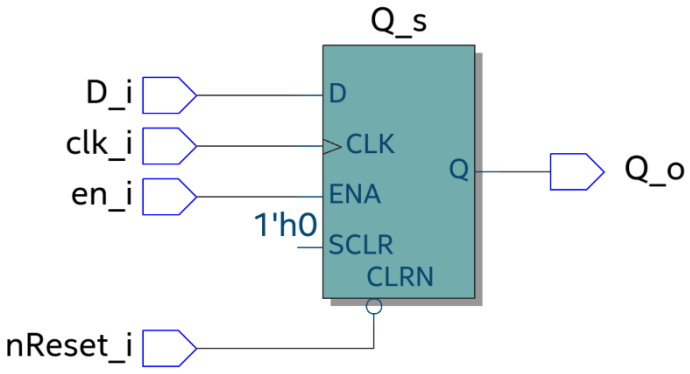
Date : **17.04.2024**

1 Dff_ar_en



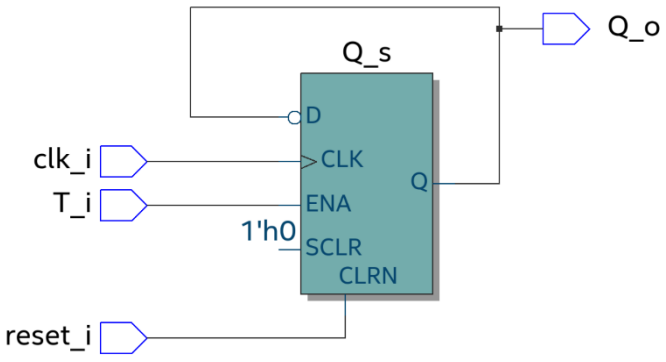

```
# vsim -voptargs=""+acc"" work.dff_ar_tb
# Start time: 22:12:09 on Apr 17,2024
# ** Note: (vsim-3813) Design is being optimized due to module recompi
# Loading std.standard
# Loading std.textio(body)
# Loading ieee.std_logic_1164(body)
# Loading work.dff_ar_tb(test_bench)#1
# Loading work.dff_ar(comport)#1
VSIM 16> run -all
# ** Note: >> Debut de la simulation
#    Time: 0 ns  Iteration: 0  Instance: /dff_ar_tb
# ** Note: >>Nombre d'erreur détectée = 0
#    Time: 552 ns  Iteration: 0  Instance: /dff_ar_tb
# ** Note: >>Fin de la simulation
#    Time: 552 ns  Iteration: 0  Instance: /dff_ar_tb
```

2 Dff_en



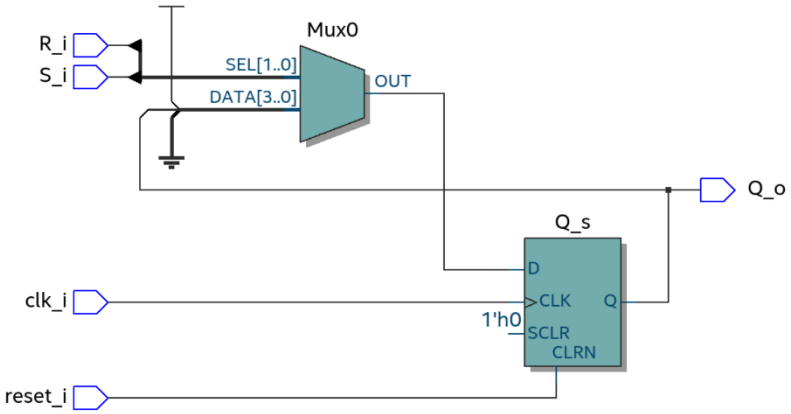

```
# vsim -voptargs=""+acc"" work.dff_en_tb
# Start time: 22:00:49 on Apr 17,2024
# ** Note: (vsim-3812) Design is being optimized...
# Loading std.standard
# Loading std.textio(body)
# Loading ieee.std_logic_1164(body)
# Loading work.dff_en_tb(test_bench)#1
# Loading work.dff_en(comport)#1
VSIM 4> run -all
# ** Note: >> Debut de la simulation
#    Time: 0 ns  Iteration: 0  Instance: /dff_en_tb
# ** Note: >>Nombre d'erreur détectée = 0
#    Time: 652 ns  Iteration: 0  Instance: /dff_en_tb
# ** Note: >>Fin de la simulation
#    Time: 652 ns  Iteration: 0  Instance: /dff_en_tb
```

3 Flipflop_t



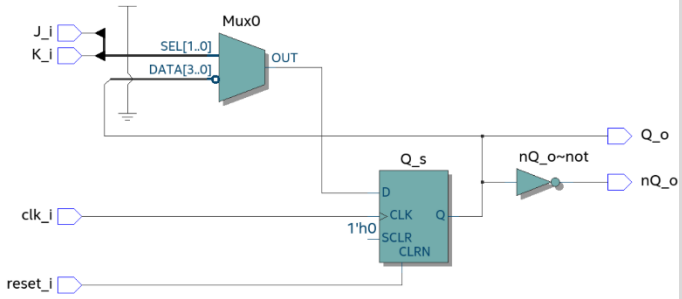

```
# vsim -voptargs=""+acc"" work.flipflop_t_tb
# Start time: 22:03:14 on Apr 17,2024
# ** Note: (vsim-3812) Design is being optimized...
# Loading std.standard
# Loading std.textio(body)
# Loading ieee.std_logic_1164(body)
# Loading work.flipflop_t_tb(test_bench)#1
# Loading work.flipflop_t(comport)#1
VSIM 6> run -all
# ** Note: >> Debut de la simulation
#    Time: 0 ns  Iteration: 0  Instance: /flipflop_t_tb
# ** Note: >>Nombre d'erreur détectée = 0
#    Time: 652 ns  Iteration: 0  Instance: /flipflop_t_tb
# ** Note: >>Fin de la simulation
#    Time: 652 ns  Iteration: 0  Instance: /flipflop_t_tb
```

4 Flipflop_rs



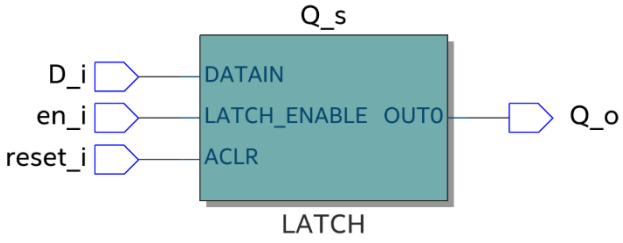

```
# vsim -voptargs=""+acc"" work.flipflop_rs_tb
# Start time: 22:04:17 on Apr 17,2024
# ** Note: (vsim-3812) Design is being optimized...
# Loading std.standard
# Loading std.textio(body)
# Loading ieee.std_logic_1164(body)
# Loading work.flipflop_rs_tb(test_bench)#1
# Loading work.flipflop_rs(comport)#1
VSIM 8> run -all
# ** Note: >> Debut de la simulation
#    Time: 0 ns  Iteration: 0  Instance: /flipflop_rs_tb
# ** Note: Test du cas SR = 11, l'état de la sortie Q est indifferent
#    Time: 852 ns  Iteration: 0  Instance: /flipflop_rs_tb
# ** Note: Verif asynchrone : état sortie Q pas vérifié
#    Time: 948 ns  Iteration: 0  Instance: /flipflop_rs_tb
# ** Note: Verif synchrone : état sortie Q pas vérifié
#    Time: 998 ns  Iteration: 0  Instance: /flipflop_rs_tb
# ** Note: >>Nombre d'erreur détectée = 0
#    Time: 1452 ns  Iteration: 0  Instance: /flipflop_rs_tb
# ** Note: >>Fin de la simulation
#    Time: 1452 ns  Iteration: 0  Instance: /flipflop_rs_tb
```

5 Flipflop_jk




```
# vsim -voptargs=""+acc"" work.flipflop_jk_tb
# Start time: 22:07:49 on Apr 17,2024
# ** Note: (vsim-3812) Design is being optimized...
# Loading std.standard
# Loading std.textio(body)
# Loading ieee.std_logic_1164(body)
# Loading work.flipflop_jk_tb(test_bench)#1
# Loading work.flipflop_jk(comport)#1
VSIM 10> run -all
# ** Note: >> Debut de la simulation
#    Time: 0 ns  Iteration: 0  Instance: /flipflop_jk_tb
# ** Note: >>Nombre d'erreur détectée = 0
#    Time: 1352 ns  Iteration: 0  Instance: /flipflop_jk_tb
# ** Note: >>Fin de la simulation
#    Time: 1352 ns  Iteration: 0  Instance: /flipflop_jk_tb
```

6 Latch_en




```
# vsim -voptargs=""+acc"" work.latch_en_tb
# Start time: 22:08:37 on Apr 17,2024
# ** Note: (vsim-3812) Design is being optimized...
# Loading std.standard
# Loading std.textio(body)
# Loading ieee.std_logic_1164(body)
# Loading work.latch_en_tb(test_bench)#1
# Loading work.latch_en(comport)#1
VSIM 12> run -all
# ** Note: >> Debut de la simulation
#    Time: 0 ns  Iteration: 0  Instance: /latch_en_tb
# ** Note: >>Nombre d'erreur détectée = 0
#    Time: 752 ns  Iteration: 0  Instance: /latch_en_tb
# ** Note: >>Fin de la simulation
#    Time: 752 ns  Iteration: 0  Instance: /latch_en_tb
```

Date : 17.04.2024

Noms des étudiants : Rafael Dousse