HAUTE ÉCOLE
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Reconfigurable & embedded
Digital Systems

Description d'additionneurs en VHDL

Départements : TIC

Unité d'enseignement CSN

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Classe : **SysLog1-A ou -B**
Salle de labo : **A07 ou A09**

Date : **13.03.2024**

Voici une proposition de chapitre. A vous de l'adapter selon le laboratoire ou de la structure choisie pour le rapport (voir présentation de votre professeur).

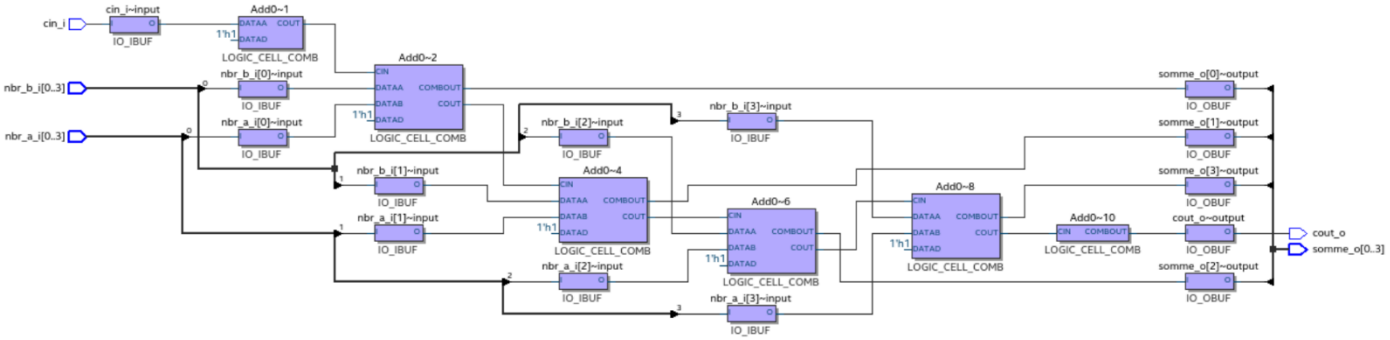
1 Log add4

```
# Start time: 14:36:37 on Mar 13,2024
# vcom -reportprogress 300 -work work ../src_tb/add4_tb.vhd
# -- Loading package STANDARD
# -- Loading package TEXTIO
# -- Loading package std_logic_1164
# -- Loading package NUMERIC_STD
# -- Compiling entity add4_tb
# -- Compiling architecture test_bench_carry of add4_tb
# -- Loading entity add4
# ** Warning: ../src_tb/add4_tb.vhd(56): (vcom-1236) Shared variables must be of a protected type.
# End time: 14:36:37 on Mar 13,2024, Elapsed time: 0:00:00
# Errors: 0, Warnings: 1
# End time: 14:36:37 on Mar 13,2024, Elapsed time: 0:03:34
# Errors: 0, Warnings: 0
# vsim -voptargs=""+acc"" work.add4_tb
# Start time: 14:36:37 on Mar 13,2024
# ** Note: (vsim-3812) Design is being optimized...
# Loading std.standard
# Loading std.textio(body)
# Loading ieee.std_logic_1164(body)
# Loading ieee.numeric_std(body)
# Loading work.add4_tb(test_bench_carry)#1
# Loading work.add4(flot_don)#1
# ** UI-Msg: (vish-4014) No objects found matching '/add4_tb/uut/ovr_o'.
# Executing ONERROR command at macro ./../wave_add4_tb.do line 15
VSIM(paused)> run -all
# ** Note: Début de la simulation
#    Time: 0 ns  Iteration: 0  Instance: /add4_tb
# ** Note: Nombre d'erreurs détectées = 0
#    Time: 51200 ns  Iteration: 0  Instance: /add4_tb
# ** Note: Fin de la simulation
#    Time: 51200 ns  Iteration: 0  Instance: /add4_tb
```

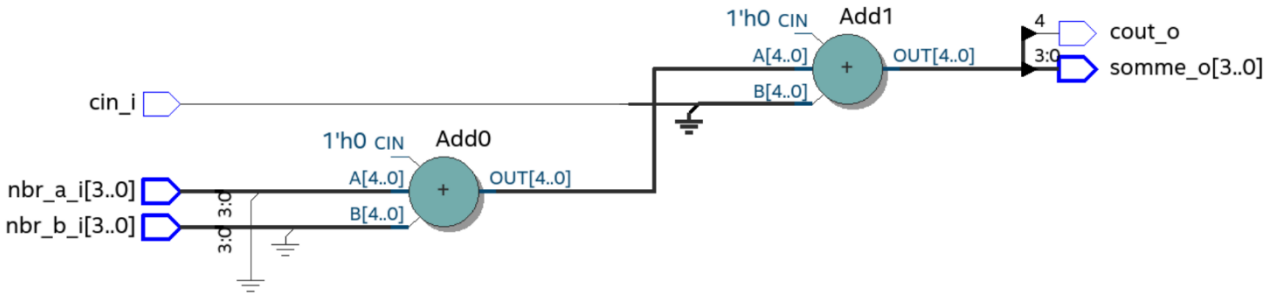
2 Log add4_full

```
# Start time: 14:33:02 on Mar 13,2024
# vcom -reportprogress 300 -work work ../src_tb/add4_full_tb.vhd
# -- Loading package STANDARD
# -- Loading package TEXTIO
# -- Loading package std_logic_1164
# -- Loading package NUMERIC_STD
# -- Compiling entity add4_tb
# -- Compiling architecture test_bench_full of add4_tb
# -- Loading entity add4_full
# ** Warning: ../src_tb/add4_full_tb.vhd(59): (vcom-1236) Shared variables must be of a protected type.
# End time: 14:33:03 on Mar 13,2024, Elapsed time: 0:00:01
# Errors: 0, Warnings: 1
# End time: 14:33:03 on Mar 13,2024, Elapsed time: 0:40:35
# Errors: 6, Warnings: 0
# vsim -voptargs=""+acc"" work.add4_tb
# Start time: 14:33:03 on Mar 13,2024
# ** Note: (vsim-8009) Loading existing optimized design _opt
# Loading std.standard
# Loading std.textio(body)
# Loading ieee.std_logic_1164(body)
# Loading ieee.numeric_std(body)
# Loading work.add4_tb(test_bench_full)#1
# Loading work.add4_full(struct)#1
# Loading work.addn(flot_don)#1
# Loading work.addn(flot_don)#2
VSIM(paused)> run -all
# ** Note: Début de la simulation
#    Time: 0 ns  Iteration: 0  Instance: /add4_tb
# ** Note: Nombre d'erreurs détectées = 0
#    Time: 51200 ns  Iteration: 0  Instance: /add4_tb
# ** Note: Fin de la simulation
#    Time: 51200 ns  Iteration: 0  Instance: /add4_tb
```

3 Vue technologique add4



4 Vue RTL add4



Date : 13.03.2024

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