Experiment 2

20D070037

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Overview of the experiment

The experiment serves the following purposes:

- To understand the concept of logic minimization using K-Map .
- To make the circuit for the given problem statement using minimum number of gates.
- To write a VHDL code to implement the Scrabble game given in the problem statement.
- To perform RTL and GATE level simulation on the design to test the design on the test-bench with a given trace-file.

The following procedure was followed by me to perform the experiment in step by step manner:

1. Read the problem statement.
2. Made the truth table for the various inputs involved.
3. Performed K-Map minimization on the output.
4. Minimized the logic even further by using complex gates, namely XOR and XNOR.
5. Wrote an HDL code to implement the final logic.
6. Compiled the code and performed RTL and GATE level simulation for the design.

The following report will start with approach that I have followed while performing the experiment followed by the the design document and the VHDL code. I will then discuss the results of the various simulations I have performed. Towards the end I will discuss the observations made while performing the experiment.

Approach to the experiment

My approach to the experiment was as follows. First I went through the problem statement and identified the concept that had to be used. In this case it was logic minimization using K-map. I first converted the problem statement into logical form. I then wrote the truth table and performed logic minimization using K-map. I did some tweaking to reduce the number of gates used even further in order to accommodate the bonus problem. At last I wrote the HDL code and performed the required simulations.

The truth table and K-Map minimization are given as follows:

Table 1: Truth Table For Logic

Letter	**Binary Value**	**Output**
A	0000	0
B	0001	1
C	0010	1
D	0011	0
E	0100	0
F	0101	0
G	0110	0
H	0111	0
I	1000	0
J	1001	0
K	1010	0
L	1011	0
M	1100	0
N	1101	1
O	1110	1
P	1111	0

Table 2: K-Map For Logic

CD	00	01	11	10
AB				
00	0	1	0	1
01	0	0	0	0
11	0	1	0	1
10	0	0	0	0

Design document and VHDL code

The aim of the experiment was to implement a Scrabble game using digital logic. We had to identify the letters for which the score was given 3 out of the first 16 letters of the alphabet using a digital circuit. Each of the 16 letters was to be represented by 4-bit binary numbers(ABCD). Each of the binary number was associated to logic 0 or logic 1 depending on if it has a value of 3 points. Accordingly, I made a truth table. Then I performed a K-Map minimization using the rules. The output logic that I got was $(A.B + \bar{A}.\bar{B}).(C.\bar{D} + \bar{C}.D)$. However after careful observation it was evident that $(A.B + \bar{A}.\bar{B})$ can be written as A XNOR B and $(C.\bar{D} + \bar{C}.D)$ can be written as C XOR D. Thus the number of logic gates involved could be reduced to a minimum of 3, including the AND gate between them. After I was convinced that the number of logic gates can not be reduced any more, I wrote the code for the logic circuit which I had got and performed the RTL and GATE level simulation.

RTL views

Following is the RTL view.

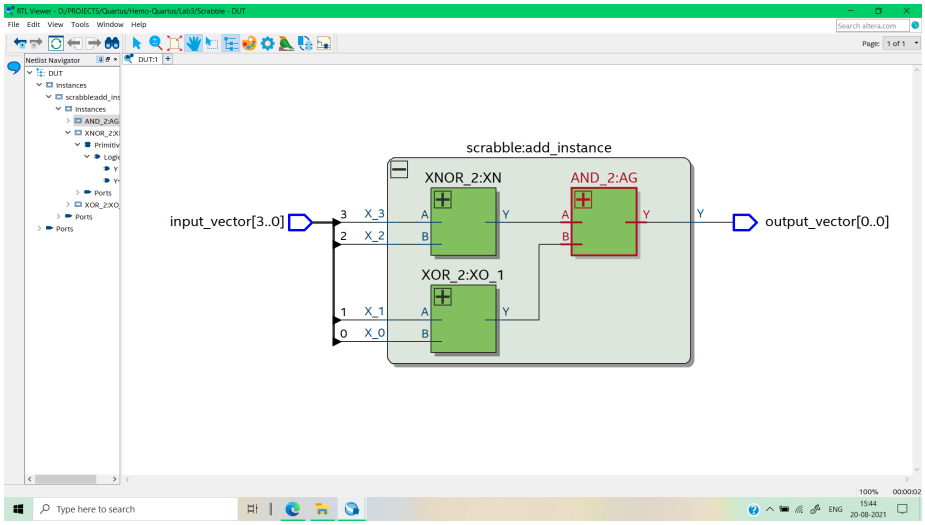

Figure 1: RTL view

DUT Input/Output Format

In the experiments the format of any vector is MSB at the leftmost side and LSB at the right most side. The input/output format for the experiment is as follows

INPUT: [A, B, C, D]
OUTPUT: [Y]
TEST-CASES:
0000 0 1
0001 1 1
0010 1 1
0011 0 1
0100 0 1
0101 0 1
0110 0 1
0111 0 1
1000 0 1
1001 0 1
1010 0 1
1011 0 1
1100 0 1
1101 1 1
1110 1 1
1111 0 1

RTL Simulation

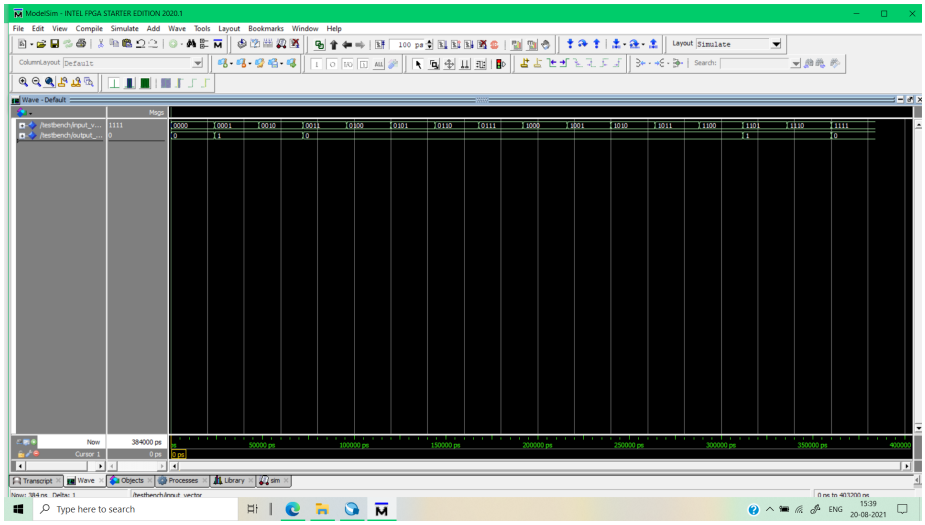

Figure 2: Waveform for RTL simulation

GATE level Simulation

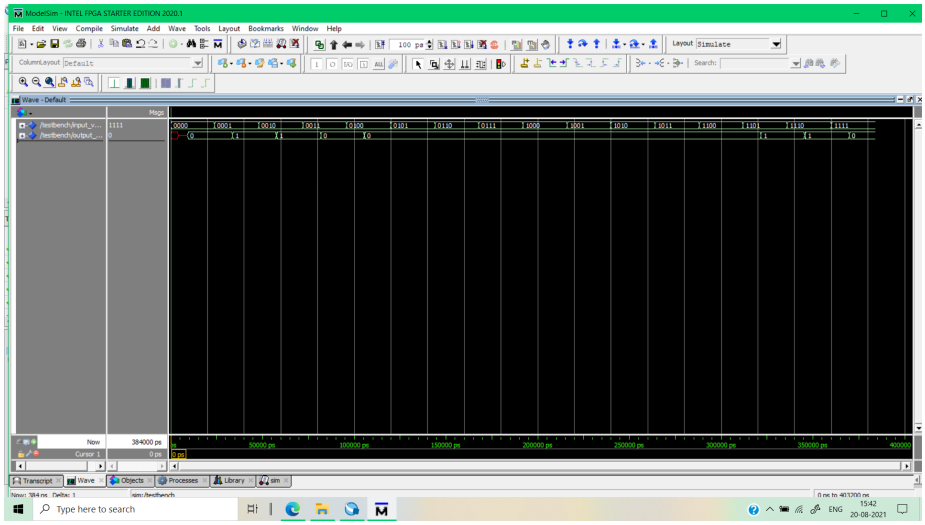

Figure 3: Waveform for GATE level simulation