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KALASALINGAM ACADEMY OF RESEARCH AND EDUCATION

(Deemed to be University)
Anand Nagar, Krishnankoil – 626 126.

END SEMESTER EXAMINATIONS, APR/MAY 2023

212CSE2102-Computer Architecture and Organization
(Common To All Sections)

Time : 180Minutes	**Degree: B.Tech**	Maximum : 100 Marks

(Answer ALL Questions of PART A and PART B)

Assessment Pattern as per Bloom's Taxonomy:

Remember	Understand	Apply	Analyze	Evaluate	Create	Total
14	84	82	0	0	0	180

	PART – A (10 × 2 = 20 Marks)	Pattern	Mapping COs	
1.	Draw the basic functional units of computer.	Remember	CO1	
2.	Convert the decimal numbers 7 and 13 to 5-bit binary numbers, and then perform subtraction. Indicate whether overflow occurs or not.	Apply	CO2	
3.	Write the add/subtract rule for performing floating point operations.	Remember	CO2	
4.	List the different types of instruction.	Remember	CO1	
5.	Explain micro programmed control.	Understand	CO3	
6.	Define pipelining.	Remember	CO3	
7.	Specify the various types of ROM.	Remember	CO4	
8.	Draw the memory hierarchy diagram in terms of speed and cost.	Remember	CO4	
9.	Mention the key objectives of USB.	Understand	CO5	
10.	What is meant by interrupt service routine?	Remember	CO5	
	PART – B (5 × 16 = 80 Marks)	**Pattern**	**Mapping COs**	
11a	Elaborate the basic addressing modes with example. Find the addressing mode and effective address of the memory operand in each of the following instruction. (a) Load 20(R1), R3 (b) Move R4, 40(R1,R2) (c) 12 (PC) (Assume the content currently in PC is 4000) Assume that Address of registers R1 and R2 are 2000 and 3000 respectively.	Apply	CO1	(16)
	[OR]			
11b	Summarize in detail how performance of computer is affected by technology and by performing a number of operations in parallel.	Understand	CO1	(16)
12a	Assuming 6-bit 2's-complement number representation, multiply the multiplicand A= 110101 by the multiplier B = 011011 using Booth algorithm and the bit-pair recoding algorithm.	Apply	CO2	(16)
	[OR]			
12b	Perform 8 divide by 3 using restoring and non restoring division.	Apply	CO2	(16)
13a	Elucidate with necessary block diagram how the processor generates the control signals for fetching and executing instructions in the correct sequence and at the right time using hardwired control.	Understand	CO3	(16)

	[OR]			

13b	Identify the type of hazard present in the given instructions if they are executed using a 5-stage pipeline processor.
	ADD R1, R2, #150
	SUB R3, R1, #25
	Elaborate in detail the various approaches to overcome the hazard with neat sketch.
		Apply	CO3	(16)

14a	Elaborate virtual memory address translation techniques in detail with neat sketch.	Understand	CO4	(16)
	[OR]			
14b	A computer system has a 16 GB main memory and 64 MB cache memory, block size is 4 KB , each consisting of 128 words and number of blocks per set is 4. 1. How many bits are there in main memory? 2. How many bits are there in each of the TAG, SET, BLOCK and WORD fields for direct-mapping and associative mapping.	Apply	CO4	(16)
15a	Enumerate how Direct Memory Access (DMA) approach controls block of data transfer between the main memory and I/O devices such as disks without frequent program-controlled intervention by the processor with diagram.	Understand	CO5	(16)
	[OR]			
15b	With diagram elaborate USB architecture and highlight how USB support the transfer of data in a simple manner.	Understand	CO5	(16)

Assessment Summary:

COs	Remember	Understand	Apply	Analyze	Evaluate	Create	Total
CO1	4	16	16	0	0	0	36
CO2	2	0	34	0	0	0	36
CO3	2	18	16	0	0	0	36
CO4	4	16	16	0	0	0	36
CO5	2	34	0	0	0	0	36
TOTAL	14	84	82	0	0	0	180

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