KALASALINGAM
ACADEMY OF RESEARCH & EDUCATION
(DEEMED TO BE UNIVERSITY)

Under sec. 3 of UGC Act 1956. Accredited by NAAC with "A" Grade

SCHOOL OF COMPUTING

DEPARTEMENT OF COMPUTER SCIENCE AND ENGINEERING

COMPUTER ARCHITECTURE AND ORGANIZATION
(212CSE2102)

COURSE INFORMATION SHEET

ACADEMIC YEAR (2023-2024)

EVEN SEMESTER

Course Coordinator : Dr.V.SATHYA NARAYANAN

Associate Professor / CSE Department

UNIVERSITY VISION	UNIVERSITY MISSION
To be a University of Excellence of International Repute in Education and Research.	M1: To provide a scholarly teaching-learning ambience which results in creating graduates equipped with skills and acumen to solve real-life problems. M2: To promote research and create knowledge for human welfare, rural and societaldevelopment. M3: To nurture entrepreneurial ambition, industrial and societal connect by creating an environment through which innovators and leaders emerge

COMPUTERE SCIENCE AND ENGINEERING DEPARTMENT	
VISION	**MISSION**
To be a department of excellence for quality education and research in various fields of Computer Science and Engineering	M1: Strive to build and maintain an academic atmosphere conducive to the highest levels of research and instruction by promoting high-quality teaching and scholarly activity. M2: To equip students with knowledge and skills in both the fundamental and applied aspects of computer science, which are necessary to solve real-world engineering challenges to meet industry and societal needs. M3: To prepare students to attain creative endeavours and entrepreneurship skills withproper ethical values and a desire to pursue life-long learning.

PROGRAMME EDUCATIONAL OBJECTIVES

PEO1: The graduates will demonstrate technical proficiency in Computer Science and Engineering during employment or higher studies.

PEO2: The graduates will imbibe problem solving skills through continuous learning and innovative mindset to provide sustainable solutions.

PEO3: The graduates will operate in a diverse environment as a professional or an entrepreneur to solve societal problems with professional ethics.

PROGRAMME SPECIFIC OUTCOMES

PSO1: Able to develop software solutions for real world problems using core computing technologies.

PSO2: Able to apply contemporary technologies such as AIML and data science for effective decision-making towards sustainable development of as smart society.

PROGRAMME OUTCOMES (R2021)

PO1 : Engineering knowledge: Apply the knowledge of mathematics, science, engineering fundamentals, and an engineering specialization to the solution of complex engineering problems.

PO2 : Problem analysis: Identify, formulate, review research literature, and analyze complex engineering problems reaching substantiated conclusions using first principles of mathematics, natural sciences, and engineering sciences.

PO3 : Design/development of solutions: Design solutions for complex engineering problems and design system components or processes that meet the specified needs with appropriate consideration for the public health and safety, and the cultural, societal, and environmental considerations.

PO4 : Conduct investigations of complex problems: Use research-based knowledge and research methods including design of experiments, analysis and interpretation of data, and synthesis of the information to provide valid conclusions.

PO5 : Modern tool usage: Create, select, and apply appropriate techniques, resources, and modern engineering and IT tools including prediction and modeling to complex engineering activities with an understanding of the limitations.

PO6 : The engineer and society: Apply reasoning informed by the contextual knowledge to assess societal, health, safety, legal and cultural issues and the consequent responsibil- ities relevant to the professional engineering practice.

PO7 : Environment and sustainability: Understand the impact of the professional engineering solutions in societal and environmental contexts, and demonstrate the knowledge of, and need for sustainable development.

PO8 : Ethics: Apply ethical principles and commit to professional ethics and responsibilities and norms of the engineering practice.

PO9 : Individual and team work: Function effectively as an individual, and as a member or leader in diverse teams, and in multidisciplinary settings.

PO10 : Communication: Communicate effectively on complex engineering activities with the engineering community and with society at large, such as, being able to comprehend and write effective reports and design documentation, make effective presentations, and give and receive clear instructions.

PO11 : Project management and finance: Demonstrate knowledge and understanding of the engineering and management principles and apply these to one's own work, as a member and leader in a team, to manage projects and in multidisciplinary environments.

PO12 : Life-long learning: Recognize the need for, and have the preparation and ability to engage in independent and life-long learning in the broadest context of technologicalchange.

ABET STUDENT OUTCOMES
Computing Accreditation Commission (CAC)

CSO1 : Analyze a complex computing problem and to apply principles of computing and other relevant disciplines to identify solutions.

CSO2 : Design, implement, and evaluates a computing-based solution to meet a given set of computing requirements in the context of the program's discipline.

CSO3 : Communicate effectively in a variety of professional contexts.

CSO4 : Recognize professional responsibilities and make informed judgments in comput-ing practice based on legal and ethical principles.

CSO5 : Function effectively as a member or leader of a team engaged in activities appropriate to the program's discipline.

CSO6 : Apply Computer Science theory and software development fundamentals to produce computing-based solutions.

Engineering Accreditation Commission (EAC)

ESO1 : Ability to identify, formulate and solve complex engineering problems by apply- ing principles of Engineering, Science, and Mathematics.

ESO2 : Ability to apply engineering design to produce solutions that meet specified needs with consideration of public health, safety, and welfare, as well as global, cultural, social, environmental, and economic factors.

ESO3 : An ability to communicate effectively with a range of audiences.

ESO4 : Ability to recognize ethical and professional responsibilities in engineering situations and make informed judgments, which must consider the impact of engineering solutions in global, economic, environmental, and societal contexts.

ESO5 : Ability to function effectively on a team whose members together provide leadership, create a collaborative and inclusive environment, establish goals, plan tasks, and meet objectives.

ESO6 : Ability to develop and conduct appropriate experimentation, analyze and interpret data, and use engineering judgment to draw conclusions.

ESO7 : Ability to acquire and apply new knowledge as needed, using appropriate learning strategies.

SYLLABUS

212CSE2102	COMPUTER ARCHITECTURE AND ORGANIZATION	L	T	P	X	Credit
		4	0	0	0	3
	Pre-requisite : Nil **Course Category** : Program Core					**Course Type:** Theory

Course Objective:

- To understand the structure, function and characteristics of computer systems.
- To describe on the fundamental design of various functional units and computer components.
- To analyze the elements of modern instructions sets and their impact on processor design, different elements of memory hierarchy and the different methods of computer I/O.

Course Outcomes:

CO1: Examine functional units of computer, bus structure and addressing mode.
CO2: Apply the knowledge of algorithms to solve arithmetic unit problems.
CO3: Demonstrate single bus, multiple bus organization and pipelining concepts
CO4: Analyse the different forms of memory and its organization.
CO5: Evaluate the various I/O interfaces.

Mapping of Course Outcomes with PO, PSO:

	POs												PSOs	
	1	2	3	4	5	6	7	8	9	10	11	12	1	2
CO1	S													
CO2	S			S									S	
CO3	S	S		S						L	M		S	M
CO4	S	S		S		M	M		L				S	M
CO5	S	S	S	S	M	M		L			M	M	S	M

UNIT I: BASIC STRUCTURE OF COMPUTERS

Generation of Computers - Progress achieved in the past years, Changes in Technology - Software Functional Units - Von Neumann model - Software Performance - Instruction Types - Examples - Instruction and Instruction Sequencing - Instruction Format - Memory Locations and Addresses - Machine addressability - Memory Operations - Load Store - Addressing Modes.

UNIT II: ARITHMETIC UNIT

Number Systems – Basic Number Representation – Integer Representation – Signed Addition and Subtraction – 2' s complement Addition - Design of Fast - Multiplication of Positive Numbers – Signed Multiplication – Bit pair Recoding of Multiplier – Restoring and Non-Restoring Division – Basic Floating Point Representation.

UNIT III: BASIC PROCESSING UNIT

Processor Organization– Register Organization - Instruction Cycle – Execution of complete instruction – Instruction Hardwired Control – Micro Programmed Control –Basic Concepts of Pipelining – Different types of Pipeline Hazards – Instruction Level Parallelism and Superscalar Operation.

UNIT IV: MEMORY SYSTEM

Computer System Memory overview – Cache memory principles – Elements of cache Design – Design and performance considerations of cache memory - Semiconductor Main Memory – ROM – External Memory–Virtual Memory Concept.

UNIT V: I/O ORGANIZATION

Need of I/O Module –Basic I/O Operations - Accessing I/O devices – Interrupts - Direct Memory Access – Buses, Bus arbitration, Types of buses - Standard I/O Interfaces (PCI, SCSI, USB).

Text Book:

1. Carl Hamacher, Zvonko Vranesic and Safwat Zaky, Computer Organization, McGraw-Hill, 6th Edition 2016.

Reference Books:

1. William Stallings, Computer Organization and Architecture – Designing for Performance, PHI pvt Ltd, 10th Edition, 2016.
2. David A.Patterson and John L.Hennessy, Computer Organization and Design: The hardware software interface, Morgan Kaufmann, 4th Edition, , 2010.
3. John P.Hayes, Computer Architecture and Organization, McGraw Hill, 3rd Edition, 2017.

WEIGHTAGE:

Component		Marks
Internal Exam 1. Sessional Examinations 2. Assignments/Seminars/Flipped Class/Quiz	: 35% : 15%	50
External Exam End Semester Exam	: 50%	50
	Total	100

COURSE INFORMATION SHEET

Course Name / Code	Computer Architecture and Organization – 212CSE2102
Degree / Branch	B.Tech., CSE
Course Credit	3 (4-0-0-0)
Course Category	Theory
Course Instructors	Dr.N.SURESH KUMAR
	Dr.A.PARIVAZHAGAN
	Dr.N.SUBBULAKSHMI
	Dr.V.SATHYA NARAYANAN
	Dr.P.MUTHUVEL
	Mr.R.MARI SELVAN
	Mr.C. SIVAMURUGAN
	Mrs.LOYOLA JASMINE
	Mr. KALAISELVAN
	Mrs.J.BENITA
	Mrs.R.DURGA MEENA
	AKBAR BADHUSHA MOHIDEEN
Course Coordinator	Dr.V.SATHYA NARAYANAN
Module Coordinator	Dr.A.PARIVAZHAGAN
Programme Coordinator	Dr. N. C. BRINDHA

1. Pre-requisite: Nil

2. Course Description:

This course aims to provide a strong foundation for students to understand computer system architecture and to apply these insights and principles to future computer designs. The course is structured around the three primary building blocks of general-purpose computing systems: processors, memories, and input/output.

This course includes the organization and architecture of computer systems hardware; instruction set architectures; addressing modes; register transfer notation; processor design and computer arithmetic; memory systems; hardware implementations of virtual memory, and input/output control and devices.

3. Career Opportunities:

Computers have become a ubiquitous part of modern life, and new applications are introduced every day. The use of computer technologies is also commonplace in all types of organizations, in academia, research, industry, government, private and business organizations. As computers become even more pervasive, the potential for computer-related careers will continue to grow and the career paths in computer-related fields will become more diverse.

4. Course Objectives:

To make acquainted the students about the functional units of computer and how each unit works along with the architectural and performance issues.

5. Course Outcomes:

At the end of the course, the students will be able to

CO1: Examine functional units of computer, bus structure and addressing mode
CO2: Apply the various algorithms to solve arithmetic unit problems.
CO3: Demonstrate single bus, multiple bus organization and pipelining.
CO4: Analyze RAM, ROM, Cache memory and virtual memory.
CO5: Explore the various I/O interfaces

6. Mapping of Course Outcomes with PO, PSO:

	POs												PSOs	
	1	2	3	4	5	6	7	8	9	10	11	12	1	2
CO1	S													
CO2	S			S									S	
CO3	S	S		S						L	M		S	M
CO4	S	S		S		M	M		L				S	M
CO5	S	S	S	S	M	M		L			M	M	S	M

MAPPING OF COURSE OUTCOMES WITH ABET STUDENT OUTCOMES:

	CSO						ESO						
	CSO1	CSO2	CSO3	CSO4	CSO5	CSO6	ESO1	ESO2	ESO3	ESO4	ESO 5	ESO 6	ESO 7
CO1	S						S						
CO2													
CO3	S	S					S	M					
CO4													
CO5	S	S					S	L					

7. Books:

Sl.		Book Name	Author(s)	Publisher	Year, Edition
Text(s)	1.	Computer Organization	Carl Hamacher, Zvonko Vranesic and Safwat Zaky	McGraw Hill, India	(6th Edition) 2016
Reference(s)	1.	Computer Organization and Architecture – Designing for Performance	William Stallings	Pearson Education	10th Edition, 2016.
	2.	Computer Architecture and Organization	John P.Hayes	McGraw Hill	3rd Edition, 2010

Sl.		Book Name	Author(s)	Publisher	Year, Edition
	3.	Computer Organization and design: The hardware software interface	David A.Patterson and John L.Hennessy	Morgan Kaufmann,	4th Edition, 2017

8. Lesson Plan:

ABBREVIATION	TEACHING METHOD
L	Class Room Lecture (Chalk Based Lecture)
EL	Smart Class Room Lecture/ Web-Facilitated Course Delivery/ Flipped Class Lecture/ Multimedia Lecture/ Animation
SS	Self-Study Topic – Student Seminar
T	Tutorial/ Case-Study/ Scenario
P	Practical/ Laboratory Demonstration/ Model Demonstration/ Simulation
GD	Group Discussion/ Debate/ Role Play
GL	Guest Lecture/ Workshop/Interview with Experts/ Webinars
IV	Industrial Visit/ Field Trip
PJ	Project Design/ Project Demonstration/Literature Survey

Week	Lecture (4 hours)	Pedagogy
Week 1	Generation of Computers, Progress achieved in the past years, Changes in Technology, Software Functional Units	Explicit Teaching
	Von Neumann model	Explicit Teaching
	Basic Operational Concepts, Connections between the processor and the memory	Explicit Teaching
	Software Performance, Processor Clock, Basic Performance equation and measurement	Explicit Teaching
Week 2	Instruction Types (zero, one, two and three Address)	Explicit Teaching/ Demonstration
	Examples of 1, 2, 3 and 0-Address Instruction	Explicit Teaching
	Instruction and Instruction Sequencing, Data transfers,ALU, Sequencing and I/O	Explicit Teaching
	Branching and condition codes	Explicit Teaching
Week 3	Memory Locations and Addresses, Machine Addressability, Big endian and littleendian	Explicit Teaching
	Memory Operations Load, Store	Explicit Teaching

	Addressing Modes	Explicit Teaching
	Example	Problem Solving
Week 4	Number Systems, Basic Number Representation	Explicit Teaching/ Demonstration
	Numerical Example	Explicit Teaching, Problem Solving
	Integer Representation	Explicit Teaching
	Signed Addition and Subtraction	Explicit Teaching, Problem Solving
Week 5	Design of Fast Adders	Explicit Teaching/ Demonstration
	Carry Save Addition of Summands	Explicit Teaching, Problem Solving
	Multiplication of Positive Numbers	Explicit Teaching, Problem Solving
	Booth Multiplication of Signed Numbers	Explicit Teaching, Problem Solving
Week 6	Bit pair Recoding of Multiplier	Explicit Teaching/ Demonstration
	Restoring Division	Explicit Teaching, Problem Solving
	Non-Restoring Division	Explicit Teaching, Problem Solving
	Basic Floating Point Representation	Explicit Teaching, Problem Solving
Week 7	Processor Organization, Fundamental Concepts	Explicit Teaching/ Demonstration
	Execution of a Complete Instruction, Hardware Components of processor	Explicit Teaching
	Single Bus Organization, Register Transfers, Performing an ALU operation	Explicit Teaching
	Multi-bus Organization, Control signals	Explicit Teaching
Week 8	Instruction Hardwired Control, control step counter	Explicit Teaching/ Demonstration
	Micro-programmed Control, control memory,organization	Explicit Teaching
	Basic Concepts of Pipelining, advantages, stages	Explicit Teaching
	Instruction Level Parallelism, stages	Explicit Teaching

Week 9	Types of pipeline hazards- Data, Control and structural	Explicit Teaching/ Demonstration
	Implementation of pipelining	Explicit Teaching
	Branch prediction, static and dynamic	Explicit Teaching
	Superscalar Operation - out of order B27execution, imprecise exception	Explicit Teaching
Week 10	Memory - Basic concepts	Explicit Teaching/ Demonstration
	Semiconductor RAMs - types, internal organizations, synchronous and Asynchronous RAMs, Dynamic memories	Explicit Teaching
	Internal organization	Explicit Teaching
	Mapping - Direct, Associative and set Associative	Explicit Teaching
Week 11	Cache memory - design considerations	Explicit Teaching/ Demonstration
	Performance consideration - hit rate, miss rate, misspenalty	Explicit Teaching
	memory interleaving and its types	Explicit Teaching
	Improving Hit Rate - Pre fetching, lock-up freecache	Explicit Teaching
Week 12	Reducing Miss Penalty - write through, write back,principle of locality	Explicit Teaching/ Demonstration
	Virtual Memory - pading, address translation, TLB,Page fault	Explicit Teaching
	Secondary Storage - fixed, removable	Explicit Teaching
	Types of secondary storage	Explicit Teaching
Week 13	Need of I/O Module, Basic I/O Operations	Explicit Teaching/ Demonstration
	Accessing I/O devices - memory mapped, pro-grammed I/O	Explicit Teaching
	Interrupts- vectored inter- rupts, interrupt nesting	Explicit Teaching
	Handling Interrupt -ISR, Daisy chaining, polling,nested	Explicit Teaching
Week 14	Direct Memory Access - organization, implementation, DMA controller	Explicit Teaching/ Demonstration
	Buses - Introduction	Explicit Teaching

	Synchronous and Asynchronous Bus	Explicit Teaching
	Bus arbitration - centralized , distributed	Explicit Teaching
Week 15	Basics on Standard I/O - protocols and standards	Explicit Teaching/ Demonstration
	serial / Parallel port	Explicit Teaching
	SCSI representation	Explicit Teaching
	Universal Serial Bus	Explicit Teaching

9. COs, Teaching Methodologies and Assessment Tools:

CO	Content Delivery Methodology	Bloom's Level	Assessment Tools	
			Direct	Indirect
CO1	Class Lectures, Tutorials Flipped Classes / Multimedia Lectures	Understand	SE–I – 60%, END SEM – 20% Assignment – 10%	Course End Survey (Course Exit Survey)
CO2	Class Lectures, Tutorials Flipped Classes/ Multimedia Lectures	Apply	SE–I – 40%, END SEM – 20% Assignment – 10%	
CO3	Class Lectures, Tutorials Flipped Classes/ Multimedia Lectures, Guest Lecture	Analyse	SE–II – 60%, END SEM – 20% Assignment – 10%,	
CO4	Class Lectures, Tutorials Flipped Classes/ Multimedia Lecture,	Apply	SE–II – 40%, END SEM – 20% Assignment / Quiz – 10%	
CO5	Class Lectures, Tutorials Flipped Classes/ Multimedia Lectures	Understand	Unit Test – 20%, END SEM – 20% Assignment / Quiz – 10%	

10. Assessment Topics:

CO	Measurement Tool	Topic(s)	Beyond Syllabus/ Self-Study	Measurement Time
CO1	Assignment - 1	Instruction Types, Addressing Modes		4 Days after Submission
CO2	Assignment - 2	Arithmetic Unit		
CO3	Assignment- 3	Basic Concepts of Pipelining	Y	
CO4	Quiz	Memory Organization	Y	
CO4	Assignment - 4	Semiconductor RAMs, ROMs		
CO5	Assignment - 5	PCI,SCSI,USB bus	Y	

11. Exam Portions

CO	Measurement Tool	Date (Tentative)	Measurement Time
CO1	Unit Test – 1	After the completion of Unit 1	2 Days after Test
CO1, CO2	Sessional Examination – I	As per Academic Calendar	3 Days after Exam
CO3	Unit Test – 2	After the completion of Unit 3	2 Days after Test
CO3, CO4	Sessional Examination – II	As per Academic Calendar	3 Days after Exam

CO	Measurement Tool	Date (Tentative)	Measurement Time
CO5	Unit test – 3	After the completion of Unit 5	2 Days after Test
CO1 to CO5	End Semester Examination	As per Academic Calendar	As per Academic Calendar

Evaluation Method

S. No	Evaluation method	Weightage (%)	Units covered
Internal Continuous Assessment (50 marks)			
1	Sessional Examination I	17.5%	I and II
2	Sessional Examination II	17.5%	III and IV
3	Assignment / Quiz (5 Nos)	15%	All units
External Assessment (50 marks)			
4	End Semester	50	All units

12. Tutorial Topics

Tutorial	Topic No(s).	Mapped CO(s)
Tutorial – 1	BASIC STRUCTURE OF COMPUTERS	CO1
Tutorial – 2	ARITHMETIC UNIT	CO2
Tutorial – 3	BASIC PROCESSING UNIT	CO3
Tutorial – 4	MEMORY SYSTEM	CO4
Tutorial – 5	I/O ORGANIZATION	CO5

13. Web Resources:

Unit No	Topic	Web link
1	**Basic Structure of computers**	1. http://www.stat.auckland.ac.nz/~dscott/782/Computers.pdf 2. https://bmsit.ac.in/public/assets/pdf/ece/studymaterial/18EC35%20-%20Module%201%20-%20Dr.%20MCH.pdf
2.	**Arithmetic Unit**	1. https://examradar.com/arithmetic-logic-unit-alu/ 2. https://www.tutorialspoint.com/arithmetic-logic-unit-alu
3.	**Basic Processing Unit**	1. www.site.uottawa.ca/~mbolic/ceg4131/Ch_14_superscalar.ppt 2. https://profile.iiita.ac.in/bibhas.ghoshal/COA_2021/lecture_slides/Basic_Processing_Unit.pdf
4	**Memory System**	1. https://www.studytonight.com/computer-architecture/memory-organization 2. https://www.geeksforgeeks.org/computer-memory/ 3. http://www.ee.ic.ac.uk/pcheung/teaching/DE1_EE/Lectures/Lecture%2012%20-%20Memory%20and%20Computer%20Architecture%20(x1).pdf

5.	**I/O organization**	1. https://www.geeksforgeeks.org/io-interface-interrupt-dma-mode/ 2. https://edurev.in/studytube/Input-Output-organization-Computer-Organization-an/9eba9196-cebf-4390-8149-5c5a9035b086_t 3. https://www.cukashmir.ac.in/cukashmir/User_Files/imagefile/DIT/Study Material/Architecture/MTIT_ComputerArchitecture_IO_4.pdf

14. Web links for similar courses offered at other Universities:

Name of the course	University/ Org	Web link
Computer Architecture and Organization	NPTEL, IIT Kharagpur	https://nptel.ac.in/courses/106105163
Computer Architecture	Princeton University	https://www.coursera.org/course/comparch
Computer System Architecture	MIT University	https://ocw.mit.edu/courses/6-823-computer-system-architecture-fall-2005/
Computer System Architecture	Stanford University	https://online.stanford.edu/courses/ee282-computer-systems-architecture

15. Topic(s) Beyond Syllabus:

1. Types of Storage Devices – Buses - RAID
2. Case studies: Intel, AMD, Qualcomm Processors
3. Symmetric and Distributed Shared Memory Architectures

16. Flipped Class Topics:

Topic(s).
Addressing modes, Multiplication of positive numbers, Pipelining, Memory Management, Direct Memory Access, IO devices examples

17. Participative Learning (if any):

- Discussion
- Workshop
- Webinar
- Case Studies

5/12/2023

Course Coordinator
(Dr.V.Sathya Narayanan)

05/12/23

Module Coordinator
(Dr.A.Parivazhagan)

Programme Coordinator
(Dr.N.C.Brintha)

06/12/23

HOD/CSE
(Dr.N.Suresh Kumar)