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Release Notes
CoreRMII v3.1

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1 Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

1.1 Revision 3.0

Added PolarFire® SoC support.

1.2 Revision 2.0

Updated changes related to CoreRMII v3.0.

1.3 Revision 1.0

Revision 1.0 was the first publication of this document. Created for CoreRMII v2.0.

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2 CoreRMII v3.1 Release Notes

2.1 Overview

These release notes accompany the production release of CoreRMII v3.1. This document provides details about the features, enhancements, system requirements, supported families, implementations, and known issues and workarounds.

2.2 Features

CoreRMII has the following features:

- Provides reduced pin-count interface for Ethernet PHYs.
- Provides media independent interface (MII) interface towards the microcontroller subsystem (MSS)-side and reduced media independent interface (RMII) on the PHY side.
- Supports 25 MHz clock operation on the MII-side, 50 MHz on the RMII-side for 10/100 Mbps mode operation.
- Provides MDIO interface as defined in clause 22 of IEEE 802.3 standard to control the transfer type, the link speed and the loopback mode.

2.3 Delivery Types

No License is required to use CoreRMII. A complete hardware description language (HDL) source code is provided for the core and testbenches.

2.4 Supported Families

- PolarFire® SoC
- PolarFire®
- IGLOO®2
- SmartFusion®2

2.5 Supported Tool Flows

CoreRMII v3.1 requires Libero® System-on-Chip (SoC) v11.0 or later.

2.6 Installation Instructions

The CoreRMII CPZ file must be installed into Libero software. This is done automatically through the Catalog update function in Libero, or the CPZ file can be manually added using the **Add Core** catalog feature. Once the CPZ file is installed in Libero, the core can be configured, generated, and instantiated within SmartDesign for inclusion in the Libero project. For more information, see the *Knowledge Based article*.

To know how to create SmartDesign project using the IP cores, refer to *Libero SoC documents page* and use the latest SmartDesign user guide.

2.7 Documentation

This release contains a copy of the *CoreRMII Handbook*. The handbook, describes the core functionality and gives step-by-step instructions on how to simulate, synthesize, and place-and-route this core, and also implementation suggestions. Refer to *Libero SoC documents page* for instructions on obtaining IP documentation.

For updates and additional information, visit the Intellectual Property pages on the Microsemi SoC Products Group website: visit:

http://www.microsemi.com/products/fpga-soc/design-resources/ip-cores.

2.8 Supported Test Environments

- Verilog user testbench
- VHDL user testbench

2.9 Resolved History

Table 1 lists the release history for CoreRMII.

Table 1 • **Release History**

Version	Date	Changes
3.1	September 2020	Added PolarFire SoC support.
3.0	April 2017	Resolved SARs listed in Table 2.
2.0	July 2013	Initial release.

2.10 Resolved Issues in v3.1 Release

There were no software action requests (SARs) resolved. PolarFire SoC support is added.

2.10.1 Resolved Issues in the v3.0 Release

Table 2 • **Resolved Issues in the v3.0 Release**

SAR Number	Changes
63024	CoreRMII display name should arguably be “CoreRMII” and not “CORERMII”.
81496	CoreRMII requirement to support MDIO/MDC interface.

2.10.2 Resolved Issues in the v2.0 Release

There were no unresolved SARs for CoreRMII v2.0. This was the first production release.

2.11 Discontinued Features and Devices

Parameters TRANSFER_SPEED, TRANSFER_TYPE and LOOPBACK, which were used for core configuration were removed in CoreRMII v3.0.

2.12 Known Limitations and Workarounds

There are no known limitations and workarounds.