HB0871
Handbook
CoreUHD_SDIRX v2.1

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1 Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

1.1 Revision 2.0

Updated changes related to CoreUHD_SDIRX v2.1.

1.2 Revision 1.0

Revision 1.0 was the first publication of this document. Created for CoreUHD_SDIRX v2.0.

2 Introduction

2.1 Overview

CoreUHD_SDIRX DirectCore IP is a Serial Digital Interface (SDI) De-framer. Core supports 1.5 Gigabits per second SDI (HD-SDI), 3 Gigabits per second SDI (3G-SDI), 6 Gigabits per second SDI (6G-SDI), and 12 Gigabits per second SDI (12G-SDI) SDI standards defined by the Society of Motion Picture and Television Engineers (SMPTE).

2.2 Features

Core has the following features:

- Compliant with SMPTE ST 292-1 (HD-SDI) standard.
- Compliant with SMPTE ST 424 (3G-SDI) standard.
- Compliant with SMPTE ST 2081-1 (6G-SDI) standard.
- Compliant with SMPTE ST 2082-1 (12G-SDI) standard.
- Supports data rates 1.485 Gb/s and 1.485/1.001 Gb/s for HD-SDI standard.
- Supports data rates 2.97 Gb/s and 2.97/1.001 Gb/s for 3G-SDI standard.
- Supports data rates 5.94 Gb/s and 5.94/1.001 Gb/s for 6G-SDI standard.
- Supports data rates 11.88 Gb/s and 11.88/1.001 Gb/s for 12G-SDI standard.
- Performs NRZI decoding and descrambling.
- Performs word alignment on SDI data stream.
- Performs removal of sync-bit from timing reference words in 12G-SDI and 6G-SDI standards.
- Performs CRC check on SDI data stream.
- Performs extraction of Video Payload Identification (VPID) data bytes.
- Performs extraction of timing reference signals (TRS).
- Performs extraction of Line Number (LN) data.

2.3 Core Version

This handbook is for CoreUHD_SDIRX version 2.1.

2.4 Supported Families

- PolarFire® SoC
- PolarFire®

2.5 Device Utilization and Performance

Device Utilization and Performance data is provided in the following table for the supported device families. The data described in this table is only indicative. The overall device utilization and performance of the core is system dependent.

Table 1 • **Device Utilization and Performance**

Family (Device)	Configuration Parameters		Utilization (Logic Elements)				Performance (MHz)
	RX_SDI_STD	RX_SDI_DW	Sequential (DFF)	Combinatorial (4LUT)	Total	%	RX_CLK Frequency
PolarFire (MPF300T)	3	20	1106	1017	2123	0.35	242
	4	40	2311	2982	5293	0.88	247
	5	80	5361	9033	14394	2.40	229
PolarFire SoC (MPFS250T)	3	20	1202	1106	2308	0.45	216
	4	40	2387	3070	5457	1.07	254
	5	80	5437	9101	14538	2.86	212

Note: The data in this table is achieved using typical synthesis and layout settings. Frequency (MHz) was set to 100 and the speed grade was -1.

3 Interface

3.1 Configuration Parameters

The following table describes the configurable parameter/generic of the core. All the parameters/generics are integer types.

Table 2 • **Parameter/Generic Descriptions**

Parameter Name	Valid Range	Default	Description
RX_SDI_STD	3, 4, 5	5	**SDI STANDARD** Configure the core for required SDI standard. • 3 – HD-SDI and 3G-SDI • 4 – 6G-SDI • 5 – 12G-SDI
RX_SDI_DW	20, 40, 80	80	**SDI DATA WIDTH** Configure the data width of the parallel SDI data stream on the transceiver interface of the core. • 20 – Select 20-bits in HD-SDI and 3G-SDI standard (when RX_SDI_STD parameter is set to 3) • 40 – Select 40-bits in 6G-SDI standard (when RX_SDI_STD parameter is set to 4) • 80 – Select 80-bits in 12G-SDI standard (when RX_SDI_STD parameter is set to 5)

3.2 Ports

All the input and output ports of the core are listed in the following table.

Table 3 • **Input and Output Signals**

Port	Width	Direction	Description
Clock and Reset			
RX_CLK	1	Input	Receive clock input. All input signals are required to be clocked on rising edge to this clock. All the output signals are clocked on rising edge of this clock. Recommended to connect to LANE***x***_RX_CLK of Transceiver. The required clock frequency is 148.5 (/1.001) MHz when data streams are transmitted at 12G-SDI, 6G-SDI or 3G-SDI data rate. The required clock frequency is 74.25 (/1.001) MHz when data streams are transmitted at HD-SDI data rate.
RX_RESETN	1	Input	Active low asynchronous reset input. The reset input is required to be synchronous to clock RX_CLK.
Transceiver Interface			
RX_SDI_DATA	RX_SDI_DW	Input	Receive data from Transceiver. SDI data stream input. Recommended to connect to LANE***x***_RX_DATA of Transceiver.

Table 3 • **Input and Output Signals *(continued)***

Port	Width	Direction	Description
RX_READY	1	Input	Receive Ready from the Transceiver. The core resets whenever RX_READY is not asserted. Recommended to connect to LANE***x***_RX_READY of Transceiver.
Data Stream Outputs			
RX_DATA_DS1	10	Output	Data Stream 1 output. DS1 in 12G-SDI, 6G-SDI, 3G-SDI, and HD-SDI standards.
RX_DATA_DS2	10	Output	Data Stream 2 output. DS2 in 12G-SDI, 6G-SDI, 3G-SDI, and HD-SDI standards.
RX_DATA_DS3	10	Output	Data Stream 3 output. DS3 in 12G-SDI and 6G-SDI standards.
RX_DATA_DS4	10	Output	Data Stream 4 output. DS4 in 12G-SDI and 6G-SDI standards.
RX_DATA_DS5	10	Output	Data Stream 5 output. DS5 in 12G-SDI standard.
RX_DATA_DS6	10	Output	Data Stream 6 output. DS6 in 12G-SDI standard.
RX_DATA_DS7	10	Output	Data Stream 7 output. DS7 in 12G-SDI standard.
RX_DATA_DS8	10	Output	Data Stream 8 output. DS8 in 12G-SDI standard.
Line Number Outputs			
RX_LN_C_DS1	11	Output	Line number extracted from C channel of DS1 data stream.
RX_LN_C _DS2	11	Output	Line number extracted from C channel of DS2 data stream.
RX_LN_C _DS3	11	Output	Line number extracted from C channel of DS3 data stream.
RX_LN_C _DS4	11	Output	Line number extracted from C channel of DS4 data stream.
RX_LN_C _DS5	11	Output	Line number extracted from C channel of DS5 data stream.
RX_LN_C _DS6	11	Output	Line number extracted from C channel of DS6 data stream.
RX_LN_C _DS7	11	Output	Line number extracted from C channel of DS7 data stream.
RX_LN_C _DS8	11	Output	Line number extracted from C channel of DS8 data stream.
RX_LN_Y_DS1	11	Output	Line number extracted from Y channel of DS1 data stream.
RX_LN_Y _DS2	11	Output	Line number extracted from Y channel of DS2 data stream.
RX_LN_Y _DS3	11	Output	Line number extracted from Y channel of DS3 data stream.
RX_LN_Y _DS4	11	Output	Line number extracted from Y channel of DS4 data stream.
RX_LN_Y _DS5	11	Output	Line number extracted from Y channel of DS5 data stream.
RX_LN_Y _DS6	11	Output	Line number extracted from Y channel of DS6 data stream.
RX_LN_Y _DS7	11	Output	Line number extracted from Y channel of DS7 data stream.
RX_LN_Y _DS8	11	Output	Line number extracted from Y channel of DS8 data stream.
VPID Data Outputs			
RX_VPID_C_DS1	32	Output	VPID data bytes extracted from C channel of DS1 data stream.
RX_VPID_C _DS2	32	Output	VPID data bytes extracted from C channel of DS2 data stream.
RX_VPID_C _DS3	32	Output	VPID data bytes extracted from C channel of DS3 data stream.

Table 3 • **Input and Output Signals *(continued)***

Port	Width	Direction	Description
RX_VPID_C _DS4	32	Output	VPID data bytes extracted from C channel of DS4 data stream.
RX_VPID_C _DS5	32	Output	VPID data bytes extracted from C channel of DS5 data stream.
RX_VPID_C _DS6	32	Output	VPID data bytes extracted from C channel of DS6 data stream.
RX_VPID_C _DS7	32	Output	VPID data bytes extracted from C channel of DS7 data stream.
RX_VPID_C _DS8	32	Output	VPID data bytes extracted from C channel of DS8 data stream.
RX_VPID_Y_DS1	32	Output	VPID data bytes extracted from Y channel of DS1 data stream.
RX_VPID_Y _DS2	32	Output	VPID data bytes extracted from Y channel of DS2 data stream.
RX_VPID_Y _DS3	32	Output	VPID data bytes extracted from Y channel of DS3 data stream.
RX_VPID_Y _DS4	32	Output	VPID data bytes extracted from Y channel of DS4 data stream.
RX_VPID_Y _DS5	32	Output	VPID data bytes extracted from Y channel of DS5 data stream.
RX_VPID_Y _DS6	32	Output	VPID data bytes extracted from Y channel of DS6 data stream.
RX_VPID_Y _DS7	32	Output	VPID data bytes extracted from Y channel of DS7 data stream.
RX_VPID_Y _DS8	32	Output	VPID data bytes extracted from Y channel of DS8 data stream.
VPID Line Number Outputs			
RX_VPID_LN_C_DS1	11	Output	Line number of VPID data extracted from C channel of DS1 data stream.
RX_VPID_LN_C _DS2	11	Output	Line number of VPID data extracted from C channel of DS2 data stream.
RX_VPID_LN_C _DS3	11	Output	Line number of VPID data extracted from C channel of DS3 data stream.
RX_VPID_LN_C _DS4	11	Output	Line number of VPID data extracted from C channel of DS4 data stream.
RX_VPID_LN_C _DS5	11	Output	Line number of VPID data extracted from C channel of DS5 data stream.
RX_VPID_LN_C _DS6	11	Output	Line number of VPID data extracted from C channel of DS6 data stream.
RX_VPID_LN_C _DS7	11	Output	Line number of VPID data extracted from C channel of DS7 data stream.
RX_VPID_LN_C _DS8	11	Output	Line number of VPID data extracted from C channel of DS8 data stream.
RX_VPID_LN_Y_DS1	11	Output	Line number of VPID data extracted from Y channel of DS1 data stream.

Table 3 • **Input and Output Signals *(continued)***

Port	Width	Direction	Description
RX_VPID_LN_Y _DS2	11	Output	Line number of VPID data extracted from Y channel of DS2 data stream.
RX_VPID_LN_Y _DS3	11	Output	Line number of VPID data extracted from Y channel of DS3 data stream.
RX_VPID_LN_Y _DS4	11	Output	Line number of VPID data extracted from Y channel of DS4 data stream.
RX_VPID_LN_Y _DS5	11	Output	Line number of VPID data extracted from Y channel of DS5 data stream.
RX_VPID_LN_Y _DS6	11	Output	Line number of VPID data extracted from Y channel of DS6 data stream.
RX_VPID_LN_Y _DS7	11	Output	Line number of VPID data extracted from Y channel of DS7 data stream.
RX_VPID_LN_Y _DS8	11	Output	Line number of VPID data extracted from Y channel of DS8 data stream.
VPID Check Sum Error Outputs			
RX_CS_C_ERROR	RX_SDI_DW/10	Output	This output Indicates checksum error is detected in the VPID packet of C channel data of the data stream output for the current frame.
RX_CS_Y_ERROR	RX_SDI_DW/10	Output	This output Indicates that CRC check error is detected on the Y channel data of the data stream output for the current frame.
CRC Error Outputs			
RX_CRC_C_ERROR	RX_SDI_DW/10	Output	This output Indicates that CRC check error is detected on the C channel data of the data stream output for the current line number.
RX_CRC_Y_ERROR	RX_SDI_DW/10	Output	This output Indicates that CRC check error is detected on the Y channel data of the data stream output for the current line number.
Status Outputs			
RX_ALIGNED	1	Output	This output signal indicates that the word alignment block has detected the 3FF 000 000 pattern on the SDI data stream and the data stream is aligned to the required word boundary.

Table 3 • **Input and Output Signals *(continued)***

Port	Width	Direction	Description
RX_DS_MUX	1	Output	This output signal indicates the data stream multiplex type of the individual data streams of the SDI data stream. If this output is low, when the core is operating at 12G-SDI or 6G-SDI data rates, then it indicates Type1 multiplex is detected on the input data streams (one instance of TRS Words, Line Number Words, CRC Words, etc in each data stream). If this output is high, when the core is operating at 12G-SDI or 6G-SDI data rates, it indicates Type2 multiplex is detected on the input data streams (two instances of TRS Words, Line Number Words, CRC Words, etc in each data stream). If this output is low, when the core is operating at 3G-SDI data rate, then it indicates 3G-SDI Level A mapping is detected on the input data stream. If this output is high, when the core is operating at 3G-SDI data rate, then it indicates 3G-SDI Level B mapping is detected on the input data stream. This output shall be ignored when the core is operating at the HD-SDI data rate. Once multiplex type/mapping type is detected, the output remains unchanged until there is change in multiplex type/mapping type on the input SDI data stream.
RX_TRS	1	Output	This output signal indicates that data on the data stream outputs is first TRS word of the respective data stream.
RX_SAV	1	Output	This output signal indicates that XYZ words indicating SAV are output on data stream outputs. In case of Type 1 data multiplex, the signal asserts high for one clock cycle, when XYZ word indicating SAV is output. In case of Type 2 data multiplex, the signal asserts high for two clock cycles, when XYZ (C channel) and XYZ (Y channel) words indicating SAV are output.
RX_EAV	1	Output	This output signal indicates that XYZ words indicating EAV are output on data stream outputs. In case of Type 1 data multiplex, the signal asserts high for one clock cycle, when XYZ word indicating EAV is output. In case of Type 2 data multiplex, the signal asserts high for two clock cycles, when XYZ (C channel) and XYZ (Y channel) words indicating EAV are output.
RX_VANC	1	Output	This output signal indicates that the vertical ancillary (VANC) data is output on data streams outputs.
RX_HANC	1	Output	This output signal indicates that the horizontal ancillary (HANC) data is output on data streams outputs.
RX_AV	1	Output	This output signal indicates that the active video (AV) data is output on data streams outputs.
RX_DS_C	1	Output	This output signal indicates the C channel data of the respective data stream is output on the data stream outputs. This output is valid when RX_DS_MUX is high (Type2 data stream multiplexing). This output shall be ignored when RX_DS_MUX is low (Type1 data stream multiplexing).

Table 3 • **Input and Output Signals *(continued)***

Port	Width	Direction	Description
RX_DS_Y	1	Output	This output signal indicates the Y channel data of the respective data stream is output on the data stream outputs. This output is valid when RX_DS_MUX is high (Type2 data stream multiplexing). This output shall be ignored when RX_DS_MUX is low (Type1 data stream multiplexing).
RX_BAD_TRS	1	Output	This output indicates that the TRS information on the SDI data stream is not valid TRS as mentioned in SMPTE standard. This output goes high whenever bad TRS is detected. This does not affect the data stream de-framing performed by the core.

Note: x can be 0, 1, 2, and 3.

Note: All the ports with suffix _DS1 and _DS2 are available in HD-SDI standard, 3G-SDI standard, 6G-SDI standard, and 12G-SDI standard.

Note: All the ports with suffix _DS3 and _DS4 are available in both 6G-SDI standard and 12G-SDI standard.

Note: All the ports with suffix _DS5, _DS6, _DS7, and _DS8 are available only in 12G-SDI standard.

Note: When RX_DS_MUX output is high (Type2 data stream multiplexing), the Line Number Outputs, VPID Data Outputs, VPID Line Number Outputs, VPID Check Sum Error Outputs and CRC Error Outputs with suffix _C carries the respective information related to C channel of the respective data stream and with suffix _Y carries the respective information related to Y channel of the respective data stream.

Note: When RX_DS_MUX output is low (Type1 data stream multiplexing), the Line Number Outputs, VPID Data Outputs, VPID Line Number Outputs, VPID Check Sum Error Outputs and CRC Error Outputs with suffix _C carries the respective information related to the respective data stream. All the signals with suffix _Y shall be ignored.

Note: The VPID Data Outputs are 32-bit each. Bits [7:0] is the Byte1 extracted from the VPID data packet, Bits [15:8] is the Byte2 extracted from the VPID data packet, Bits [23:16] is the Byte3 extracted from the VPID data packet, Bits [31:24] is the Byte4 extracted from the VPID data packet.

Note: The VPID Check Sum Error Outputs and CRC Error Outputs has one bit for each data stream. Bit [0] corresponds to DS1, Bit [1] corresponds to DS2, Bit [2] corresponds to DS3, Bit [3] corresponds to DS4, Bit [4] corresponds to DS5, Bit [5] corresponds to DS6, Bit [6] corresponds to DS7, and Bit [7] corresponds to DS8.

4 Functional Descriptions

CoreUHD_SDIRX is an SDI Deframer. The core accepts the SDI data stream and extracts the video data by deframing the SDI data stream. The deframing is performed as per the SMPTE SDI protocol specification for the SDI standard configured.

As per the SMPTE 6G-SDI and 12G-SDI specifications the individual data streams of the SDI data stream can be of either Type1 multiplex type or Type2 multiplex type based on the image mapping standards.

- **Type1 multiplex:** Each data stream has a single instance of TRS words, Line Numbers, CRC Words and so on.
- **Type2 multiplex:** Each data stream has two instances of TRS words, Line Numbers, CRC Words and so on.

The core is capable of handling both Type1 and Type2 multiplex SDI data stream. The core detects the type of the multiplexing and reports it on the RX_DS_MUX output.

In case of the Type2 multiplex data streams, the core performs LN extraction, VPID extraction and CRC checking on both channels of the multiplexed data stream.

As per the SMPTE 3G-SDI image mapping specification two types of mappings are specified.

- **Level A mapping:** Each data stream has a single instance of TRS words, Line Numbers, CRC Words, and so on (This is similar to Type 1 multiplexing present in 12G-SDI and 6G-SDI).
- **Level B mapping:** Each data stream has two instances of TRS words, Line Numbers, CRC Words, and so on (This is similar to Type 2 multiplexing present in 12G-SDI and 6G-SDI).

The core is capable of accepting both Level A and Level B mapped SDI data stream. The core detects the type of mapping and reports it on the RX_DS_MUX output.

In case of the Level B multiplex data streams, the core performs LN insertion, VPID insertion, and CRC generation and insertion on both channels of the multiplexed data stream.

Figure 1 • **CoreUHD_SDIRX Block Diagram in 3G-SDI and HD-SDI Standard**

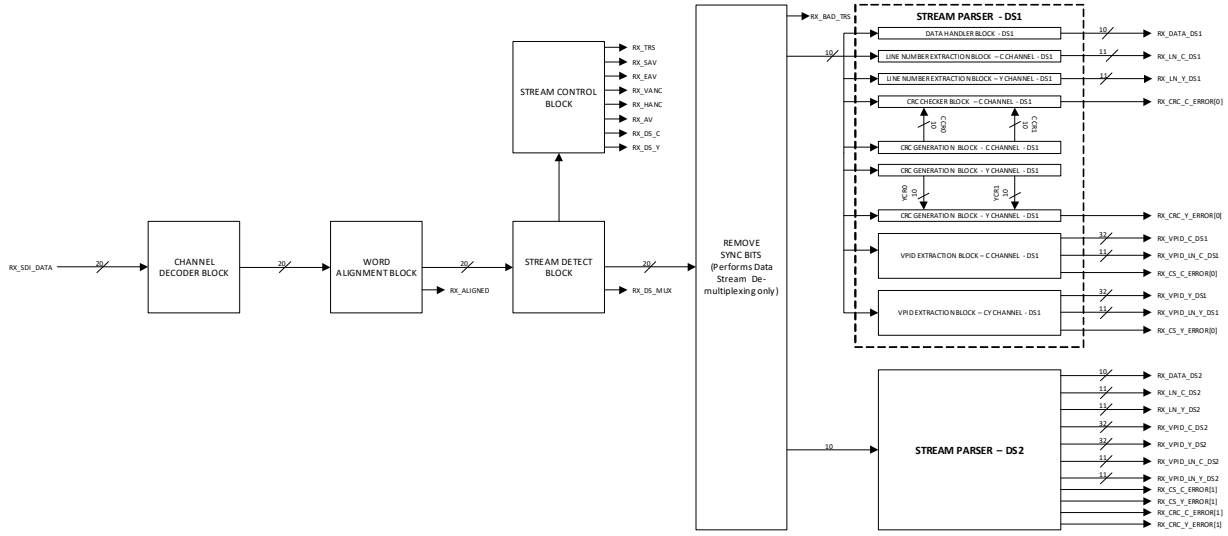


Figure 2 • **CoreUHD_SDIRX Block Diagram in 6G-SDI** Standard

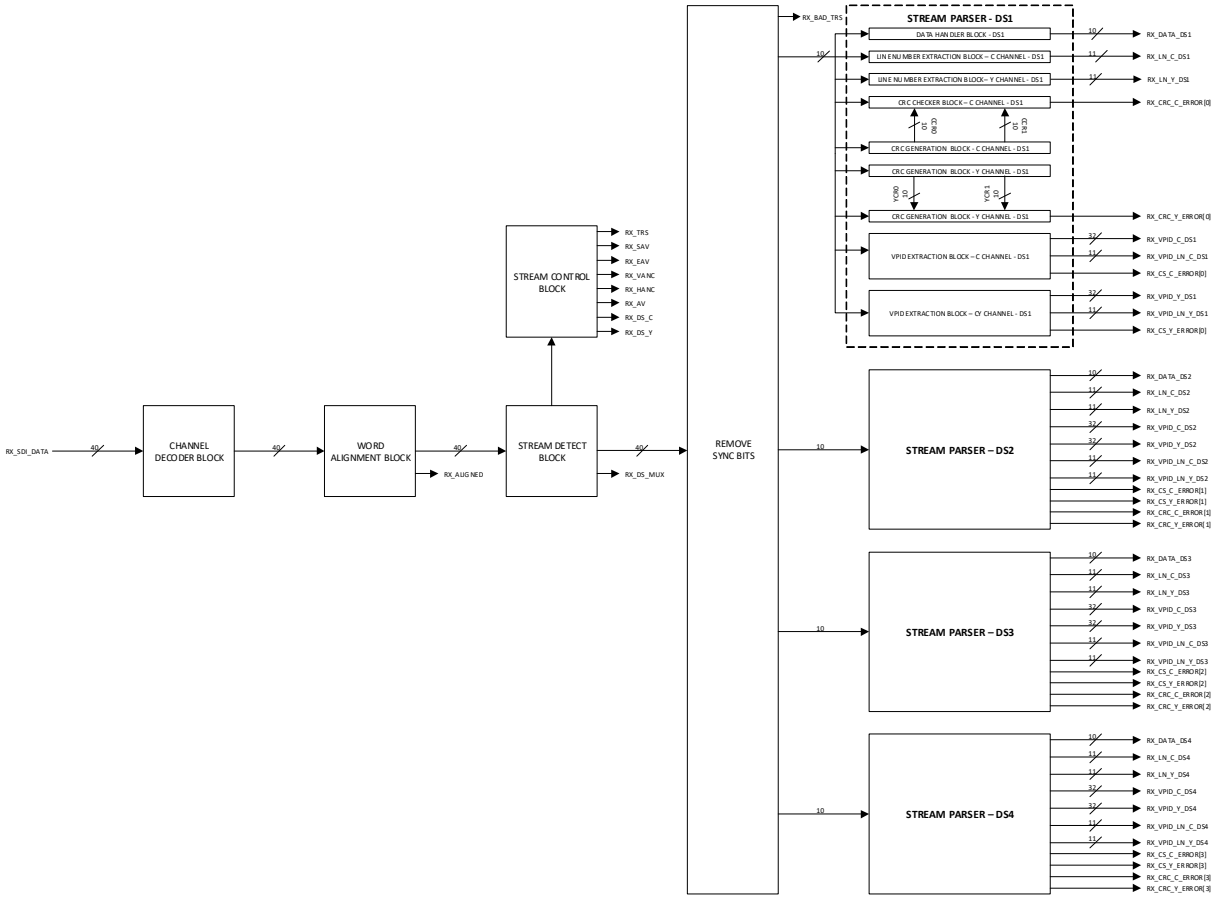
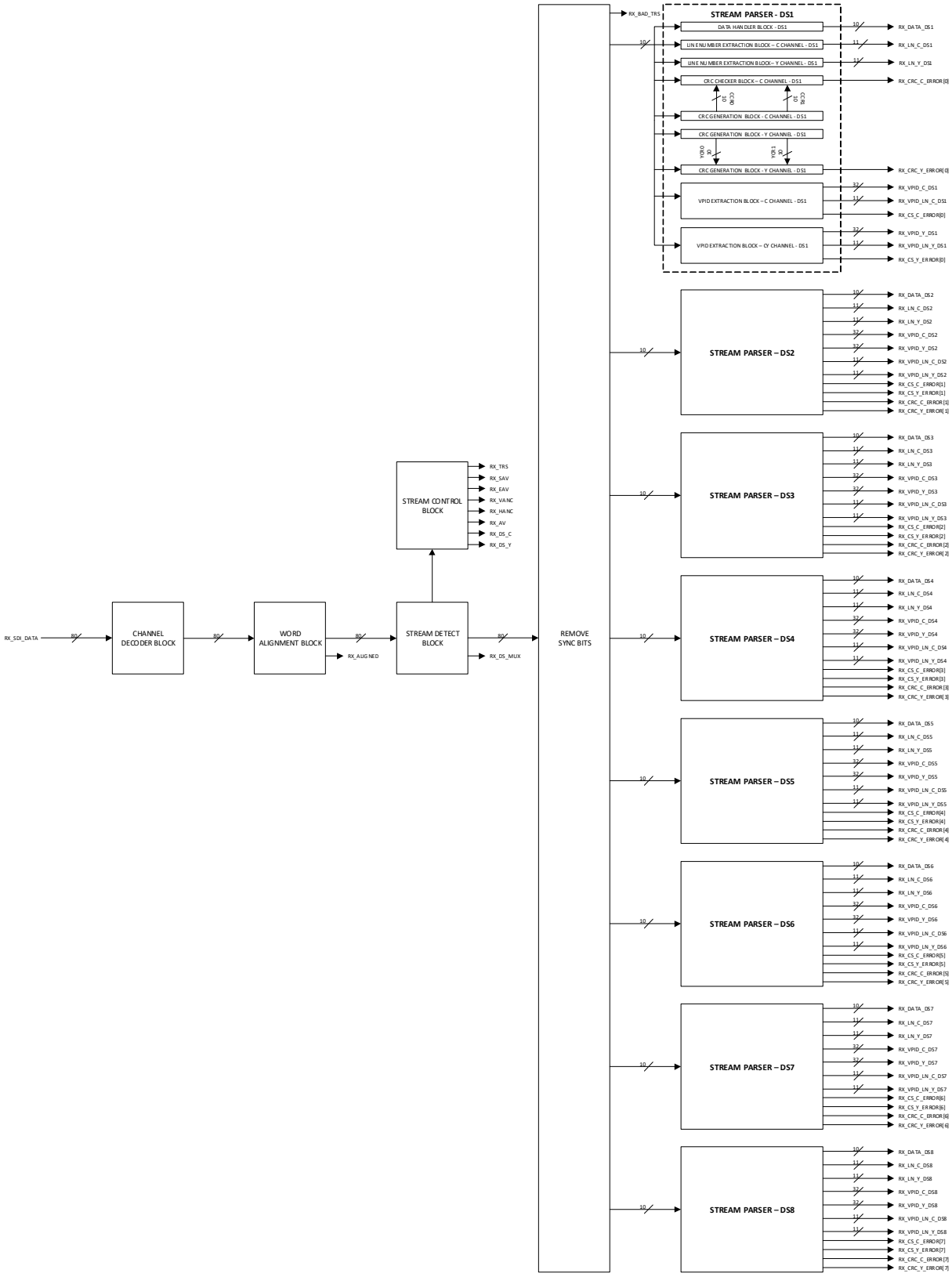


Figure 3 • **CoreUHD_SDIRX Block Diagram in 12G-SDI** Standard



The functional blocks of the core are described in the following sections:

4.1 Channel Decoder Block

Channel Decoder Block performs the scrambled NRZI decoding on the SDI data stream input. The channel decoding is performed as per the polynomials specified in the SMPTE specification.

G1(X) = $\mathbf{X^9 + X^4 + 1}$ and $\mathbf{G_2(X) = X + 1}$

4.2 Word Alignment Block

Word Alignment Block aligns the input SDI data stream to the required word boundary. The word boundary alignment is performed by searching the **3FF 000 000** timing reference pattern in the SDI data stream.

The block aligns the data stream to 80-bit boundary in 12G-SDI standard, 40-bit boundary in 6G-SDI standard and 20-bit boundary in HD-SDI and 3G-SDI standard. The block generates data aligned signal once the data stream is aligned to the required boundary.

4.3 Stream Detect Block

Stream Detect Block detects the timing reference words in the input SDI data stream and generates the control signals required for the stream control block and sync bits removal block.

The block generates signal to indicate the first word of the timing reference words. Also, the block detects the multiplex type of the data stream input based on the timing reference words.

4.4 Sync Bits Removal Block

Sync Bits Removal Block performs the removal of sync bit from the timing reference words. Two LSBs of 10-bit 3FF word replaced by 01b and that of 10-bit 000 word replaced by 10b during sync bits insertion before transmitting, is removed in this block. Two LSBs are replaced with 11b and 00b for the 3FD and 002 timing reference words respectively. The core performs sync bits removal only in 12G-SDI standard and 6G-SDI standard.

4.5 Stream Control Block

Stream Control Block generates the control signals for the sync bits removal block, the line number extraction block, the VPID extraction block, the CRC generation block, and the CRC checker block.

The block generates the status signals. These status signals indicate, which of the component of the data stream is present on the data stream outputs.

4.6 Data Handler Block

Data Handler Block delays the data stream by the required clock cycles to align with the status outputs.

4.7 Line Number Extraction Block

Line Number Extraction Block extracts the line number packets LN0 and LN1 from the input data stream. The block decodes the line number data from the LN0 and LN1 line number packets as define in the SMPTE specification.

4.8 VPID Extraction Block

The VPID Extraction Block extracts the video payload bytes from the VPID packets available on the input data stream for the current frame. The block also outputs the line number value in which the VPID packets are detected for the current frame.

The block also generates the VPID checksum error signal when the VPID checksum value calculated by the block do not match the VPID checksum value extracted from the VPID packets of the data stream.

4.9 CRC Generation Block

CRC Generation Block computes the CRC value for each line of the input data stream. The CRC computation is as per the CRC polynomial specified in the SMPTE specification.

CRC(X) = $\mathbf{X^{18} + X^5 + X^4 + 1}$

The 18-bit CRC generated is encoded to and from CR0 and CR1 CRC packets as defined in SMPTE specification.

4.10 CRC Checker Block

CRC Checker Block compares the CRC packets extracted from the data stream with the CRC value calculated by the core on the data stream.

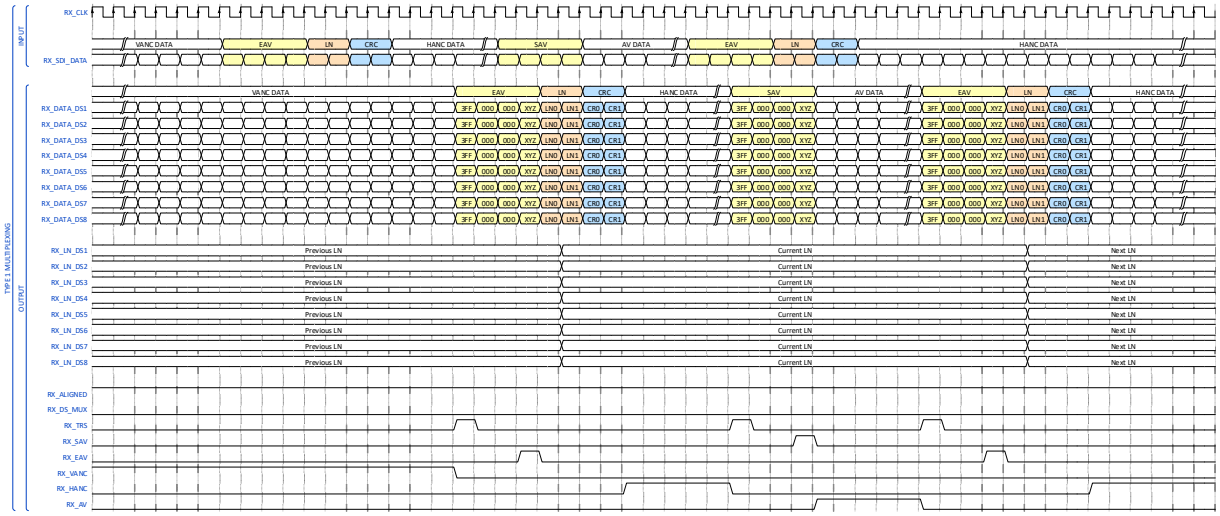
The block generates the CRC error signal for one cycle when the CRC value calculated by the core do not match the CRC value extracted from the data stream.

5 Timing Diagrams

5.1 Type1 Multiplex Data Stream

The following figure shows the timing diagram for 12G-SDI standard and 6G-SDI standard Type1 10-bit multiplex data stream. Refer the following timing diagram for HD-SDI standard and 3G-SDI standard - Level A mapping.

Figure 4 • **Timing Diagram for Type1 10-bit Multiplex Data Stream**



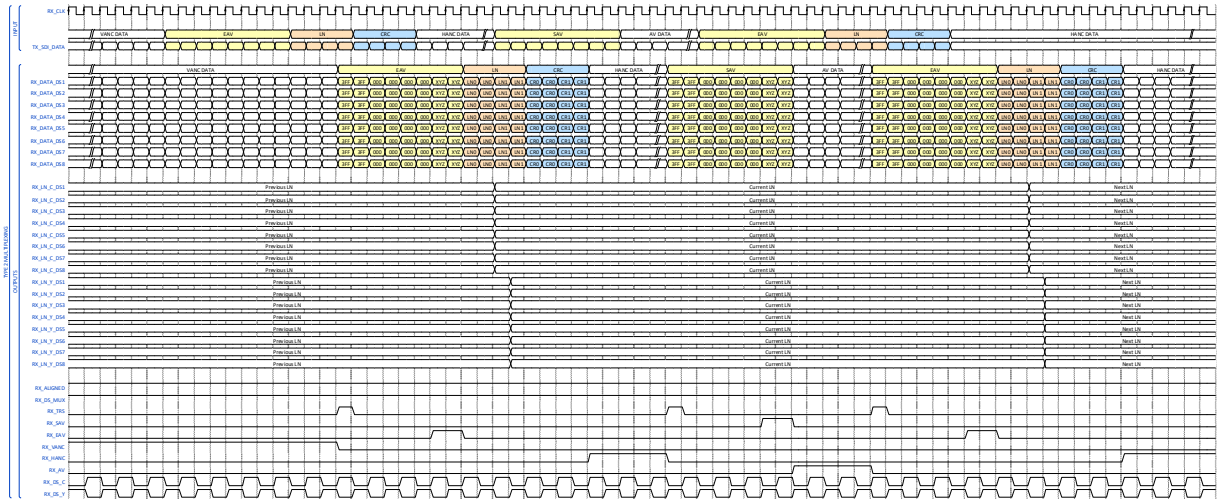
Note: In 6G-SDI standard, ignore the ports with suffix _DS5, _DS6, _DS7, and _DS8.

Note: In HD-SDI standard and 3G-SDI standard - Level A mapping, ignore the ports with suffix _DS3, _DS4, _DS5, _DS6, _DS7, and _DS8.

5.2 Type2 Multiplex Data Stream

The following figure shows the timing diagram for 12G-SDI standard and 6G-SDI standard Type2 10-bit multiplex data stream. Refer the following timing diagram for 3G-SDI standard - Level B mapping.

Figure 5 • **Timing Diagram for Type2 10-bit Multiplex Data Stream**



Note: In 6G-SDI standard, ignore the ports with suffix _DS5, _DS6, _DS7, and _DS8.

Note: In HD-SDI standard and 3G-SDI standard - Level A mapping, ignore the ports with suffix _DS3, _DS4, _DS5, _DS6, _DS7, and _DS8.

6 Tool Flow

6.1 License

Core is available in two versions:

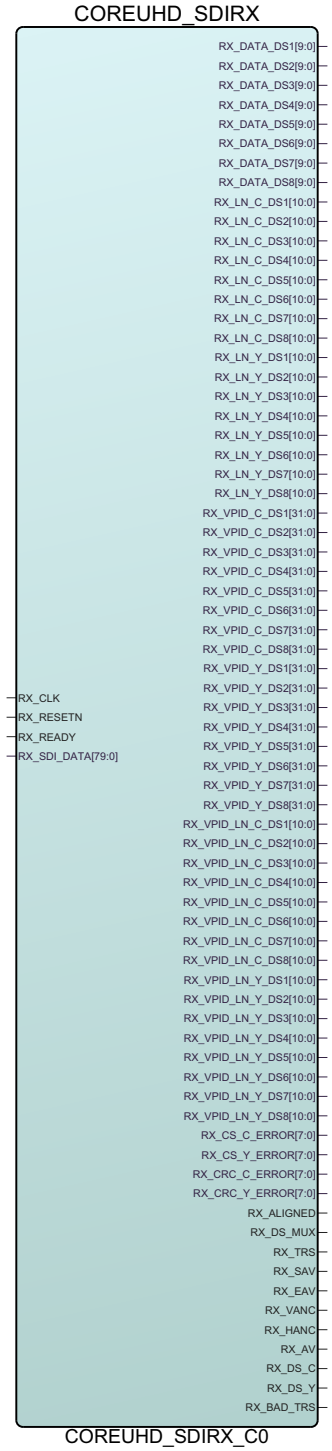
- **Evaluation:** Evaluation version is available for free and supports 4 hours of the functionality on silicon while operating at 12G-SDI, 6G-SDI and 3G-SDI data rates, and 8 hours of the functionality on silicon while operating at HD-SDI data rate.
- **Obfuscated:** Obfuscated version is license locked and is available only with Libero Platinum license.

6.2 Using core in Libero SmartDesign

Core is pre-installed in the SmartDesign IP deployment design environment or Core is downloaded from the online repository.

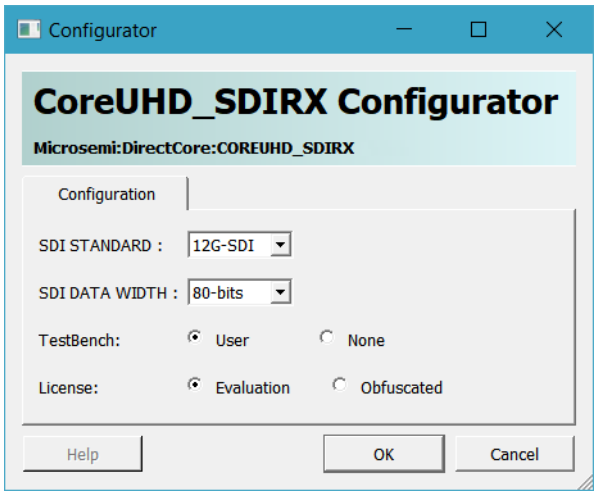
An example of the core instantiated in Libero SmartDesign is shown in the following figure:

Figure 6 • **Core Instance Full I/O View in SmartDesign**



The core can be configured using the configuration GUI in the SmartDesign, as shown in the following figure:

Figure 7 • **Configuring the Core in SmartDesign**



For more information on using the SmartDesign to instantiate and generate cores, visit *https://www.microsemi.com/product-directory/design-resources/1750-libero-soc#documents* page for the latest version of SmartDesign user guide.

6.3 Simulation Flows

The User Testbench is provided along with the core.

To run the user testbench simulations, do the following steps:

1. Select **User** option for the Testbench flow in the **Core Configuration** window. When SmartDesign generates the design files, it also generates the user testbench files.
2. Set the design root to the core instantiation in the Libero design hierarchy pane.
3. Click **Simulation** in the Libero **Design Flow** window. This invokes ModelSim and automatically runs the user testbench simulation.

6.4 Synthesis in Libero

To run synthesis on the core, do the following steps:

1. Set the design root to the IP component instance.
2. Run the **Synthesis** tool from the Libero **Design Flow** pane.

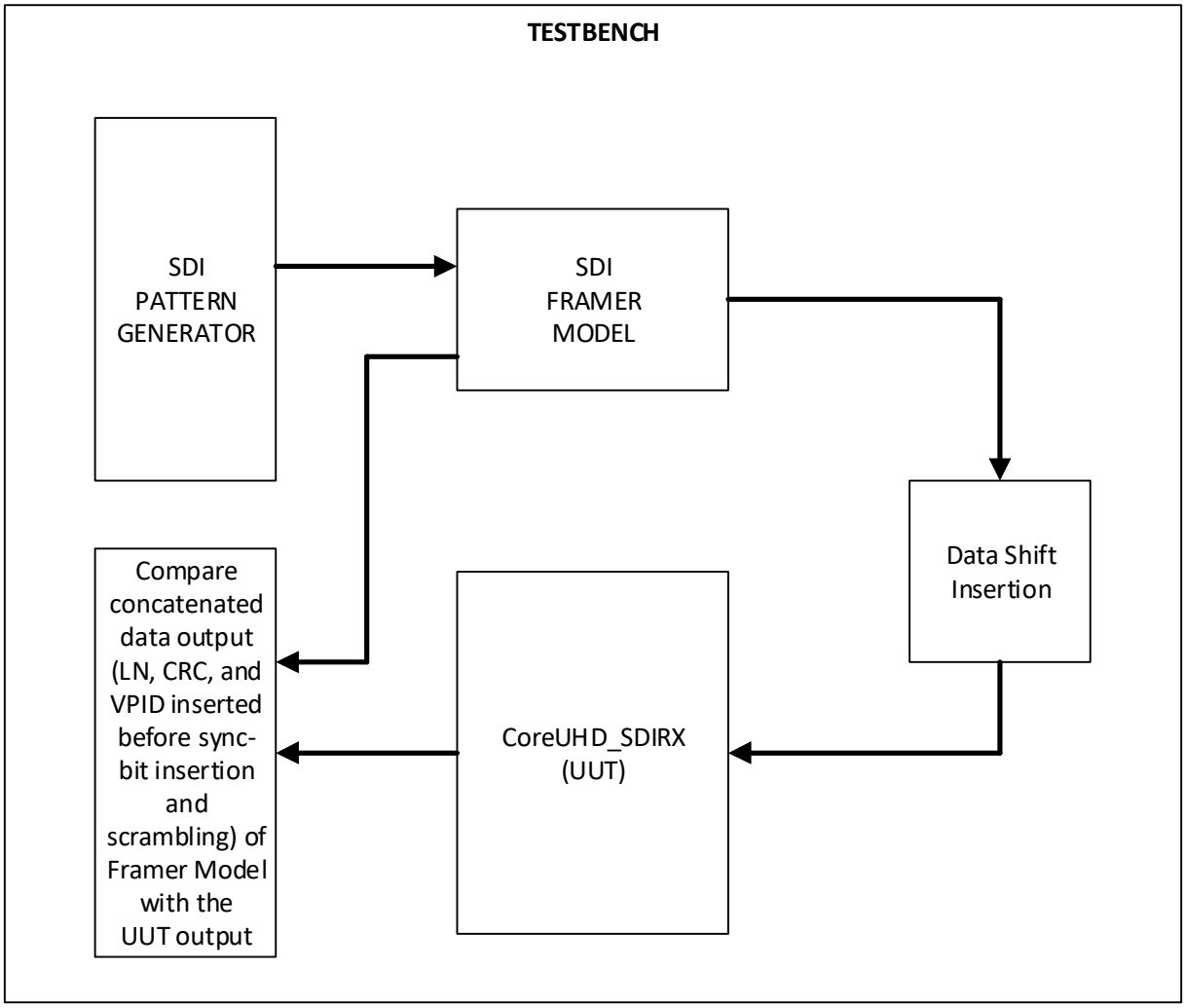
6.5 Place-and-Route in Libero

When the design is synthesized, run the **Place-And-Route** tool from the Libero **Design Flow** pane.

7 Testbench

User Testbench is provided with the core that verifies a few of the features.

Figure 8 • **User Testbench**



The testbench core instance are: Unit Under Test (UUT), an SDI Pattern Generator, an SDI Framer Model, and a Data Comparison Block.

The testbench configures the SDI Pattern Generator, the SDI Framer Model, and the UUT with the parameters for which the core is being configured from configurator GUI.

The pattern generator generates the data streams, line number data, VPID data, VPID line number data, and control signals required to connect to the SDI Framer Model, based on the standard configured.

The SDI Framer Model performs the framing of the raw video into the SDI data stream. The SDI data output of the SDI Framer Model is connected in loop back to the SDI data input of the UUT. The UUT recovers the video data from the SDI data stream.

The data comparator block compares the data stream output from the UUT with the data stream input of the Framer Model. This block also monitors the CRC error flag. This block reports, if there is any CRC error or data comparison error.

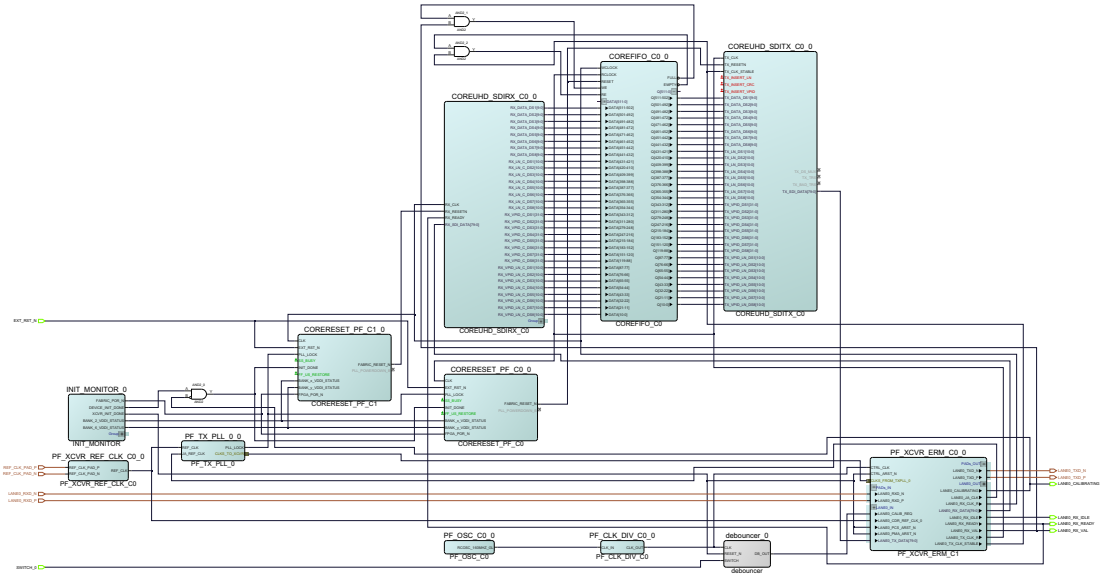
8 System Integration

In this example design:

- CoreUHD_SDIRX (COREUHD_SDIRX_C0_0) is configured in required SDI standard (HD-SDI and 3G-SDI/6G-SDI/12G-SDI). This core de-frames the SDI data stream into raw video data.
- CoreUHD_SDITX (COREUHD_SDITX_C0_0) is configured in required SDI standard (HD-SDI and 3G-SDI/6G-SDI/12G-SDI), same as COREUHD_SDIRX_C0_0. COREUHD_SDITX_C0_0 frames the raw data into SDI data stream.
- In HD-SDI standard, PF_XCVR_ERM (PF_XCVR_ERM_C0_0) is configured for data rate of 1485 Mbps in PMA mode with Receiver Calibration set to “CDR”, 20-bit interface data width, and 148.5 MHz reference clock.
- In 3G-SDI standard, PF_XCVR_ERM (PF_XCVR_ERM_C0_0) is configured for data rate of 2970 Mbps in PMA mode with Receiver Calibration set to “CDR”, 20-bit interface data width, and 148.5 MHz reference clock.
- In 6G-SDI standard, PF_XCVR_ERM (PF_XCVR_ERM_C0_0) is configured for data rate of 5940 Mbps in PMA mode with Receiver Calibration set to “CDR”, 40-bit interface data width, and 148.5 MHz reference clock.
- In 12G-SDI standard, PF_XCVR_ERM_C0_0 is configured for data rate of 11880 Mbps in PMA standard with Receiver Calibration set to “On Demand and First Lock”, 80-bit interface data width, and 148.5 MHz reference clock.
- XCVR_INIT_DONE signal of PF_INIT_MONITOR (INIT_MONITOR_0) is connected to PCS_RST_N, PMA_RST_N, and CTRL_ARST_N reset inputs of PF_XCVR_ERM_C0_0.
- LANE0_CDR_REF_CLK_0 input of PF_XCVR_ERM_C0_0 is driven by 148.5 MHz clock from REF_CLK of PF_XCVR_REF_CLK (PF_XCVR_REF_CLK_C0_0).
- CTRL_CLK (ERM clock) of PF_XCVR_ERM_C0_0 is driven by 40MHz clock generated from 160 MHz clock driven by OSC (PF_OSC_C0_0) using clock divider (PF_CLK_DIV_C0_0). This is applicable only for 6G-SDI and 12G-SDI data rates.
- The JA_CLK port of the PF_XCVR_ERM_C0_0 is enabled for jitter cleaning purpose.The value of JA PLL reference clock frequency in TX_PLL configurator should be the same as RX JA clock frequency in the Transceiver configurator.
- PF_TXPLL (PF_TX_PLL_0_0) is configured in jitter cleaning mode. REF_CLK of PF_XCVR_REF_CLK_C0_0 drives the REF_CLK input of PF_TX_PLL_0_0. JA_CLK port of the PF_XCVR_ERM_C0_0 drives the JA_REF_CLK input port of PF_TX_PLL_0_0.
- FABRIC_RESET_N from CoreRESET_PF (CORERESET_PF_C0_0) is connected to TX_RESETN input of COREUHD_SDITX_C0_0. FABRIC_RESET_N from CoreRESET_PF (CORERESET_PF_C1_0) is connected to RX_RESETN input of COREUHD_SDIRX_C0_0.
- RX_CLK of COREUHD_SDIRX_C0_0 is driven from LANE0_RX_CLK_R of PF_XCVR_ERM_C0_0 and TX_CLK of COREUHD_SDITX_C0_0 is driven from LANE0_TX_CLK_R of PF_XCVR_ERM_C0_0.
- The raw video data from COREUHD_SDIRX_C0_0 is looped back onto COREUHD_SDITX_C0_0 through CoreFIFO (COREFIFO_C0_0).
- The TX_INSERT_LN, TX_INSERT_CRC, and TX_INSERT_VPID inputs of COREUHD_SDITX_C0_0 are tied high, enabling insertion of LN packets, CRC packets, and VPID packets.
- The C channel line number outputs, the C channel VPID data outputs, and the C channel VPID line number outputs of COREUHD_SDIRX_C0_0 are connected to the respective line number inputs, the VPID inputs, and the VPID line number inputs of COREUHD_SDITX_C0_0.

Note: Based on the image format transmitted, user can connect either C channel line number outputs, VPID outputs, and VPID line number outputs or Y channel line number outputs, VPID outputs, and VPID line number outputs from COREUHD_SDIRX_C0_0 to the line number inputs, the VPID inputs, and the VPID line number inputs of COREUHD_SDITX_C0_0.

Figure 9 • **System Integration**



9 References

- SMPTE ST 292-1 - 1.5 Gb/s Signal/Data Serial Interface
- SMPTE ST 424 - 3 Gb/s Signal/Data Serial Interface
- SMPTE ST 2081-1 - 6 Gb/s Signal/Data Serial Interface
- SMPTE ST 2082-1 - 12 Gb/s Signal/Data Serial Interface
- SMPTE ST 352 - Payload Identification Codes for Serial Digital Interface
- *UG0667 - Microsemi PolarFire FPGA User Guide*