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Release Notes
CoreAPB3 v4.2

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51300069. 6.0 9/20

1 Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

1.1 Revision 6.0

Added PolarFire® SoC support.

1.2 Revision 5.0

Added RTG4™ and IGLOO®2 support.

1.3 Revision 4.0

The following is a summary of the changes in revision x.x of this document.

- A greater range of memory space configurations are now supported. Slave slot size can range from 256 bytes to 256 Mbytes.
- Combining of slave slots is now possible. This allows multiple regions of the memory map to be accessed through a single slave interface (S16). This feature may be useful when accessing MSS resources in a SmartFusion or SmartFusion2 SoC FPGA device.
- More flexible indirect addressing support, and left shifting of the upper 4 address bits from the master is now available when the master address bus width is less than 32 bits.

1.4 Revision 3.0

Added indirect addressing mode and capability to hide unused slots in SmartDesign canvas.

1.5 Revision 2.0

Minor updates.

1.6 Revision 1.0

The first publication of this document.

Contents

Tables

2 CoreAPB3 v4.2

This document accompanies the release of CoreAPB3 v4.2. It describes the features and enhancements of CoreAPB3 v4.2. This document contains information about the system requirements, supported families, implementations, and known issues and workarounds.

2.1 Features

- Supports up to 16 advanced peripheral bus (APB) slaves.
- Supports master data bus width of 8, 16, or 32 bits.
- Supports master address bus widths ranging from 12 bits to 32 bits.
- Enables a master with an address bus width less than 32 bits to address a memory space of up to 4 Gbytes (232 bytes) by indirect addressing.
- Allows combination of several of the 16 slave slots to have access to all of these slots through a single slave interface.

2.2 Interfaces

CoreAPB3 has a single APB mirrored master interface. This interface must be connected to an APB3 master. CoreAPB3 has 16 APB mirrored slave interfaces that can be connected to APB peripherals.

Microsemi® recommends using SmartDesign to connect and configure CoreAPB3 when creating a system design.

2.3 Delivery Types

CoreAPB3 is licensed in two ways: Obfuscated and register transfer level (RTL).

2.3.1 Obfuscated

Complete RTL code is provided for the core. This enables the core to be instantiated with SmartDesign. Simulation, synthesis, and layout can be performed within Libero® System-on-Chip (SoC). The RTL code for the core is obfuscated.

2.3.2 RTL

Complete RTL source code is provided for the core.

2.4 Supported Families

- PolarFire® SoC
- PolarFire®
- SmartFusion®2
- SmartFusion
- Microsemi Fusion®
- IGLOO®
- IGLOO®e
- IGLOO®PLUS
- ProASIC®3
- ProASIC®3E
- ProASIC®3L
- Axcelerator®
- RTAX-S
- IGLOO2
- RTG4™

2.5 Supported Tool Flows

Use Libero v8.6 or later with CoreAPB3 v4.2 release.

2.6 Installation Instructions

The CoreAPB3 CPZ file must be installed into Libero software. This is done automatically through the Catalog update function in Libero, or the CPZ file can be manually added using the **Add Core** catalog feature. Once the CPZ file is installed in Libero, the core can be configured, generated, and instantiated within SmartDesign for inclusion in the Libero project. For more information, see the *Knowledge Based article*.

To know how to create SmartDesign project using the IP cores, refer to *Libero SoC documents page* and use the latest SmartDesign user guide.

2.7 Documentation

This release contains a copy of the *CoreAPB3 Handbook*. The handbook, describes the core functionality and gives step-by-step instructions on how to simulate, synthesize, and place-and-route this core, and also implementation suggestions. Refer to *Libero SoC documents page* for instructions on obtaining IP documentation.

For updates and additional information, visit the Intellectual Property pages on the Microsemi SoC Products Group website: visit:

http://www.microsemi.com/products/fpga-soc/design-resources/ip-cores.

2.8 Known Issues and Workarounds

There are no known issues in this release.

2.9 Resolved Issues

- There were no software action requests (SARs) resolved in v4.2. PolarFire SoC support added.
- There were no software action requests (SARs) resolved in v4.1. RTG4 support was added in this version.
- Table 1, page 7 lists the SARs that were resolved in the CoreAPB3 v4.0 release.

Table 1 • **Resolved SARs in CoreAPB3 v4.0 Release**

SARs	Description
38846	Minor issue with docs packaging
40428	Indirect addressing feature through slave slot address is not consistent.
40429	Simulation loading error due to the improper part select statement in the RTL
41606	CoreAPB3: VHDL version has issues with indirect addressing
42977	Slot combining not working properly
42978	Can have ghost bits in slave address when bit shifting used
42979	BFM files missing from simulation file-sets for obfuscated license

- Table 2, page 7 lists the SARs that were resolved in the CoreAPB3 v3.0 release.

Table 2 • **Resolved SARs in CoreAPB3 v3.0 Release**

SAR	Description
11962	CCZ Verification: Handbook not available.
14963	Validation should warn if all slots disabled.
23643	Add show/hide slave bus interfaces based on slot enable parameters.
23644	Add indirect addressing registers to allow full 32 bit PADDR access from one slot.
23690	XPATH equations needed to differentiate memory map slot addresses and ranges.
23737	PCLK and PRESETN inputs need to be added due addition of internal registers.