RN0247
Release Notes
CorePCIe_AXItoAHBL v2.0

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1 Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

1.1 Revision 1.0

The first publication of this document. Created for CorePCIe_AXItoAHBL v2.0.

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2 CorePCIe_AXItoAHBL v2.0

2.1 Overview

These release notes accompany the production release of CorePCIe_AXItoAHBL v2.0. This document provides details about the features, enhancements, system requirements, supported families, implementations, and known issues and workarounds.

2.2 Features

The CorePCIe_AXItoAHBL IP provides an interface (bridge) between an AXI domain and an AHBL domain. It is an AXI slave and an AHBL master. It allows an AXI bus system to be connected to an AHBL bus, enabling the AXI master to communicate with the AHBL slave.

The IP core is recommended to be used with SmartFusion2, IGLOO2, and RTG4 PCIe AXI Master to connect to an AHBL slave or AHBL sub-system.

CorePCIe_AXItoAHBL has the following features:

- Compliant to AMBA3 AXI and AMBA3 AHB-Lite specifications
- Provides an interface between the AXI domain and the AHBL domain
- AXI and AHBL domains are synchronous (common clock for both AXI and AHBL interfaces)
- Converts 64-bit AXI write/read transactions into 32-bit AHBL write/read transactions, respectively
- Supports only 64-bit AXI transactions
- Supports only INCR type AXI burst transactions
- Generates only SINGLE AHB transfers using undefined length burst
- Generates only IDLE and NON-SEQUENTIAL AHB transfer type
- Controls the bus responses from AHBL-Slave to AXI-Master

The following features are not supported in CorePCIe_AXItoAHBL:

- Locked and exclusive transactions, that is AxLOCK
- Auxiliary signals, that is AxCACHE and AxPROT
- Write interleaving transactions
- FIXED and WRAP burst transactions
- Does not generate HMASTLOCK and HPROT

2.3 Delivery Types

Core is freely available. Complete clear RTL source code is provided.

2.4 Supported Families

- SmartFusion®2
- IGLOO®2
- RTG4™

2.5 Supported Tool Flows

Core requires Libero® v11.0 or later.

2.6 Installation Instructions

The core must be installed into Libero software. This is done automatically through the Catalog update function in Libero, or the CPZ file can be manually added using the **Add Core** catalog feature. Once the CPZ file is installed in Libero, the core can be configured, generated, and instantiated within SmartDesign for inclusion in the Libero project. For more information, see the *Knowledge Based article*.

To know how to create SmartDesign project using the IP cores, refer to the *SmartDesign User guide*.

2.7 Documentation

This release contains a copy of the *CorePCIe_AXItoAHBL Handbook*. The handbook, describes the core functionality and gives step-by-step instructions on how to simulate, synthesize, and place-and-route this core, and implementation suggestions. For more information about obtaining IP documentation, refer to the *Libero SoC Online Help*.

For updates and additional information, visit the Intellectual Property pages on the Microsemi SoC Products Group website: visit:

http://www.microsemi.com/products/fpga-soc/design-resources/ip-cores.

2.8 Supported Test Environments

No testbench is provided with the core.

2.9 Resolved Issues in v2.0 Release

Table 1 • **Resolved Issues in v2.0 Release**

SAR Number	Summary	Description	Issue in IGLOO2, SmartFusion2, and RTG4	Issue in Soft IP version
117324	AHB Master of G4 PCIe core can fail	WVALID should arrive before AWVALID, then the AXI-AHB logic may return incorrect data under certain traffic conditions.	Yes	No
35913	Concurrent read and write	If ARVALID asserted in the same cycle as BVALID, then wrong data may be returned. It was reported on the REVFIC block, not on the AXI-AHB block. The failure is similar to 117324.	Maybe	No
28745	RREADY de-assertion	Issue identified on REVFIC. In both REVFIC and PCIESS, not an issue as RREADY does not de-assert if already asserted and no RVALID.	No, PLDA core will not de-assert RREADY until after RVALID cycle.	No
30243 (117841)	Fails, if all WSTRBS off	AXI-AHB logic incorrectly handles WSTRB=00.	No, PLDA core will not generate WSTRB=00.	No
117628	HSIZE is greater than bus width	During IDLE cycles, HSIZE can go to 2'b11. This causes no functional issue. The code is updated to prevent verification monitors from generating a warning.	No, issue in soft version found in development.	No
117706	AHB burst crosses the 1KB address boundary	Issue in new soft code was resolved.	No, issue in soft version found in development.	No
117877	AXI RDATA changed before RREADY	Issue detected in verification of soft version if RREADY is de-asserted before an RVALID transfer.	No, issue in soft version found in development.	No
118167	Arbitration	AXI-AHB may complete concurrent read operation to the same address before write resulting in older data being returned. This will not cause functional issues but is non-ideal.	Yes, but system still functions correctly.	No

2.10 Discontinued Features and Devices

There are no discontinued features and devices.

2.11 Known Limitations and Workarounds

There are no known limitations and workarounds.