UG0646
User Guide
Image Enhancement IP

Microsemi
a Microchip company

Microsemi Headquarters
One Enterprise, Aliso Viejo,
CA 92656 USA
Within the USA: +1 (800) 713-4113
Outside the USA: +1 (949) 380-6100
Sales: +1 (949) 380-6136
Fax: +1 (949) 215-4996
Email: sales.support@microsemi.com
www.microsemi.com

About Microsemi

Microsemi, a wholly owned subsidiary of Microchip Technology Inc. (Nasdaq: MCHP), offers a comprehensive portfolio of semiconductor and system solutions for aerospace & defense, communications, data center and industrial markets. Products include high-performance and radiation-hardened analog mixed-signal integrated circuits, FPGAs, SoCs and ASICs; power management products; timing and synchronization devices and precise time solutions, setting the world's standard for time; voice processing devices; RF solutions; discrete components; enterprise storage and communication solutions, security technologies and scalable anti-tamper products; Ethernet solutions; Power-over-Ethernet ICs and midspans; as well as custom design capabilities and services. Learn more at www.microsemi.com.

50200646. 4.0 7/21

Contents

Figures

Tables

1 Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

1.1 Revision 4.0

The following is a summary of the changes in this revision.

- Added Key Features, page 3 and Supported Families, page 3.
- Added Table 2, page 6, Table 3, page 6, and Table 4, page 7.
- Updated Table 5, page 7.
- Added License, page 7, Encrypted, page 7, and RTL, page 7.

1.2 Revision 3.0

The resource utilization reports were updated. For more information, see Resource Utilization, page 8.

1.3 Revision 2.0

The following is a summary of changes made in this revision.

- Updated Figure 1, page 4 and Table 1, page 5. For more information, see Figure 1, page 4.

1.4 Revision 1.0

The first publication of this document.

2 Introduction

Image Enhancement IP enables you to adjust the brightness, contrast, and color balance of a final video Image according to personal preferences. These calculations are done in the RGB domain.

The inputs to Image Enhancement IP in terms of brightness and contrast are as follows:

$$R\_CONST\_I = (R_{gain} \times contrast\_factor)/10$$

$$G\_CONST\_I = (G_{gain} \times contrast\_factor)/10$$

$$B\_CONST\_I = (B_{gain} \times contrast\_factor)/10$$

$$COMMON\_CONST\_I = 128 \times (brightness - ((128 \times contrast\_factor)/10))$$

where,

$$contrast\_factor = \frac{325 \times (contrast + 128)}{(387 - contrast) \times 32}$$

R_{gain}, G_{gain}, and B_{gain} are the red, green, and blue gain values.

The output RGB values are calculated from the above inputs based on the following equations:

$$R_{out} = COMMON\_CONST\_I + R\_CONST\_I \times R_{in}$$

$$G_{out} = COMMON\_CONST\_I + G\_CONST\_I \times G_{in}$$

$$B_{out} = COMMON\_CONST\_I + B\_CONST\_I \times B_{in}$$

Where,

R_{in}, G_{in}, and B_{in} are the red, green and blue values of input data.

R_{out}, G_{out}, and B_{out} are the red, green and blue values of output data.

2.1 Key Features

- Supports image enhancement in terms of brightness, contrast, saturation, and hue
- Supports data width of 8,10 and 12
- Supports Native and AXI4 Stream Video Interface for video data transfer
- Supports Native and AXI4-Lite Configuration Interface for parameter modification

2.2 Supported Families

- PolarFire® SoC
- PolarFire®
- RTG4™
- IGLOO®2
- SmartFusion®2

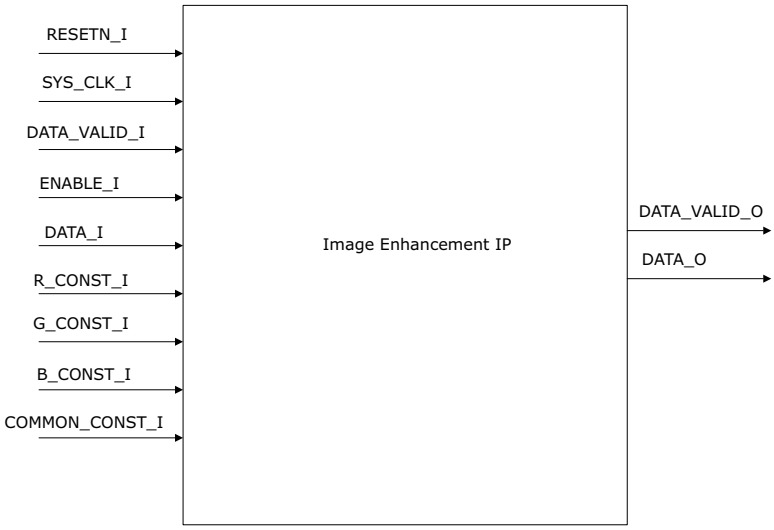
3 Hardware Implementation

This section describes the design description and inputs and outputs of the Image Enhancement IP.

3.1 Design Description

The following figure shows the block diagram of the Image Enhancement IP.

Figure 1 • **Block Diagram**



When the ENABLE_I and DATA_VALID_I signal goes high the R, G, and B values of the output is computed from the inputs according to the formula given in the introduction section. DATA_O is valid when DATA_VALID_O (which is equivalent to DATA_VALID_I with two clock cycle delay) goes high.

3.2 Inputs and Outputs

The following table lists the input and output ports of the Image Enhancement IP.

Table 1 • **Input and Output ports for 1 pixel Native Video Interface**

Port Name	Direction	Width	Description
RESETN_I	Input	1 bit	Active low asynchronous reset signal to design
SYS_CLK_I	Input	1 bit	System clock
DATA_VALID_I	Input	1 bit	Input data valid signal This signal is asserted high when the data is valid
ENABLE_I	Input	1 bit	Enable signal Should be '1' to enable image enhancement operation
DATA_I	Input	3*G_PIXEL_WIDTH bits	Input RGB data DATA_I[3* G_PIXEL_WIDTH -1] to DATA_I[2*G_PIXEL_WIDTH] represents R input DATA_I[2* G_PIXEL_WIDTH -1] to DATA_I[G_PIXEL_WIDTH] represents G input DATA_I[G_PIXEL_WIDTH -1] to DATA_I[0] represents B input
R_CONST_I	Input	10 bits	Input constant to multiply with R data
G_CONST_I	Input	10 bits	Input constant to multiply with G data
B_CONST_I	Input	10 bits	Input constant to multiply with B data
COMMON_CONST_I	Input	20 bits	Input constant with brightness and contrast
DATA_VALID_O	Output	1 bit	Output data valid signal This signal is asserted high when the data is valid
DATA_O	Output	3*G_PIXEL_WIDTH bits	Enhanced RGB data DATA_O[3* G_PIXEL_WIDTH -1] to DATA_O[2*G_PIXEL_WIDTH] represents enhanced R output DATA_O[2* G_PIXEL_WIDTH -1] to DATA_O[G_PIXEL_WIDTH] represents enhanced G output DATA_O[G_PIXEL_WIDTH -1] to DATA_O[0] represents enhanced B output

Table 2 • Input and Output Ports for 4-pixel Native Video Interface

Port Name	Type	Width	Description
RESETN_I	Input	1 bit	Active low asynchronous reset signal to design
SYS_CLK_I	Input	1 bit	System clock
DATA_VALID_I	Input	1 bit	Asserted high when input data is valid
ENABLE_I	Input	1 bit	Input Enable signal should be 'high' to enable image enhancement operation
DATA_I	Input	3*G_PIXELS*G_PIXEL_WIDTH bits	Input RGB Data
R_CONST_I	Input	10 bits	Input constant to multiply with R data
G_CONST_I	Input	10 bits	Input constant to multiply with G data
B_CONST_I	Input	10 bits	Input constant to multiply with B data
COMMON_CONST_I	Input	20 bits	Input constant with brightness and contrast
DATA_VALID_O	Output	1 bit	Asserted high when output data is valid
DATA_O	Output	3*G_PIXELS*G_DATA_WIDTH bits	Output Video Data

Table 3 • Input and Output Ports for AXI4 Stream Video Interface

Port Name	Type	Width	Description
RESETN_I	Input	1 bit	Active low asynchronous reset signal to design
SYS_CLK_I	Input	1 bit	System clock
TREADY_O	Output	1 bit	Output target ready
TDATA_I	Input	3*G_PIXELS*G_PIXEL_WIDTH bit	Input Video Data
TVALID_I	Input	1 bit	Input Video Valid
TUSER_I	Input	4 bits	Bit 0 = frame end Bit 1 = unused Bit 2 = unused Bit 3 = unused
TDATA_O	Output	3*G_PIXELS*G_PIXEL_WIDTH bit	Output Video Data
TVALID_O	Output	1 bit	Output Video Valid
TUSER_O	Output	4 bits	Bit 0 = frame end Bit 1 = unused Bit 2 = unused Bit 3 = unused
TLAST_O	Output	1 bit	Output Video End of Frame
TSTRB_O	Output	G_DATA_WIDTH/8	Output Video Data strobe
TKEEP_O	Output	G_DATA_WIDTH/8	Output Video Data Keep

IP has four specific register through that user can dynamically control the operation of IP.

Table 4 • **Register Map and Description**

Address (hex)	Register name	Type	Description
0x004	R_CONST_ADDR	Read/Write	Input constant to multiply with R data
0x008	G_CONST_ADDR	Read/Write	Input constant to multiply with G data
0x00C	B_CONST_ADDR	Read/Write	Input constant to multiply with B data
0x010	SECOND_CONST_ADDR	Read/Write	Input constant with brightness and contrast

3.3 Configuration Parameters

The following table lists the configuration parameters used in the hardware implementation of the Image Enhancement. These parameters are generic and can be varied based on the application requirement.

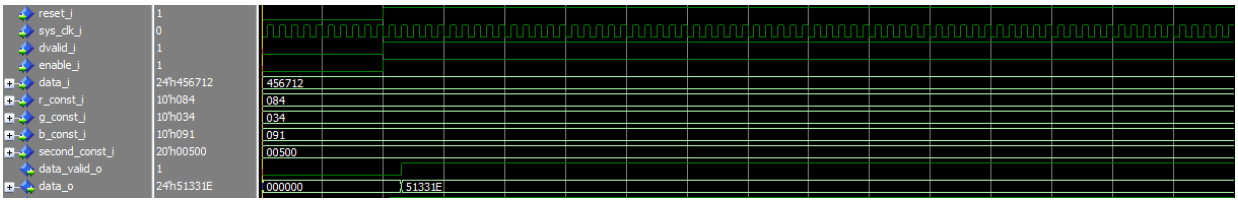
Table 5 • **Configuration Parameter**

Parameter Name	Description
Number of Pixels	Number of pixels per clock 1 and Number of pixels per clock 4
Pixel Width	Bit width of each pixel
Video Interface	Native Video Interface and AXI4 Stream Video Interface
Configuration Interface	Native Configuration Interface and AXI4-Lite Configuration Interface

3.4 Timing Diagrams

The following figure shows the timing diagram of the Image Enhancement IP.

Figure 2 • **Timing Diagram**



3.5 License

Image Enhancement clear RTL is license locked, and the encrypted RTL is available for free.

3.5.1 Encrypted

Complete RTL code is provided for the core, allowing it to be instantiated with the SmartDesign tool.

Simulation, synthesis, and layout can be performed within Libero® System-on-Chip (SoC). The RTL code is encrypted for the core.

3.5.2 RTL

Complete RTL source code is provided for the core.

3.6 Resource Utilization

The Image Enhancement IP is implemented on SmartFusion®2 System-on-Chip (SoC) Field Programmable Gate Array (FPGA) device (M2S150T-1152 FC package) and PolarFire® FPGA (MPF300TS-1FCG1152E package).

Table 6 • **Resource Utilization on PolarFire[1]**

Resource	Usage
DFFs	173
4-input LUTs	139
MACC	3
RAM1Kx18	0
RAM64x18	0

1. For G_PIXEL_WIDTH = 8.

Table 7 • **Resource Utilization on SmartFusion2[1]**

Resource	Usage
DFFs	173
4-input LUTs	141
MACC	3
RAM1Kx18	0
RAM64x18	0

1. For G_PIXEL_WIDTH = 8.