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Release Notes
CoreAHBL2AHBL_Bridge v2.2

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1 Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

1.1 Revision 3.0

Updated for CoreAHBL2AHBL_Bridge v2.2.

1.2 Revision 2.0

Updated for CoreAHBL2AHBL_Bridge v2.1.

1.3 Revision 1.0

The first publication of this document. Created for CoreAHBL2AHBL_Bridge v2.0.

Contents

2 CoreAHBL2AHBL_Bridge v2.2

These release notes accompany the production release of CoreAHBL2AHBL_Bridge v2.2. This document provides details about the features, enhancements, system requirements, supported families, implementations, and known issues and workarounds.

2.1 Features

CoreAHBL2AHBL_Bridge has the following features:

- Two different asynchronous clock domains for the master and slave interfaces
- Single read, single write transactions
- Burst Mode—INCR and WRAP with busy transfer type
- Extended HREADY

2.2 Delivery Types

CoreAHBL2AHBL_Bridge does not require a license to be used and instantiated. The complete RTL source code is available for the core

2.3 Supported Families

- PolarFire® SoC
- PolarFire®
- IGLOO®2
- SmartFusion®2
- RTG4™

2.4 Supported Tool Flows

CoreAHBL2AHBL_Bridge requires Libero® System-on-Chip (SoC) software v11.0 or later.

2.5 Installation Instructions

The CoreAHBL2AHBL_Bridge CPZ file must be installed into Libero software. This is done automatically through the Catalog update function in Libero, or the CPZ file can be manually added using the **Add Core** catalog feature. Once the CPZ file is installed in Libero, the core can be configured, generated, and instantiated within SmartDesign for inclusion in the Libero project. For more information, see the *Knowledge Based article*.

To know how to create a SmartDesign project using IP cores, refer to the *SmartDesign User guide*.

2.6 Documentation

This release contains a copy of the *CoreAHBL2AHBL_Bridge Handbook*. The handbook describes the core functionality and gives step-by-step instructions on how to simulate, synthesize, and place-and-route this core, and also implementation suggestions. Refer to the *Libero SoC Online Help* for instructions on obtaining IP documentation.

For updates and additional information, visit the Intellectual Property pages on the Microsemi SoC Products Group website: visit:

http://www.microsemi.com/products/fpga-soc/design-resources/ip-cores

2.7 Supported Test Environments

Verilog user test bench.

2.8 Resolved Issues in v2.2 Release

Table 1 • **Resolved SARs in CoreAHBL2AHBL_Bridge v2.2 Release**

SAR	Description
113040	Resolved Synthesis failing issue when multiple instances of the core is used in Libero SmartDesign.
115868	Added memory map feature.
116375	Resolved Simulation failing issue because of error in bfmtovec_compile.tcl file.
117408	Resolved duplicate module issue when CoreAHBL2AHBL_Bridge is used with CoreAXI4Interconnect.

2.9 Resolved Issues in v2.1 Release

Table 2 • **Resolved SARs in CoreAHBL2AHBL_Bridge v2.1 Release**

SAR	Description
97506	Changed the architecture of the core to increase the throughput.

2.10 Discontinued Features and Devices

There are no discontinued features in this release.

2.11 Known Limitations and Workarounds

There are no known limitations associated with CoreAHBL2AHBL_Bridge.