RN0064
Release Notes
CoreSDR_AHB v4.4

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1 Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

1.1 Revision 4.0

Updated the document for CoreSDR_AHB v4.4. Resolved SARs in CoreSDR_AHB v4.4 release, see Table 1, page 2.

1.2 Revision 3.0

Resolved SARs in CoreSDR_AHB v4.3 release, see Table 2, page 2.

1.3 Revision 2.0

Resolved SARs in CoreSDR_AHB v4.1 release, see Table 3, page 3.

1.4 Revision 1.0

This was the first publication of this document. Created for CoreSDR_AHB v4.0.

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2 CoreSDR AHB

This release notes accompanies the production release of CoreSDR_AHB IP Core. This document provides details about the features, system requirements, supported families, implementations, and known issues and workarounds.

2.1 Features

CoreSDR_AHB supports the following features:

- Provides high performance, Single Data Rate (SDR) controller for standard SDRAM chips, and dual in-line memory modules (DIMMs)
- Provides synchronous interface and fully pipelined internal architecture
- Supports up to 1024 MB of memory
- Bank management logic monitors the status of up to 8 SDRAM banks
- Support for Advanced High-performance Bus (AHB) slave interface
- Data access of 8, 16, and 32 bits are allowed by masters

2.2 Interfaces

Supported interface is AHB Lite.

2.3 Delivery Types

No license is required for this core.

2.3.1 Register Transfer Level (RTL)

Complete RTL source code is provided for the core and testbenches.

2.4 Supported Families

The following list of families are supported:

- PolarFire® SoC
- PolarFire®
- RTG4™
- IGLOO®2
- SmartFusion®2
- SmartFusion®
- ProASIC®3
- ProASIC3E
- ProASIC3L
- Fusion

2.5 Supported Tool Flows

Use Libero SoC v10.0 or later with this CoreSDR_AHB release.

2.6 Installation Instructions

The CoreSDR_AHB CPZ file must be installed into Libero software. This is done automatically through the Catalog update function in Libero, or the CPZ file can be manually added using the **Add Core** catalog feature. Once the CPZ file is installed in Libero, the core can be configured, generated, and instantiated within SmartDesign for inclusion in the Libero project. Refer to the *Libero SoC Online Help* for instructions on core installation, licensing, and general use.

To know how to create SmartDesign project using the IP cores, refer to the *SmartDesign User guide*.

2.7 Documentation

This release contains a copy of the *CoreSDR Handbook*. The handbook, describes the core functionality and gives step-by-step instructions on how to simulate, synthesize, and place-and-route this core, and also suggests implementation changes. Refer to the *Libero SoC Online Help* for instructions on obtaining IP documentation.

For updates and additional information about the software, devices, and hardware, visit the Intellectual Property pages on the Microsemi SoC Products Group website: visit:

http://www.microsemi.com/products/fpga-soc/design-resources/ip-cores.

2.8 Supported Test Environments

Verilog user testbench.

2.9 Resolved Issues in the v4.4 Release

Table 1 lists the Software Action Requests (SARs) that were resolve in the CoreSDR_AHB v4.4 release.

Table 1 • **Resolved SARs in CoreSDR_AHB v4.4 Release**

SAR	Description
79466	Added support for RTG4.
31123, 103906, 104483	Updated Handbook with the relevant fixes: • REF range • Version number • Review latency parameter calculations
104010	Added support for AHB Burst transactions. This involves adding two Memory buffer for write and read data path and change control logic for read, write, and Hready and so on. This is a major enhancement.
50630	Updated minimum REF value in GUI to support wider range of values.
91017	CoreSDR addressing, fixed coladdr in the DUT Module sdr_fastsdram.

2.10 Resolved Issues in the v4.3 Release

Table 2 lists the Software Action Requests (SARs) that were resolve in the CoreSDR_AHB v4.3 release.

Table 2 • **Resolved SARs in CoreSDR_AHB v4.3 Release**

SAR	Description
58830	Added SmartFusion2 and IGLOO2 support.
44307	Wrote a write data into the memory before it latched on the AHB interface.

2.11 Resolved Issues in the v4.1 Release

Table 3 lists the SARs that were resolve in the CoreSDR_AHB v4.1 release.

Table 3 • **Resolved SARs in CoreSDR_AHB v4.1 Release**

SAR	Description
19346	Added support to IGLOO, IGLOOe, IGLOO PLUS, and SmartFusion device family.

2.12 Discontinued Features and Devices

VHDL support has been discontinued in this release.

2.13 Known Limitations and Workarounds

There are no known issues in this release.