HB0510
Handbook
CoreMMC v3.1

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1 Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

1.1 Revision 3.0

Added PolarFire® SoC support.

1.2 Revision 2.0

Updated for v3.0 release.

- Added details of additional multiple block support registers.
- Updated user testbench information to reflect new BFM based testbench.
- Modified prefixes of all interrupt related bits to prevent naming clashes with single and multiple block prefix convention.
- Additional information provided for clock register description.
- Renamed DMA control signals.
- Updated utilization data including information on achieving >104 MHz timing.
- Added VHDL support.
- Width of Write and Read Data FIFOs updated from 8- to 32-bits.

1.3 Revision 1.0

The first publication of this document.

2 Preface

2.1 About this Document

This handbook describes the CoreMMC module and how to use it.

2.2 Intended Audience

FPGA designers using Libero® System-on-Chip (SoC).

3 Introduction

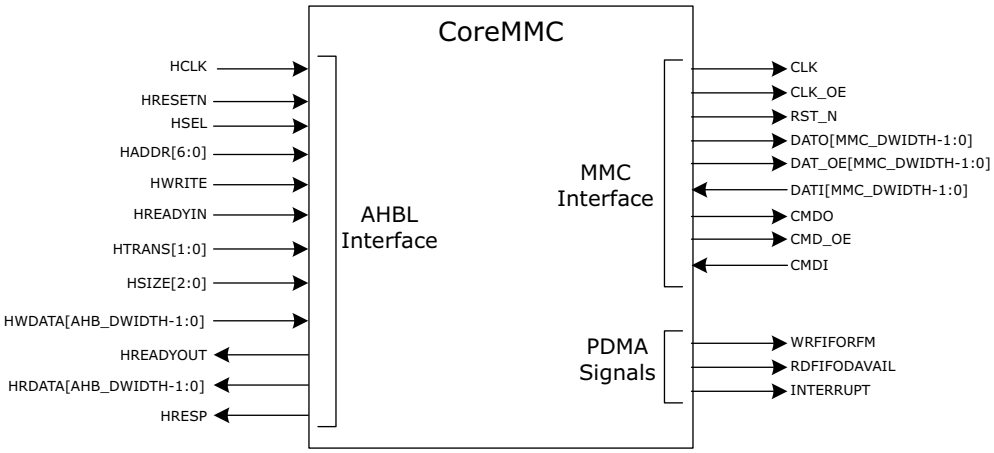
CoreMMC provides an embedded MultiMedia Card (eMMC) controller to interface with eMMC devices. eMMC devices can be utilized to expand the on-board storage capacity for larger applications or to store user data. The core is parameterized to allow user specifications of MMC data bus width and FIFO depth and is conformant to the JEDEC eMMC 4.41 standard specification.

CoreMMC consists of an AMBA high-performance Bus-Lite (AHB-Lite) slave interface designed to connect to an AHB-Lite bus. Block write and read data FIFOs can be accessed by an AHB-Lite master along with the CoreMMC registers.

eMMC is a version of the MMC standard that provides a unified command or control interface for various memory types, mostly for high-capacity, high-performance, low-cost multimedia storage purposes. Communication is achieved using an (up to) 10-bit bus and a control protocol that is defined as part of the JEDEC eMMC standard. For more information, refer to the *JEDEC eMMC 4.41 Standard Specification* document.

eMMC abstracts the complex and divergent Flash interface of various vendors and allows better design modularity and portability.

Figure 1 • **CoreMMC I/O Signal Diagram**



3.1 Supported Families

- PolarFire® SoC
- PolarFire®
- IGLOO®2
- SmartFusion®2

3.2 Key Features

- Up to 52 MHz MMC clock rate, making for a maximum of ~52 MBs throughput at 8-bit data width (This is the theoretical throughput of CoreMMC. Actual throughput is affected by eMMC device throughput and AHB bandwidth)
- Configurable data bus widths
  - 1-/4-/8-bit
- Supports block mode transfer:
  - Single block write
  - Multiple block write
  - Single block read
  - Multiple block read
- Cyclic Redundancy Check (CRC) protection for both commands and data transfers
- AHB-Lite compliant
  - Command, response, write, and read data registers for indirect access to MMC part
  - 8-/16-/32-bit AHB transfers
- Write DATA FIFO:
  - To decouple AHB from MMC bus for write data transfers
  - Depth configurable from 512 Bytes to 32 KBs
  - Overrun and underrun error flags
- Read DATA FIFO:
  - To decouple AHB from MMC bus for read data transfers
  - Depth configurable from 512 Bytes to 32 KBs
  - Overrun and underrun error flags
- Interrupt generation:
  - Command sent and response received interrupts
  - Error flag interrupts
  - Single block write and read done interrupts
  - Multiple block write and read done interrupts
- Automatic sleep mode for eMMC when clock is low

3.3 Limitations

It does not support:

- Sequential mode transfers
- ECC error correction (handled on the device side instead)
- Stream read and stream write
- Double Data Rate (DDR)

3.4 Core Version

This handbook supports CoreMMC version 3.1.

3.5 Supported Interfaces

CoreMMC is available with the following interfaces:

- AHB-Lite slave interface
- Interrupt request interface
- MMC master interface
- Peripheral direct memory access (PDMA) interface

For more information about these interfaces, refer to the I/O Signals, page 6.

3.6 Utilization and Performance

CoreMMC is implemented in several devices of Microsemi using standard speed grades.

Table 1 and Table 2 list a summary of various implementations data.

Table 1 • **CoreMMC Device Utilization and Performance (Minimum Configuration - Default synthesis settings**

	Logic Elements		Utilization		Performance	
Family	**Sequential**	**Combinatorial**	**Device**	**Total%**	**(MHz)**	**RAM**
SmartFusion2	988	1,787	M2S050	4.65	120	8 Blocks of uSRAM
IGLOO2	988	1,787	M2GL050	4.65	120	8 Blocks of uSRAM
PolarFire	776	1,532	MPF300T	0.53	150	2 Blocks of LSRAM

Note: Data in this table was achieved using the Verilog RTL with typical synthesis and layout settings. Top-level parameters or generics were set as: MMC_DWIDTH = 0, FIFO_DEPTH = 0.

Note: FPGA resources and performance data for the PolarFire SoC family is similar to PolarFire family.

Table 2 • **CoreMMC Device Utilization and Performance (Maximum Configuration - Default synthesis settings**

	Logic Elements		Utilization		Performance	
Family	**Sequential**	**Combinatorial**	**Device**	**Total%**	**(MHz)**	**RAM**
SmartFusion2	2,030	2,866	M2S050	5.35	110	32 Blocks of LSRAM
IGLOO2	2,030	2,866	M2GL050	5.35	110	32 Blocks of LSRAM
PolarFire	2,030	2,891	MPF300T	1.0	130	32 Blocks of LSRAM

Note: Data in this table was achieved using the Verilog RTL with typical synthesis and layout settings. Top-level parameters or generics were set as: MMC_DWIDTH = 3, FIFO_DEPTH = 3.

Note: FPGA resources and performance data for the PolarFire SoC family is similar to PolarFire family.

3.7 Reference Documents

The following are the documents referred to in this document.

- JEDEC eMMC 4.41 Standard Specification
- SanDisk eMMC 4.41 I/F Preliminary Datasheet
- AMBA® 3 AHB-Lite Protocol

4 Design Description

4.1 Verilog or VHDL Parameters

Table 3 describes the CoreMMC parameters (Verilog) or generics (VHDL) for configuring the RTL code. All parameters and generics are integer types.

Table 3 • **CoreMMC Parameters or Generics Descriptions**

Name	Valid Range	Default	Description
MMC_DWIDTH	0, 2, 3	0	Serial data bus width, allowed to be 1-/4-/8-bit as per the JEDEC eMMC 4.41 standard. 0: 1- bit 2: 4-bit 3: 8-bit
FIFO_DEPTH	0-3	0	0: 512 B 1: 4 K 2: 16 K 3: 32 K

4.2 I/O Signals

Table 4 describes the port signals for the CoreMMC macro as shown in Figure 1, page 5.

Table 4 • **CoreMMC I/O Signal Descriptions**

Name	Type	Description
eMMC signals (to eMMC slave)		
CLK	Out	Clock output to MMC device. Derived from the HCLK at frequency determined by clock register.
CLK_OE	Out	Clock output enable. To be used by a slave MMC device to enter into low power mode when no operation is in progress. Refer to the *JEDEC eMMC 4.41 Standard Specification* document.
RST_N	Out	Hard reset for eMMC device. Active Low signal. Only operational for slave device if enabled within the slave device.
DATO[MMC_DSIZE-1:0]	Out	Data output for bi-directional bus in push-pull mode
DATI[MMC_DSIZE-1:0]	In	Data input from bi-directional bus in push-pull mode
DAT_OE[MMC_DSIZE-1:0]	Out	Output enable for data bus
CMDO	Out	Command bus output
CMDI	In	Command bus input
CMD_OE	Out	Output enable for command bus
AHB slave signals		
HCLK	In	AHB system clock
HRESETN	In	AHB system reset. The signal is active Low. Asynchronous assertion and synchronous de-assertion. This is used to reset AHB registers in the block. Assertion of this signal causes RST_N to be asserted.

Table 4 • **CoreMMC I/O Signal Descriptions *(continued)***

Name	Type	Description
HSEL	In	AHB-Lite slave select. This signal indicates that the current transfer is intended for the selected slave.
HADDR[6:0]	In	AHB-Lite address. 7-bit address on the AHB-Lite interface.
HWRITE	In	AHB-Lite write. When High, it indicates that the current transaction is a write. When Low, it indicates that the current transaction is a read.
HREADYIN	In	When High, the HREADY signal indicates to the master and all slaves, that the previous transfer is complete.
HREADYOUT	Out	When High, the HREADYOUT signal indicates that the transfer has finished on the bus. This signal can be driven Low to extend a transfer.
HTRANS[1:0]	In	AHB-Lite transfer type. Indicates the transfer type of the current transaction. b00: IDLE b01: BUSY b10: NONSEQUENTIAL b11: SEQUENTIAL (not supported) **Note:** Note: The PDMA engine only performs single cycle accesses (no bursts), so sequential transfers are not supported.
HSIZE	In	AHB-Lite transfer size. Indicates the size of the current transfer (8-/16-/32-/64-bit transactions only): bx00: 8-bit (byte) transaction bx01: 16-bit (half word) transaction bx10: 32-bit (word) transaction bx11: 64-bit (double word) transaction (not supported)
HWDATA[31:0]	In	AHB-Lite write data. Write data from the AHB-Lite master to the AHB-Lite slave.
HRESP	Out	AHB-Lite response status. When driven High at the end of a transaction, it indicates that the transaction has completed with errors. When driven Low at the end of a transaction, it indicates that the transaction has completed successfully.
HRDATA[31:0]	Out	AHB-Lite read data. Read data from the AHB-Lite slave to the AHB-Lite master.
Interrupt or Status signals (to DMA engine)		
WRFIFORFM	Out	Indicates that there is room to store another 32-bit word in the write FIFO
RDFIFODAVAIL	Out	Indicates that there is a 32-bit word available to read from the read FIFO.
INTERRUPT	Out	Interrupt output, asserted if any of the masked interrupt bits in the ISR/SBISR/MBISR are asserted.

Note: All signals are active High (logic 1) unless otherwise noted.

5 Register Map and Descriptions

5.1 Register Summary

Table 5 • **CoreMMC Internal Register Address Map**

Address	Register Name	Mnemonic	Type	Width (bits)	Reset Value	Description (8-bit)
0x00	Status register	SR	R/W	8	0x18	Indicates the status of transactions in the core such as response received and errors logged. This register does not cause interrupts to be asserted.
0x01	Version register	VR	R	8	0x3	This register defines the version of core along with the parameters used to generate the core. Default values are shown based on default parameters.
0x02	Major Version Register	MJVR	R	8	0x3	Indicates the major version of core version number.
0x03	Minor Version Register	MIVR	R	8	0x0	Indicates the minor version of core version number.
0x04	Command Index	CMDX	R/W	8	0x0	Command Index (command register 0) defines the command number to be sent to the slave device.
0x08	Command Arg1	Arg1	R/W	8	0x0	Command Argument1. Sets the first byte of the argument for the Command being issued to the slave. Argument1, Argument2, Argument3, and Argument4 compose the full argument. All four bytes can be written together.
0x09	Command Arg2	Arg2	R/W	8	0x0	Command Argument2. Sets the Second byte of the argument for the Command being issued to the slave.
0x0a	Command Arg3	Arg3	R/W	8	0x0	Command Argument3. Sets the Third byte of the argument for the Command being issued to the slave.
0x0b	Command Arg4	Arg4	R/W	8	0x0	Command Argument4. Sets the Fourth byte of the argument for the Command being issued to the slave. Writing this register causes command to be sent to slave device (whether written as Argument4 or as word write to Argument4, Argument3, Argument2, and Argument1).
0x10	Response Register0	RR0	R	8	0x0	Response Register 0
0x14	Response Register1	RR1	R	8	0x0	Response Register 1
0x15	Response Register2	RR2	R	8	0x0	Response Register 2
0x16	Response Register3	RR3	R	8	0x0	Response Register 3
0x17	Response Register4	RR4	R	8	0x0	Response Register 4
0x18	Response Register5	RR5	R	8	0x0	Response Register 5

Table 5 • **CoreMMC Internal Register Address Map *(continued)***

Address	Register Name	Mnemonic	Type	Width (bits)	Reset Value	Description (8-bit)
0x19	Response Register6	RR6	R	8	0x0	Response Register 6
0x1a	Response Register7	RR7	R	8	0x0	Response Register 7
0x1b	Response Register8	RR8	R	8	0x0	Response Register 8
0x1c	Response Register9	RR9	R	8	0x0	Response Register 9
0x1d	Response Register10	RR10	R	8	0x0	Response Register 10
0x1e	Response Register11	RR11	R	8	0x0	Response Register 11
0x1f	Response Register12	RR12	R	8	0x0	Response Register 12
0x20	Response Register13	RR13	R	8	0x0	Response Register 13
0x21	Response Register14	RR14	R	8	0x0	Response Register 14
0x22	Response Register15	RR15	R	8	0x0	Response Register 15
0x24	Write Data Register	WDR	W	32	0x0	Write Data register (32 bits)
0x28	Read Data Register	RDR	R	32	0x0	Read Data register (32 bits)
0x2C	Interrupt Mask Register	IMR	R/W	8	0x0	Indicates the bits in the ISR that can cause the interrupt to be asserted. When a bit is set to 1 in this register, if the corresponding bit in ISR is asserted, then the Interrupt line is asserted.
0x2D	Singe Block Interrupt Mask Register	SBIMR	R/W	8	0x0	Indicates the bits in the SBISR that can cause the interrupt to be asserted. When a bit is set to 1 in this register, if the corresponding bit in SBISR is asserted, then the Interrupt line is asserted.
0x2E	Multiple Block Interrupt Mask Register	MBIMR	R/W	8	0x0	Indicates the bits in the MBISR that can cause the interrupt to be asserted. When a bit is set to 1 in this register, if the corresponding bit in MBISR is asserted, then the Interrupt line is asserted.
0x30	Interrupt Status Register	ISR	R	8	0x0	Interrupt status register
0x31	Single Block Interrupt Status Register	SBISR	R	8	0x0	Single block interrupt status register
0x32	Multiple Block Interrupt Status Register	MBISR	R	8	0x0	Multiple block interrupt status register
0x34	Interrupt Clear Register	ICR	W	8	0x0	Interrupt clear register
0x35	Single Block Interrupt Clear Register	SBICR	W	8	0x0	Single block interrupt clear register
0x36	Multiple Block Interrupt Clear Register	MBICR	W	8	0x0	Multiple block interrupt clear register
0x38	Control Register	CTRL	R/W	8	0x0C	Control register
0x39	Single Block Control and Status Register	SBCSR	R/W	8	0x0	Single block control and status register

Table 5 • **CoreMMC Internal Register Address Map *(continued)***

Address	Register Name	Mnemonic	Type	Width (bits)	Reset Value	Description (8-bit)
0x3A	Multiple Block Control and Status Register	MBCSR	R/W	8	0x0	Multiple block control and status register
0x3C	Response Time-out Register	RSPTO	R/W	8	0x40	Response timeout register
0x40	Data Time-out Register	DATATO	R/W	32	0x400	Data timeout register
0x44	Block Length Register	BLR	R/W	16	0x200	Block length
0x48	Data Control Register	DCTRL	R/W	8	0x00	Data size control
0x4C	Clock Register	CLKR	R/W	8	0x3F	Clock register
0x50	Block Count Register	BCR	R/W	16	0x00	Block count register

Note: Values shown in tables are in hexadecimal format; type designations: R = read only; W = write only; R/W = read/write

5.2 Status Register

This register contains the status and error bits pertaining to the operation of CoreMMC.

Note: This register does not actually reflect the status of the slave MMC device. Information on the MMC device can be extracted by checking the Response Registers. Table 6 shows the CoreMMC status register.

Table 6 • **Status Register**

HADDR [6:0]	Register Name	Type	Width	Reset Value	Description
0x00	Status	R/W	8	0x18	Status register provides the information on the internal status of the core and error flags.

Table 7 • **Status Register Bits**

Bit(s)	Type	Name	Description
7	R	rdre	Response data ready: Status bit indicates the response waiting to be read from RR0-RR15. Reading any of those registers will clear this bit.
6	R	swff	Write FIFO full. Status bit indicates that the write FIFO is currently full.
5	R	srff	Read FIFO full. Status bit indicates that the read FIFO is currently full.
4	R	swfe	Write FIFO empty. Status bit indicates that the write FIFO is currently empty.
3	R	srfe	Read FIFO empty. Status bit indicates that the read FIFO is currently empty.
2	R/W	ebod	Buffer overflow detected. While receiving a block of data from the MMC device, a full read FIFO was detected. This bit stays set until it is cleared by writing a 1 to it.
1	R/W	ebud	Buffer underrun detected. While writing a block of data, the write FIFO ran out of bytes. This bit stays set until it is cleared by writing a 1 to it.
0	R/W	ecrd	CRC error detected. CRC mismatch on incoming response from MMC slave. This bit stays set until it is cleared by writing a 1 to it.

Note: All bits are active High unless otherwise indicated.

5.3 CoreMMC Version Register

This register contains the version of the core and the parameters used to generate the instance of the core. Table 8 shows the CoreMMC version register.

Table 8 • **Version Register**

HADDR[6:0]	Register Name	Type	Width	Reset Value	Description
0x01	Version	R/W	8	0x03	This register provides the version of core along with the parameters used to generate the core. Default values depend on configuration values. Default values are shown based on the default parameters.

Table 9 • **Version Register Bit Definitions**

Bit(s)	Type	Name	Description
7:6	R	-	Reserved
5:4	R	fifo_dep	FIFO Depth. The value of parameter FIFO_DEPTH used to generate core.
3:2	R	mmc_dw	MMC Data Width. Based value of parameter MMC_DWIDTH used to generate core. mmc_dw encoding is: 00: 1-bit 01: 4-bit 10: 8-bit **Note:** This coding is different to MMC_DWIDTH codes.
1:0	R	rev	Revision of this instance of CoreMMC. rev coding is: 0, 1, 2: Initial CoreMMC instance 3: Refer to the Major Version and Minor Version registers for information on this instances version

Note: All bits are active High unless otherwise indicated.

5.4 Major Version Register

This register contains the major version of the core. Table 10 shows the CoreMMC major version register.

Table 10 • **Major Version Register**

HADDR[6:0]	Register Name	Type	Width	Reset Value	Description
0x02	Major Version	R	8	0x03	This register contains the major version number of the core.

5.5 Minor Version Register

This register contains the minor version of the core. Table 11 shows the CoreMMC minor version register.

Table 11 • **Minor Version Register**

HADDR[6:0]	Register Name	Type	Width	Reset Value	Description
0x03	Minor Version	R	8	0x00	This register contains the minor version number of the core.

5.6 Command Index Register

Command Index (or command register 0) defines the command number to be sent to the slave device.

Table 12 • **Command Index Register**

HADDR[6:0]	Register Name	Type	Width	Reset Value	Description
0x04	CMDX	R/W	8	0x0	Command Index (or command register 0) defines the command number to be sent to the slave device.

Table 13 • **Command Index Register Bit Definitions**

Bit(s)	Type	Name	Description
7:6	R	-	Reserved
5:0	R/W	CMDX	Command Index (or command register 0)

Note: All bits are active High unless otherwise indicated.

5.7 Command Argument1 Register

This register contains the first byte of command argument to be sent to the MMC slave.

Table 14 • **Command Argument1 Register**

HADDR[6:0]	Register Name	Type	Width	Reset Value	Description
0x08	Arg1	R/W	8	0x0	Command Argument1. Sets the first byte of the argument for Command to be sent to the slave. Argument1, Argument2, Argument3, and Argument4 compose the full argument. All four bytes can be written together.

5.8 Command Argument2 Register

This register contains the second byte of command argument to be sent to the MMC slave.

Table 15 • **Command Argument2 Register**

HADDR[6:0]	Register Name	Type	Width	Reset Value	Description
0x09	Arg2	R/W	8	0x0	Command Argument2. The second byte of argument for Command to be sent to the slave.

5.9 Command Argument3 Register

This register contains the third byte of command argument to be sent to the MMC slave.

Table 16 • **Command Argument3 Register**

HADDR[6:0]	Register Name	Type	Width	Reset Value	Description
0x0a	Arg3	R/W	8	0x0	Command Argument3. The third byte of argument for Command to be sent to the slave.

5.10 Command Argument4 Register

This register contains the fourth byte of command argument to be sent to the MMC slave.

Table 17 • **Command Arg4 Register**

HADDR[6:0]	Register Name	Type	Width	Reset Value	Description
0x0b	Arg4	R/W	8	0x0	Command Argument4. The fourth byte of argument for Command to be sent to the slave. The writing of this byte initiates the sending of a command (composed of CMDX, Arg1, Arg2, Arg3, and Arg4) to the slave MMC device. Once Argument4 is written, these four registers (CMDX, Arg1, Arg2, Arg3, and Arg4) should not be written again until the command is completed (sent as indicated by stacsi bit or timed-out as indicated by stasbi in ISR).

5.11 Response Register0

This register contains the first byte of the response received from the slave MMC device. This is updated by the core when starri is set and cleared when Argument4 register is written.

Table 18 • **Response Register0**

HADDR[6:0]	Register Name	Type	Width	Reset Value	Description
0x10	RR0	R	8	0x0	Response Register0. First byte of response from the MMC device.

5.12 Response Register1

This register contains the second byte of the response received from the slave MMC device. This is updated by the core when starri is set and cleared when Argument4 register is written.

Table 19 • **Response Register1**

HADDR[6:0]	Register Name	Type	Width	Reset Value	Description
0x14	RR1	R	8	0x0	Response Register1. Second byte of response from the MMC device.

5.13 Response Register2

This register contains the third byte of the response received from the slave MMC device. This is updated by the core when starri is set and cleared when Argument4 register is written.

Table 20 • **Response Register2**

HADDR[6:0]	Register Name	Type	Width	Reset Value	Description
0x15	RR2	R	8	0x0	Response Register2. Third byte of response from the MMC device.

5.14 Response Register3

This register contains the fourth byte of the response received from the slave MMC device. This is updated by the core when starri is set and cleared when Argument4 register is written.

Table 21 • **Response Register3**

HADDR[6:0]	Register Name	Type	Width	Reset Value	Description
0x16	RR3	R	8	0x0	Response Register3. Fourth byte of response from the MMC device.

5.15 Response Register4

This register contains the fifth byte of the response received from the slave MMC device. This is updated by the core when starri is set and cleared when Argument4 register is written.

Table 22 • **Response Register4**

HADDR[6:0]	Register Name	Type	Width	Reset Value	Description
0x17	RR4	R	8	0x0	Response Register4. Fifth byte of response from the MMC device.

5.16 Response Register5

This register contains the sixth byte of the response received from the slave MMC device. This is updated by the core when starri is set and cleared when Argument4 register is written.

Table 23 • **Response Register5**

HADDR[6:0]	Register Name	Type	Width	Reset Value	Description
0x18	RR5	R	8	0x0	Response Register5. Sixth byte of response from the MMC device.

5.17 Response Register6

This register contains the seventh byte of the response received from the slave MMC device. This is updated by the core when starri is set and cleared when Argument4 register is written.

Table 24 • **Response Register6**

HADDR[6:0]	Register Name	Type	Width	Reset Value	Description
0x19	RR6	R	8	0x0	Response Register6. Seventh byte of response from the MMC device.

5.18 Response Register7

This register contains the eighth byte of the response received from the slave MMC device. This is updated by the core when starri is set and cleared when Argument4 register is written.

Table 25 • **Response Register7**

HADDR[6:0]	Register Name	Type	Width	Reset Value	Description
0x1A	RR7	R	8	0x0	Response Register7. Eighth byte of response from the MMC device.

5.19 Response Register8

This register contains the ninth byte of the response received from the slave MMC device. This is updated by the core when starri is set and cleared when Argument4 register is written.

Table 26 • **Response Register8**

HADDR[6:0]	Register Name	Type	Width	Reset Value	Description
0x1B	RR8	R	8	0x0	Response Register8. Ninth byte of response from the MMC device.

5.20 Response Register9

This register contains the tenth byte of the response received from the slave MMC device. This is updated by the core when starri is set and cleared when Argument4 register is written.

Table 27 • **Response Register9**

HADDR[6:0]	Register Name	Type	Width	Reset Value	Description
0x1C	RR9	R	8	0x0	Response Register9. Tenth byte of response from the MMC device.

5.21 Response Register10

This register contains the eleventh byte of the response received from the slave MMC device. This is updated by the core when starri is set and cleared when Argument4 register is written.

Table 28 • **Response Register10**

HADDR[6:0]	Register Name	Type	Width	Reset Value	Description
0x1D	RR10	R	8	0x0	Response Register10. Eleventh byte of response from the MMC device.

5.22 Response Register11

This register contains the twelfth byte of the response received from the slave MMC device. This is updated by the core when starri is set and cleared when Argument4 register is written.

Table 29 • **Response Register11**

HADDR[6:0]	Register Name	Type	Width	Reset Value	Description
0x1E	RR11	R	8	0x0	Response Register11. Twelfth byte of response from the MMC device.

5.23 Response Register12

This register contains the thirteenth byte of the response received from the slave MMC device. This is updated by the core when starri is set and cleared when Argument4 register is written.

Table 30 • **Response Register12**

HADDR[6:0]	Register Name	Type	Width	Reset Value	Description
0x1F	RR12	R	8	0x0	Response Register12. Thirteenth byte of response from the MMC device.

5.24 Response Register13

This register contains the fourteenth byte of the response received from the slave MMC device. This is updated by the core when starri is set and cleared when Argument4 register is written.

Table 31 • **Response Register13**

HADDR[6:0]	Register Name	Type	Width	Reset Value	Description
0x20	RR13	R	8	0x0	Response Register13. Fourteenth byte of response from the MMC device.

5.25 Response Register14

This register contains the fifteenth byte of the response received from the slave MMC device. This is updated by the core when starri is set and cleared when Argument4 register is written.

Table 32 • **Response Register14**

HADDR[6:0]	Register Name	Type	Width	Reset Value	Description
0x21	RR14	R	8	0x0	Response Register14. Fifteenth byte of response from the MMC device.

5.26 Response Register15

This register contains the sixteenth byte of the response received from the slave MMC device. This is updated by the core when starri is set and cleared when Argument4 register is written.

Table 33 • **Response Register15**

HADDR[6:0]	Register Name	Type	Width	Reset Value	Description
0x22	RR15	R	8	0x0	Response Register15. Sixteenth byte of response from the MMC device.

5.27 Write Data Register

This register provides access to the Write FIFO. Writing to this register pushes the write data into the FIFO. The FIFO width is fixed at 32 bits. The FIFO depth is defined by the FIFO_DEPTH parameter at the time of instantiation.

Table 34 • **Write Data Register**

HADDR[6:0]	Register Name	Type	Width	Reset Value	Description
0x24	WDR	W	32	0x0	Write Data register. Data written to this register gets pushed into Write Data FIFO and is sent to the slave MMC device when a block write is performed.

Note: Only 32-bit operations should be performed on this register. Writing an 8- or 16-bit value to this register will have no effect.

5.28 Read Data Register

This register provides access to the Read FIFO. Reading from this register pops the read data from the FIFO. The FIFO width is fixed at 32 bits. The FIFO depth is defined by the FIFO_DEPTH parameter at the time of instantiation.

Table 35 • **Read Data Register**

HADDR[6:0]	Register Name	Type	Width	Reset Value	Description
0x28	RDR	R	32	0x0	Read Data register. Data read from this register gets popped from the Read Data FIFO. The Read Data FIFO is written with the data from the slave MMC device when a block read is performed.

Note: Only 32-bit operations should be performed on this register. Reading an 8- or 16-bit value from this register will neither return valid data nor empty the Read Data FIFO.

5.29 Interrupt Mask Register

The interrupt mask register is used to determine the interrupt status bits in the Interrupt Status register that trigger an interrupt. Table 36 shows the Interrupt Mask register.

Table 36 • **Interrupt Mask Register**

HADDR[6:0]	Register Name	Type	Width	Reset Value	Description
0x2C	IMR	R/W	8	0x0	This register determines the status bits that trigger an interrupt.

Table 37 • **Interrupt Mask Register Bit Definitions**

Bit(s)	Type	Name	Description
7	R/W	mskuer	When stauer is set, assert an interrupt.
6	R/W	msksbi	When stasbi is set, assert an interrupt.
5	R/W	msktbi	When statbi is set, assert an interrupt.
4	R/W	msktxi	When statxi is set, assert an interrupt.
3	R/W	mskrri	When starri is set, assert an interrupt.
2	R/W	mskcsi	When stacsi is set, assert an interrupt.
1	R/W	mskboi	When staboi is set, assert an interrupt.
0	R/W	mskbui	When stabui is set, assert an interrupt.

Note: All bits are active High unless otherwise indicated.

5.30 Single Block Interrupt Mask Register

The single block interrupt mask register is used to determine the status bits in the single block interrupt status register that trigger an interrupt. Table 38 shows the single block interrupt mask register.

Table 38 • **Single Block Interrupt Mask Register**

HADDR[6:0]	Register Name	Type	Width	Reset Value	Description
0x2D	SBIMR	R/W	8	0x0	This register determines the single block status bits that trigger an interrupt.

Table 39 • **Single Block Interrupt Mask Register Bit Definitions**

Bit(s)	Type	Name	Description
7	R/W	msksbwdatainfifoto	When stasbwdatainfifoto is set, assert an interrupt.
6	R/W	msksbwbusyto	When stasbwbusyto is set, assert an interrupt.
5	R/W	msksbwcrcstaerr	When stasbwcrcstaerr is set, assert an interrupt.
4	R/W	msksbrstperr	When stasbrstperr is set, assert an interrupt.
3	R/W	msksbrstto	When stasbrstto is set, assert an interrupt.

Table 39 • **Single Block Interrupt Mask Register Bit Definitions *(continued)***

Bit(s)	Type	Name	Description
2	R/W	msksbcrcerr	When stasbcrcerr is set, assert an interrupt.
1	R/W	msksbrdone	When stasbrdone is set, assert an interrupt.
0	R/W	msksbwdone	When stasbwdone is set, assert an interrupt.

Note: All bits are active High unless otherwise indicated.

5.31 Multiple Block Interrupt Mask Register

The multiple block interrupt mask register is used to determine the status bits in the multiple block interrupt status register that trigger an interrupt. Table 40 shows the multiple block interrupt mask register.

Table 40 • **Multiple Block Interrupt Mask Register**

HADDR[6:0]	Register Name	Type	Width	Reset Value	Description
0x2E	MBIMR	R/W	8	0x0	This register determines the multiple block status bits that trigger an interrupt.

Table 41 • Multiple Block Interrupt Mask Register Bit Definitions

Bit(s)	Type	Name	Description
7	R/W	mskmbwdatainfifoto	When stambwdatainfifoto is set, assert an interrupt.
6	R/W	mskmbwbusyto	When stambwbusyto is set, assert an interrupt.
5	R/W	mskmbwcrcstaerr	When stambwcrcstaerr is set, assert an interrupt.
4	R/W	mskmbrstperr	When stambrstperr is set, assert an interrupt.
3	R/W	mskmbrstto	When stambrstto is set, assert an interrupt.
2	R/W	mskmbcrcerr	When stambcrcerr is set, assert an interrupt.
1	R/W	mskmbrdone	When stambrdone is set, assert an interrupt.
0	R/W	mskmbwdone	When stambwdone is set, assert an interrupt.

Note: All bits are active High unless otherwise indicated.

5.32 Interrupt Status Register

The interrupt status register stores the current status and errors bits for the transactions performed. These bits are set regardless of the interrupt mask register. Table 42 describes the interrupt status register.

Table 42 • Interrupt Status Register

HADDR[6:0]	Register Name	Type	Width	Reset Value	Description
0x30	ISR	R	8	0x0	This register provides status and error flags of transactions.

Table 43 • Interrupt Status Register Bit Definitions

Bit(s)	Type	Name	Description
7	R	stauer	User error is detected. Write FIFO overrun or Read FIFO underrun error.
6	R	stasbi	Response start bit error detected or time-out error while waiting for a response.
5	R	statbi	Stop bit error is detected on response to command.
4	R	statxi	Transmit bit error is detected on response to command.
3	R	starri	Response to command received.
2	R	stacsi	Command sent.
1	R	staboi	Buffer overflow occurred. Read FIFO was full when more data attempted to be written into it during Block Read.
0	R	stabui	Underrun occurred. Write FIFO was empty when more data attempted to be sent during block write.

Note: All bits are active High unless otherwise indicated.

5.33 Single Block Interrupt Status Register

The single block interrupt status register provides the current status and error bits for single block read or write transactions performed. These bits are set regardless of the single block interrupt mask register.

Table 44 describes the single block interrupt status register.

Table 44 • **Single Block Interrupt Status Register**

HADDR[6:0]	Register Name	Type	Width	Reset Value	Description
0x31	SBISR	R	8	0x0	This register provides the status and error bits for single block read or write transactions.

Table 45 • **Single Block Interrupt Status Register Bit Definitions**

Bit(s)	Type	Name	Description
7	R	stasbwdatainfifoto	Single block Write FIFO timeout. Asserted when less than block length amount of data in the Write FIFO after the period defined in the DATOTO register at the start of a single block write transfer. Prevents Write FIFO underruns during single block write transfers.
6	R	stasbwbusyto	Single block write busy timeout. Set when eMMC slave device holds DAT0 low for longer than the period defined in DATATO register at the start of a single block write transfer. Indicates that the slave device is not ready to receive data.
5	R	stasbwcrcstaerr	Single block write CRC response error. Set when start bit of CRC Status frame not received within period defined in DATATO register or when no valid stop bit detected for CRC status frame.
4	R	stasbrstperr	Single Block Read Stop Error. Set when valid stop bit not detected on all active DATI lines.
3	R	stasbrstto	Single Block Read start time-out. Set when no incoming start-bit found on DATI for period defined in DATATO register.
2	R	stasbcrcerr	Single block read or write encountered CRC error.
1	R	stasbrdone	Single block read done.
0	R	stasbwdone	Single block write done.

Note: All bits are active High unless otherwise indicated.

5.34 Multiple Block Interrupt Status Register

The multiple block Interrupt status register provides the current status and error bits for multiple block read or write transactions performed. These bits are set regardless of the multiple block interrupt mask register. Table 46 describes the multiple block interrupt status register.

Table 46 • **Multiple Block Interrupt Status Register**

HADDR[6:0]	Register Name	Type	Width	Reset Value	Description
0x32	MBISR	R	8	0x0	This register provides the status and error bits for multiple block read or write transactions.

Table 47 • **Multiple Block Interrupt Status Register Bit Definitions**

Bit(s)	Type	Name	Description
7	R	stambwdatainfifoto	Multiple block Write FIFO timeout. Asserted when less than block length amount of data in the Write FIFO after the period defined in the DATOTO register at the start of a block within a multiple block write transfer. Prevents Write FIFO underruns during Multiple block write transfers.
6	R	stambwbusyto	Multiple block write busy timeout. Set when eMMC slave device holds DAT0 low for longer than the period defined in DATATO register at the start of a block within a multiple block write transfer. Indicates that the slave device is not ready to receive data.
5	R	stambwcrcstaerr	Multiple block write CRC response error. Set when start bit of CRC Status frame not received within period defined in DATATO register or when no valid stop bit detected for CRC status frame for a block within a multiple block write transfer.
4	R	stambrstperr	Multiple Block Read Stop Error. Set when valid stop bit not detected on all active DATI lines for a block within a multiple block read transfer.
3	R	stambrstto	Multiple Block Read start time-out. Set when no incoming start-bit found on DAT for period defined in DATATO register for a block within a multiple block read transfer.
2	R	stambcrcerr	Multiple block read or write encountered CRC error.
1	R	stambrdone	Multiple block read done.
0	R	stambwdone	Multiple block write done.

Note: All bits are active High unless otherwise indicated.

5.35 Interrupt Clear Register

The interrupt clear register is a write-only register used to clear (individually) the ISR bits described in Table 43.This can clear an interrupt, if the associated bit is set in the interrupt mask register. Table 48 describes the interrupt clear register.

Table 48 • **Interrupt Clear Register**

HADDR[6:0]	Register Name	Type	Width	Reset Value	Description
0x34	ICR	W	8	0x0	This register clears (individually) the corresponding bit in the interrupt status register described in Table 42.

Table 49 • **Interrupt Clear Register Bit Definitions**

Bit(s)	Type	Name	Description
7	W	clruer	Clear stauer bit
6	W	clrsbi	Clear stasbi bit
5	W	clrtbi	Clear statbi bit
4	W	clrtxi	Clear statxi bit
3	W	clrrri	Clear starri bit
2	W	clrcsi	Clear stacsi bit
1	W	clrboi	Clear staboi bit
0	W	clrbui	Clear stabui bit

Note: All bits are active High unless otherwise indicated.

5.36 Single Block Interrupt Clear Register

The single block interrupt clear register is a write-only register used to clear (individually) the single block interrupt status register bits described in Table 45. This can clear an interrupt if the associated bit is set in the single block interrupt mask register. Table 53 describes the single block interrupt clear register.

Table 50 • **Single Block Interrupt Clear Register**

HADDR[6:0]	Register Name	Type	Width	Reset Value	Description
0x35	SBICR	W	8	0x0	Single block interrupt clear register. This register clears (individually) the corresponding bit in the single block interrupt status register described in Table 44.

Table 51 • **Single Block Interrupt Clear Register Bit Definitions**

Bit(s)	Type	Name	Description
7	W	clrsbwdatainfifoto	Clear stasbwdatainfifoto bit
6	W	clrsbwbusyto	Clear stasbwbusyto bit
5	W	clrsbwcrcstaerr	Clear stasbwcrcstaerr bit
4	W	clrsbrstperr	Clear stasbrstperr bit
3	W	clrsbrstto	Clear stasbrstto bit
2	W	clrsbcrcerr	Clear stasbcrcerr bit
1	W	clrsbrdone	Clear stasbrdone bit
0	W	clrsbwdone	Clear stasbwdone bit

Note: All bits are active High unless otherwise indicated.

5.37 Multiple Block Interrupt Clear Register

The multiple block interrupt clear register is a write-only register used to clear (individually) the multiple block interrupt status register bits described in Table 47. This can clear an interrupt if the associated bit is set in the multiple block interrupt mask register. Table 52 describes the multiple block interrupt clear register.

Table 52 • **Multiple Block Interrupt Clear Register**

HADDR[6:0]	Register Name	Type	Width	Reset Value	Description
0x36	MBICR	W	8	0x0	Multiple block interrupt clear register. This register clears (individually) the corresponding bit in the multiple block interrupt status register described in Table 46.

Table 53 • **Multiple Block Interrupt Clear Register Bit Definitions**

Bit(s)	Type	Name	Description
7	W	clrmbwdatainfifoto	Clear stambwdatainfifoto bit
6	W	clrmbwbusyto	Clear stambwbusyto bit
5	W	clrmbwcrcstaerr	Clear stambwcrcstaerr bit
4	W	clrmbrstperr	Clear stambrstperr bit
3	W	clrmbrstto	Clear stambrstto bit
2	W	clrmbcrcerr	Clear stambcrcerr bit
1	W	clrmbrdone	Clear stambrdone bit
0	W	clrmbwdone	Clear stambwdone bit

Note: All bits are active High unless otherwise indicated.

5.38 Control Register

The Control register provides the control bits to define the operation of the core and to drive hardware pins to the eMMC slave device. Table 54 describes the control register.

Table 54 • **Control Register**

HADDR[6:0]	Register Name	Type	Width	Reset Value	Description
0x38	CTRL	R/W	8	0x0C	This register provides the control bits for the operation of the core.

Table 55 • **Control Register Bit Definitions**

Bit(s)	Type	Name	Description
7	R	Busy	Slave device is indicating that it is busy by asserting DAT[0] low.
6	R	-	Reserved.
5	W	fiforeset	FIFO reset. Used to initialize the address pointers and flags in the Read and Write FIFOs back to default values.
4	R/W	cmdFrcLow	Force CMD line to 0 (low). Used for boot operation.
3	R	midle	MMC Idle. When set to 1, it indicates that the core is in Idle state (not sending command, or expecting response). This bit does not reflect when the core is transmitting/receiving data.
2	R/W	clkoe	CLK Output Enable. Enables CLK or disables it to allow the slave device to enter Low-power mode.
1	R/W	slrst	Slave Reset. When set, it applies a reset to the eMMC slave device through RST_N pin.
0	R/W	swrst	Software Reset. When set, it holds core in reset state and asserts RST_N pin Low.

Note: All bits are active High unless otherwise indicated.

5.39 Single Block Control and Status Register

The single block control and status register provides control of single block read and write transactions and associated status bits from these operations. Table 56 describes the single block control and status register.

Table 56 • **Single Block Control and Status Register**

HADDR[6:0]	Register Name	Type	Width	Reset Value	Description
0x39	SBCSR	R/W	8	0x0	This register provides control and status bits for single block reads and writes.

Table 57 • **Single Block Control and Status Register Bit Definitions**

Bit(s)	Type	Name	Description
7	R	-	Reserved.
6:4	R	sbwst	Single Block Write Status - CRC Status bits. Updated when either stasbwdone, stasbcrcerr or stasbwcrcstaerr set for single block write transfers. (Good CRC Status results = 010)
3	R	sbcrcerr	Single Block CRC Error. Set when sbwdone or sbrdone asserted, if CRC error detected. Cleared by writing 1 to clrsbcrcerr in Single Block Interrupt Clear register.
2	R	sbdone	Single Block Done. Cleared when single block write or read start is set (sbwstrt or sbrstrt). Set by hardware when Single Block Write or Read is completed.
1	R/W	sbrstrt	Single Block Read Start. Initiates the read of a block of the length defined in the Block Length register from the eMMC slave device. Only held set for 1 HCLK period.
0	R/W	sbwstrt	Single Block Write Start. Initiates the write of a block of the length defined in Block Length register to the eMMC slave device. Only held set for 1 HCLK period.

Note: All bits are active High unless otherwise indicated.

5.40 Multiple Block Control and Status Register

The multiple block control and status register provides control of multiple block read and write transactions and associated status bits from these operations. Table 58 describes the multiple block control and status register.

Table 58 • **Multiple Block Control and Status Register**

HADDR[6:0]	Register Name	Type	Width	Reset Value	Description
0x3A	MBCSR	R/W	8	0x0	This register provides control and status bits for multiple block reads and writes.

Table 59 • **Multiple Block Control and Status Register Bit Definitions**

Bit(s)	Type	Name	Description
7	R	-	Reserved.
6:4	R	mbwst	Multiple Block Write Status - CRC Status bits. Updated when either stambwdone, stambcrcerr or stambwcrcstaerr set for multiple block write transfer. (Good CRC Status results = 010)
3	R	mbcrcerr	Multiple Block CRC Error. Set when mbwdone or mbrdone asserted, if CRC error detected. Cleared by writing 1 to clrmbcrcerr in the Multiple Block Interrupt Clear register.
2	R	mbdone	Multiple Block Done. Cleared when multiple block write or read start is set (mbwstrt or mbrstrt). Set by hardware when Multiple Block Write or Read is completed.
1	R/W	mbrstrt	Multiple Block Read Start. Initiates a multiple block read of number of blocks defined in the Block Count register, with the number of bytes per block as per Block Length register. Only held set for 1 HCLK period.
0	R/W	mbwstrt	Multiple Block Write Start. Initiates a multiple block write of number of blocks defined in the Block Count register, with the number of bytes per block as per Block Length register. Only held set for 1 HCLK period.

Note: All bits are active High unless otherwise indicated.

5.41 Response Timeout Register

This register defines the number of clock ticks of HCLK, that the core waits for a response from the slave device after it has issued a command before timing out and setting the stasbi bit in the interrupt status register.

Table 60 • **Response Timeout Register**

HADDR[6:0]	Register Name	Type	Width	Reset Value	Description
0x3C	RSPTO	R/W	8	0x40	Length of time (in HCLK ticks) that core waits for a response from the slave device.

5.42 Data Timeout Register

This register provides the number of clock ticks of HCLK, that the core waits for under the following circumstances:

- Single/Multiple block write
  - Slave to indicate that it's idle by releasing DAT[0] (high), before timing out and setting either the stasbwbusyto bit in the SBISR or the stambwbusyto bit in the MBISR.
  - User to load at least a block length amount of data into the Write FIFO before timing out and setting either the stasbwdatainfifoto bit in the SBISR or the stambwdatainfifoto bit in the MBISR. The timeout guards against the occurrence of write underruns during single/multiple block write transfers.
- Single/Multiple block read
  - Slave to load a valid start bit onto to the data bus before timing out and setting either the stasbrstto bit in the SBISR or the stambrstto bit in the MBISR.

Table 61 • **Data Timeout Register**

HADDR[6:0]	Register Name	Type	Width	Reset Value	Description
0x40	DATATO	R/W	32	0x400	Length of time (in HCLK ticks) that core waits for, for the cases mentioned in the Data Timeout Register description above.

5.43 Block Length Register

This register specifies the length in bytes of data blocks to the core. This register must be written before initiating single or multiple block write and read transfers.

Note: The block length must be specified to the eMMC slave device through a user initiated command and response sequence. Writing to this register does not specify the block length to the eMMC slave.

Table 62 • **Block Length Register**

HADDR[6:0]	Register Name	Type	Width	Reset Value	Description
0x44	BlockLen	R/W	16	0x200	Sets the length in bytes of data blocks used for single or multiple block write and read transfers.

5.44 Data Control Register

The register defines the number of DAT bus bits that the core drives/samples during data transfers. This register must be defined by the user before initiating data transfers. This is a separate action from setting the MMC_DWIDTH parameter at the time of instantiation but is dependent upon the MMC_DWIDTH value set at the time of instantiation. For instance, the core may have been instantiated with a 4-bit MMC DAT width but operationally may be set to drive/sample 1-bit of the DAT bus. In this instance, the core can also be configured to drive/sample 4-bits (via dsize), but cannot be configured to drive/sample 8-bits.

Table 63 • **Data Control Register**

HADDR[6:0]	Register Name	Type	Width	Reset Value	Description
0x48	DCTRL	R/W	8	0x00	Data Control - defines size of active bits of DAT.

Table 64 • **Data Control Register Bit Definitions**

Bit(s)	Type	Name	Description
7:2	R	-	Reserved
1:0	R/W	dsize	DAT Size - number of active DAT bits. User cannot select a size greater than the size instantiated in the core, specified via MMC_DWIDTH. dsize coding is as follows: 00 - 1-bit 01: 4-bit (Only available for MMC_DWIDTH = 4-bit or 8-bit) 10: 8-bit (Only available for MMC_DWIDTH = 8-bit) 11: reserved

Note: All bits are active High unless otherwise indicated.

5.45 Clock Register

This register defines the period for the CLK pin (MMC interface clock). The value of CLKHP defines the half clock period for the CLK.

A suitable value needs to be written to this register initially before any commands are sent to the eMMC slave to generate a ~400 KHz MMC clock from the HCLK input (as per the initialization clock frequency defined in the JEDEC specification).

After the initialization command-response sequences are completed with the eMMC slave device, the user can initiate a SWITCH command to inform the eMMC slave device to change over to high-speed mode. A new value can then be written to this register to derive the desired run-time MMC interface clock frequency.

To achieve maximum overall system throughput, depending on the application, it may be beneficial to ensure that the processor controlling CoreMMC is running at its maximum operating frequency (along with HCLK). Choose the CLKHP value based on this such that the MMC interface clock is running as close as possible to the 52 MHz maximum as defined in the *JEDEC eMMC 4.41 Standard Specification* document, as the overall system throughput is impacted by the AHB bandwidth.

Note: The default value set in this register is sufficient to derive a 400 KHz initialization MMC interface clock from a 50 MHz HCLK input. If the HCLK input differs from 50 MHz, a suitable value must be written to this register before performing any command-response transactions with the eMMC slave device.

Table 65 • **Clock Register**

HADDR[6:0]	Register Name	Type	Width	Reset Value	Description
0x4C	CLKR	RW	8	0x3f	Clock Register - defines half period of CLK signal.

Table 66 • Clock Register Bit Definitions

Bit(s)	Type	Name	Description
7:0	R/W	CLKHP	CLK Half Period - defines the half period of the MMC interface clock (CLK), where the frequency of CLK is defined by the formula: $f_{CLK} = \frac{f_{HCLK}}{2(CLKHP + 1)}$ Example CLKHP values and the resultant CLK generated: CLKHP CLK 00: HCLK/2 01: HCLK/4 02: HCLK/6 03: HCLK/8 04: HCLK/10 … 255: HCLK/512

Note: The maximum CLK operating frequency is HCLK/2 to support the 3 ns hold time of the MMC interface defined in the *JEDEC eMMC 4.41 Standard Specification* document. Data is loaded onto the bus by CoreMMC 1 HCLK cycle after the rising edge of CLK - Hold time is therefore equal to the period of HCLK.

5.46 Block Count Register

This register specifies the number of blocks in a multiple block transfer to the core. This register must be written to before initiating multiple block write or read transfers.

Note: The block count must be specified to the eMMC slave device through a user initiated command and response sequence. Writing to this register does not specify the block count to the eMMC slave.

Table 67 • Block Count Register

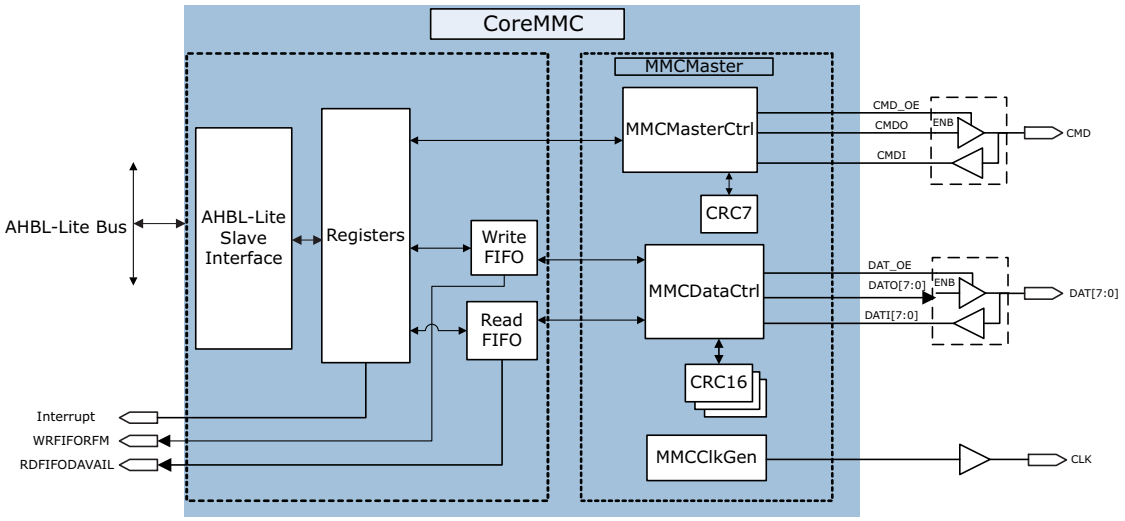
HADDR[6:0]	Register Name	Type	Width	Reset Value	Description
0x50	BlockCnt	R/W	16	0x00	Specifies the number of blocks in a multiple block transfer.

6 Design Details

6.1 System Overview

The CoreMMC provides a slave AHB-Lite interface and a master MMC interface. The AHB-Lite interface provides the slave interface for a host to access the control and status registers in the core and to initiate transactions to an MMC slave device connected to the MMC master interface. Additionally, FIFO status signals are provided to the PDMA. Figure 2 shows the top-level block diagram.

Figure 2 • **CoreMMC Block Diagram**



6.2 Functional Description of the MMC Controller

This section describes the components of the CoreMMC controller and how the controller operates. The following are the primary functional blocks:

- AHB-Lite slave interface
- Registers
- Write FIFO
- Read FIFO
- MMC master

6.2.1 AHB-Lite Slave Interface

The AHB-Lite slave interface provides the functionality to interface to an AHB-Lite master as defined in the AMBA 3 AHB-Lite Protocol. This slave interface supports 8-/16-/32-bit access, as defined by HSIZE. Sequential transfers are not supported.

6.2.2 Registers

The register block decodes the address of access from AHB-Lite slave and performs the requested read or write operation. It also latches status and error flags from the MMC master as it executes and controls the reading or writing of Read or Write FIFOs by the host.

6.2.3 Write FIFO

The Write FIFO provides storage for block writes to the MMC slave device. The host writes the data into the FIFO, and the MMC master block reads the data out during write transactions on MMC DAT lines. The Write FIFO can contain multiple blocks of data to write (depends on the size of the core instantiated). The Write FIFO detects overruns of excess data writes into it from the host, and underrun errors of attempting to read an empty FIFO by the MMC master and sets associated bits in the register block.

6.2.4 Read FIFO

The Read FIFO provides storage for block reads from the MMC slave device. The MMC master block writes the data into the FIFO, and the AHB-Lite slave block reads the data out. The Read FIFO can contain multiple blocks of data to read (depends on the size of the core instantiated). The Read FIFO detects overruns of excess data writes into it from the MMC master block and underrun errors of attempting to read an empty FIFO by the AHB-Lite slave block and sets associated bits in the register block.

6.2.5 MMC Master

The MMC master implements transactions on the MMC bus as defined in the *JEDEC eMMC 4.41 Standard Specification* document, under the direction of the host. It is composed of the following primary blocks:

- MMC master controller: Controls command-response transactions on the CMD pins. It drives out the command based on CR0-CR5 and checks and stores the expected response in RR0-RR15.
- MMC data controller: Controls the write block and read block transactions on DAT pins. Indicates to the MMC master controller when the slave is busy (that is when DAT0 is held low).
- CRC7: Provides CRC7 computation for command-response on CMD.
- CRC16: Provides CRC16 for data transactions on DAT pin(s). There can be multiple CRC16 blocks in the core depending on the MMC_DWIDTH specified (one per pin).
- Clock Generator: Generates the CLK signal from HCLK based on the configuration.

The MMC master implements the MMC bus protocol as defined in the *JEDEC eMMC 4.41 Standard Specification* document.

6.2.5.1 MMC Protocol

Each MMC bus operation consists of a command (host to device), response (device to host), and a possible data transfer. Commands are well-defined 48-bit tokens. Responses are either 48 bits or 136 bits. Both commands and responses are protected by 7-bit CRC headers generated by CoreMMC. Data packets are fixed at the block length * 8 (for single data bus width), block length * 2 (for 4-bit data bus width), or block length (for 8-bit data bus width). Data packets are protected by 16-bit CRC headers generated by CoreMMC.

The MMC protocol is based on command and data bitstreams that are initiated by a start bit and terminated by a stop bit. Additionally, the MMC controller provides a reference clock and is the only master interface that can initiate a transaction.

- Command: A token transmitted serially on the CMD pin that starts an operation.
- Response: A token from the card transmitted serially on the CMD pin in response to certain commands.
- Data: Transferred serially using the data pins for data movement commands.

All transactions are controlled by the host. The host configures the CoreMMC and the attached slave device such as configuring the number of DAT bits to be used (1, 4, or 8) or setting the block length for read and write transactions. All communications to the attached MMC slave device are performed using commands and responses as defined in the *JEDEC eMMC 4.41 Standard Specification* document. This communication uses the command and response registers in the core.

6.2.5.2 Operating Modes

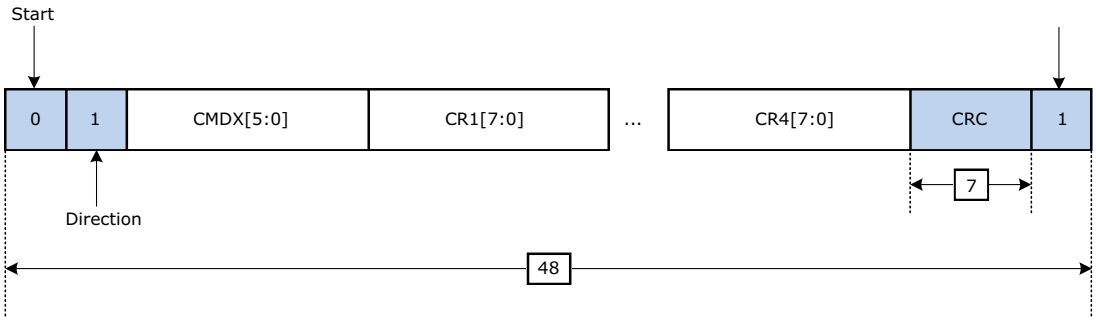
There are five operation modes as defined in the MMC 4.41 standard in the *JEDEC eMMC 4.41 Standard Specification* document.

- Boot mode: The MMC device is in the state immediately following either one of these three conditions: power-cycle, hardware reset (using RST signals), or CMD0 transmission with argument 0xF0F0F0F0. Refer to the AMBA 3 AHB-Lite Protocol for a full list of eMMC commands and their usage. This mode is not currently supported.
- Card Identification mode: After booting, the MMC device is in Card Identification mode until the set_RCA command (CMD3) is received from the host (CoreMMC).
- Interrupt mode: This mode allows the MMC device to interrupt the host (CoreMMC) and indicate that data is ready to be transmitted; this is an optional feature and is not implemented in this version of CoreMMC.
- Data Transfer mode: This is the default mode for the MMC, after an RCA has been assigned to it after the Card Identification mode. Data transfer commands can be issued from this state.
- Inactive mode: The MMC device enters into inactive mode, if the operating voltage range or access mode is not valid or CMD15 (GO_INACTIVE_STATE command) is received.

6.2.5.3 Command Registers

These registers store the command data to be transmitted from CoreMMC to the slave device and sent on the CMD pin. The CMD data consists of 38 bits of data (48 bits, minus 1 start bit, 1 stop bit, 1 direction bit, and 7 CRC bits). Figure 3 shows the full MMC command.

Figure 3 • **Command Register use in MMC Command Token**



The Command registers send the most-significant bit first to the CMDO pin. CR0 is defined as the command index register. These are the 6 bits that define the type of command for the slave. Registers CMD1 to CMD4 define the arguments for the command.

Writing to CR4 (command register 4) also initiates a command from the host to the slave with the command data currently present in CR0-CR4, when possible the slave may hold the bus by pulling CMD low. The command registers CR0-CR4 should be written in sequence. CR1-CR4 can be written together as a 32-bit word that causes the command transaction to be initiated. Similarly, a 16-bit half-word write to CR3-CR4 also initiates the command transaction as well as a byte write to CR4.

6.2.5.4 Response Registers

The CoreMMC response registers (RR0 - RR 15) are used to store and return a response to the host from the MMC slave device. This is a 38-bit value unless the response is R2, which is the CID or CSD register of the MMC device and is 128 bits long (that is, 138 minus 1 stop bit, 1 start bit, 1 transmission bit, and 7 CRC bits). Beyond the size difference for R2 responses, the formats of the response registers are the same as the command registers. The response data is stripped off the 7 CRC bits and stored in these read-only registers after each response.

For a 38-bit response (any response other than R2), only the first 6 registers (RR0-RR5) are updated. RR5 has the CRC and stop-bit from the received response stored to aid debugging (that is, RR5[7:0] = {CRC[6:0], Stop-Bit}). The unused response registers are zeroed out.

After each response, the stored data is overwritten. If this data is required, it can be read back after each operation. The response registers are cleared when a command is initiated and are set when srri is set. The response registers maintain their values until another command is initiated.

6.2.5.5 Multiple Block Writes

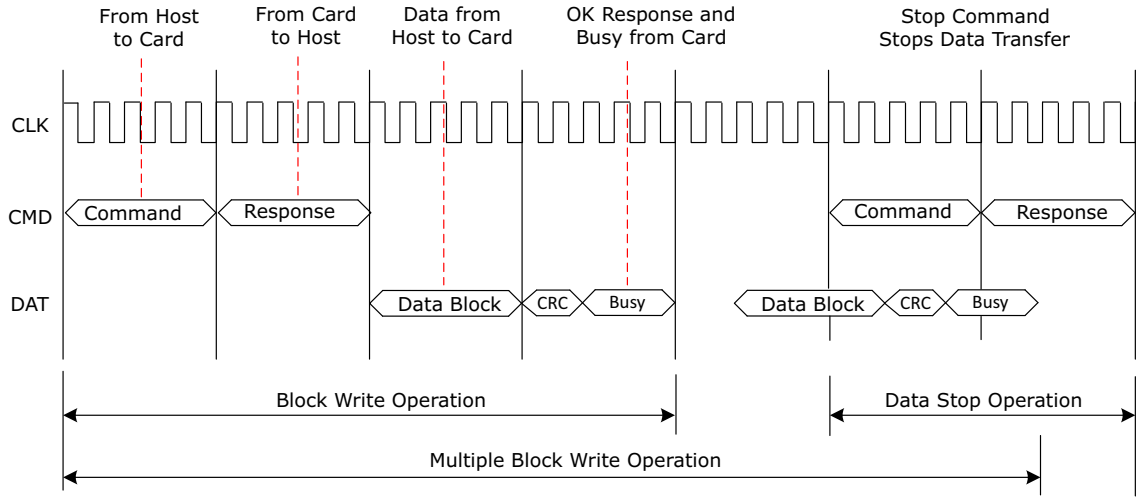
The host can send multiple blocks with two command-response transactions. The host must specify the number of blocks in the multiple blocks write transfer to CoreMMC via the block count register and to the eMMC slave device by issuing CMD23. If the block size differs from that already defined in the block length register then the register needs to be updated with the new block length and the slave notified of the new block length by issuing CMD16.

The host must fill the Write FIFO with the transfer size amount of data (to avoid an underrun situation) or fill the FIFO completely depending upon if the transfer is larger than the FIFO size instantiated. For interrupt driven operation, the host must set the mask accordingly in the MBIMR and IMR registers, generate interrupt off multiple blocks write related status and error bits, and issue CMD25 through the command registers. The host must set the mbwstrt bit in the multiple block control and status registers.

The mbwdone bit is asserted in the MBISR when the transfer is complete. When this fails, if an error occurs, an interrupt is generated off one of the multiple blocks write related error bits in the MBISR or the ISR. Write FIFO underrun must not occur because of the data in FIFO timeout logic as the start bit of the next block in a multi block transfer loads out onto DAT when there is sufficient data to complete the transfer of this block in the Write FIFO.

Note: A suitable value needs to be specified to the DATATO register to ensure that host is allowed sufficient time to load data into the Write FIFO and also to allow the slave device being slow to respond with CRC status, or while the slave is performing background operations indicated by DAT0 being held low for extended periods (typically writing to Flash).

Figure 4 • **Multiple Block Write Operation**



Note: The clock is representative and does not show the exact number of clock cycles for the full transaction.

6.2.5.6 Multiple Block Reads

The host must ensure that the number of bytes to be received from the slave device can be held in the Read FIFO (to ensure no overrun on writes of data into FIFO from the MMC bus). The host can clear the content of the Read FIFO by setting the FIFO reset bit in the control register, which clears the contents of the write FIFO also. This resets the FIFO flags and status bits.

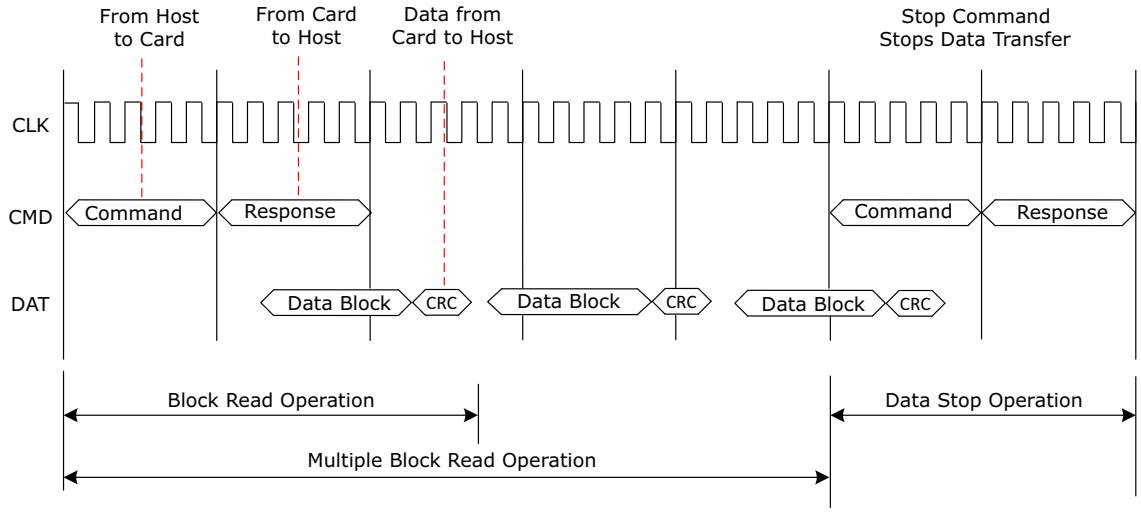
The host must specify the number of blocks in the multiple block read transfer to CoreMMC via the block count register and to the eMMC slave device by issuing CMD23. If the block size differs from that already defined in the block length register then the register needs to be updated with the new block length and the slave notified of the new block length by issuing CMD16.

The host needs to set the mbrstrt bit in the MBCSR to inform CoreMMC to get ready to receive multiple blocks of data from the eMMC slave device. The host must issue CMD18 to the slave device, which kicks off the multi block transfer from the slave.

The mbrdone bit is asserted in the MBISR when the transfer is complete. When this fails, if an error occurs, an interrupt is generated off one of the multiple blocks read related error bits in the MBISR or the ISR. To prevent the occurrence of Read FIFO overruns, ensure that the total multiple block transfer can be contained in the Read FIFO instantiated.

Note: A suitable value needs to be specified to the DATATO register to ensure that the host allows the slave to respond with the start bit of the next block within the multiple block transfer. This can be a significantly large delay. Refer to the eMMC slave device manufacturer's documentation denoted by NAC cycles in the *JEDEC eMMC 4.41 Standard Specification* document.

Figure 5 • **Multiple Block Read Operation**



6.2.5.7 AHB-Lite Interface Timing

Figure 6 and Figure 7 show typical write cycle and read cycle timing relationships relative to the system clock, HCLK.

Figure 6 • **AHB-Lite Read Transfer**

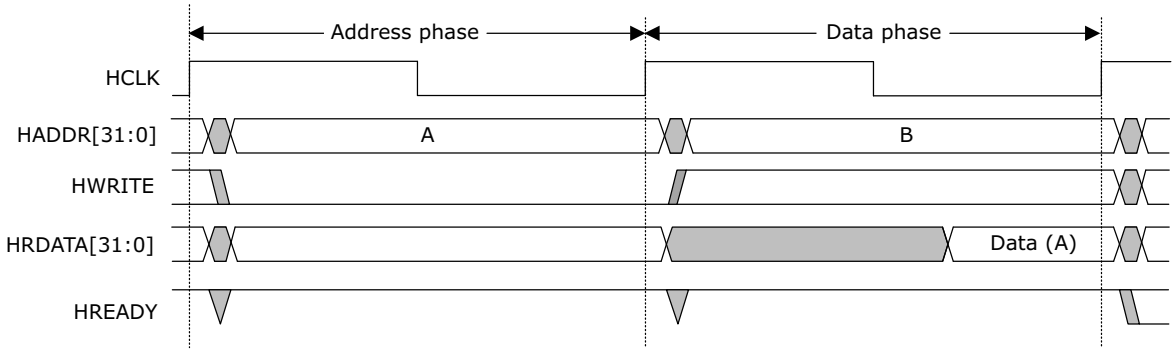
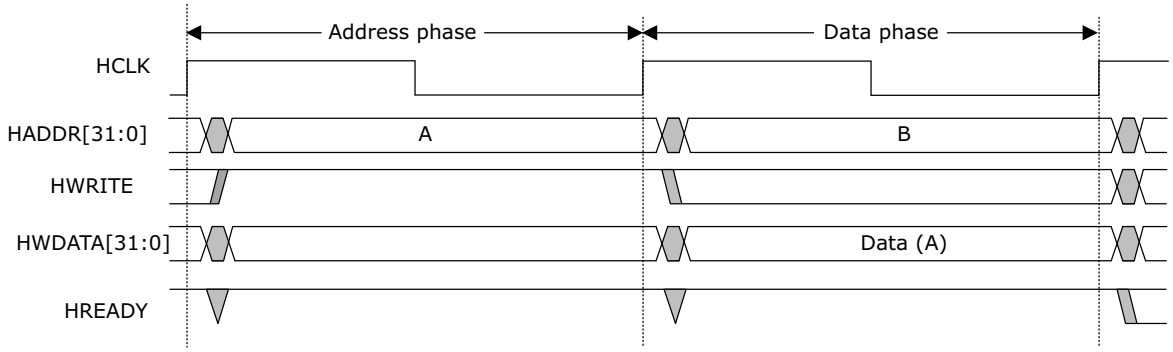


Figure 7 • **AHB-Lite Write Transfer**



6.2.5.8 Programming Example

An example sequence on programming an eMMC device is shown in the following steps. It is a basic sequence to program the SanDisk SDIN5C2-8G part on the Microsemi SmartFusion2 Development Kit to perform basic reads and writes.

Note: By default the reset_n is not operational and boot mode not available (by JEDEC spec). The eMMC chip powers up into Idle state.

1. CMD0 0x0: // move to idle state.
2. CMD1 0x40_00_00_80: // read OCR
3. Check response has busy bit High (no Busy), that is, Response 0xC0_FF_80_80 (FF_80 voltage ranges) – when ready not Busy, eMMC moves into Ready state.
4. CMD2 0xFF_FF_FF_FF: // read CID

   Response R0-R15 - 45, 1, 0, 53, 45, 4d, 30, 38, 47. 90, 52, E7, 9B, 6, BF, 1
5. CMD3 0x0001_FFFF: // set RCA – Relative Card Address

   Response CMD3, Card Status[31:0] - 0x00_00_05_00; // no errors, in Indent state
6. CMD9 0x0001_FFFF: // Send_CSD – get card specific data

   Response R0-15 - D0, 0F, 00, 32, 0F, 59, 03, FF, FF, FF, FF, FF, 92, 40, 40, 11

   Vers code in EXT_CSD, Version 4.1-4.2-4.3, 10ms
7. CMD7 0x0001_FFFF: // Go to transfer state

   Response R0-R4 - 7, 00, 00, 07, 00
8. CMD16 0x4: // Set_BlockLen - setting to 4 bytes

   Response R0-R4 - 0x10, 00,00,09, 00
9. CMD17 0x0: // Read_Single_Block

   Response R0-R4 – 0x11, 20, 00, 09, 00 - block length error (example of an error when block length is not supported by the device)
10. CMD16 0x200: // Set_BlockLen – 512 bytes

    Response R0-R4 - 0x10, 00,00,09, 00
11. CMD6 0x03B7_0200: // set EXT_CSD 8-bit width data

    Response R0-R4 - 0x6, 00,00,08, 00 - note bit[8] in status indicates not ready

Note: Core must have MMC_DWIDTH parameter set to 2'b11 and register Data Control Register must have dsize=2'b10 – that is, all most support 8-bit DAT bus.

12. CMD13 0x0001_fffe: // Send_Status from card 1

    Response R0-R4 - 0xD, 00,00,09, 00 - bit[8] in status indicates ready
13. CMD24 0x0:L: // Write_Single_Block, sector 0x0

    Response R0-R4 – 0x18, 00, 00, 09, 00 - no error – in Trans state
14. CMD17 0x0: // Read_Single_Block

    Response R0-R4 – 0x11, 00, 00, 09, 00 - no error – in Trans state

To verify the correct operation, Read Data from the block read in RDR can be compared with the data written in block write.

7 Tools Flows

7.1 Licensing

No license is required for this core.

7.1.1 RTL

Complete RTL source code is provided for the core and testbenches.

7.2 SmartDesign

CoreMMC is pre-installed in the SmartDesign IP Deployment design environment. Figure 8 shows configuring the core using the configuration GUI within the SmartDesign.

To know how to create SmartDesign project using the IP cores, refer to *Libero SoC documents page* and use the latest SmartDesign user guide.

Figure 8 • **CoreMMC I/O View**

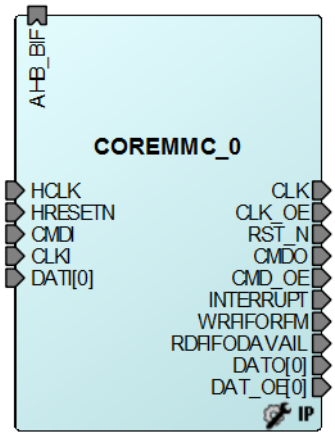
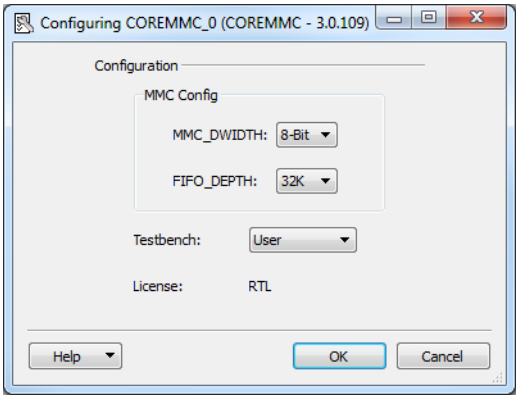


Figure 9 • **CoreMMC SmartDesign Configuration with Associated Parameters**



7.3 Simulation Flows

The user testbench for CoreMMC is included in all releases.

To run simulations, select the User Testbench flow within SmartDesign and click **Save** and generate on the **Generate pane**. The user testbench is selected through the Core testbench configuration GUI.

When SmartDesign generates the Libero SoC project, it installs the user testbench files.

To run the user testbench, set the design route to the CoreMMC instantiation in the Libero SoC design hierarchy pane and click **Simulation** in the Libero SoC design flow window. This invokes ModelSim® and automatically runs the simulation.

7.3.1 User Testbench

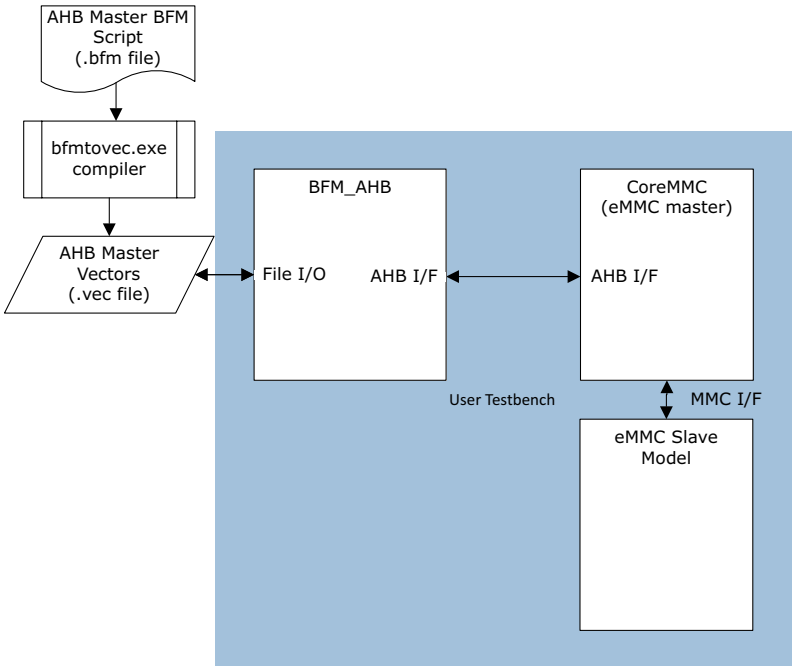
Figure 10 shows the hierarchal structure of the CoreMMC simulation testbench, which includes an instance of CoreMMC, an eMMC slave model, and a BFM AHB master.

User tests are defined in the user_tb.bfm script, which is compiled into a vector file and passed via a parameter to the BFM AHB master. The BFM master emulates the operation of an AHB master controlling CoreMMC to communicate with an eMMC slave. The user_tb.bfm script packaged along with CoreMMC performs single and multiple block read and write transactions with the eMMC slave. An extensive set of procedures are defined in the user_tb.bfm script, which demonstrates the intended flow for AHB master controlling CoreMMC. The calls to these procedures in the user_tb.bfm script can be modified to generate custom simulation cases if required.

The eMMC slave model is a primitive model of an eMMC slave device with basic support functionality for a limited set of eMMC commands such as 6, 16, 17, 18, 23, 24, 25, and single and multiple block data transfers with 16 addressable 512-byte sectors.

Note: Support for SWITCH command (CMD6) is only implemented for writing to the DATA_WIDTH segment [183] of the EXT_CSD for configuring the number of DAT bits that the eMMC slave model actively drives/samples.

Figure 10 • **CoreMMC User Testbench**



7.4 Synthesis in Libero SoC

After setting the design root appropriately for your design, follow these steps to run the Synthesis:

1. Click **Synthesis** in the Libero SoC software. The **Synthesis** window appears, displaying the Synplicity® project.
2. Set Synplicity to use the Verilog 2001 standard, if Verilog is used.
3. Click **Run** to run the Synthesis.

7.5 Place-and-Route in Libero SoC

After setting the design route appropriately for your design, and running Synthesis, click **Layout** in the Libero SoC software to invoke Designer. CoreMMC requires no special place-and-route settings.