

CorePWM v4.1

Handbook

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Table of Contents

Introduction	5
Core Overview	5
Supported Families	5
Core Version	6
Supported Interfaces	6
Utilization and Performance	6
1 Design Description	11
Functional Blocks	11
I/O Signals	12
Register Map	15
Configuration Example	21
APB Interface Timing	24
2 Tool Flows	25
SmartDesign	25
Importing into Libero IDE	27
Simulation Flows	27
Synthesis in the Libero IDE	28
Place-and-Route in Libero IDE	28
3 Example Applications	29
General Purpose PWM Application – Temperature Monitor	29
DAC	29
4 Software Driver	33
A List of Document Changes	35
B Product Support	37
Customer Service	37
Actel Customer Technical Support Center	37
Actel Technical Support	37
Website	37
Contacting the Customer Technical Support Center	37
Index	39

Introduction

Core Overview

Intended Use

CorePWM is a general purpose, multi-channel pulse width modulator (PWM) module for motor control, tone generation, battery charging, heating elements, and more.

In General Purpose PWM mode, duty cycle updates can be performed asynchronously or synchronously, based on parameter selection. In synchronous mode, all channels are updated at the beginning of the PWM period, which is useful for motor control and can be used to keep a constant dead band space between channel waveforms. Asynchronous mode is relevant to applications such as LED control, where synchronous updates are not required. Asynchronous mode lowers the area size, reducing shadow register requirements.

In addition to the general purpose PWM modes, there is a "Low Ripple DAC" mode that creates a minimum period pulse train whose High/Low average is that of the chosen duty cycle. When used with a low-pass filter (such as a simple RC circuit), a DAC can be created with far better bandwidth and ripple performance than a standard PWM algorithm can achieve. This type of DAC is ideally suited for fine tuning of power supply output levels.

CorePWM also provides support for tachometer monitoring of 3- and 4-wire fans. Incoming tachometer data is read by the firmware through the APB interface to calculate fan speed.

Key Features

- Configuration updates for all channels can be synchronized to the beginning of the PWM period, allowing precise updates and maintaining phase alignments between channels
- Configurable resolution based on the APB bus width
- Low-cost PWM solution with up to 16 separate PWM digital outputs, configurable via a register interface
- For DAC applications: Optional, per-channel Low Ripple DAC mode, allowing for greater resolution output of a given filter
- Low-cost TACHOMETER solution with up to 16 separate TACH digital inputs, configurable via a register interface
- All PWM outputs are double-edge-controlled
- Per-channel fixed register option for lower tile count
- Edge control based on a configurable PWM period with prescaler value and 0% to 100% duty cycle capability
- Set High, set Low, and Toggle Edge-Control modes
- Can be programmed on-the-fly from a microcontroller, such as Core8051s, CoreABC
- Can be used to perform open or closed-loop margining of power supplies

Supported Families

- IGLOO[®]/e
- ProASIC[®]3/E/L
- Fusion
- ProASIC^{PLUS}[®]
- Axcelerator[®]
- RTAX-S
- RTAX-DSP

Core Version

This handbook supports CorePWM version 4.1.

Supported Interfaces

CorePWM is available with an APB interface, which is described in the “APB Interface Timing” section on page 24.

Utilization and Performance

CorePWM has been implemented in several of Actel’s device families. A summary of various implementation data is listed in the following tables (using standard speed grades).

As shown in Table 1 through Table 8 on page 9, it is recommended to fix all registers that are not used, via parameters, to ensure optimal synthesis tile reduction.

Table 1 · CorePWM Device Utilization and Performance (one 8-bit DAC channel configuration)

Family	Tiles			Utilization		Performance (MHz)
	Sequential	Combinatorial	Total	Device	Total	
IGLOO®/e	20	96	116	AGLE600	1.0%	72
ProASIC®3/E	20	76	96	A3P250	2.0%	96
Fusion	20	76	96	AFS600	1.0%	101
ProASIC ^{PLUS} ®	20	102	122	APA300	1.0%	101
Axcelerator®	20	31	51	AX250	1.0%	252
RTAX-S	20	31	51	RTAX250S	1.0%	223

Note: Data in this table were achieved using typical synthesis and layout settings. Top-level parameters/generics were set as follows: PWM_NUM = 1, APB_DWIDTH = 8; DAC_MODE1 = 1 (DAC mode), FIXED_PRESCALE_EN = 1, FIXED_PRESCALE = 0, FIXED_PERIOD_EN = 1, FIXED_PERIOD = 1, SHADOW_REG_EN1 = 0.

Table 2 · CorePWM Device Utilization and Performance
(one 16-bit DAC channel configuration)

Family	Tiles			Utilization		Performance (MHz)
	Sequential	Combinatorial	Total	Device	Total	
IGLOO/e	54	147	201	AGLE600V2	2.0%	59
ProASIC3/E	54	111	165	A3P250	3.0%	85
Fusion	54	111	165	AFS600	1.0%	94
ProASIC ^{PLUS}	55	209	264	APA200	3.0%	74

Note: Data in this table were achieved using typical synthesis and layout settings. Top-level parameters/generics were set as follows: PWM_NUM = 1, APB_DWIDTH = 16; DAC_MODE1 = 1 (DAC mode), FIXED_PRESCALE_EN = 1, FIXED_PRESCALE = 0, FIXED_PERIOD_EN = 1, FIXED_PERIOD = 1, SHADOW_REG_EN1 = 1.

Table 2 · CorePWM Device Utilization and Performance
(one 16-bit DAC channel configuration) (continued)

Axcelerator	57	53	110	AX250	2.0%	210
RTAX-S	57	53	110	RTAX250S	1.0%	176

Note: Data in this table were achieved using typical synthesis and layout settings. Top-level parameters/generics were set as follows: PWM_NUM = 1, APB_DWIDTH = 16; DAC_MODE1 = 1 (DAC mode), FIXED_PRESCALE_EN = 1, FIXED_PRESCALE = 0, FIXED_PERIOD_EN = 1, FIXED_PERIOD = 1, SHADOW_REG_EN1 = 1.

Table 3 · CorePWM Device Utilization and Performance
(one 8-bit general purpose PWM channel configuration)

Family	Tiles			Utilization		Performance (MHz)
	Sequential	Combinatorial	Total	Device	Total	
IGLOO/e	15	55	70	AGLE600V2	1.0%	82
ProASIC3/E	15	55	70	A3P250	1.0%	130
Fusion	15	55	70	AFS600	1.0%	144
ProASIC ^{PLUS}	15	58	73	APA300	1.0%	141
Axcelerator	16	40	56	AX250	1.0%	181
RTAX-S	16	40	56	RTAX250S	1.0%	187

Note: Data in this table were achieved using typical synthesis and layout settings. Top-level parameters/generics were set as follows: PWM_NUM = 1, APB_DWIDTH = 8; DAC_MODE1 = 0 (general purpose PWM mode), FIXED_PRESCALE_EN = 1, FIXED_PRESCALE = 0, FIXED_PERIOD_EN = 1, FIXED_PERIOD = 8, FIXED_PWM_POS_EN1 = 1, FIXED_PWM_POSEDGE1 = 0, FIXED_PWM_NEG_EN1 = 0, FIXED_PWM_NEGEDGE1 = 0, SHADOW_REG_EN1 = 0

Table 4 · CorePWM Device Utilization and Performance
(one 16-bit general purpose PWM channel configuration)

Family	Tiles			Utilization		Performance (MHz)
	Sequential	Combinatorial	Total	Device	Total	
IGLOO/e	91	272	363	AGLE600V2	3.0%	46
ProASIC3/E	91	275	366	A3P250	6.0%	72
Fusion	91	275	366	AFS600	3.0%	79
ProASIC ^{PLUS}	127	482	609	APA300	6.0%	59
Axcelerator	93	145	238	AX250	6.0%	110
RTAX-S	93	145	238	RTAX250S	6.0%	88

Note: Data in this table were achieved using typical synthesis and layout settings. Top-level parameters/generics were set as follows: PWM_NUM = 1, APB_DWIDTH = 16; DAC_MODE1 = 0 (General Purpose PWM mode); SHADOW_REG_EN1 = 1, FIXED_PRESCALE_EN = 1, FIXED_PRESCALE = 64.

Table 5 · CorePWM Device Utilization and Performance (8-bit multiple-output configuration example: 3 DAC mode outputs without shadow update register)

Family	Tiles			Utilization		Performance (MHz)
	Sequential	Combinatorial	Total	Device	Total	
IGLOO/e	58	208	266	AGLE600V2	2.0%	76
ProASIC3/E	58	150	208	A3P250	3.0%	101
Fusion	58	150	208	AFS600	2.0%	109
ProASIC ^{PLUS}	58	280	338	APA300	4.0%	101
Axcelerator	58	66	124	AX250	2.0%	250
RTAX-S	58	66	124	RTAX250S	2.0%	217

Note: Data in this table were achieved using typical synthesis and layout settings. Top-level parameters/generics were set as follows: `PWM_NUM = 3`, `APB_DWIDTH = 8`; `DAC_MODE1`, `DAC_MODE2`, and `DAC_MODE3 = 1` (DAC Mode) `FIXED_PERIOD_EN = 1`, `FIXED_PERIOD = 1`, `FIXED_PRESCALE_EN = 1`, `FIXED_PRESCALE = 0`, `SHADOW_REG_EN1 = 0`, `SHADOW_REG_EN2 = 0`, `SHADOW_REG_EN3 = 0`.

Table 6 · CorePWM Device Utilization and Performance (12-bit multiple-output configuration example: 3 DAC mode outputs, 3 general purpose PWM mode outputs)

Family	Tiles			Utilization		Performance (MHz)
	Sequential	Combinatorial	Total	Device	Total	
IGLOO/e	212	723	935	AGLE600V2	7.0%	45
ProASIC3/E	212	694	906	A3P250	15.0%	74
Fusion	212	694	906	AFS600	7.0%	82
ProASIC ^{PLUS}	229	1054	1,283	APA300	16.0%	67
Axcelerator	216	307	523	AX250	12.0%	103
RTAX-S	216	307	523	RTAX250S	12.0%	87

Note: Data in this table were achieved using typical synthesis and layout settings. Top-level parameters/generics were set as follows: `PWM_NUM = 6`, `APB_DWIDTH = 16`; `DAC_MODE1`, `DAC_MODE2`, and `DAC_MODE3 = 1` (DAC mode), `DAC_MODE4`, `DAC_MODE5`, and `DAC_MODE6 = 0` (general purpose PWM mode), `FIXED_PRESCALE_EN = 1`, `FIXED_PRESCALE = 8`, `SHADOW_REG_EN1 = 0`, `SHADOW_REG_EN2 = 0`, `SHADOW_REG_EN3 = 0`, `SHADOW_REG_EN4 = 0`, `SHADOW_REG_EN5 = 0`, `SHADOW_REG_EN6 = 0`.

Table 7 · CorePWM Device Utilization and Performance (one 16-bit general purpose PWM channel and one TACH input configuration)

Family	Tiles			Utilization		Performance (MHz)
	Sequential	Combinatorial	Total	Device	Total	
IGLOO/e	314	768	082	AGLE600V2	8.0%	47
ProASIC3/E	314	768	082	A3P250	18.0%	75
Fusion	314	768	1,082	AF600	8.0%	83
ProASIC ^{PLUS}	328	1,043	1,371	APA300	17.0%	70
Axcelerator	319	483	802	AX250	19.0%	103
RTAX-S	319	483	802	RTAX250S	19.0%	87

Note: Data in this table were achieved using typical synthesis and layout settings. Top-level parameters/generics were set as follows: CONFIG_MODE = 1, PWM_NUM=3, TACH_NUM=3, APB_DWIDTH=16; DAC_MODE1=0 (General Purpose PWM mode), FIXED_PRESCALE_EN=1, FIXED_PRESCALE=8, FIXED_PERIOD_EN=0, FIXED_PWM_POS_EN1=1, FIXED_PWM_POSEDGE1=0, FIXED_PWM_NEG_EN1=0, FIXED_PWM_NEGEDGE1=0, SHADOW_REG_EN1=0, FIXED_PWM_POS_EN2=1, FIXED_PWM_POSEDGE2=0, FIXED_PWM_NEG_EN2=0, FIXED_PWM_NEGEDGE2=0, SHADOW_REG_EN2=0, FIXED_PWM_POS_EN3=1, FIXED_PWM_POSEDGE3=0, FIXED_PWM_NEG_EN3=0, FIXED_PWM_NEGEDGE3=0, SHADOW_REG_EN3=0

Table 8 · CorePWM Device Utilization and Performance (one TACH input configuration with 16-bit APB data width)

Family	Tiles			Utilization		Performance (MHz)
	Sequential	Combinatorial	Total	Device	Total	
IGLOO/e	207	389	596	AGLE600V2	4.0%	52
ProASIC3/E	207	383	590	A3P250	10.0%	89
Fusion	207	383	590	AF600	4.0%	98
ProASIC ^{PLUS}	207	506	713	APA300	9.0%	92
Axcelerator	209	269	478	AX250	5%	114
RTAX-S	209	269	478	RTAX250S	11%	101

Note: Data in this table were achieved using typical synthesis and layout settings. Top-level parameters/generics were set as follows: CONFIG_MODE = 2, TACH_NUM=3, APB_DWIDTH=16.

Design Description

Functional Blocks

The CorePWM (pulse width modulation) macro generates up to 16 general purpose PWM signals, as shown in [Figure 1-1](#). CorePWM includes a Register Interface block, Timebase Generation block, TACH INF block, and PWM Generation block.

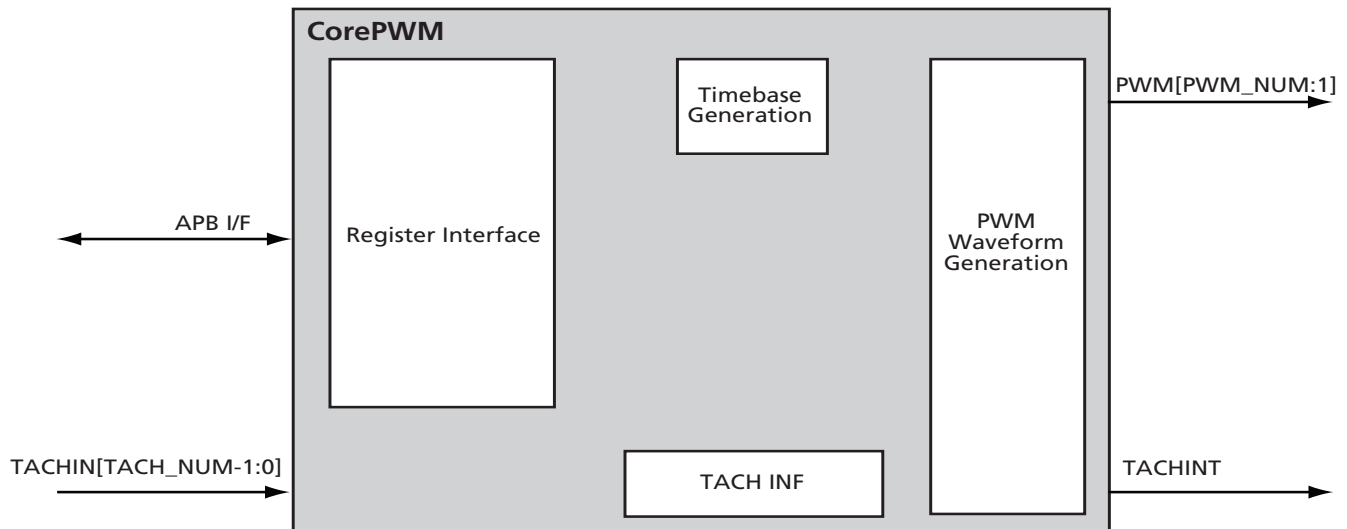


Figure 1-1 · CorePWM Block Diagram

The **Register Interface** block connects to an APB bus for PWM register configuration and updating. Descriptions for all registers are given in [Table 1-3 on page 15](#). A Shadow Register may be used so that PWM waveform updates occur only at the beginning of a PWM period. A shadow register holds all values and writes them when the SYNC_UPDATE register is set to 1. In other words, for all channel synchronous updates, write a "1" to the SYNC_UPDATE register after writing to all the channel registers.

The **Timebase Generation** block accepts PRESCALE and PERIOD register values and produces a PERIOD count. The number of system clocks between PERIOD counts is equal to the PRESCALE value.

The **PWM Waveform Generation** block has two modes:

General Purpose PWM mode takes input Period_cnt counter values and compares them with the register values for all the PWM positive and negative edge locations. When a comparison is met, each respective output waveform is set to the correct high/low/toggle value. An example General Purpose PWM waveform configuration is demonstrated in [Figure 1-3 on page 21](#). The example explains the relationship between the Prescale and Period register values, and how to configure the PWM waveforms with a given Prescale/Period timebase.

Low Ripple DAC mode is intended to drive a low-pass filter, typically a single-pole RC filter. Narrow pulses of constant width are spread evenly over time such that the average voltage is equal to the duty cycle. The output of the filter is then a DC voltage directly proportional to the duty cycle. This type of pulse train allows for much lower ripple at the output of the filter, and benefits from either higher bandwidth and/or smaller R and C values.

In the Tach interface module, the width of the decrementing counter is configured to 16 bits. The Tach interface module is used to measure the period of the TACHIN[x] signal by measuring between two successive positive or negative edges of TACHIN[x]. The measured value will be stored in the corresponding input's TACHPULSEDUR register. The measured value will be read by the firmware through the APB interface. The access to the control and status registers of the Tach interface module is through the APB interface. The stored value in TACHPULSEDUR will correspond to the count for half of a revolution of a four pole fan. When determining the speed for other than four pole fans, the algorithm

that converts the counter value to RPMs must be adjusted by the firmware. TACH INF supports 16- and 32-bit APB interface, but it does not support 8-bit interfaces.

To accurately measure the speed of 3-wire fans, you must turn on the fan periodically and long enough to get a complete tach measurement, often referred to as PWM pulse stretching. The PWM_STRETCH register allows you to set the desired PWMx signals to the level specified by PWM_STRETCH_VALUE. The following algorithm can be used to measure the speed of 3-wire fans. This algorithm assumes that the TACHMODEy bit is set to '1' (one-shot mode):

- Software enables pulse stretching by writing a '1' to PWM_STRETCHx, which forces PWMx to PWM_STRETCH_VALUEx. This requirement is not enforced by the hardware.
- Software can add a delay to ensure the fan tachometer circuitry is operational before enabling fan speed measurement.
- Software clears the TACHSTATUSy bit, enabling a one-time Tach measurement on the input signal TACHINy corresponding to one of the fans controlled by PWMx
- Software receives an interrupt and verifies that the Tach measurement for TACHINy has been completed (via TACHSTATUSy bit)
- Software disables pulse stretching by writing a '0' to PWM_STRETCHx.

I/O Signals

The port signals for the CorePWM macro are defined in [Table 1-1 on page 13](#) and illustrated in [Figure 1-2](#). All signals are either Input (input only) or Output (output only).

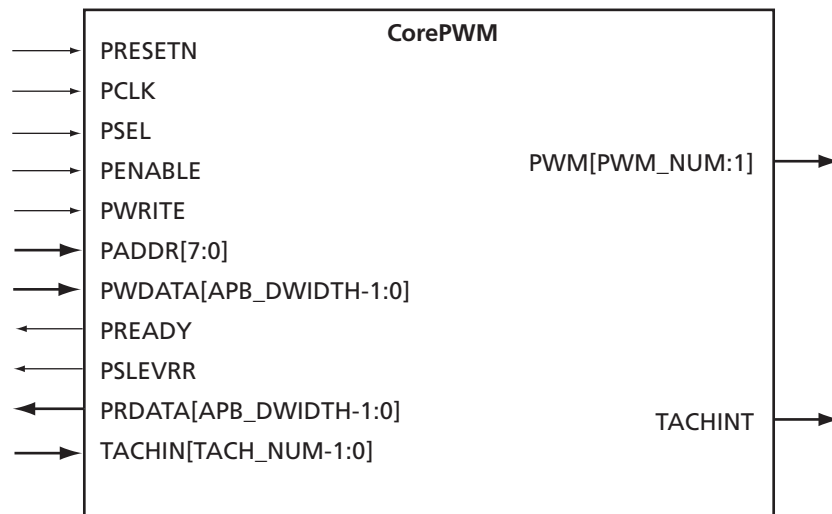


Figure 1-2 · CorePWM I/O Signal Diagram

Table 1-1 · CorePWM I/O Signal Descriptions

Name	Type	Description
System Signals		
PRESETN	Input	Active low asynchronous reset
PCLK	Input	System clock – all operations and status shall be synchronous to the rising edge of this clock signal
Microcontroller Signals		
PSEL	Input	Select line for CorePWM
PENABLE	Input	Read output enable
PWRITE	Input	Write enable
PADDR[7:0]	Input	Register address
PWDATA[APB_DWIDTH-1:0]	Input	Write address/data input
PREADY	Output	Ready signal, tied High
PSLVERR	Output	Transfer error signal, tied Low
PRDATA[APB_DWIDTH-1:0]	Output	Read data output
PWM Signals		
PWM[PWM_NUM:1]	Output	Pulse width modulation output
TACH Signals		
TACHIN[TACH_NUM -1:0]	Input	TACH input
TACHINT	Output	Interrupt output for the tachometer. This signal indicates a TACHSTATUS register bit has been set to one. The polarity of this signal is controlled by the TACHINT_ACT_LEVEL configurable option.

Note: All signals active-High (logic 1) unless otherwise noted.

Verilog/VHDL Parameters

CorePWM has parameters (Verilog) and generics (VHDL) for configuring the RTL code, described in [Table 1-2](#). All parameters and generics are integer types.

Table 1-2 · CorePWM Parameters/Generics Descriptions

Name	Description
CONFIG_MODE	When 0, supports PWM only (legacy with dead banding support) When 1, supports both PWM and TACH When 2, supports TACH only
PWM_NUM	Number of PWM outputs from 1 to 16. This parameter is used only when CONFIG_MODE is set to 0 or 1.
APB_DWIDTH	PWM resolution and APB bus width from 8 to 32. This parameter must be set to either 16 or 32 when CONFIG_MODE is either 1 or 2.
FIXED_PRESCALE_EN	Fixed Prescale Enable. FIXED_PRESCALE_EN hardwires the register, disallowing APB write-access, and reducing tile count. This parameter is used only when CONFIG_MODE set to 0 or 1.
FIXED_PRESCALE	Hardwired PRESCALE[APB_DWIDTH -1:0] register value. This parameter is used only when CONFIG_MODE set to 0 or 1.
FIXED_PERIOD_EN	Fixed Period Enable. FIXED_PERIOD_EN hardwires the register, disallowing APB write-access, and reducing tile count. This parameter is used only when CONFIG_MODE set to 0 or 1.
FIXED_PERIOD	Hardwired PERIOD[APB_DWIDTH -1:0] register value. This parameter is used only when CONFIG_MODE set to 0 or 1.
SHADOW_REG_EN _x	Shadow Register Enable. Synchronizes all register modification changes to the beginning of the PWM cycle; that is, when PERIOD Count = 0. This parameter is used only when CONFIG_MODE set to 0 or 1.
DAC_MODE _x	DAC mode. 1 = Low ripple DAC mode; 0 = General purpose PWM mode. <i>Note:</i> _x refers to each channel, from 1 to 16. This parameter is used only when CONFIG_MODE set to 0 or 1.
FIXED_PWM_POS_EN _x	Fixed per channel Positive Edge Enable. <i>Note:</i> _x refers to each channel, from 1 to 16. FIXED_PWM_POS_EN _x hardwires the register, disallowing APB write-access, and reducing tile count. In a typical PWM application, either the FIXED_PWM_POS_EN _x or the FIXED_PWM_NEG_EN _x could be set if one of those edges do not need to be software controlled with APB write-accesses. Fixing both edges would result in static output. This parameter is used only when CONFIG_MODE set to 0 or 1.
FIXED_PWM_POSEDGE _x	Hardwired POSEDGE[APB_DWIDTH -1:0] register value. <i>Note:</i> _x refers to each channel, from 1 to 16. This parameter is used only when CONFIG_MODE set to 0 or 1.

Table 1-2 · CorePWM Parameters/Generics Descriptions

FIXED_PWM_NEG_EN _x FIXED_DAC_OUT_EN _x	<p>Fixed per channel Negative Edge Enable.</p> <p><i>Note:</i> <i>x</i> refers to each channel, from 1 to 16. FIXED_PWM_NEG_EN_x hardwires the register, disallowing APB write-access, and reducing tile count.</p> <p>In a typical PWM application, either the FIXED_PWM_NEG_EN_x or the FIXED_PWM_POS_EN_x could be set if one of those edges do not need to be software-controlled with APB write-accesses. Fixing both edges would result in static output.</p> <p>For DAC applications, the FIXED_PWM_POS_EN_x value is unconnected while the FIXED_DAC_OUT_EN_x value would typically be disabled, as using it would result in static output.</p> <p>This parameter is used only when CONFIG_MODE set to 0 or 1.</p>
FIXED_PWM_NEGEDGE _x FIXED_DAC_LEVELOUT _x	<p>Hardwired NEGEDGE[APB_DWIDTH -1:0] register value. When in DAC Mode, this parameter also fixes DAC_x_LEVELOUT, which is typically not fixed in DAC applications, as it would only create a static duty cycle output. Note: <i>x</i> refers to each channel, from 1 to 16.</p> <p>This parameter is used only when CONFIG_MODE set to 0 or 1.</p>
PWM_STRETCH_VALUE _x	<p>Defines PWM_x level when PWM_STRETCH_x is set to 1.</p> <p>When 0, PWM_x is set to 0 if PWM_STRETCH_x is set to 1;</p> <p>When 1, PWM_x is set to 1 if PWM_STRETCH_x is set to 1 (default).</p> <p>This parameter is used only when CONFIG_MODE set to either 1 or 2.</p>
TACH_NUM	<p>Number of Tachometer inputs from 1 to 16. This parameter is used only when CONFIG_MODE set to 1 or 2.</p>
TACH_EDGE _y	<p>Fixed per Tachometer input edge select. Selects the edge used to capture the counter value for the TACH_[x] input signals. 0, capture counter value on falling edge of TACH_[x] (default); 1, capture counter value on rising edge of TACH_[x]. This parameter is used only when CONFIG_MODE set to 1 or 2.</p>
TACHINT_ACT_LEVEL	<p>Selects active Low or active High TACHINT interrupt: 0, active Low interrupt (default); 1, active High interrupt. This parameter is used only when CONFIG_MODE set to 1 or 2.</p>

Register Map

All registers are based on APB width parameter selection; default is 8 bits.

Table 1-3 · CorePWM Register Definitions

Register Name	Paddr[7:0]	Description	Type	Default
PRESCALE	0x00	<p>PWM MODE: The system clock cycle is multiplied with the PRESCALE value resulting in the minimum PERIOD count timebase.</p> <p>DAC MODE: The Prescale and Period Registers could be used in conjunction with the shadow register to synchronize DAC LEVELOUT.</p>	R/W	0x08
PERIOD	0x04	PWM MODE: The PRESCALE value is multiplied with the PERIOD value yielding the PWM waveform cycle.	R/W	0x08
PWM_ENABLE_0_7	0x08	Bitwise channel enables for PWM/DAC channels 1 through 8.	R/W	0x00
PWM_ENABLE_8_15	0x0C	Bitwise channel enables for PWM/DAC channels 9 through 16.	R/W	0x00

Table 1-3 · CorePWM Register Definitions (continued)

SYNC_UPDATE	0xE4	<p>SYNC_UPDATE: When this bit is set to "1" and SHADOW_REG_EN is selected, all POSEDGE and NEGEDGE registers are updated synchronously. Synchronous updates to the PWM waveform occur only when SHADOW_REG_EN is asserted and SYNC_UPDATE is set to "1".</p> <p>When this bit is set to "0", all the POSEDGE and NEGEDGE registers are updated asynchronously.</p>	R/W	0x00
PWM1_POSEDGE	0x10	PWM MODE: Sets the positive edge of the output with respect to the PERIOD resolution. When APB writes to this register, all the channels are updated.	R/W	0x00
PWM1_NEGEDGE <i>DAC1_LEVELOUT</i>	0x14	<p>PWM MODE: Sets the negative edge of the output with respect to the PERIOD resolution.</p> <p>DAC MODE: Sets the desired output level, from 0-100%.</p>	R/W	0x00
PWM2_POSEDGE	0x18	PWM MODE: Sets the positive edge of the output with respect to the PERIOD resolution.	R/W	0x00
PWM2_NEGEDGE <i>DAC2_LEVELOUT</i>	0x1C	<p>PWM MODE: Sets the negative edge of the output with respect to the PERIOD resolution.</p> <p>DAC MODE: Sets the desired output level, from 0-100%.</p>	R/W	0x00
PWM3_POSEDGE	0x20	PWM MODE: Sets the positive edge of the output with respect to the PERIOD resolution.	R/W	0x00
PWM3_NEGEDGE <i>DAC3_LEVELOUT</i>	0x24	<p>PWM MODE: Sets the negative edge of the output with respect to the PERIOD resolution.</p> <p>DAC MODE: Sets the desired output level, from 0-100%.</p>	R/W	0x00
PWM4_POSEDGE	0x28	PWM MODE: Sets the positive edge of the output with respect to the PERIOD resolution.	R/W	0x00
PWM4_NEGEDGE <i>DAC4_LEVELOUT</i>	0x2C	<p>PWM MODE: Sets the negative edge of the output with respect to the PERIOD resolution.</p> <p>DAC MODE: Sets the desired output level, from 0-100%.</p>	R/W	0x00
PWM5_POSEDGE	0x30	PWM MODE: Sets the positive edge of the output with respect to the PERIOD resolution.	R/W	0x00
PWM5_NEGEDGE <i>DAC5_LEVELOUT</i>	0x34	<p>PWM MODE: Sets the negative edge of the output with respect to the PERIOD resolution.</p> <p>DAC MODE: Sets the desired output level, from 0-100%.</p>	R/W	0x00
PWM6_POSEDGE	0x38	PWM MODE: Sets the positive edge of the output with respect to the PERIOD resolution.	R/W	0x00
PWM6_NEGEDGE <i>DAC6_LEVELOUT</i>	0x3C	<p>PWM MODE: Sets the negative edge of the output with respect to the PERIOD resolution.</p> <p>DAC MODE: Sets the desired output level, from 0-100%.</p>	R/W	0x00
PWM7_POSEDGE	0x40	PWM MODE: Sets the positive edge of the output with respect to the PERIOD resolution.	R/W	0x00
PWM7_NEGEDGE <i>DAC7_LEVELOUT</i>	0x44	<p>PWM MODE: Sets the negative edge of the output with respect to the PERIOD resolution.</p> <p>DAC MODE: Sets the desired output level, from 0-100%.</p>	R/W	0x00
PWM8_POSEDGE	0x48	PWM MODE: Sets the positive edge of the output with respect to the PERIOD resolution.	R/W	0x00

Table 1-3 · CorePWM Register Definitions (continued)

PWM8_NEGEDGE <i>DAC8_LEVELOUT</i>	0x4C	PWM MODE: Sets the negative edge of the output with respect to the PERIOD resolution. <i>DAC MODE</i> : Sets the desired output level, from 0-100%.	R/W	0x00
PWM9_POSEDGE	0x50	PWM MODE: Sets the positive edge of the output with respect to the PERIOD resolution.	R/W	0x00
PWM9_NEGEDGE <i>DAC9_LEVELOUT</i>	0x54	PWM MODE: Sets the negative edge of the output with respect to the PERIOD resolution. <i>DAC MODE</i> : Sets the desired output level, from 0-100%.	R/W	0x00
PWM10_POSEDGE	0x58	PWM MODE: Sets the positive edge of the output with respect to the PERIOD resolution.	R/W	0x00
PWM10_NEGEDGE <i>DAC10_LEVELOUT</i>	0x5C	PWM MODE: Sets the negative edge of the output with respect to the PERIOD resolution. <i>DAC MODE</i> : Sets the desired output level, from 0-100%.	R/W	0x00
PWM11_POSEDGE	0x60	PWM MODE: Sets the positive edge of the output with respect to the PERIOD resolution.	R/W	0x00
PWM11_NEGEDGE <i>DAC11_LEVELOUT</i>	0x64	PWM MODE: Sets the negative edge of the output with respect to the PERIOD resolution. <i>DAC MODE</i> : Sets the desired output level, from 0-100%.	R/W	0x00
PWM12_POSEDGE	0x68	PWM MODE: Sets the positive edge of the output with respect to the PERIOD resolution.	R/W	0x00
PWM12_NEGEDGE <i>DAC12_LEVELOUT</i>	0x6C	PWM MODE: Sets the negative edge of the output with respect to the PERIOD resolution. <i>DAC MODE</i> : Sets the desired output level, from 0-100%.	R/W	0x00
PWM13_POSEDGE	0x70	PWM MODE: Sets the positive edge of the output with respect to the PERIOD resolution.	R/W	0x00
PWM13_NEGEDGE <i>DAC13_LEVELOUT</i>	0x74	PWM MODE: Sets the negative edge of the output with respect to the PERIOD resolution. <i>DAC MODE</i> : Sets the desired output level, from 0-100%.	R/W	0x00
PWM14_POSEDGE	0x78	PWM MODE: Sets the positive edge of the output with respect to the PERIOD resolution.	R/W	0x00
PWM14_NEGEDGE <i>DAC14_LEVELOUT</i>	0x7C	PWM MODE: Sets the negative edge of the output with respect to the PERIOD resolution. <i>DAC MODE</i> : Sets the desired output level, from 0-100%.	R/W	0x00
PWM15_POSEDGE	0x80	PWM MODE: Sets the positive edge of the output with respect to the PERIOD resolution.	R/W	0x00
PWM15_NEGEDGE <i>DAC15_LEVELOUT</i>	0x84	PWM MODE: Sets the negative edge of the output with respect to the PERIOD resolution. <i>DAC MODE</i> : Sets the desired output level, from 0-100%.	R/W	0x00
PWM16_POSEDGE	0x88	PWM MODE: Sets the positive edge of the output with respect to the PERIOD resolution.	R/W	0x00
PWM16_NEGEDGE <i>DAC16_LEVELOUT</i>	0x8C	PWM MODE: Sets the negative edge of the output with respect to the PERIOD resolution. <i>DAC MODE</i> : Sets the desired output level, from 0-100%.	R/W	0x00

Table 1-3 · CorePWM Register Definitions (continued)

PWM_STRETCH	0x90	When 0, the state of PWMx is determined by PWMx_POSEDGE/ NEGEDGE register settings. When 1, PWMx is set to PWM_STRETCH_VALUE _x .	R/W	0x0000
TACHPRESCALE	0x94	Clock prescale setting. Determines effective clock rate for the counter based on PCLK: 0000 = divide by 1 (default) 0001 = divide by 2 0010 = divide by 4 0011 = divide by 8 0100 = divide by 16 0101 = divide by 32 0110 = divide by 64 0111 = divide by 128 1000 = divide by 256 1001 = divide by 512 1010 = divide by 1,024 1011 = divide by 2,048 Others = divide by 2,048	R/W	0x0
TACHSTATUS	0x98	TACH status register which contains one bit per TACH input, indicating whether the respective TACHPULSEDUR register has been updated at least once since the bit was cleared. The bits in this register gets cleared by writing “1”, “0” does not have any effect.	R/ W1C	0x0000
TACHIRQMASK	0x9C	TACH interrupt mask register with one bit per tachometer signal, indicating whether CorePWM needs to assert an interrupt if the respective bit in TACHSTATUS register is asserted.	R/W	0x0000
TACHMODE	0xA0	TACH Mode. Sets the measurement mode used for each TACH input. When 0: TACH input is continuously measured and stored in the respective TACHPULSEDUR register . When 1: A one-time measurement is performed only if the respective bit in TACHSTATUS register is cleared.	R/W	0x0000
TACHPULSEDUR_0	0xA4	Stores the number of timer ticks between two successive positive (or negative) edges from the TACHIN[0]. The edge to be used is configurable. If the number of timer ticks exceeds the maximum register value, the value of 0 shall be stored instead.	R	0x0000
TACHPULSEDUR_1	0xA8	Stores the number of timer ticks between two successive positive (or negative) edges from the TACHIN[1]. The edge to be used is configurable. If the number of timer ticks exceeds the maximum register value, the value of 0 shall be stored instead.	R	0x0000
TACHPULSEDUR_2	0xAC	Sstores the number of timer ticks between two successive positive (or negative) edges from the TACHIN[2]. The edge to be used is configurable. If the number of timer ticks exceeds the maximum register value, the value of 0 shall be stored instead.	R	0x0000

Table 1-3 · CorePWM Register Definitions (continued)

TACHPULSEDUR_3	0xB0	Stores the number of timer ticks between two successive positive (or negative) edges from the TACHIN[3]. The edge to be used is configurable. If the number of timer ticks exceeds the maximum register value, the value of 0 shall be stored instead.	R	0x0000
TACHPULSEDUR_4	0xB4	Stores the number of timer ticks between two successive positive (or negative) edges from the TACHIN[4]. The edge to be used is configurable. If the number of timer ticks exceeds the maximum register value, the value of 0 shall be stored instead.	R	0x0000
TACHPULSEDUR_5	0xB8	Stores the number of timer ticks between two successive positive (or negative) edges from the TACHIN[5]. The edge to be used is configurable. If the number of timer ticks exceeds the maximum register value, the value of 0 shall be stored instead.	R	0x0000
TACHPULSEDUR_6	0xBC	Stores the number of timer ticks between two successive positive (or negative) edges from the TACHIN[6]. The edge to be used is configurable. If the number of timer ticks exceeds the maximum register value, the value of 0 shall be stored instead.	R	0x0000
TACHPULSEDUR_7	0xC0	Stores the number of timer ticks between two successive positive (or negative) edges from the TACHIN[7]. The edge to be used is configurable. If the number of timer ticks exceeds the maximum register value, the value of 0 shall be stored instead.	R	0x0000
TACHPULSEDUR_8	0xC4	Stores the number of timer ticks between two successive positive (or negative) edges from the TACHIN[8]. The edge to be used is configurable. If the number of timer ticks exceeds the maximum register value, the value of 0 shall be stored instead.	R	0x0000
TACHPULSEDUR_9	0xC8	Stores the number of timer ticks between two successive positive (or negative) edges from the TACHIN[9]. The edge to be used is configurable. If the number of timer ticks exceeds the maximum register value, the value of 0 shall be stored instead.	R	0x0000
TACHPULSEDUR_10	0xCC	Stores the number of timer ticks between two successive positive (or negative) edges from the TACHIN[10]. The edge to be used is configurable. If the number of timer ticks exceeds the maximum register value, the value of 0 shall be stored instead.	R	0x0000
TACHPULSEDUR_11	0xD0	Stores the number of timer ticks between two successive positive (or negative) edges from the TACHIN[11]. The edge to be used is configurable. If the number of timer ticks exceeds the maximum register value, the value of 0 shall be stored instead.	R	0x0000
TACHPULSEDUR_12	0xD4	Stores the number of timer ticks between two successive positive (or negative) edges from the TACHIN[12]. The edge to be used is configurable. If the number of timer ticks exceeds the maximum register value, the value of 0 shall be stored instead.	R	0x0000
TACHPULSEDUR_13	0xD8	Stores the number of timer ticks between two successive positive (or negative) edges from the TACHIN[13]. The edge to be used is configurable. If the number of timer ticks exceeds the maximum register value, the value of 0 shall be stored instead.	R	0x0000
TACHPULSEDUR_14	0xDC	Stores the number of timer ticks between two successive positive (or negative) edges from the TACHIN[14]. The edge to be used is configurable. If the number of timer ticks exceeds the maximum register value, the value of 0 shall be stored instead.	R	0x0000

Table 1-3 · CorePWM Register Definitions (continued)

TACHPULSEDUR_15	0xE0	Stores the number of timer ticks between two successive positive (or negative) edges from the TACHIN[15]. The edge to be used is configurable. If the number of timer ticks exceeds the maximum register value, the value of 0 shall be stored instead.	R	0x0000
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Note: Od = decimal; Ox = hexadecimal; Ob = binary.

Configuration Example

Figure 1-3 demonstrates how several register configurations affect General Purpose and Low Ripple DAC PWM output waveform generation.

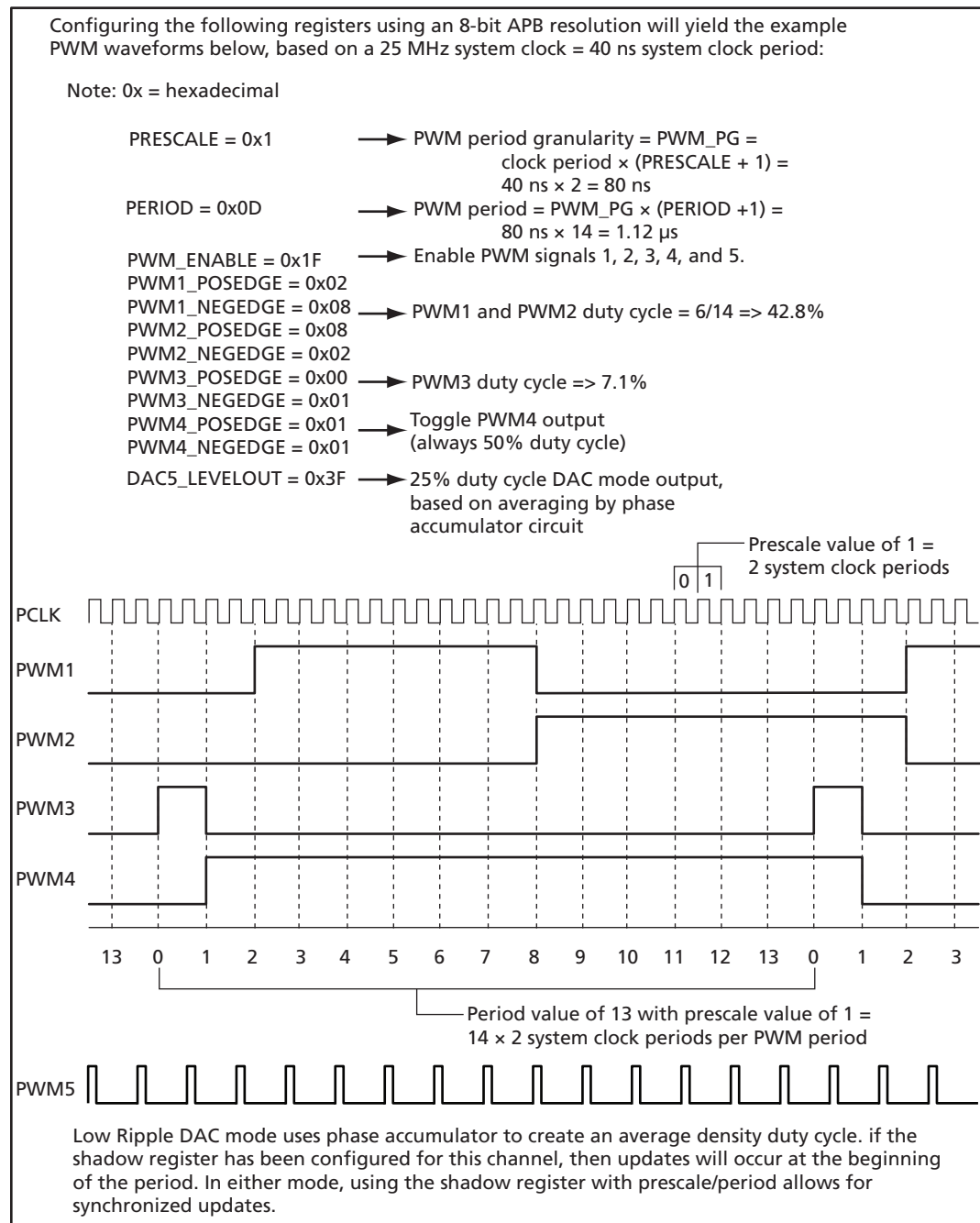


Figure 1-3 · CorePWM Waveform Generation Example

Figure 1-4 to Figure 1-7 on page 23 demonstrate how to avoid overlapping of the dead banding issue using the register configurations of channel 1 and channel 2 as a pair. Both channel 1(PWM1) and channel 2(PWM2) are updated after writing a “1” to the SYNC_UPDATE configuration register to avoid overlapping of dead band space..

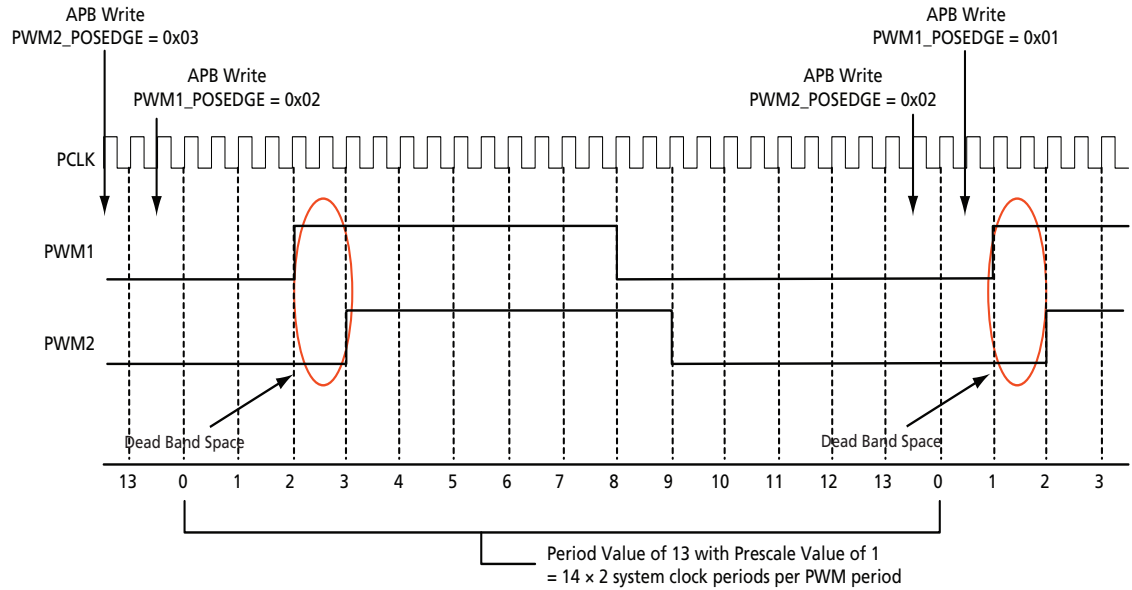


Figure 1-4 · Dead Band Space Example

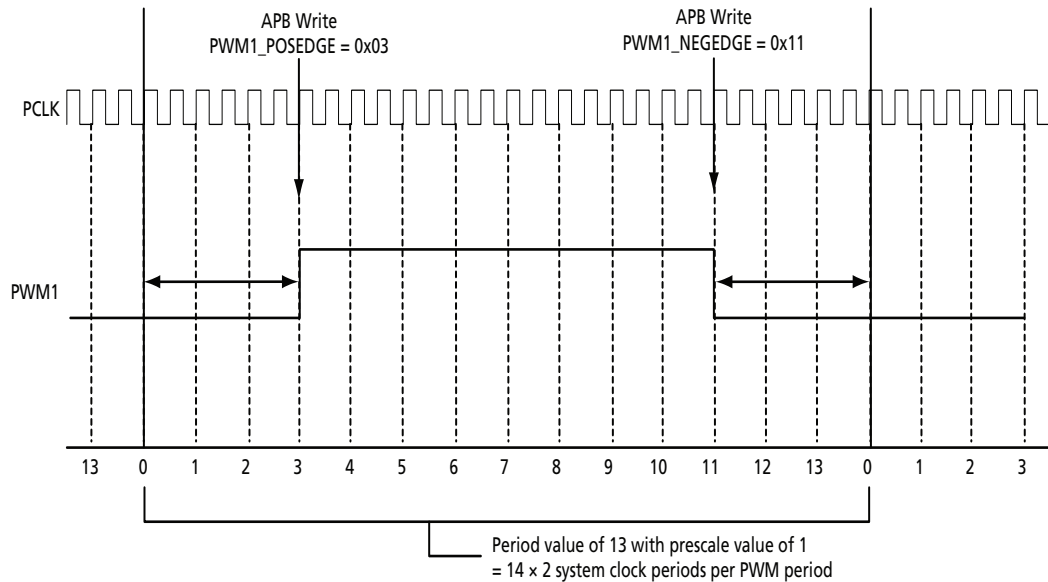


Figure 1-5 · Center-Aligned PWM Waveform Example

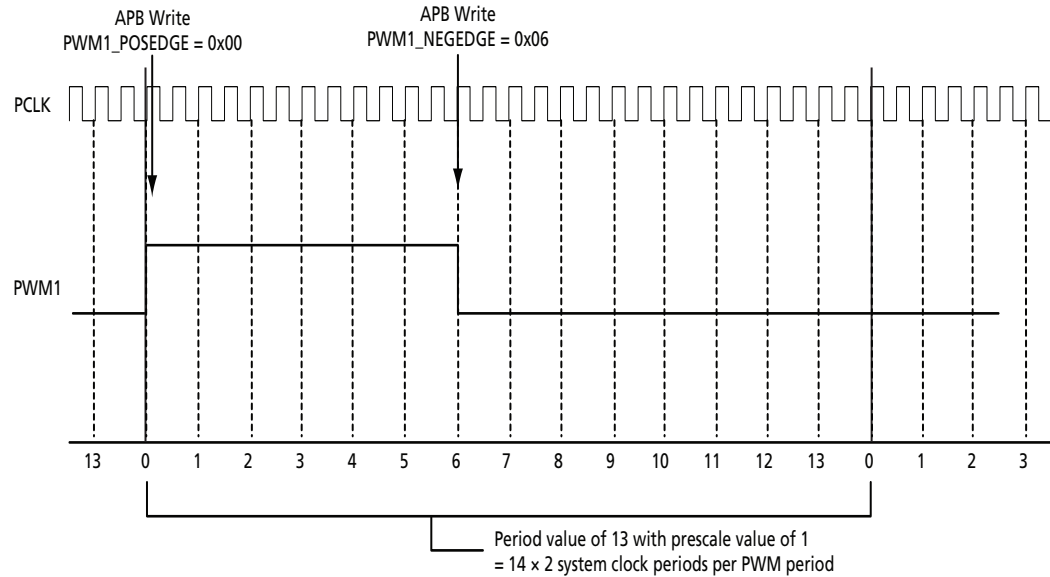


Figure 1-6 · Left-Aligned PWM Waveform Example

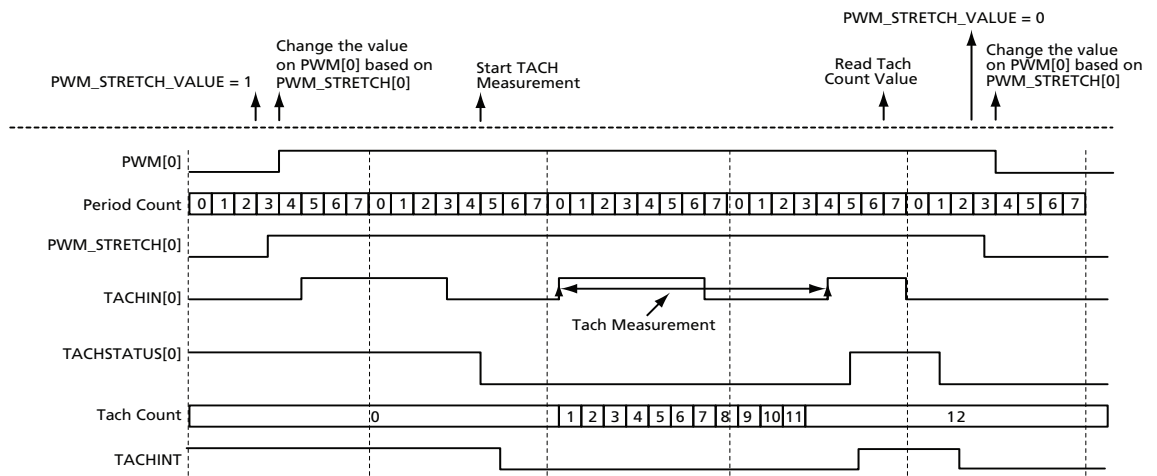


Figure 1-7 · Tach Measurement

APB Interface Timing

Figure 1-8 and Figure 1-9 depict typical write cycle and read cycle timing relationships relative to the system clock.

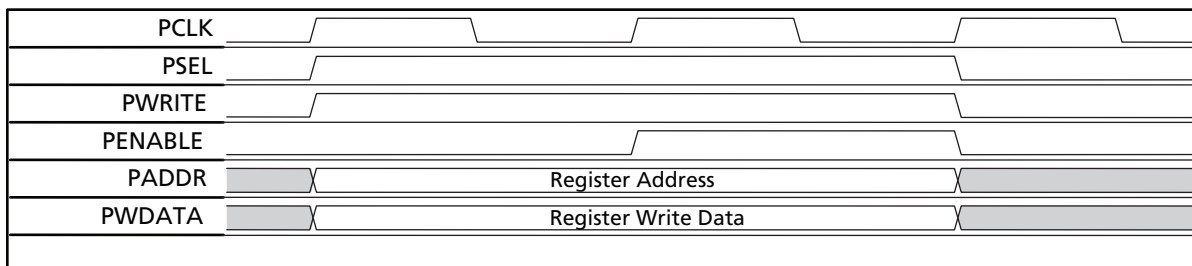


Figure 1-8 · Data Write Cycle

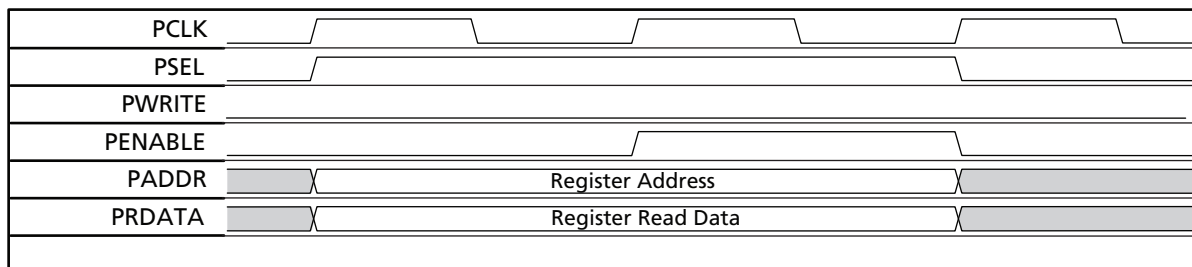


Figure 1-9 · Data Read Cycle

Tool Flows

CorePWM is licensed in two ways. Depending on your license, tool flow functionality may be limited.

Obfuscated

Complete RTL code is provided for the core, allowing the core to be instantiated with SmartDesign. Simulation, Synthesis, and Layout can be performed within Libero IDE. The RTL code for the core is obfuscated¹ and some of the testbench source files are not provided. Instead, they are precompiled into the compiled simulation library.

RTL

Complete RTL source code is provided for the core and testbenches.

SmartDesign

The core can be configured using the configuration GUI within SmartDesign. An example of configuring one channel for PWM mode operation is shown in [Figure 2-1 on page 26](#). Note the following in this example:

- Number of PWM Channels is 1.
- APB bit width and corresponding PWM resolution is 8 bits.
- The Prescale value (the number of clock ticks between Period ticks) is selected to be Fixed at 64, reducing the tile count, as no registers are used.
- The Period value is not Fixed and hence software-controlled.
- The Shadow Update Register is enabled, allowing for synchronized PWM updates at the beginning of the Period count.
- The Positive edge of the PWM is not Fixed and hence software-controlled.
- The Negative edge of the PWM waveform is Fixed at Period count 0.
- The User Testbench is selected to be generated.

1. Obfuscated means formatting and comments have been removed from the RTL source files, and all instance and net names have been replaced with random character sequences.

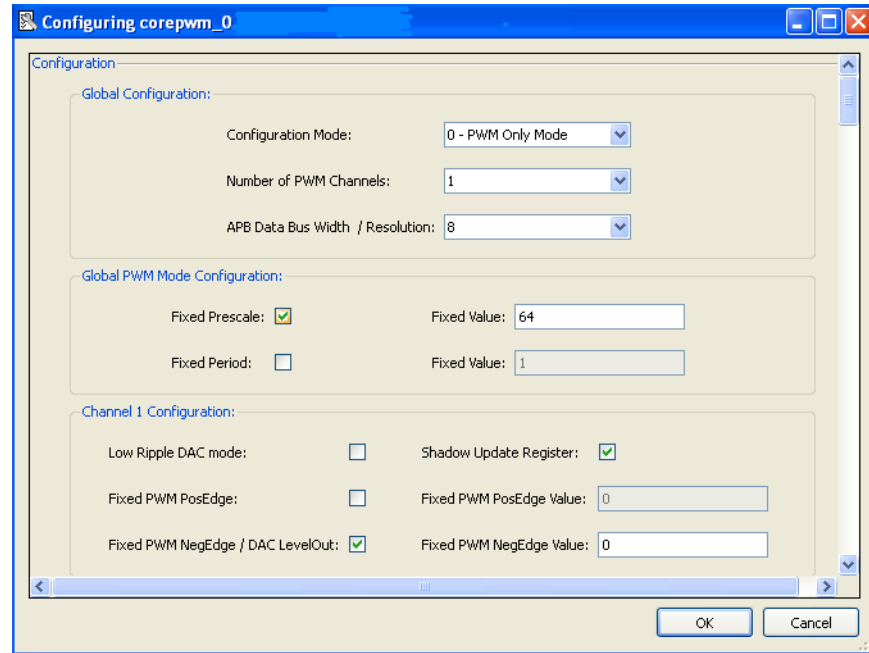


Figure 2-1 · CorePWM Configuration within SmartDesign – PWM Mode

An example of configuring one Channel for low ripple DAC operation is shown in [Figure 2-2 on page 27](#). Note the following in this example:

- Number of PWM Channels is 1.
- APB bit width and corresponding PWM/DAC resolution is 8 bits.
- The Prescale and Period Values can be used in conjunction with the Shadow Update Register to update DAC1_LEVELOUT values at a given period. For example, 3 DACs could be updated simultaneously based on the Prescale and Period values if the Shadow Update Register is enabled. In this example, the DAC1_LEVELOUT value is updated whenever the APB bus updates the DAC1_LEVELOUT register.
- The DAC LevelOut value is not Fixed and hence software-controlled. Note the DAC1_LEVELOUT value is synonymous with a Duty Cycle value; i.e., an 8-bit DAC1_LEVELOUT hex value of 7F is equal to an average duty cycle of 50% and will yield half of the full analog value after RC filtering.
- Note the “Fixed PWM PosEdge” value does not apply to DAC mode channel.
- The User Testbench is selected to be generated.

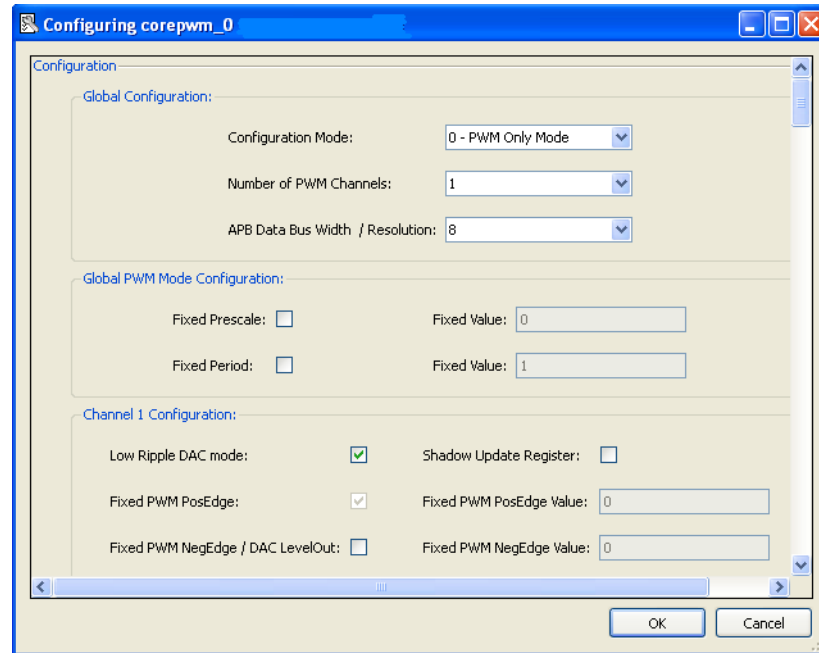


Figure 2-2 · CorePWM Configuration within SmartDesign – DAC Mode

Importing into Libero IDE

CorePWM is available for download to the SmartDesign IP Catalog, via the Libero IDE web repository. For information on using SmartDesign to instantiate, configure, connect, and generate cores, refer to the Libero IDE online help.

Simulation Flows

To run simulations, select the user testbench within the SmartDesign CorePWM configuration GUI, right-click, and select **Generate Design**. When SmartDesign generates the design files, it will install the appropriate testbench files. Set the design root to the CorePWM instantiation in the Libero IDE design hierarchy pane, and click the **Simulation** icon in the Libero IDE Design Flow window. This will invoke ModelSim® and automatically run simulation.

A simplified block diagram of the User Testbench is shown in [Figure 2-3](#). The user testbench instantiates the CorePWM macro and provides a Register Write Stimulus process, Register Read process, and a PWM output duty cycle check process.

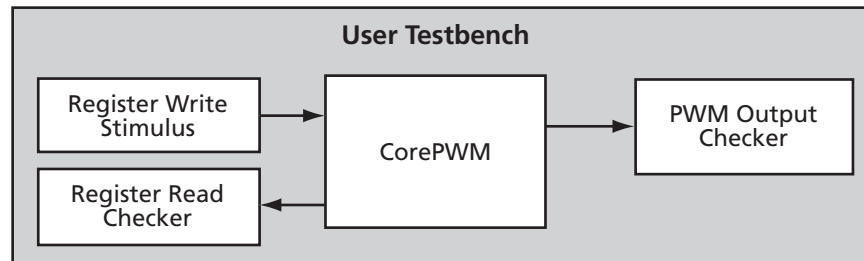


Figure 2-3 · CorePWM Verification Testbench

Synthesis in the Libero IDE

Having set the design route appropriately, click the **Synthesis** icon in Libero IDE. The Synthesis window appears, displaying the Synplicity® project. Set Synplicity to use the Verilog 2001 standard if Verilog is being used. To run Synthesis, select the **Run** icon.

Place-and-Route in Libero IDE

Having set the design route appropriately and run Synthesis, click on the **Layout** icon in Libero IDE to invoke Designer. CorePWM requires no special place-and-route settings.

Example Applications

For General Purpose PWM applications, a duty cycle calculator is available online to assist in calculating the PWM POSEDGE and NEGEDGE register values, given a requested duty cycle. This is provided on the Actel website as a downloadable Excel spreadsheet:

http://www.actel.com/documents/duty_cycle_calc.zip

For DAC applications, a low ripple DAC calculator is also available online:

http://www.actel.com/documents/low_ripple_dac_calc.zip

General Purpose PWM Application – Temperature Monitor

A typical temperature monitor application using CorePWM is shown in Figure 3-1. In this example, fan speed is controlled by fluctuations in the NTC thermistor's resistive value. As shown, changes in the input voltage to the voltage monitor port will be converted to a digital value via the ADC and forwarded to an on-chip microcontroller (such as Core8051s). The microcontroller algorithm will periodically configure/reconfigure CorePWM registers based on the thermistor value and/or the fan's tachometer value.

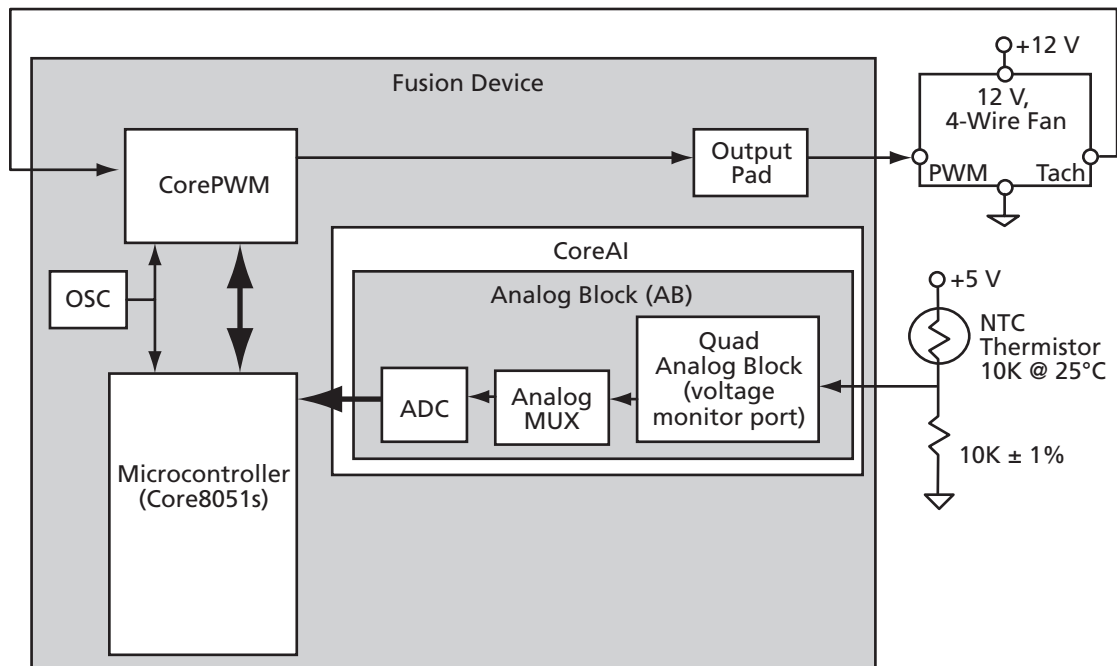


Figure 3-1 · Temperature/Voltage Monitor Application Using CorePWM in a Fusion Device

DAC

A typical DAC application using CorePWM is shown in Figure 3-2 on page 30. In this example, PWM output is averaged to a varying DC voltage. At reset, the PWM duty cycle, or level out value, is 100% and the voltage increases to the rail of 12 volts. The PWM duty cycle / level out value changes to 75% and then 50%, and the output of the RC filter follows this by dropping to 8 volts and then 6 volts. The generated ripple voltage is a function of the RC circuit values, the APB system clock period, and the PWM duty cycle.

As shown, a field-effect transistor (FET) is used to increase and decouple the output voltage/current from the Fusion device. The load is monitored and changes to the PWM output are processed via a microcontroller (Core8051s, CoreABC, etc.).

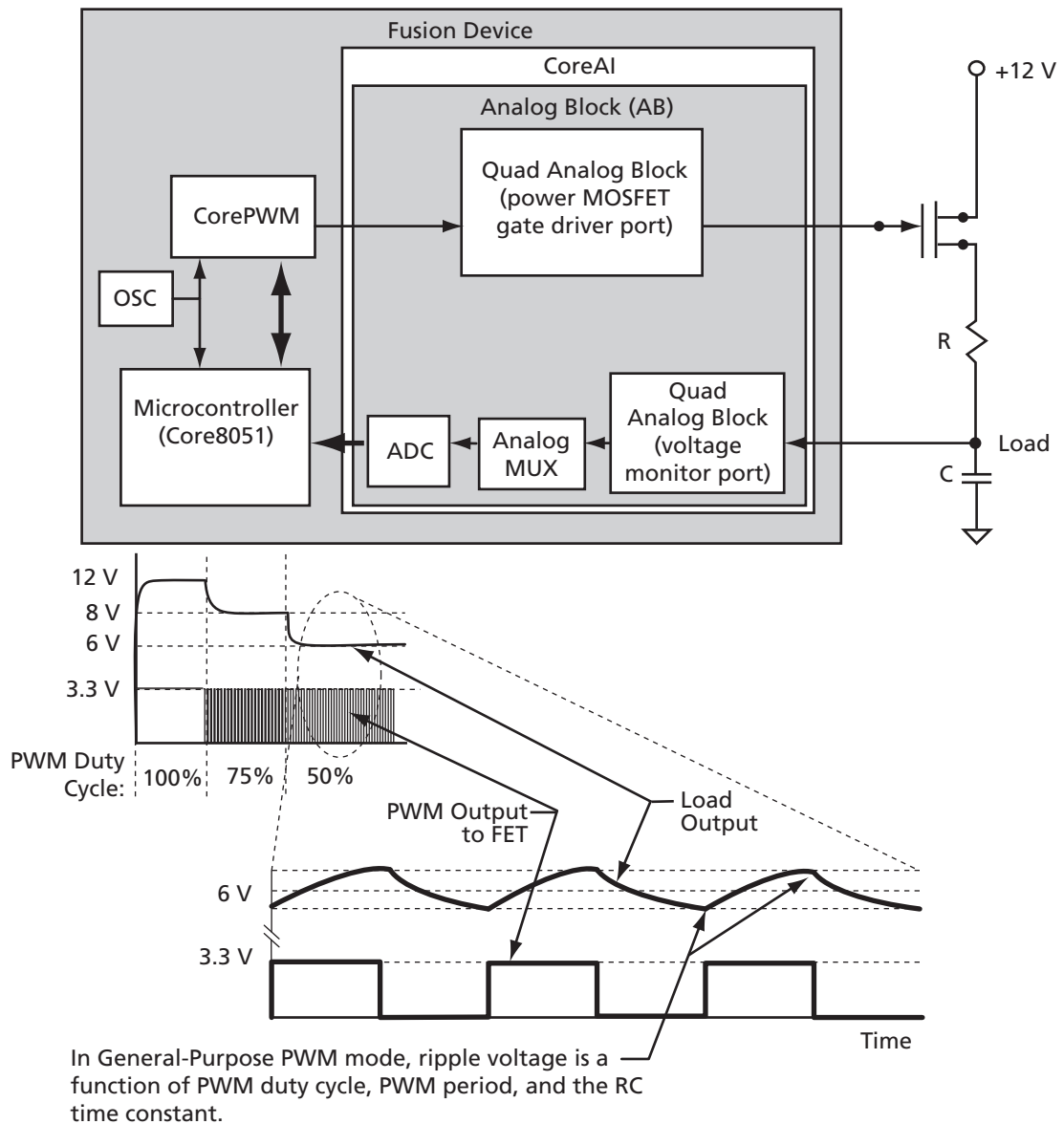


Figure 3-2 · DAC Application Using CorePWM in Fusion Device

The FET, in this case, is used to illustrate the ability to extend the DAC's output to 12 V. For most applications, 3.3 V is sufficient. Higher clock speeds (and therefore lower ripple) can be achieved by driving the RC filter with a general purpose TTL output.

Using Low Ripple DAC mode has the added benefit of requiring a smaller time constant for the filter, which allows for smaller R and C components to be used. A Low Ripple DAC calculator is available to assist in determining the ideal values for R and C.

Software Driver

Drivers for CorePWM are available via the Firmware Catalog tool provided with Libero IDE. For more information on the Firmware Catalog, refer to www.actel.com/products/software/firmwarecat/default.aspx.

List of Document Changes

The following table lists critical changes that were made in the current version of the document.

Previous Version	Changes in Current Version (5020113-1)	Page
5020113-1	Updated core version to v4.1.	N/A
5020113-0	Updated “Utilization and Performance” tables.	6–9
	Added low-cost TACHOMETER solution with up to 16 digital inputs.	N/A
	Added center-aligned PWM support.	22
	Updated tool flow to support Libero IDE v8.5 and SmartDesign.	25
	Updated Figure 1-3, Figure 1-5, and Figure 1-6 in the “Configuration Example” section.	21, 22, 23
	Updated Figure 3-2.	30
	Updated the “Software Driver” section.	33

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Index

A

Actel

- electronic mail 37
- telephone 38
- web-based technical support 37
- website 37

APB interface timing 24

applications 29

C

configuration examples 21

contacting Actel

- customer service 37
- electronic mail 37
- telephone 38
- web-based technical support 37

CorePWM

- key features 5
- version 6

customer service 37

D

DAC 29

E

example

- 1 channel for low ripple DAC 26
- DAC application 30
- temperature monitor 29

F

functional blocks 11

I

importing into Libero IDE 27

M

modes

- General Purpose PWM 11

Low Ripple DAC 11

O

overview 5

P

parameters, Verilog and VHDL 14

place-and-route 28

port signals 12

product support 37–38

- customer service 37
- electronic mail 37
- technical support 37
- telephone 38
- website 37

R

register map 15

S

simulation 27

simulation flows 27

SmartDesign 25

software driver 33

supported interfaces 6

synthesis 28

T

technical support 37

tool flows 25

- importing into Libero IDE 27

- simulation 27

- SmartDesign 25

U

utilization and performance 6

W

web-based technical support 37



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