RN0081
Release Notes
CoreAXItoAHBL v3.6

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1 Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

1.1 Revision 10.0

Updated changes related to CoreAXItoAHBL v3.6.

1.2 Revision 9.0

Updated changes related to CoreAXItoAHBL v3.5.

1.3 Revision 8.0

Updated changes related to CoreAXItoAHBL v3.4.

1.4 Revision 7.0

Updated changes related to CoreAXItoAHBL v3.3.

1.5 Revision 6.0

Updated changes related to CoreAXItoAHBL v3.2.

1.6 Revision 5.0

Updated changes related to CoreAXItoAHBL v3.1.

1.7 Revision 4.0

Updated changes related to CoreAXItoAHBL v3.0.

1.8 Revision 3.0

Updated changes related to CoreAXItoAHBL v2.2.

1.9 Revision 2.0

Updated changes related to CoreAXItoAHBL v2.1.

1.10 Revision 1.0

The first publication of this document. Created for CoreAXItoAHBL v2.0.

Contents

2 CoreAXItoAHBL v3.6

2.1 Overview

These release notes accompany the production release of CoreAXItoAHBL. This document provides details about the features, enhancements, system requirements, supported families, implementations, and known issues and workarounds.

2.2 Features

- Provides an interface (bridge) between the Advanced eXtensible Interface (AXI) domain and Advanced High-performance Bus Lite (AHB-Lite) domain
- Supports both AXI3 and AXI4 protocol
- Makes alternate AXI write and AXI read transactions possible
- Supports AXI data bus width of 32-bits, with transfer size of 32/16/8 bit
- Supports AXI data bus width of 64-bits, with transfer size of 64/32/16/8 bit
- Maximum number of AXI beats or transfers of 256 when AXI4 interface is selected
- Maximum number of AXI beats or transfers of 16 when AXI3 interface is selected
- Supports unaligned AXI write / read transactions
- Permits the AXI and AHBL clocks to be derived from asynchronous sources
- Supports narrow transfers for the last transfer in AXI write transactions using write strobes
- Provides ERROR/OKAY response for every AXI master transaction
- Supports AHB data bus width of 32-bits
- Prevents sequential AHBL transfers from crossing 1 KB boundaries

2.3 Delivery Types

CoreAXItoAHBL is freely distributed with Microsemi Libero® System-on-Chip (SoC). Complete HDL source code is provided for the core and testbenches.

2.4 Supported Families

CoreAXItoAHBL is a generic core and supports all the device families.

2.5 Supported Tool Flows

CoreAXItoAHBL requires Libero v11.0 or later.

Note: CoreAXItoAHBL is compatible with Libero SoC and Libero SoC PolarFire. Unless specified otherwise, this document uses the name Libero to identify Libero SoC and Libero SoC PolarFire.

2.6 Installation Instructions

The CoreAXItoAHBL CPZ must be installed into Libero software. This is done automatically through the Catalog update function in Libero, or the CPZ file can be manually added using the **Add Core** catalog feature. Once the CPZ file is installed in Libero, the core can be configured, generated, and instantiated within SmartDesign for inclusion in the Libero project. For more information, see the *Knowledge Based article*.

To know how to create SmartDesign project using the IP cores, refer to the *SmartDesign User guide*.

2.7 Documentation

This release contains a copy of the *CoreAXItoAHBL Handbook*. The handbook, describes the core functionality and gives step-by-step instructions on how to simulate, synthesize, and place-and-route this core, and also implementation suggestions. Refer to the *Libero SoC Online Help* for instructions on obtaining IP documentation.

For updates and additional information about the software, devices, and hardware, visit the Intellectual Property pages on the Microsemi SoC Products Group website: visit:

http://www.microsemi.com/products/fpga-soc/design-resources/ip-cores.

2.8 Supported Test Environments

The following test environments are supported:

- VHDL user testbench
- Verilog user testbench

2.9 Resolved Issues in the v3.6 Release

Table 1 • **Resolved Issues in the v3.6 Release**

SAR Number	Changes
115706	Added AXI4 support.
115705	Provided option to select between AHB Mirror Slave BIF or AHB Master BIF when core is instantiated in Libero SmartDesign.
115867	Added memory map support.

2.10 Resolved Issues in the v3.5 Release

Table 2 • **Resolved Issues in the v3.5 Release**

SAR Number	Changes
108962	Added support for 32bit AXI data interface.

2.11 Resolved Issues in the v3.4 Release

Table 3 • **Resolved Issues in the v3.4 Release**

SAR Number	Changes
106317	Fixed the single read transaction failure issue, when AXI and AHB clocks are asynchronous and ACLK:HCLK clock ratio is more than 2:1.

2.12 Resolved Issues in the v3.3 Release

Table 4 • **Resolved Issues in the v3.3 Release**

SAR Number	Changes
96561	Enhance core to facilitate the use of CoreAXItoAHBL with MiV RV32 AXI cores.
99662	Repackage core as a generic core.

2.13 Resolved Issues in the v3.2 Release

Table 5 • **Resolved Issues in the v3.2 Release**

SAR Number	Changes
90363	CoreAXItoAHBL need support for 16-bit and 8-bit AXI data transfer size.

2.14 Resolved Issues in the v3.1 Release

Table 6 • **Resolved Issues in the v3.1 Release**

SAR Number	Changes
82615	CoreAXItoAHBL need support for 32-bit AXI data transfer size.

2.15 Resolved Issues in the v3.0 Release

Table 7 • **Resolved Issues in the v3.0 Release**

SAR Number	Changes
69879	Complete re-design of the core. Unaligned address support added as part of the re-design.

2.16 Resolved Issues in the v2.2 Release

Table 8 • **Resolved Issues in the v2.2 Release**

SAR Number	Changes
58944	The core mishandles AXI bursts.

2.17 Resolved Issues in the v2.1 Release

Table 9 • **Resolved Issues in the v2.1 Release**

SAR Number	Changes
57249	RValid generation depending on RReady.

2.18 Discontinued Features and Devices

There are no discontinued features for this release.

2.19 Known Limitations and Workarounds

This release does not support the following:

- Narrow transfers using write strobes are not permitted for fixed address, AXI write transactions. For example, WSTRB = 8'h7F (for 64-bit transfers), WSTRB = 8'h07 (for 32-bit transfers), and WSTRB = 8'h01 (for 16-bit transfers).
- Sparse assertion of the write strobes (holes in the write strobes) are not supported by the core. For example, WSTRB = 8'h5F (for 64-bit transfers) and WSTRB = 8'h05 (for 32-bit transfers).