RN0239
Release Notes
CoreAXItoAXIConnect v2.0

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1 Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

1.1 Revision 1.0

This is the first publication of this document. Created for CoreAXItoAXIConnect v2.0.

Contents

2 CoreAXItoAXIConnect

This release notes accompanies the production release of CoreAXItoAXIConnect IP Core. This document provides details about the features, system requirements, supported families, implementations, and known issues and workarounds.

2.1 Key Features

This IP is used as a connector between the two CoreAXI4Interconnect modules. An AXI to AXI Connector that connects a slave interface of one CoreAXI4Interconnect module with the master interface of another CoreAXI4Interconnect module with no intervening logic.

2.2 Delivery Types

CoreAXItoAXIConnect is licence free.

2.2.1 Register Transfer Level (RTL)

The complete RTL source code is provided for the core.

2.3 Supported Families

The following list of families support are supported:

- PolarFire® SoC
- PolarFire®
- SmartFusion®2
- IGLOO®2
- RTG4™

2.4 Supported Tool Flows

Requires Libero® System-on-Chip (SoC) v12.2 or later.

2.5 Installation Instructions

The CoreAXItoAXIConnect CPZ file must be installed into Libero software. This is done automatically through the Catalog update function in Libero, or the CPZ file can be manually added using the **Add Core** catalog feature. Once the CPZ file is installed in Libero, the core can be configured, generated, and instantiated within SmartDesign for inclusion in the Libero project. For more information, see the *Knowledge Based article*.

To know how to create SmartDesign project using the IP cores, refer to the *SmartDesign User guide*.

2.6 Documentation

This release contains a copy of the CoreAXItoAXIConnect Handbook. The handbook describes the core functionality and gives step-by-step instructions on how to simulate, synthesize, and place-and-route this core and implementation suggestions.

For updates and additional information, visit the Intellectual Property pages on the Microsemi SoC Products Group website: visit:

http://www.microsemi.com/products/fpga-soc/design-resources/ip-cores.

2.7 Known Issues and Workarounds

There are no known limitations and workarounds for CoreAXItoAXIConnect.

2.8 Resolved Issues

No SARs - Initial Release.