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## CoreJTAGDebug 4.0 Release Notes

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### Overview

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These release notes accompany the production release of CoreJTAGDebug v4.0. They provide details about the features, enhancements, system requirements, supported families, implementations, and known issues and workarounds.

### Features

CoreJTAGDebug has the following key features:

- Provides the fabric access to the JTAG interface through the JTAG TAP.
- Provides the fabric access to the JTAG interface through the GPIO pins.
- Configures the IR Code support for the JTAG tunneling.
- Supports the linking of multiple devices through the JTAG TAP.
- Supports the multi-processor debugging.
- Promotes separate clock and reset signals to the low-skew routing resources.
- Supports both active-low and active-high target resetting.
- Supports the JTAG Security Monitor Interface (UJTAG\_SEC) for PolarFire devices.

### Delivery Types

No license is required to use CoreJTAGDebug. Complete RTL source code is provided for the core and testbenches.

### Supported Families

- PolarFire®
- RTG4™
- IGLOO®2
- SmartFusion®2
- SmartFusion®
- ProASIC3/3E/3L
- IGLOO
- IGLOOe/+

### Supported Tool Flows

CoreJTAGDebug v4.0 requires Libero® System-on-Chip (SoC) v12.5 or later.

### Installation Instructions

The CoreJTAGDebug CPZ file must be installed into Libero software. This is done automatically through the Catalog update function in Libero, or the CPZ file can be manually added using the Add Core catalog feature. Once the CPZ

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file is installed in Libero, the core can be configured, generated, and instantiated within SmartDesign for inclusion in the Libero project.

Refer to the [Libero SoC Online Help](#) for further instructions on core installation, licensing, and general use.

## Documentation

This release contains a copy of the CoreJTAGDebug user guide. The user guide describes the IP core functionalities and provides step-by-step instructions on how to simulate, synthesize, and place-androute this IP core, and also provides implementation solutions. Refer to the [Libero SoC Online Help](#) for further instructions on obtaining IP documentation.

For updates and additional information about the software, devices, and hardware, visit the **Intellectual Property** pages on the **Microchip FPGA Products Group** website: visit: [www.microsemi.com/products/fpga-soc/design-resources/ip-cores](http://www.microsemi.com/products/fpga-soc/design-resources/ip-cores).

## Supported Test Environments

A Verilog testbench is packaged with CoreJTAGDebug.

## Release History

The following table lists the release history for CoreJTAGDebug.


**Table 1. Release History**

Version	Date	Changes
4.0	April 2021	The following is the summary of changes in this version: <ul style="list-style-type: none"><li>• Added support for the UJTAG_SEC macro.</li><li>• Replaced output signal TGT_TRSTB_x with TGT_TRST_x and TGT_TRSTN_x, with only one appearing in the smart design depending on the active level configured from GUI.</li></ul>
3.1	May 2019	Added BUFD macros for PolarFire family and removed CLKINT macro's from RTL.
3.0	September 2018	Enhanced interface and Device chaining support. Also added GPIO debugging.
1.0	November 2016	Initial release.

## Known Limitations and Workarounds

For RTG4, the following DRC warning displays post-synthesis with a list of clocks that are not radiation hardened.

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	The following clocks or resets are driven by fabric-generated or local nets and are not single event transient (SET) mitigated.
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This warning can be ignored as CoreJTAGDebug is only used for system development purposes and will not be used in a radiation environment.

## Revision History

Revision	Date	Description
A	April 2021	<p>The following is the list of changes in revision A of the document:</p> <ul style="list-style-type: none"><li>• The document was updated for CoreJTAG 4.0 release.</li><li>• The document was migrated to the Microchip template.</li><li>• The document number was updated to DS50003146A from 51300172.</li><li>• Added support for UJTAG_SEC for PolarFire.</li><li>• Replaced output signal TGT_TRSTB_x with TGT_TRST_x and TGT_TRSTN_x, with only one appearing in the smart design depending on the active level configured from GUI.</li></ul>
3.0	May 2019	<p>This section is updated for CoreJTAGDebug v3.1 release. The major changes in this release are:</p> <ul style="list-style-type: none"><li>• Added BUFD macros for PolarFire family and removed CLKINT macro's from RTL.</li><li>• Removed CLKINT macros around uj_jtag module because these are now added automatically in Libero SoC v12.1.</li></ul>
2.0	September 2018	<p>This section is updated for CoreJTAGDebug v3.0 release. The major changes in this release are:</p> <ul style="list-style-type: none"><li>• Support is available for multiple JTAG devices through FlashPro header and through GPIO. For more information about device chaining.</li><li>• Support is available for multiple UJ_JTAG devices.</li></ul>
1.0	November 2016	<p>Revision 1.0 was the first publication of this document. It was created for CoreJTAGDebug v2.0.</p>

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