
CoreReset_PF v2.1 Release Notes

This document accompanies the production release for CoreReset_PF v2.1. It describes the features of the initial release of the IP core. It also has information about system requirements, supported families, known issues and workarounds.

Key Features

Following is the key feature:

- Synchronous negation of resets to ensure recovery time of downstream flip flops is met.

Delivery Types

No license is required to use CoreReset_PF. Complete RTL source code is provided for the core.

Supported Families

- PolarFire

Supported Tool Flows

Use Libero® System-on-Chip (SoC) PolarFire software v12.0 or later with this CoreReset_PF release.

Installation Instructions

The CoreReset_PF CPZ file must be installed in Libero. This is completed automatically through the Catalog update function in Libero, or the CPZ can be manually added using the **Add Core** catalog feature. Once installed in the Libero catalog, the core can be instantiated and configured.

Refer to the Using DirectCore in Libero IDE User Guide or [Libero SoC Online Help](#) for further instructions on core installation, licensing and general use.

Documentation

This release contains a copy of the CoreReset_PF handbook, which describes the core functionality, gives step-by-step instructions on how to synthesize, and place-and-route this core, and also provides implementation suggestions.

This document can be viewed by right-clicking on CoreReset_PF instantiation in SmartDesign and selecting **Help -> CoreReset_PF_HB.pdf**.

For more information about Intellectual Property, visit: <http://www.microsemi.com/products/fpga-soc/design-resources/ip-cores>. For updates and additional information about software, FPGAs, and hardware, visit: www.microsemi.com.

Release History

Table 1 Release History

Version	Date	Changes
2.1	December 2017	Included core in Peripheral section in Libero.
2.0	September 2017	Initial release.

Known Limitations

There are no known limitations associated with CoreReset_PF.



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