UG0640
User Guide
Bayer Interpolation

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1 Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

1.1 Revision 6.0

The following is a summary of changes in this revision.

- Updated Figure 2, page 4, Figure 4, page 9, Figure 5, page 9, Figure 8, page 11, Figure 9, page 12, Figure 10, page 12, Figure 11, page 12, and Figure 15, page 14.
- Added the following sections.
  - Key Features, page 3
  - Supported Families, page 3
- Added Table 2, page 6 through Table 4, page 7.
- Updated Table 3, page 6 and Table 5, page 7.
- Updated tables such Interfaces, page 5.
- Added the following sections.
  - License, page 9
  - Encrypted, page 9
  - RTL, page 9
- Replaced Figure 8, page 11.
- Updated Resource Utilization, page 16.
- Updated Testbench, page 10.
- Updated Simulation Results, page 15.
- Updated the Notes in Resource Utilization, page 16.

1.2 Revision 5.0

The following is a summary of changes in this revision.

- Updated Introduction, page 2.
- Updated Figure 1, page 2, Figure 2, page 4, Figure 4, page 9, and Figure 5, page 9.
- Updated tables such Interfaces, page 5.
- Updated Resource Utilization, page 16.
- Updated Testbench, page 10.
- Updated Simulation Results, page 15.

1.3 Revision 4.0

Updated the resource utilization.

1.4 Revision 3.0

Updated the testbench information.

1.5 Revision 2.0

The following is a summary of the changes in this revision.

- Added the Testbench section.

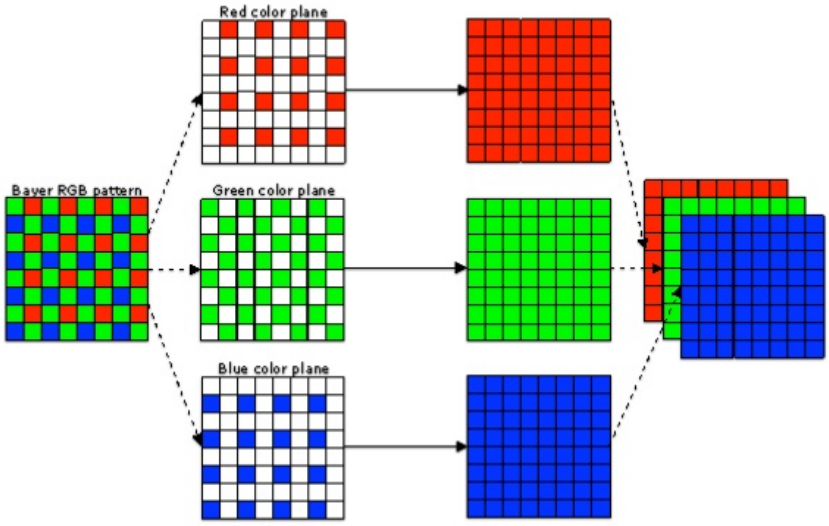
1.6 Revision 1.0

The first publication of this document.

2 Introduction

Bayer Interpolation coverts an image in Bayer color filter array format to RGB per pixel format. The following figure shows the demosaicing of a Bayer format image.

Figure 1 • **Demosaicing of Bayer format Image**



There are several standard interpolation methods. The simplest interpolation method is bilinear interpolation. The Bayer interpolation IP uses the bilinear interpolation methods to covert a Bayer format image to RGB format.

2.1 Bilinear Interpolation

The bilinear algorithm processes each pixel separately and finds out the missing components in it by applying linear interpolation to the available ones.

The formulas for calculating missing component at a particular pixel by considering 3x3 window are as follows.

Green component at red and blue pixel

$$G(i, j) = \frac{1}{4} \cdot \sum G(i + m, j + n)$$

where (m,n) = {(0,-1)(0,1)(-1,0)(1,0)}

Red component at blue pixel

$$R(i, j) = \frac{1}{4} \cdot \sum R(i + m, j + n)$$

where (i,j) = {(-1,-1)(-1,1)(1,-1)(1,1)}

Red component at green pixel

$$R(i, j) = \frac{1}{2} \cdot \sum R(i + m, j + n)$$

where (m,n) = {(0,-1)(0,1)} or (m,n) = {(-1,0)(1,0)}

Blue component at red pixel

$$B(i, j) = \frac{1}{4} \cdot \sum B(i + m, j + n)$$

where (m,n) = {(-1,-1)(-1,1)(1,-1)(1,1)}

Blue component at green pixel

$$B(i, j) = \frac{1}{2} \cdot \sum B(i + m, j + n)$$

where (m,n) = {(0,-1)(0,1)} or (m,n) = {(-1,0)(1,0)}

2.2 Key Features

- Converts color filter array to RGB using Bilinear Interpolation
- Uses Freeman Median Filtering
- Supports data width of 8, 10, and 12
- Supports 1 pixel and 4-pixel mode
- Supports Native and AXI4 Stream Video Interface for video data transfer
- Supports Native and AXI4-Lite Configuration Interface for parameter modification

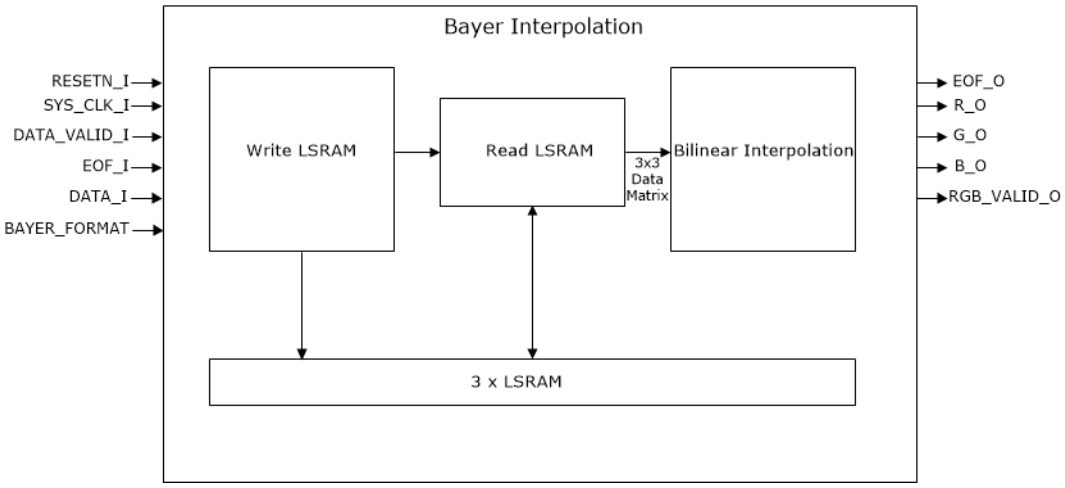
2.3 Supported Families

- PolarFire® SoC
- PolarFire®
- RTG4™
- IGLOO®2
- SmartFusion®2

3 Hardware Implementation

The following figure shows the block diagram of Bayer interpolation.

Figure 2 • **Bayer Interpolation Block Diagram**



The Bayer interpolation IP consists of the following three submodules.

- Write LSRAM, page 4
- Read LSRAM, page 4
- Bilinear Interpolation, page 4

3.1 Write LSRAM

The raw image data coming from camera sensor is written into 3 different LSRAM. The 1st, 4th, 7th …… line of the frame are written to LSRAM1, the 2nd, 5th, 8th …… line of the frame are written into LSRAM2 and the 3rd, 6th, 9th ….. line of the frame are written into LSRAM3. The LSRAM addresses and write enable signals are generated by write LSRAM submodule.

3.2 Read LSRAM

The read submodule generates the read enable signals and the addresses to read from LSRAM. It also has the 3x3 window logic which reads the 3x3 window from LSRAMs and feeds to the bilinear interpolation block. The pixel at which the color components are to be computed is placed at the center of the 3x3 window. Then the window slides right to compute the value of the next pixel in the line.

For the first line of the frame, the first row of the 3x3 window is all zeros, the second row is LSRAM1 data and third row is LSRAM2 data. For the second line, the first row is LSRAM1 data, second row is LSRAM2 data and third row is LSRAM3 data. For the third line, the first row is LSRAM2 data, second row is LSRAM3 data and third row is LSRAM1 data and so on.

3.3 Bilinear Interpolation

The bilinear interpolation module computes the R, G and B value for the center element of the 3x3 data matrix coming from read LSRAM module. It computes the R, G and B value based on the bilinear interpolation formulae described in Bilinear Interpolation, page 2.

The Bayer interpolation IP automatically detects the video resolution. The IP uses the data from first frame to compute the horizontal and vertical resolution. As a result, the IP does not generate output (data valid is zero) during the first frame.

4 Interfaces

This section describes the input/output ports and configuration parameters of the Bayer Interpolation IP.

4.1 Ports

The following tables show the input and output ports of Bayer interpolation.

Table 1 • **Input and Output Ports for 1 pixel Native Video Mode**

Port Name	Type	Width	Description
RESETN_I	Input	1 bit	Active low asynchronous reset signal to design
SYS_CLK_I	Input	1 bit	System clock
DATA_VALID_I	Input	1 bit	Asserted high when input data is valid
EOF_I	Input	1 bit	End of frame input signal
DATA_I	Input	G_DATA_WIDTH bits	Bayer data input
BAYER_FORMAT	Input	2 bits	BAYER_FORMAT = 0, then Bayer format is RGGB BAYER_FORMAT = 1, then Bayer format is GRBG BAYER_FORMAT = 2, then Bayer format is GBRG BAYER_FORMAT = 3, then Bayer format is BGGR
RGB_VALID_O	Output	1 bit	Asserted high when output data is valid
R_O	Output	G_DATA_WIDTH bits	Provides the red component output
G_O	Output	G_DATA_WIDTH bits	Provides the green component output
B_O	Output	G_DATA_WIDTH bits	Provides the blue component output
EOF_O	Output	1 bit	End of frame output. The first EOF_I is skipped and subsequent EOF_I inputs are passed through.

Table 2 • **Input and Output Ports for 4 pixel Native Video Interface**

Port Name	Type	Width	Description
RESETN_I	Input	1 bit	Active low asynchronous reset signal to design
SYS_CLK_I	Input	1 bit	System clock
DATA_VALID_I	Input	1 bit	Asserted high when input data is valid
EOF_I	Input	1 bit	End of frame input signal
DATA_I	Input	G_PIXELS*G_DATA_WIDTH bits	Bayer data input
BAYER_FORMAT	Input	2 bits	BAYER_FORMAT = 0, then Bayer format is RGGB BAYER_FORMAT = 1, then Bayer format is GRBG BAYER_FORMAT = 2, then Bayer format is GBRG BAYER_FORMAT = 3, then Bayer format is BGGR
RGB_VALID_O	Output	1 bit	Asserted high when output data is valid.
EOF_O	Output	1 bit	End of frame output. The first EOF_I is skipped and subsequent EOF_I inputs are passed through.
DATA_O	Output	3*G_PIXELS*G_DATA_WIDTH bits	Output Video Data

Table 3 • **Input and Output Ports for AXI4 Stream Video Interface**

Port Name	Type	Width	Description
RESETN_I	Input	1 bit	Active low asynchronous reset signal to design
SYS_CLK_I	Input	1 bit	System clock
TREADY_O	Output	1 bit	Output Slave ready
TDATA_I	Input	G_PIXELS*G_DATA_WIDTH bit	Input Video Data
TVALID_I	Input	1 bit	Input Video Valid
TUSER_I	Input	4 bits	bit 0 = End of frame bit 1 = unused bit 2 = unused bit 3 = unused
TDATA_O	Output	G_PIXELS*G_DATA_WIDTH bit	Output Video Data
TVALID_O	Output	1 bit	Output Video Valid
TUSER_O	Output	4 bits	bit 0 = End of frame bit 1 = 0 bit 2 = 0 bit 3 = 0
TSTRB_O	Output	G_DATA_WIDTH/8	Output Video Data strobe
TKEEP_O	Output	G_DATA_WIDTH/8	Output Video Data Keep
TLAST_O	Output	1 bit	Output End of frame

IP has one specific register through which user can dynamically control the operation of IP.

Table 4 • **Register Map and Description**

Address (hex)	Register name	Type	Description
0x000	BAYER_ADDR_0	Read/Write	BAYER_FORMAT = 0, then Bayer format is RGGB BAYER_FORMAT = 1, then Bayer format is GRBG BAYER_FORMAT = 2, then Bayer format is GBRG BAYER_FORMAT = 3, then Bayer format is BGGR

4.2 Configuration Parameters

The following table shows the description of the configuration parameters used in the hardware implementation of Bayer Interpolation. These are generic parameters and can be varied as per the requirement of the application.

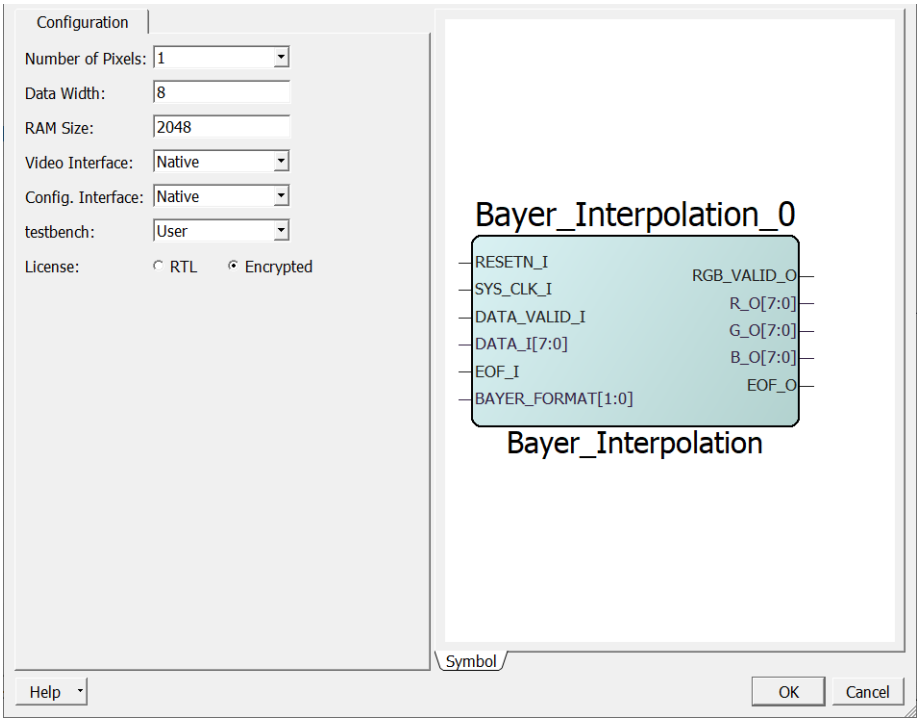
Table 5 • **Configuration Parameters**

Name	Description
Number of Pixel	Number of pixels per clock 1 and Number of pixels per clock 4
Data Width	Width of each pixel
RAM Size	Size of the RAM to store one horizontal line. Choose values which are powers of 2, such as 2048, and 4096
Video Interface	Native Video Interface and AXI4 Stream Video Interface
Configuration Interface	Native Configuration Interface and AXI4-Lite Configuration Interface

4.3 IP Configurator

The IP configurator is shown in the following figure.

Figure 3 • **IP Configurator**



5 Timing Diagrams

The following figure shows the timing diagram of Bayer Interpolation.

Figure 4 • **Bayer Interpolation Showing first and second frame**

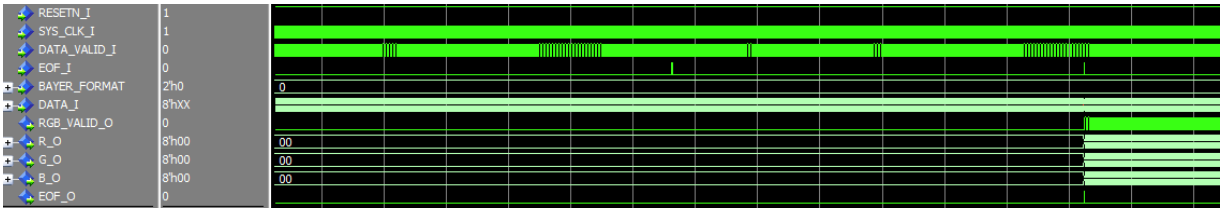
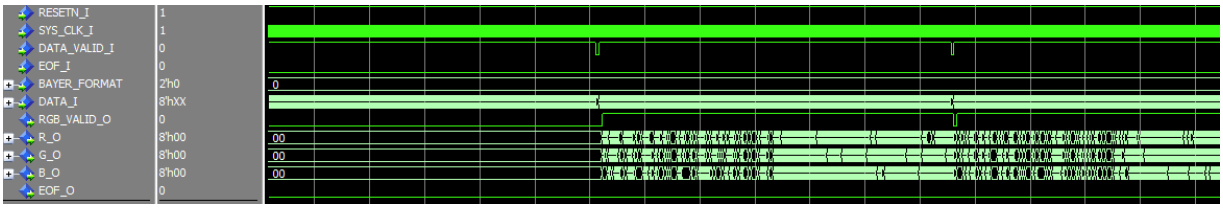


Figure 5 • **Bayer Interpolation Showing first three lines of second frame**



5.1 License

Bayer Interpolation clear RTL is license locked, and the encrypted RTL available for free.

5.1.1 Encrypted

Complete RTL code is provided for the core, allowing it to be instantiated with the SmartDesign tool. Simulation, synthesis, and layout can be performed within Libero® System-on-Chip (SoC). The RTL code is encrypted for the core.

5.1.2 RTL

Complete RTL source code is provided for the core.

6 Testbench

A testbench is provided to check the functionality of Bayer Interpolation IP. This testbench is working only in Native Video Interface and Native Configuration Interface with a data width of 8, and the number of pixels is 1. The following table shows the parameters that can be configured according to the application.

Table 6 • **Testbench Configuration Parameters**

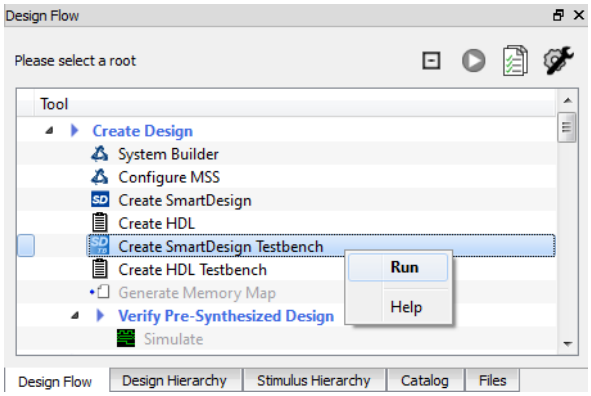
Name	Description
CLKPERIOD	Clock Period
g_PIXELS	Number of pixels per clock
g_DATAWIDTH	Width of each pixel
g_DISPLAY_RESOLUTION	Horizontal resolution
g_VERT_DISPLAY_RESOLUTION	Vertical resolution
WAIT	Number of clock cycles delay between transmission of two input lines
IMAGE_FILE_NAME	Input (image) file name

6.1 Simulation Steps

The following steps describe how to simulate the core using the testbench:

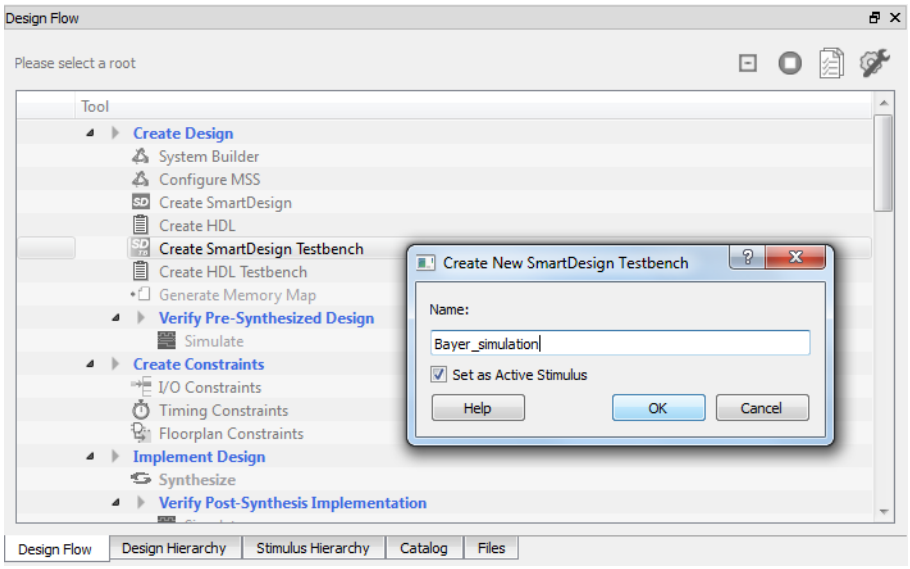
1. On Libero SoC Design Flow, expand **Create Design** and open **Create SmartDesign Testbench** as shown in the following figure.

Figure 6 • **Opening New SmartDesign Testbench**



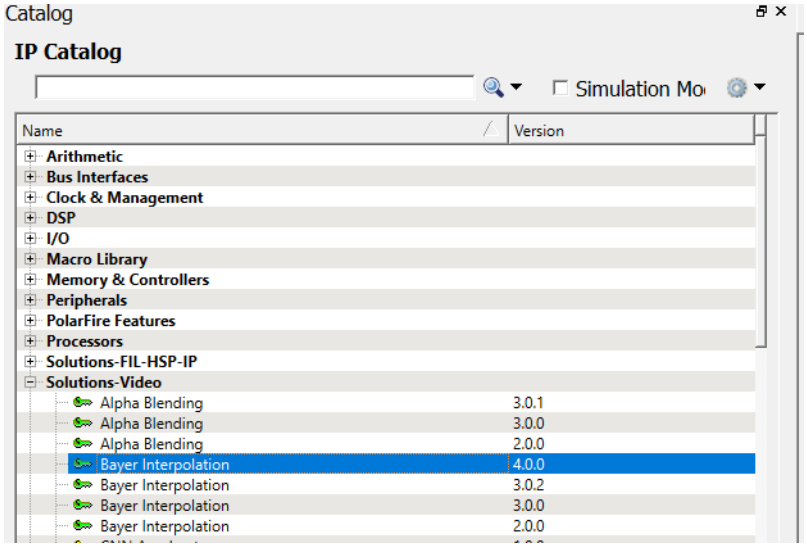
2. Enter a name for the SmartDesign testbench and click **OK** as shown in Figure 7, page 11.
   The SmartDesign testbench is created, and a canvas appears to the right of the Design Flow pane.

Figure 7 • **Creating a SmartDesign Testbench**



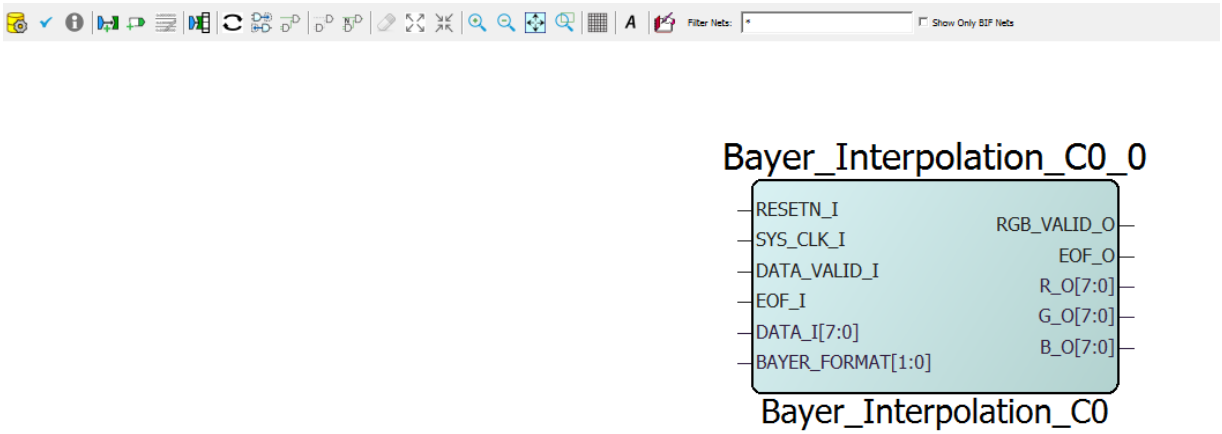
3. Go to Libero SoC Catalog > View > Windows > Catalog, and then expand **Solutions-Video**.

Figure 8 • **Bayer Interpolation Core in Libero SoC Catalog**



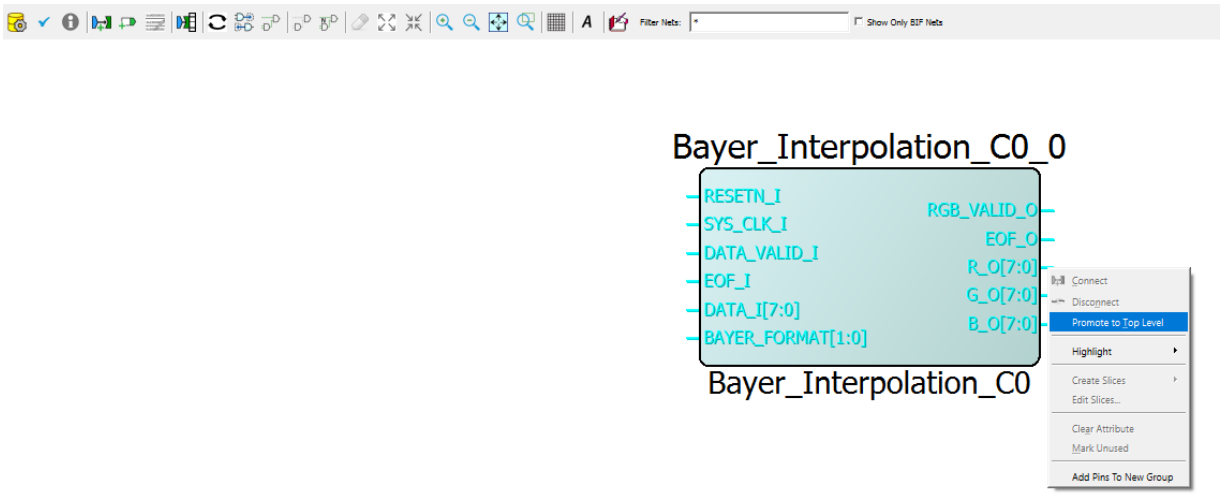
4. Drag and drop the Bayer IP core in to the new SmartDesign testbench canvas. The IP appears as shown in the following figure.

Figure 9 • **Bayer Interpolation Core on SmartDesign Testbench Canvas**



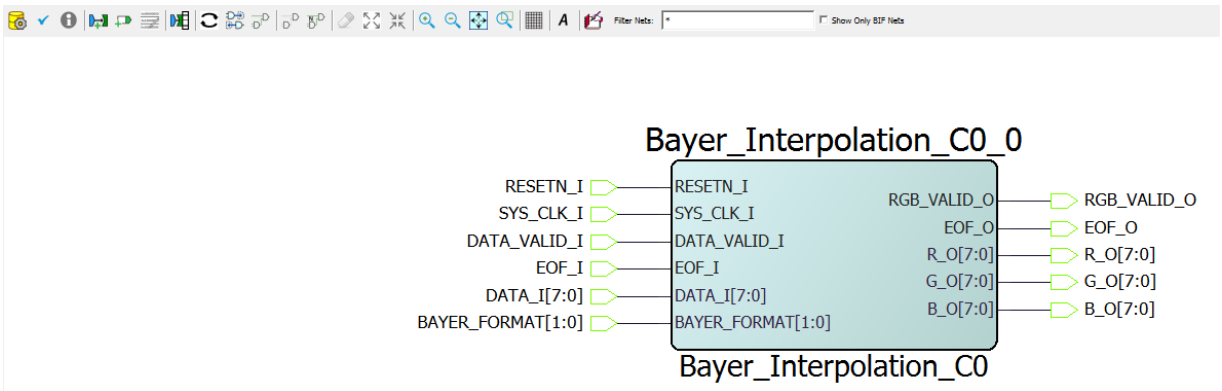
5. Select all of the ports and promote them to top level as shown in the following figure.

Figure 10 • **Promote to Top-Level**



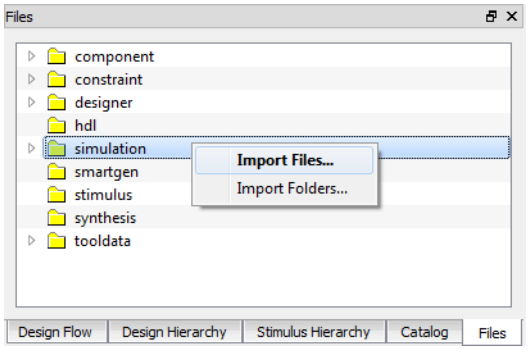
6. To generate the testbench component, select **Generate Component** from the SmartDesign toolbar, as highlighted in the following figure.

Figure 11 • **Generating Bayer Component with Ports Promoted to Top Level**



7. Go to the **Files** tab and select **simulation** > **Import Files** as shown in the following figure.

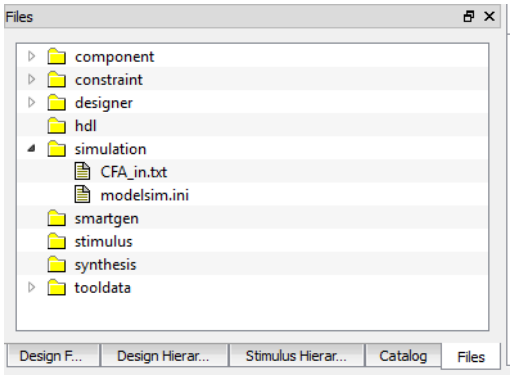
Figure 12 • **Import Files**



8. Import the CFA file from the following path:
   `..\<Project_name>\component\Microsemi\SolutionCore\Bayer_Interpolation\4.0.0\Stimulus`
   To import a different file, browse the folder that contains the required file, and click **Open**.

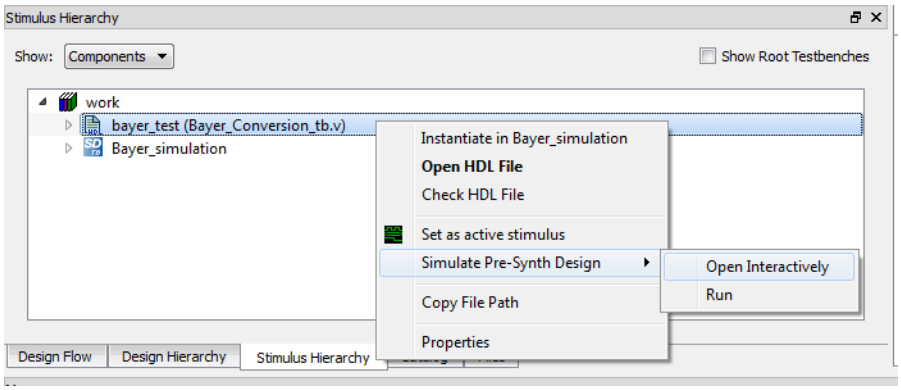
The imported file is listed under simulation as shown in the following figure.

Figure 13 • **Imported File**



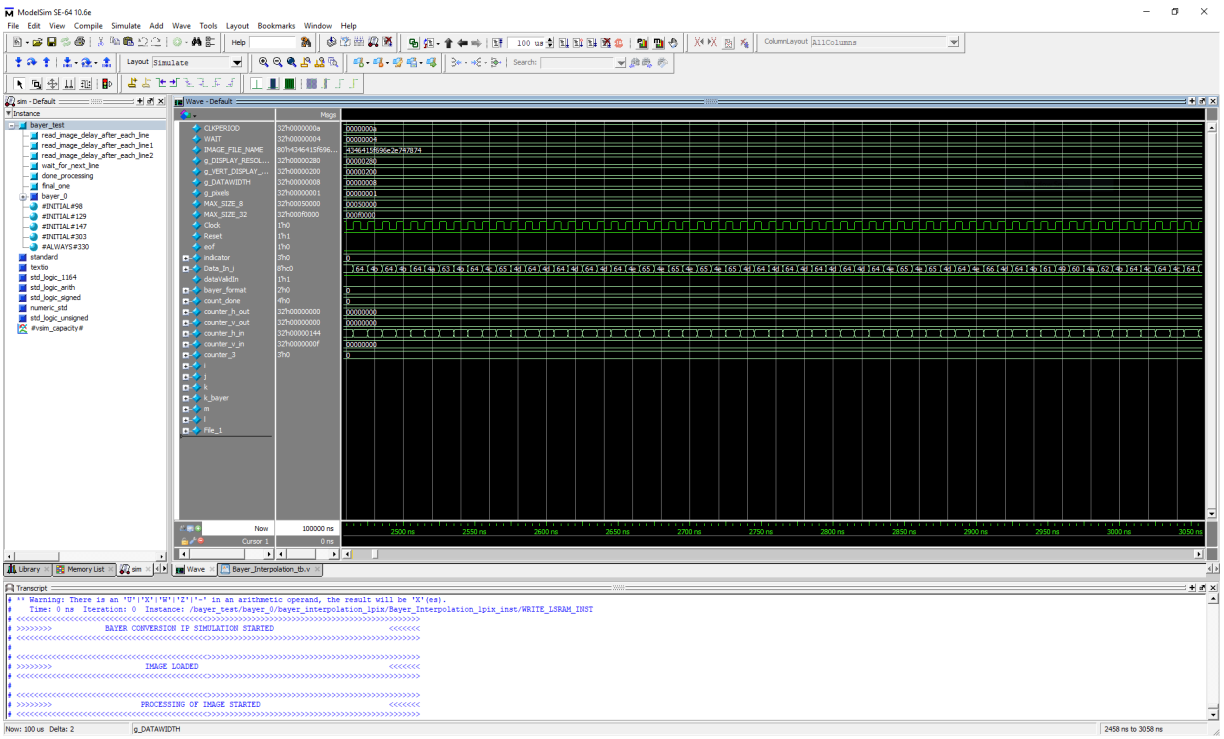
9. Go to the **Stimulus Hierarchy** tab and select **bayer_test (Bayer_interpolation_tb.v)** > **Simulate Pre-Synth Design** > **Open Interactively**. The IP is simulated for one frame.

Figure 14 • **Simulating Pre-Synthesis Design**



ModelSim opens with the testbench file as shown in the following figure.

Figure 15 • **ModelSim Simulation Window**



If the simulation is interrupted due to the runtime limit specified in the DO file, use the `run -all` command to complete the simulation.

The testbench output image file appears in the `Files/simulation` folder after the simulation completes.

7 Simulation Results

The following figure shows the input Bayer image.

Figure 16 • **Input Bayer Image**

Output RGB Image

The following figure shows the output RGB image.

Figure 17 • **Output RGB Image**

8 Resource Utilization

Bayer Interpolation is implemented on the PolarFire® FPGA (MPF300TS - 1FCG1152E package). The following figure shows the resource utilization report after synthesis.

Table 7 • **Resource Utilization of Number of Pixels = 1**

Resource	Usage
DFFs	306
4LUTs	707
LSRAM18K	3
MACC	0

Note: For Data Width = 8, RAM Size = 2048 and Number of Pixels = 1.

Table 8 • **Resource Utilization of Number of Pixels = 4**

Resource	Usage
DFFs	450
4LUTs	1572
LSRAM18K	12
MACC	0

Note: For Data Width = 8, RAM Size = 2048 and Number of Pixels = 4.