CoreAXItoAHBL v2.2 Release Notes

This release note accompanies the production release for the CoreAXItoAHBL v2.2 IP core. This release note document provides details about the features, supported families, system requirements, implementations, and known limitations and workarounds.

Features

CoreAXItoAHBL is a highly configurable core and has the following features:

- Provides an interface (bridge) between the advanced extensible interface (AXI) domain and advanced high-performance bus (AHB) domain
- Makes alternate AXI write transaction and AXI read transactions possible
- Supports AXI data bus width of 64-bits, maximum burst size upto 8 bytes and maximum number of beats/transfer of 16
- Supports AHB data bus width of 32-bits
- Provides ERROR/OKAY response for every AXI master transaction
- Provides output signal to indicate whether the incoming AXI read/write address is aligned or unaligned address

Delivery Types

CoreAXItoAHBL is licensed as register transfer level (RTL).

RTL

Complete RTL source code is provided for the core and test benches.

Supported Families

- SmartFusion®2
- IGLOO®2

Supported Tool Flows

CoreAXItoAHBL v2.2 requires Libero® System-on-Chip (SoC) software v11.0 or later.

Installation Instructions

For the RTL version of the core, the FlexLM® license must be installed before the core can be exported. Consult the Libero SoC online help for the instructions on core installation and licensing.

Documentation

This release contains a copy of the *CoreAXItoAHBL handbook*, which describes the core functionality, gives step-by-step instructions on how to simulate, synthesize, and place-and-route this core provides implementation suggestions.

For updates and additional information about the software, devices, and hardware, visit the Intellectual Property pages on the Microsemi® website at: www.microsemi.com/soc.

Supported Test Environments

The following test environments are supported:

- Verilog User Testbench
- VHDL User Testbench

Release History

There are resolved issues in the CoreAXItoAHBL v2.2 release.

Table 1 Release History

Version	Date	Changes
2.2	September 2014	As listed in Table 2.
2.1	June 2014	As listed in Table 3.
2.0	February 2013	Initial release.

Resolved Issues in the v2.2 Release

Table 2 lists the software action requests (SARs) that were resolved in the CoreAXItoAHBL v2.2 release.

Table 2 Resolved SARs in CoreAXItoAHBL v2.2 Release

SAR	Description
58944	The core mishandles AXI bursts.

Resolved Issues in the v2.1 Release

Table 2 lists the software action requests (SARs) that were resolved in the CoreAXItoAHBL v2.1 release.

Table 3 Resolved SARs in CoreAXItoAHBL v2.1 Release

SAR	Description
57249	RValid generation depending on RReady.

Discontinued Features and Devices

There are no discontinued features for the release of CoreAXItoAHBL v2.2.

Known Limitations

This release of CoreAXItoAHBL v2.2 does not support the following:

- During AXI-AHB write transfers, some of the byte lanes may not to be valid. In such case, the AXI write transaction is translated into multiple AHBL write transactions of shorter size as per the valid byte lane.

  This feature is currently not supported in this release.

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