RN0103
Release Notes
CoreMMC v3.1

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1 Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

1.1 Revision 3.0

Added PolarFire® SoC support.

1.2 Revision 2.0

Updated changes related to CoreMMC v3.0.

- Added Multiple block support
- FIFO width changed from 8- to 32-bit
- DMA control signals asserted on a 32-bit basis
- Created BFM based user testbench
- Added VHDL support
- Added IGLOO®2 support

1.3 Revision 1.0

Revision 1.0 was the first publication of this document. Created for CoreMMC v2.0.

2 CoreMMC v3.1 Release Notes

This document accompanies the release of CoreMMC v3.1. It describes the features and enhancements. It also contains the information on system requirements, supported families, implementations, known issues and workarounds, and resolved issues with the previous version.

2.1 Features

CoreMMC has the following features:

- Up to 52 MHz MMC clock rate, making for a maximum of ~52 MBs throughput at 8-bit data width (Theoretical throughput of CoreMMC. Actual throughput will be affected by eMMC device throughput & AHB bandwidth)
- Configurable data bus widths
  - 1-/4-/8-bit
- Supports Block mode transfer:
  - Single block write
  - Multiple block write
  - Single block read
  - Multiple block read
- Cyclic Redundancy Check (CRC) protection for both commands and data transfers
- AHB-Lite compliant
  - Command, Response, Write, and Read Data registers for indirect access to MMC part
  - 8-/16-/32-bit AHB transfers
- Write DATA FIFO:
  - To decouple AHB from MMC bus for write data transfers
  - Depth configurable from 512 Bytes to 32 KBs
  - Overrun and Underrun error flags
- Read DATA FIFO:
  - To decouple AHB from MMC bus for read data transfers
  - Depth configurable from 512 Bytes to 32 KBs
  - Overrun and Underrun error flags
- Interrupt generation:
  - Command Sent and Response Received interrupts
  - Error flag interrupts
  - Single block write & read done interrupts
  - Multiple block write & read done interrupts
- Automatic Sleep mode for eMMC when clock pulled Low

2.2 Supported Interfaces

CoreMMC supports the following interfaces:

- AHB-Lite slave interface
- Interrupt request interface
- MMC master interface
- Peripheral Direct Memory Access (PDMA) interface

2.3 Delivery Types

A License is not required for using CoreMMC v3.1. Complete Verilog and VHDL source code is provided for the core and testbenches.

2.4 Supported Families

CoreMMC supports the following families:

- PolarFire® SoC
- PolarFire®
- IGLOO®2
- SmartFusion®2

2.5 Supported Tool Flows

CoreMMC supports the following tools:

- Libero System-on-Chip (SoC) software v11.1 or later

2.6 Installation Instructions

The CoreMMC CPZ file must be installed into Libero software. This is done automatically through the Catalog update function in Libero, or the CPZ file can be manually added using the **Add Core** catalog feature. Once the CPZ file is installed in Libero, the core can be configured, generated, and instantiated within SmartDesign for inclusion in the Libero project. For more information, see the *Knowledge Based article*.

To know how to create SmartDesign project using the IP cores, refer to *Libero SoC documents page* and use the latest SmartDesign user guide.

2.7 Documentation

This release contains a copy of the *CoreMMC Handbook*. The handbook, describes the core functionality and gives step-by-step instructions on how to simulate, synthesize, and place-and-route this core, and also implementation suggestions. Refer to *Libero SoC documents page* for instructions on obtaining IP documentation.

For updates and additional information, visit the Intellectual Property pages on the Microsemi SoC Products Group website: visit:

http://www.microsemi.com/products/fpga-soc/design-resources/ip-cores.

2.8 Supported Test Environments

- Verilog user testbench
- VHDL user testbench

2.9 Known Issues and Workarounds

CoreMMC does not support:

- Sequential mode transfers
- Stream Read and Stream Write
- ECC error correction (handled on the device side instead)
- Double Data Rate (DDR) for this release
- Boot mode
- VHDL 2008 syntax must be selected when using VHDL source code

2.10 Resolved Issues in v3.1 Release

There were no software action requests (SARs) resolved. PolarFireSoC support is added.

2.11 Resolved Issues in the v3.0 Release

Table 1 lists the SARs that were resolved in the CoreMMC v3.0 release

Table 1 • **Resolved SARs in CoreMMC v3.0 Release**

SAR	Description
67363	Clock Register description updated in Handbook.
67461	Added multiple block support to increase CoreMMC throughput.
54007	VHDL support added.

2.12 Resolved Issues in the v2.0 Release

Initial release.