UG0656
User Guide
PWM Scaling v4.1

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Contents

Figures

Tables

1 Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

1.1 Revision 2.0

The following is a summary of the changes in revision 2.0 of this document.

- Added the IP version to the document title.
- Removed g_STD_IO_WIDTH configuration parameter from Configuration Parameter, page 4 and Resource Utilization, page 4.

1.2 Revision 1.0

Revision 1.0 is the first publication of this document.

2 Introduction

Pulse width modulation (PWM) scaling is used to scale down the voltages computed from the field oriented control (FOC) to fit within the PWM carrier wave magnitude range. It also adds a bias to shift negative voltages to positive level. The PWM scaling performs the following functions:

- Scaling of phase voltages according to the following equation:

$$V_{ph\_o} = ((pwm\_period\_i \times 32768 + pwm\_gain\_i \times V_{Ph\_i})/2)/65536$$

- To use the advantage of voltage boost provided by space vector modulation (SVM), pwm_gain_i can be multiplied by a factor of 1.15 as shown in the following equation:

$$pwm\_gain\_i = \frac{pwm\_period\_i \times 1182}{1024}$$

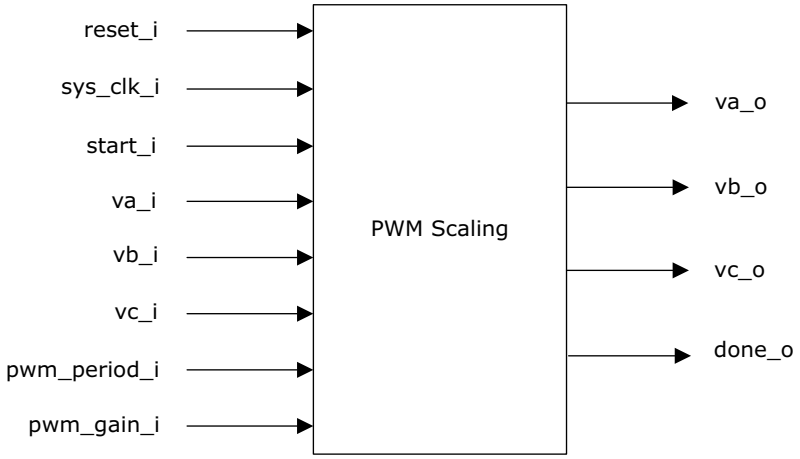
- Generates PWM with specified PWM frequency. PWM period that configures the PWM frequency is configured using the following equation:

$$pwm\_period = \frac{sys\_clock\ \ frequency}{2 \times pwm\ \ frequency}$$

3 Hardware Implementation

The following figure shows the block diagram of PWM scaling.

Figure 1 • **System-Level Block Diagram of PWM Scaling**



The PWM scaling calculates the scaled phase voltages. The number of clock cycles between the start_i and done_o is 4 x g_NO_MCYCLE_PATH constant. After a computation is triggered, the next start must be triggered only after 4 x g_NO_MCYCLE_PATH clock cycles.

3.1 Inputs and Outputs

The following table lists the input and output ports of PWM scaling.

Table 1 • **Inputs and Outputs of PWM Scaling**

Signal Name	Direction	Description
reset_i	Input	Active low asynchronous reset signal
sys_clk_i	Input	System clock
start_i	Input	A single bit start signal that must go high for one clock cycle to start PWM scaling computations
va_i	Input	Phase A voltage input
vb_i	Input	Phase B voltage input
vc_i	Input	Phase C voltage input
pwm_period_i	Input	PWM period value in number of system clock cycles
pwm_gain_i	Input	PWM gain input
va_o	Output	Scaled phase A voltage output
vb_o	Output	Scaled phase B voltage output
vc_o	Output	Scaled phase C voltage output
done_o	Output	Indicates completion of scaling operations is high for one clock cycle

3.2 Configuration Parameter

The following table shows the description of the configuration parameter used in the hardware implementation of PWM scaling. This is a generic parameter and can be varied as per the requirement of the application.

Table 2 • **Configuration Parameter**

Signal Name	Description
g_NO_MCYCLE_PATH	Defines the number of clock delays required before asserting the multiplier done signal.

3.3 Resource Utilization

PWM scaling is implemented on the SmartFusion®2 system-on-chip (SoC) field programmable gate array (FPGA) and IGLOO®2 devices. The following table lists the resource utilization report after synthesis.

Table 3 • **Resource Utilization Report of PWM Scaling**

Cell Usage	Count
Sequential elements	70
Combinational logic	50
MACC	1
RAM1Kx18	0
RAM64x18	0