UG0682

User Guide

Pattern Generator

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Microsemi

Power Matters.™

Contents

1 Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

1.1 Revision 1.0

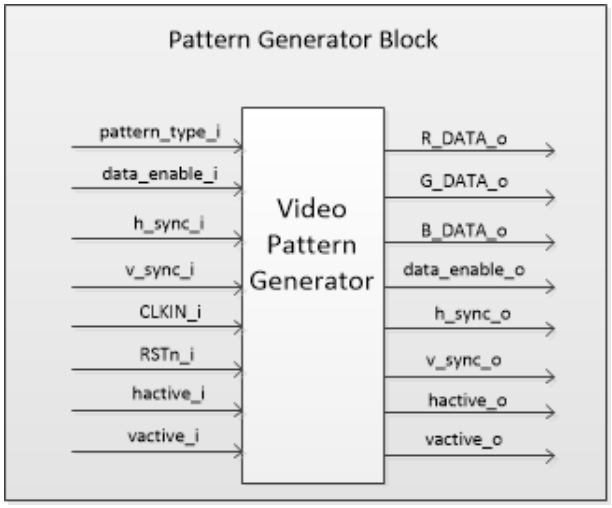
Revision 1.0 is the first publication of this document.

2 Introduction

The pattern generator IP generates the test patterns in RGB Video Format for troubleshooting and analyzing the complete video solutions. The test pattern IP generates following four different types of video test patterns.

- Color Bar pattern
- Solid Red
- Solid Green
- Solid Blue

Figure 1 • Top-Level Block Diagram of Pattern Generator



The pattern generator IP is configurable and can generate test patterns for any video resolution (1024x768, 1280x720, 1280x800 etc.) for which it is configured. For example if the video resolution is 1024x768 then the value of the parameter g_video_resolution is configured as 32'h400, similarly if the video resolution is 1280x720 then the parameter g_video_resolution is configured as 32'h500. The input signal pattern_type_i defines the type of the video pattern to be generated. If the value of input signal pattern type is

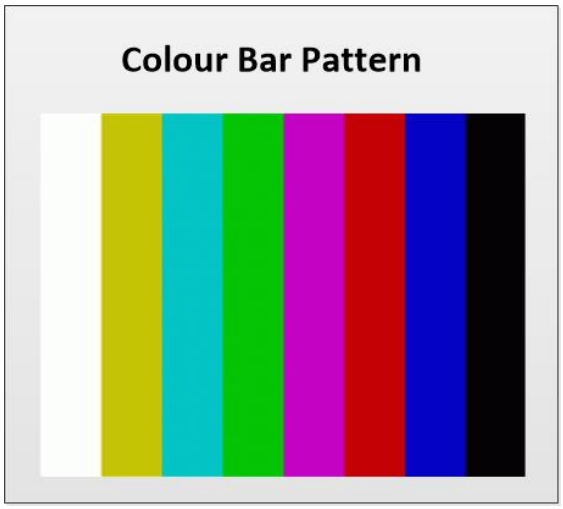
- 3'b000 – Colour Bar pattern is generated
- 3'b001 – solid RED is generated
- 3'b010 – sold GREEN is generated
- 3'b011 – solid Blue is generated

The pattern generator IP will generate the patterns based on the input data_enable_i signal, If the data_enable_i signal is high the desired pattern is generated else the output pattern is not generated. This pattern generator IP operates at the system clock CLKIN_i. The output of the pattern generator IP is 24-bit data which comprises of R, G, B data of 8-bit each. The input signals h_sync_i, v_sync_i and data_enable_i, hactive_i,vactive_i are 2-stage flopped inside the pattern generator block to compensate for the latency of R, G and B data and transmitted out as h_sync_o, v_sync_o, data_enable_o, hactive_o and vactive_o respectively.

3 Hardware Implementation

The following figure shows the color bar pattern generated from the pattern generator. To generate the color bar pattern, a pattern generator counter is implemented. The counter is enabled when the data_enable_i signal is high while it is disabled when the data_enable_i input signal is low. It is a configurable free running counter, when the counter value reached the value configured in parameter video_resolution it resets to zero.

Figure 2 • Color Bar Pattern Generated from Pattern Generator



3.1 Inputs and Outputs

The following table shows the input and output ports of Pattern Generator.

Table 1 • Inputs and Outputs of Pattern Conversion

Signal Name	Direction	Width	Description
RSTn_i	Input	-	Active low asynchronous reset signal to design
CLKIN_i	Input	-	System clock
data_enable_i	Input	-	Data_enable signal, if high Test pattern is generated
h_sync_i	Input	-	Horizontal Sync Input
v_sync_i	Output	-	Vertical Sync Input
hactive_i	Output	-	Horizontal active input signal
vactive_i	Output	-	Vertical active input signal
Pattern_type_i	Output	[2:0]	Input signal which defines the type of test pattern to be generated
R_DATA_o		[g_DWIDTH-1:0]	Output R-DATA
G_DATA_o		[g_DWIDTH-1:0]	Output G-DATA
B_DATA_o		[g_DWIDTH-1:0]	Output B-DATA
Data_enable_o		-	Output data enable signal
H_sync_o		-	Output sorizontal sync signal
V_sync_o		-	Output vertical sync signal
hactive_o		-	Output horizontal active signal

Signal Name	Direction	Width	Description
vactive_o		-	Output vertical active signal

3.2 Configuration Parameters

The following table shows the configuration parameters used in the hardware implementation of Pattern Generator. These are generic parameters and can be varied based on the application requirements.

Table 2 • Configuration Parameters

Signal Name	Description
g_Video_Resolution	Width of the data I/O
g_COUNT_WIDTH	Horizontal resolution bit width
g_DWIDTH	Horizontal resolution

3.3 Testbench

A test bench has been provided to check the functionality of the pattern generator core.

Table 3 • Testbench Configuration Parameters

Name	Description
CLKPERIOD	Clock Period

3.4 Resource Utilization

The following table lists the resource utilization of the Pattern Generator block implemented in the SmartFusion®2 and PolarFire system-on-chip (SoC) FPGA device M2S150T-FBGA1152 package and PolarFire FPGA (MPF300TS_ES - 1FCG1152E package).

Table 4 • Resource Utilization Report

Resource	Usage
DFFs	25
4-Input LUTs	63
MACC	0
RAM1Kx18	0
RAM64x18	0

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