RN0040
Release Notes
CoreDDS v3.1

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1 Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

1.1 Revision 3.0

Added PolarFire® SoC support.

1.2 Revision 2.0

The following is a summary of the changes in revision 2.0 of CoreDDS v3.0.

- Graphic user interface; support for SmartFusion®2, IGLOO®2, RTG4™, and PolarFire® families; major design changes
- Added Taylor series phase correction
- Improved dither generator randomness
- Added frequency and phase modulation ports

1.3 Revision 1.0

The first publication of this document.0

Contents

2 CoreDDS v3.1

This document provides information about the features and enhancements, system requirements, supported families, implementations, and known issues and workarounds.

2.1 Key Features

CoreDDS supports the following features:

- Sine, cosine, or quadrature generator
- Up to 32 bits phase accumulator
- Up to 2^{20} effective LUT depth
- ¼ wave memory saving architecture
- Output sample bit resolution 4 to 32 bits
- Optional phase dithering for spurious-free dynamic range (SFDR) improvement
- Optional trigonometric wave correction for SFDR improvement
- User configurable output polarity
- Optional built-in dynamically controlled phase and frequency offsets
- Controllable pipeline latency

2.2 Supported Interfaces

No standard interface available.

2.3 Delivery Types

No License is required to use CoreDDS. Complete RTL source code is provided for the core.

2.4 Supported Families

The following FPGA families are supported by the CoreDDS:

- PolarFire® SoC
- PolarFire®
- RTG4™
- IGLOO®2
- SmartFusion®2

2.5 Supported Tool Flows

The following tools are supported by the CoreDDS:

- Libero® System-on-Chip (SoC) software v11.7 or later.
- Windows and Linux operating systems

2.6 Installation Instructions

The CoreDDS CPZ file must be installed into Libero software. This is done automatically through the Catalog update function in Libero, or the CPZ file can be manually added using the **Add Core** catalog feature. Once the CPZ file is installed in Libero, the core can be configured, generated, and instantiated within SmartDesign for inclusion in the Libero project. For more information, see the *Knowledge Based article*.

To know how to create SmartDesign project using the IP cores, refer to *Libero SoC documents page* and use the latest SmartDesign user guide.

2.7 Documentation

This release contains a copy of the *CoreDDS Handbook*. The handbook, describes the core functionality and gives step-by-step instructions on how to simulate, synthesize, and place-and-route this core, and also implementation suggestions. Refer to *Libero SoC documents page* for instructions on obtaining IP documentation.

For updates and additional information, visit the Intellectual Property pages on the Microsemi SoC Products Group website: visit:

http://www.microsemi.com/products/fpga-soc/design-resources/ip-cores.

2.8 Supported Test Environments

The following test environments are supported by the CoreDDS:

- VHDL user testbench
- Verilog user testbench

2.9 Resolved Issues in the v3.1 Release

There were no software action requests (SARs) resolved. PolarFire SoC support is added.

2.10 Resolved Issues in the v3.0 Release

The following table lists the software action requests (SARs) resolved in the v3.0 release of CoreDDS.

Table 1 • **Resolved SARs in CoreDDS v3.0 Release**

SAR	Description
63075	Provide support for SmartFusion2, IGLOO2, and RTG4 families

2.11 Discontinued Features and Devices

Supports the FPGA families listed in Supported Families, page 5.

2.12 Known Limitations and Workarounds

Phase offset cannot exceed the value of $2^{31} – 1$.