RN0074
Release Notes
CoreFIFO v3.0

Microsemi
a Microchip company

Microsemi Headquarters
One Enterprise, Aliso Viejo,
CA 92656 USA
Within the USA: +1 (800) 713-4113
Outside the USA: +1 (949) 380-6100
Sales: +1 (949) 380-6136
Fax: +1 (949) 215-4996
Email: sales.support@microsemi.com
www.microsemi.com

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1 Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

1.1 Revision 10.0

The following are the changes made in this revision.

- Updated changes related to CoreFIFO v3.0.
- Added CoreFIFO v3.0 Migration, page 11.

1.2 Revision 9.0

The following are the changes made in this revision.

- Added PolarFire SoC support.

1.3 Revision 8.0

Updated changes related to CoreFIFO v2.7.

1.4 Revision 7.0

Updated changes related to CoreFIFO v2.6.

1.5 Revision 6.0

Updated changes related to CoreFIFO v2.5.

1.6 Revision 5.0

Updated changes related to CoreFIFO v2.4.

1.7 Revision 4.0

Updated changes related to CoreFIFO v2.3.

1.8 Revision 3.0

Updated changes related to CoreFIFO v2.2.

1.9 Revision 2.0

Updated changes related to CoreFIFO v2.1.

1.10 Revision 1.0

Revision 1.0 was the first publication of this document. Created for CoreFIFO v2.0.

Contents

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2 CoreFIFO v3.0

2.1 Overview

These release notes accompany the production release of CoreFIFO v3.0. This document provides details about the features, enhancements, system requirements, supported families, implementations, and known issues and workarounds.

2.2 Features

- Dual and single clock operation
- Clock edge - positive/negative
- Full/empty flag generation
- Almost full and almost empty flag generation
- Empty/full stop generation
- Write and read count
- Variable aspect ratio (depth/width)
- Error status generation with overflow and underflow
- Write acknowledge and read data valid generation
- Supports large RAM and micro RAM or controller only option
- Almost full and almost empty single threshold value for assertion
- Pipelining in the memory read data paths (controller with memory option)
- Pre-fetch mode option to provide read data in the same clock cycle
- FWFT (First-Word Fall-Through)
- ECC capability for RTG4, PolarFire, and PolarFire SoC device families

2.3 Delivery Types

CoreFIFO does not require a license. Complete RTL source code is provided for the core and testbenches.

2.4 Supported Families

- PolarFire® SoC
- PolarFire®
- RTG4™
- IGLOO®2
- SmartFusion®2

2.5 Supported Tool Flows

CoreFIFO v3.0 requires Libero® System-on-Chip (SoC) software v11.0 or later.

2.6 Installation Instructions

The CoreFIFO CPZ file must be installed into Libero software. This is done automatically through the Catalog update function in Libero, or the CPZ file can be manually added using the **Add Core** catalog feature. Once the CPZ file is installed in Libero, the core can be configured, generated, and instantiated within SmartDesign for inclusion in the Libero project. For more information, see the *Knowledge Based article*.

To know how to create SmartDesign project using the IP cores, refer to *Libero SoC documents page* and use the latest SmartDesign user guide.

2.7 Documentation

This release contains a copy of the *CoreFIFO Handbook*. The handbook, describes the core functionality and gives step-by-step instructions on how to simulate, synthesize, and place-and-route this core, and also implementation suggestions. Refer to *Libero SoC documents page* for instructions on obtaining IP documentation.

For updates and additional information, visit the Intellectual Property pages on the Microsemi SoC Products Group website: visit:

http://www.microsemi.com/products/fpga-soc/design-resources/ip-cores.

2.8 Supported Test Environments

The following test environments are supported:

- VHDL user testbench
- Verilog user testbench

2.9 Resolved Issues in the v3.0 Release

Table 1 • **Resolved issues in the v3.0 Release**

SAR Number	Changes
107634	CoreFIFO GUI option to generate RAM's based on HighSpeed or LowPower.
112344	Difference in behavior of CoreFIFO between v2.6 and v2.7.
100673	CoreFIFO synchronizer enhancement needs better description in handbook.
113122	Timing constraints for CoreFIFO.
94791	CoreFIFO: EMPTY flag behavior to be documented for different configuration. Handbook is updated accordingly.
109048	Synthesis Error: Net driven by multiple drivers issues.
107693	CoreFIFO customer enhancement requests.
101842	CoreFIFO for RTG4 is not SET mitigated.
109556	CoreFIFO requirement from NGC.
113985	Undefined variable: almost fully de-assert in CoreFIFO.
118664	CoreFIFO: Handbook enhancement.
118927	Incomplete Die information in TGI code for CoreFIFO.
119129	SET mitigation issue for Active High Reset Polarity.
119068	Improper values of WRCNT and RDCNT values for FULL and EMPTY flags assertion respectively.
120146	Discontinue Clock Polarity feature (WCLK_EDGE and RCLK_EDGE) for CoreFIFO

2.10 Resolved Issues in the v2.8 Release

Table 2 • **Resolved Issues in the v2.8 Release**

SAR Number	Changes
115858	ECC logic is optimized in CoreFIFO with PolarFire device.

2.11 Resolved Issues in the v2.7 Release

Table 3 • **Resolved Issues in the v2.7 Release**

SAR Number	Changes
91876	CoreFIFO should double sync the reset with write and read clock.
87120	Support for async reset option for RTG4.
93202	Overflow flag not getting asserted.
95499	CoreFIFO post configuration indicates ”controller only”.
94791	EMPTY flag behavior to be documented.
93440	EMPTY flag is mentioned as synchronous in HB where as in case of FWFT, it is combinational.
87688	Remove or modify incorrect entry “run run -all” in packager attributes.
98462	glitches on EMPTY and DVLD not getting asserted with PREFETCH or FWFT with single word in FIFO.
97984	PF CoreFIFO does not enable SB_CORRECT/ DB_DETET for valid configuration.

2.12 Resolved Issues in the v2.6 Release

Table 4 • **Resolved Issues in the v2.6 Release**

SAR Number	Changes
43498	Missing Modules in Libero Design Hierarchy.
80253	RTG4 uses sync reset, but the Handbook mentions async.
80609	Support for PolarFire.
80679	MEMWD and MEMRD are bypassed for controller mode.

2.13 Resolved Issues in the v2.5 Release

Table 5 • **Resolved Issues in the v2.5 Release**

SAR Number	Changes
68070	CoreFIFO address counter issue (not getting rolled off).
68113	ECC capability missing for RTG4.

2.14 Resolved Issues in the v2.4 Release

Table 6 • **Resolved Issues in the v2.4 Release**

SAR Number	Changes
66456	RTG4 DRC check failure.
65631	CoreFIFO HB: reset is shown as active-low, however it can be configured to active low/high in the GUI.

2.15 Resolved Issues in the v2.3 Release

Table 7 • **Resolved Issues in the v2.3 Release**

SAR Number	Changes
57411	Add support for RTG4.
60654	CoreFIFO with prefetch, single clk is not working.
60021	CoreFIFO behavior with gated clock.
60185	Timing diagrams and FWFT issue (simulation).

2.16 Resolved Issues in the v2.2 Release

Table 8 • **Resolved Issues in the v2.2 Release**

SAR Number	Changes
56536	FWFT (First Word Fall Through) FIFO implementation.
57411	Add support for RTG4.
54647	CoreFIFO does not retain data when RE is de-asserted.
55148	Data lost when data is read back after empty de-assertion.
56537	CoreFIFO issue when the pre-fetch option is checked.

2.17 Resolved Issues in the v2.1 Release

Table 9 • **Resolved Issues in the v2.1 Release**

SAR Number	Changes
51140	CoreFIFO FIFOs do not operate correctly when the prefetch option is checked.
50808	CoreFIFO simulation errors when "vhdl2008" is checked in the Libero GUI.
49361	Data output is zero from RAM when read/write enable are configured as active low.
49133	Issue with CoreFIFO during compile stage when multiple corefifos are used along with MSS in VHDL.
48624	CoreFIFO prompts error for duplicate instances in VHDL.
48300	SmartFusion2 CoreFIFO simulation is not correct.
48299	CoreFIFO 2.0.101 issue in SF2.
43498	Missing modules in Libero Design Hierarchy > Components view.

2.18 Resolved Issues in the v2.0 Release

Table 10 • **Resolved Issues in the v2.0 Release**

SAR Number	Changes
46695	One word is missing (read extra after read en de-assertion) in prefetch mode on de-asserting the rd_en and asserting it back.

2.19 Discontinued Features and Devices

The parameter RESET_POLARITY, WCLK_EDGE(Write Clock), and RCLK_EDGE(Read Clock) is discontinued in the release of CoreFIFO v3.0.

2.20 Known Limitations and Workarounds

The user testbench in CoreFIFO v3.0 release provides support for single fixed parameter configuration only.

2.21 CoreFIFO v3.0 Migration

2.21.1 Migration to CoreFIFO v3.0

- When migrating to CoreFIFO v3.0 from earlier versions the user can expect following SmartDesign and logs windows.

Figure 1 • **Expected SmartDesign view when migrating to CoreFIFO v3.0**

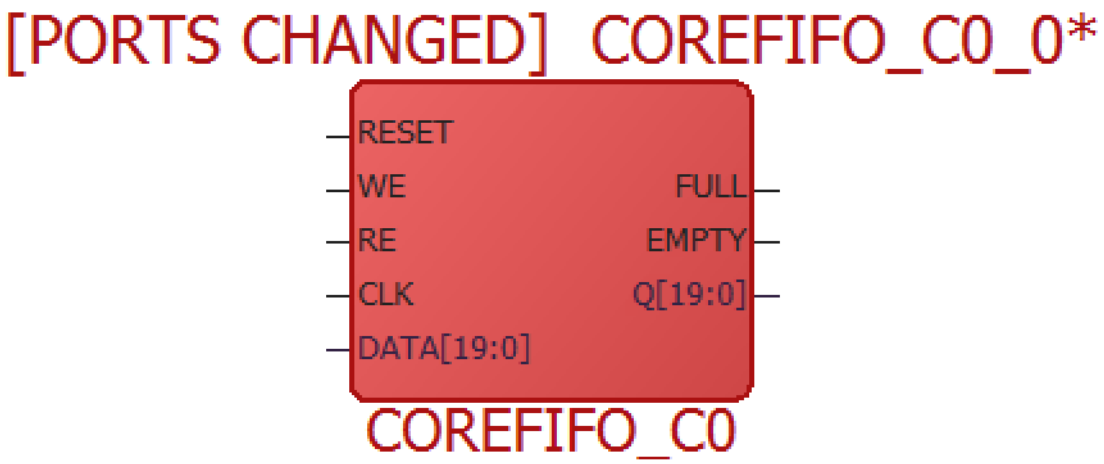


Figure 2 • **Updating SmartDesign to CoreFIFO v3.0 using Update Component option**

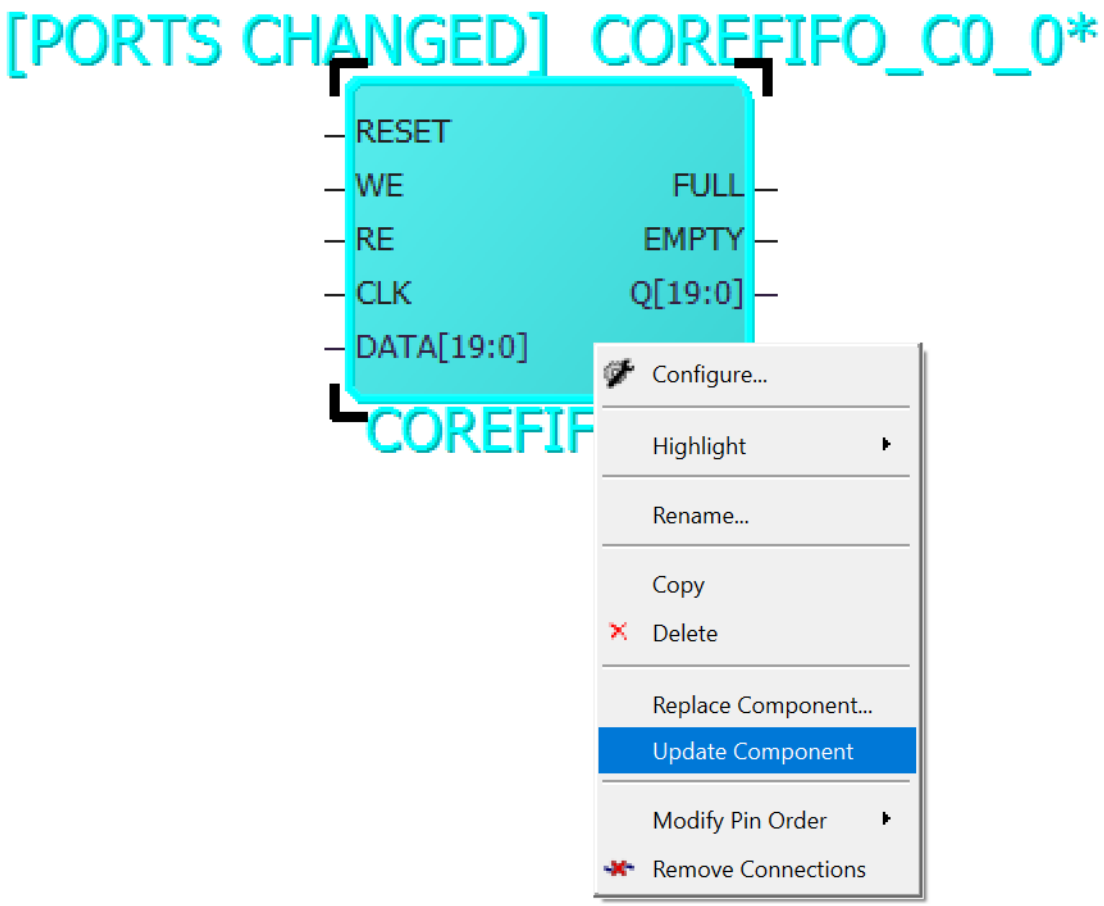
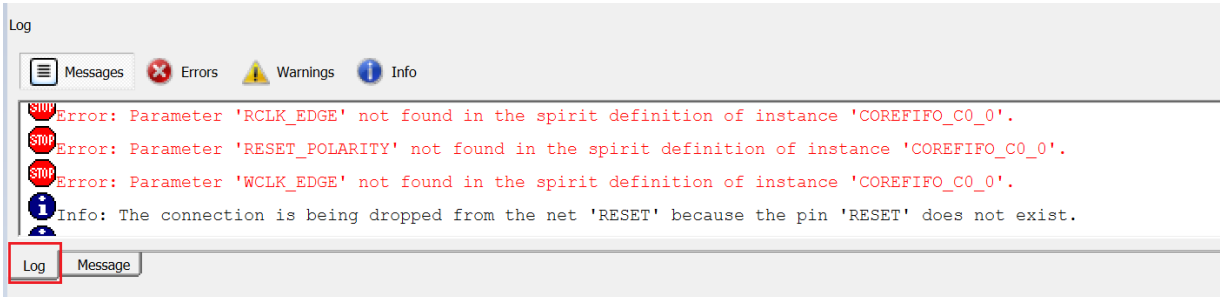


Figure 3 • **Log messages window when migrating to CoreFIFO v3.0**



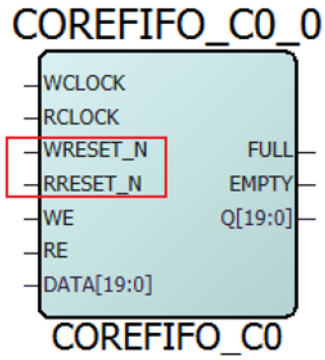
Note: User can safely ignore errors reported in the log window.

2.21.2 Independent reset ports for write and read clock domain for dual clock FIFO

Changes

- When Clocks (SYNC) parameter is configured in dual clock mode (SYNC=0), two reset ports, WRESET_N and RRESET_N are exposed to the top-level ports.

Figure 4 • **SmartDesign configured for SYNC = 0**



Impact

- In the earlier version of the CoreFIFO, only one reset port (RESET) is used (for dual clock FIFO mode). This reset (RESET) input is synchronized internally with respect to the WCLK and RCLK domains.
- For CoreFIFO v3.0, two separate resets (WRESET_N and RRESET_N) ports (for dual clock FIFO mode) are exposed to the user. The user shall synchronize these two resets into the respective clock domain (WRESET_N in WCLK and RRESET_N in RCLK domain) **external** to the IP core.
- CoreFIFO v3.0 is not backward compatible for RESET port connection.
- User can refer to Figure 5 and Figure 6 for asynchronous and synchronous reset synchronizer respectively

Figure 5 • **Asynchronous Reset Synchronizer (When Reset type - SYNC_RESET is set to 0) – external to the IP Core**

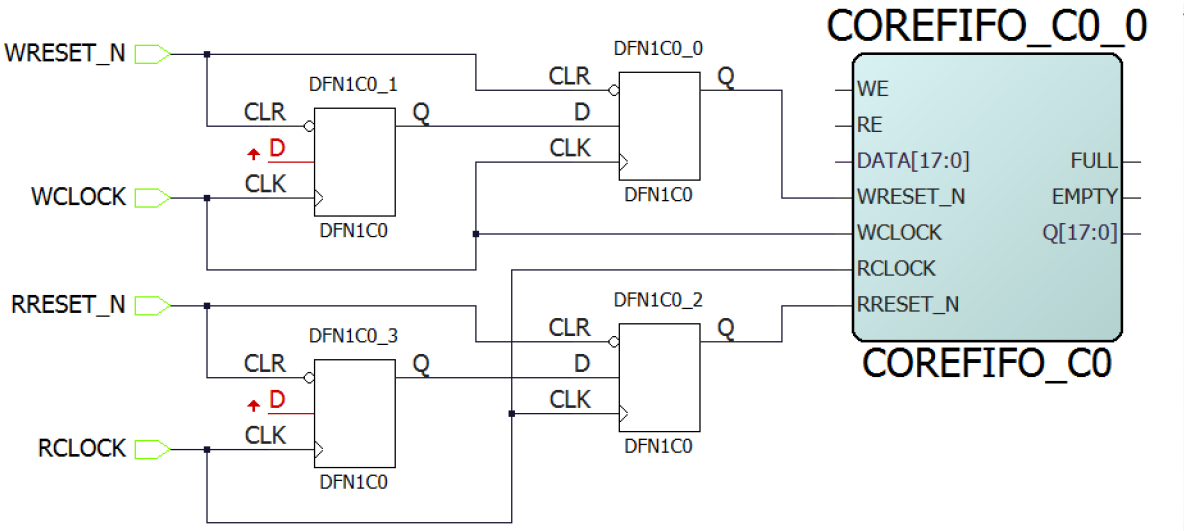
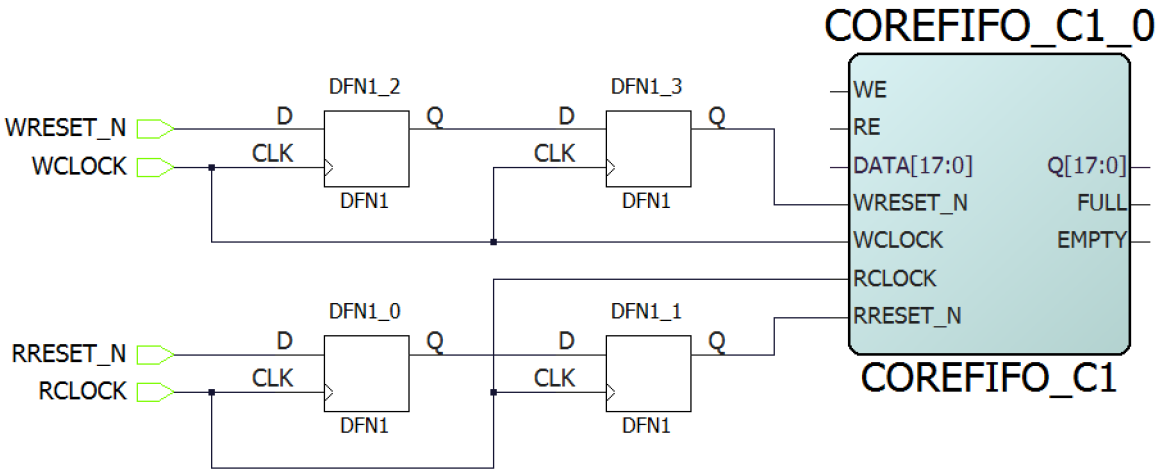


Figure 6 • **Synchronous Reset Synchroniser (When SYNC_RESET is set to 1) – external to the IP Core**



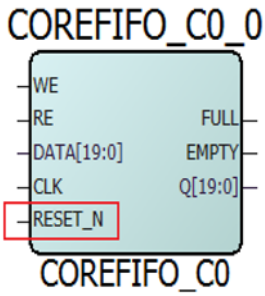
Note: In the above example figures only two flop synchronisers are shown.

2.21.3 Reset Port Name Change for Single Clock Mode FIFO

Changes

When Clocks (SYNC) parameter is configured in single clock mode (SYNC = 1), single reset port RESET_N is exposed to the top-level ports.

Figure 7 • **SmartDesign configured for SYNC=1**



Impact

When updating designs to CoreFIFO v3.0 for single clock mode (SYNC = 1) configuration. Then the user must update the component as the port name is changed from RESET to RESET_N.

2.21.4 Discontinue Reset Polarity Feature (RESET_POLARITY)

Changes

Removed RESET_POLARITY parameter.

Impact

- CoreFIFO v3.0 is not backward compatible for designs using active high polarity.
- For the designs requiring Active High reset polarity, the corresponding reset port should be inverted (NOT gate) external to the IP core.

2.21.5 Discontinue Clock Polarity feature (WCLK_EDGE and RCLK_EDGE)

Changes

Removed WCLK_EDGE and RCLK_EDGE parameters.

Impact

- CoreFIFO v3.0 is not backward compatible for designs using negative edge clock polarity.
- For the designs using negative edge clock polarity, the clock port should be inverted **external** to the IP core.