CoreResetP v7.1 Release Notes

These release notes accompany the production release of CoreResetP v7.1. This document provides details about the features, enhancements, system requirements, supported families, implementations, and known issues and workarounds.

Features

- Sequences reset signals in a SmartFusion®2 or IGLOO®2 device.
- Interacts with CoreConfigP to ensure that reset releases are coordinated with the initialization of the peripheral blocks in a SmartFusion2 or IGLOO2 device. The relevant peripheral blocks are the double data rate (DDR) controllers and the high speed serial interface (SERDESIF) blocks.

Delivery Types

CoreResetP is delivered as register transfer level (RTL) code. The core is freely available and unlicensed.

Supported Families

- SmartFusion2
- IGLOO2

Supported Tool Flows

Use Libero v11.4 software or later with CoreResetP v7.1 release.

Installation Instructions

CoreResetP is available through the Libero SoC IP Catalog. The core can be downloaded from a remote web-based repository to the local vault. Once installed in Libero SoC, the core can be instantiated, configured, connected, and generated using the SmartDesign tool. The System Builder tool automatically instantiates and connects CoreResetP when constructing a design.

Known Issues and Workarounds

There are no known issues in this release.

Release History

Table 1 provides the release history of CoreResetP.

Table 1. Release History of CoreResetP

Version	Date	Changes
7.1	May 2016	Minor change to the configuration GUI: “090” is replaced with “060 or 090”.
7.0	June 2014	Added SDIF0_0_CORE_RESET_N and SDIF0_1_CORE_RESET_N outputs (and corresponding SOFT_SDIF0_0_CORE_RESET and SOFT_SDIF0_1_CORE_RESET inputs). Renamed CONFIG_DONE input to CONFIG1_DONE. Added SDIF_RELEASED output and CONFIG2_DONE input. Added DDR_READY and SDIF_READY outputs. Renamed FAB_RESET_N output to MSS_HPMS_READY and removed SOFT_FAB_RESET input. Removed USER_FAB_RESET_N output and SOFT_USER_FAB_RESET input. (INIT_DONE is essentially the same signal as USER_FAB_RESET_N.) Removed CLR_INIT_DONE input. Removed EXT_RESET_IN_N input. Renamed USER_FAB_RESET_IN_N input to FAB_RESET_N.
5.1	January 2014	Updated handbook included with core.
5.0	Sept 2013	Added logic to support PCIe related functionality (HotReset and L2/P2 support). Added SOFT_* input ports that are intended to support software control of individual reset line assertion and de-assertion.
4.0	July 2013	First production release.

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