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Release Notes
CoreAXI4Interconnect v2.2

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Power Matters.

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About Microsemi

Microsemi Corporation (Nasdaq: MSCC) offers a comprehensive portfolio of semiconductor and system solutions for aerospace & defense, communications, data center and industrial markets. Products include high-performance and radiation-hardened analog mixed-signal integrated circuits, FPGAs, SoCs and ASICs; power management products; timing and synchronization devices and precise time solutions, setting the world's standard for time; voice processing devices; RF solutions; discrete components; enterprise storage and communication solutions, security technologies and scalable anti-tamper products; Ethernet solutions; Power-over-Ethernet ICs and midspans; as well as custom design capabilities and services. Microsemi is headquartered in Aliso Viejo, California, and has approximately 4,800 employees globally. Learn more at www.microsemi.com.

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1 Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

1.1 Revision 1.0

Revision 1.0 is the first publication of this document.

2 CoreAXI4Interconnect

This release notes accompanies the production release of CoreAXI4Interconnect v2.2 IP Core. This document provides details about the features, enhancements, system requirements, supported families, implementations, and known issues and workarounds.

2.1 Key Features

CoreAXI4Interconnect is a configurable core with the following features:

- AXI protocol compliant. It can be configured to support AXI4, AXI3, and AXI4-Lite protocols on all maser or slave ports, and can also be configured to support AHB-Lite protocol on master ports.
- The AXI4 Interconnect core breaks-up burst transactions of morethan 16 data beats from AXI4 masters into multiple transactions of not more than 16 beats when addressed to an AXI3 slave.
- The AXI4 Interconnect core breaks-up burst transactions of more than 1 data beats from AXI4 or AXI3 masters into multiple transactions of 1 beats when addressed to an AXI4 slave.
- The AXI4 Interconnect can be parameterised to convert AHB's undefined length bursts (burst type INCR) into sequences of pre-defined burst lengths such as 16, to optimise use with external devices.
- Interface data widths:
  - AXI4/AXI3/AHB-Lite: 32, 64, 128, 256 or 512 bits
  - AXI4-Lite: 32 or 64 bits
- Address width: Up to 64 bits
- USER width (per channel): Up to 64 bits
- ID width: Up to 8 bits
- Support for Read-only and Write-only masters and slaves, resulting in reduced resource utilization.
- Support for up to 8 masters and 8 slaves

2.2 Delivery Types

CoreAXI4Interconnect is license free.

2.2.1 RTL

Complete register transfer level (RTL) source code is provided for the core and testbenches.

2.3 Supported Families

CoreAXI4Interconnect supports the following families:

- PolarFire™
- SmartFusion®2
- IGLOO®2

2.4 Supported Tool Flows

This version of CoreAXI4Interconnect requires Libero® SoC v12.0 or later.

2.5 Installation Instructions

The CoreAXI4Interconnect `.CPZ` file must be installed in the Libero SoC. This is automatically installed through the **Catalog** update function in the Libero software, or the `.CPZ` file can be manually added using the **Add Core** catalog feature. Once installed in the Libero catalog, the core can be instantiated and configured.

For more information and instructions on core installation, licensing, and general use, see the *Using DirectCore section in Libero SoC for Classic Constraint Flow User Guide* or *Libero SoC Online Help*.

2.6 Documentation

This release contains a copy of the *CoreAXI4Interconnect Handbook*. The handbook describes the core functionality, gives step-by step instructions on how to simulate, synthesize, and place-and-route the core, and also provides implementation suggestions.

For more information about IP, visit: http://www.microsemi.com/products/fpga-soc/design-resources/ip-cores. For updates and additional information about software, FPGAs, and hardware, see: http://www.microsemi.com.

2.7 Known Issues and Workarounds

There are no known limitations or workarounds in the CoreAXI4Interconnect v2.2 release.

2.8 Release History

The following table provides the release history of CoreAXI4Interconnect.

Table 1 • **Release History**

Version	Date	Changes
2.2	April 2017	Second version of the core.
2.0	February 2017	Initial version of the core.