CoreSF2Config v3.0

Handbook

Microsemi

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Introduction

Core Overview

CoreSF2Config facilitates the configuration of peripheral blocks in a SmartFusion®2 device, including the microcontroller subsystem (MSS) double data rate (DDR) controller, known as the MDDR, fabric DDR (FDDR) controller, and high speed serial interface blocks (SERDESIF). CoreSF2Config has a mirrored master advanced peripheral bus (APB) port and several mirrored slave APB ports. The mirrored master APB port should be connected to the FIC_2_APB_MASTER master port of MSS and the mirrored slave APB ports should be connected to the APB slave ports of the blocks that need to be configured.

Key Features

- Facilitates APB based configuration of the MDDR, FDDR, and SERDESIF peripheral blocks in a SmartFusion2 device.

Supported Microsemi® FPGA Families

CoreSF2Config supports the following family:

- SmartFusion2

Core Version

This handbook supports CoreSF2Config v3.0.

Interface Description

Ports

The ports present on CoreSF2Config are listed in Table 1.

Table 1 CoreSF2Config Ports

Port Name	Type	Description
Mirrored Master Port (connect to FIC_2_APB_MASTER interface of MSS)		
FIC_2_APB_M_PRESET_N	Input	Active low reset
FIC_2_APB_M_PCLK	Input	Clock
FIC_2_APB_M_PSEL	Input	Select
FIC_2_APB_M_PENABLE	Input	Enable
FIC_2_APB_M_PWRITE	Input	Write/read indication
FIC_2_APB_M_PADDR[15:2]	Input	Address
FIC_2_APB_M_PWDATA[31:0]	Input	Write data
FIC_2_APB_M_PRDATA[31:0]	Output	Read data
FIC_2_APB_M_PREADY	Output	Ready
FIC_2_APB_M_PSLVERR	Output	Slave error
Slave Clock and Reset (connect to peripheral blocks)		
APB_S_PCLK	Output	Clock signal to all peripheral APB interfaces
APB_S_PRESET_N	Output	Active low reset signal to all peripheral APB interfaces
Mirrored Slave Port (connect to MDDR_APB_SLAVE port of MSS)		
MDDR_PSEL	Output	Select
MDDR_PENABLE	Output	Enable
MDDR_PWRITE	Output	Write/read indication
MDDR_PADDR[15:2]	Output	Address
MDDR_PWDATA[31:0]	Output	Write data
MDDR_PRDATA[31:0]	Input	Read data
MDDR_PREADY	Input	Ready
MDDR_PSLVERR	Input	Slave error
Mirrored Slave Port (connect to FDDR APB slave port)		
FDDR_PSEL	Output	Select
FDDR_PENABLE	Output	Enable
FDDR_PWRITE	Output	Write/read indication
FDDR_PADDR[15:2]	Output	Address
FDDR_PWDATA[31:0]	Output	Write data

Port Name	Type	Description
FDDR_PRDATA[31:0]	Input	Read data
FDDR_PREADY	Input	Ready
FDDR_PSLVERR	Input	Slave error
Mirrored Slave Port (connect to SERDESIF_0 APB slave port)		
SDIF0_PSEL	Output	Select
SDIF0_PENABLE	Output	Enable
SDIF0_PWRITE	Output	Write/read indication
SDIF0_PADDR[15:2]	Output	Address
SDIF0_PWDATA[31:0]	Output	Write data
SDIF0_PRDATA[31:0]	Input	Read data
SDIF0_PREADY	Input	Ready
SDIF0_PSLVERR	Input	Slave error
Mirrored Slave port (connect to SERDESIF_1 APB slave port)		
SDIF1_PSEL	Output	Select
SDIF1_PENABLE	Output	Enable
SDIF1_PWRITE	Output	Write/read indication
SDIF1_PADDR[15:2]	Output	Address
SDIF1_PWDATA[31:0]	Output	Write data
SDIF1_PRDATA[31:0]	Input	Read data
SDIF1_PREADY	Input	Ready
SDIF1_PSLVERR	Input	Slave error
Mirrored Slave Port (connect to SERDESIF_2 APB slave port)		
SDIF2_PSEL	Output	Select
SDIF2_PENABLE	Output	Enable
SDIF2_PWRITE	Output	Write/read indication
SDIF2_PADDR[15:2]	Output	Address
SDIF2_PWDATA[31:0]	Output	Write data
SDIF2_PRDATA[31:0]	Input	Read data
SDIF2_PREADY	Input	Ready
SDIF2_PSLVERR	Input	Slave error
Mirrored Slave port (connect to SERDESIF_3 APB slave port)		
SDIF3_PSEL	Output	Select
SDIF3_PENABLE	Output	Enable
SDIF3_PWRITE	Output	Write/read indication
SDIF3_PADDR[15:2]	Output	Address
SDIF3_PWDATA[31:0]	Output	Write data

Port Name	Type	Description
SDIF3_PRDATA[31:0]	Input	Read data
SDIF3_PREADY	Input	Ready
SDIF3_PSLVERR	Input	Slave error
Signals (connect to CoreSF2Reset)		
CONFIG_DONE	Output	Indicates the completion of configuration to CoreSF2Reset.
INIT_DONE	Input	Indicates the completion of initialization from CoreSF2Reset.
CLR_INIT_DONE	Output	Control signal that can be used to clear the INIT_DONE output from CoreSF2Reset.

Note: All signals in this table are active high unless otherwise stated.

Tool Flows

SmartDesign

Figure 1 shows how CoreSF2Config is typically connected in a SmartDesign design.

Note: The mirrored slave ports of CoreSF2Config are peripheral specific; that is, each port should be connected to a particular peripheral block as indicated by port names. In SmartDesign, hovering over the mirrored slave ports (labeled S) on the CoreSF2Config symbol with the mouse pointer shows the names of signals. For example, the port with signal names matching MDDR_* should be connected to the MDDR APB configuration port (labeled MDDR_APB_SLAVE on the MSS symbol).

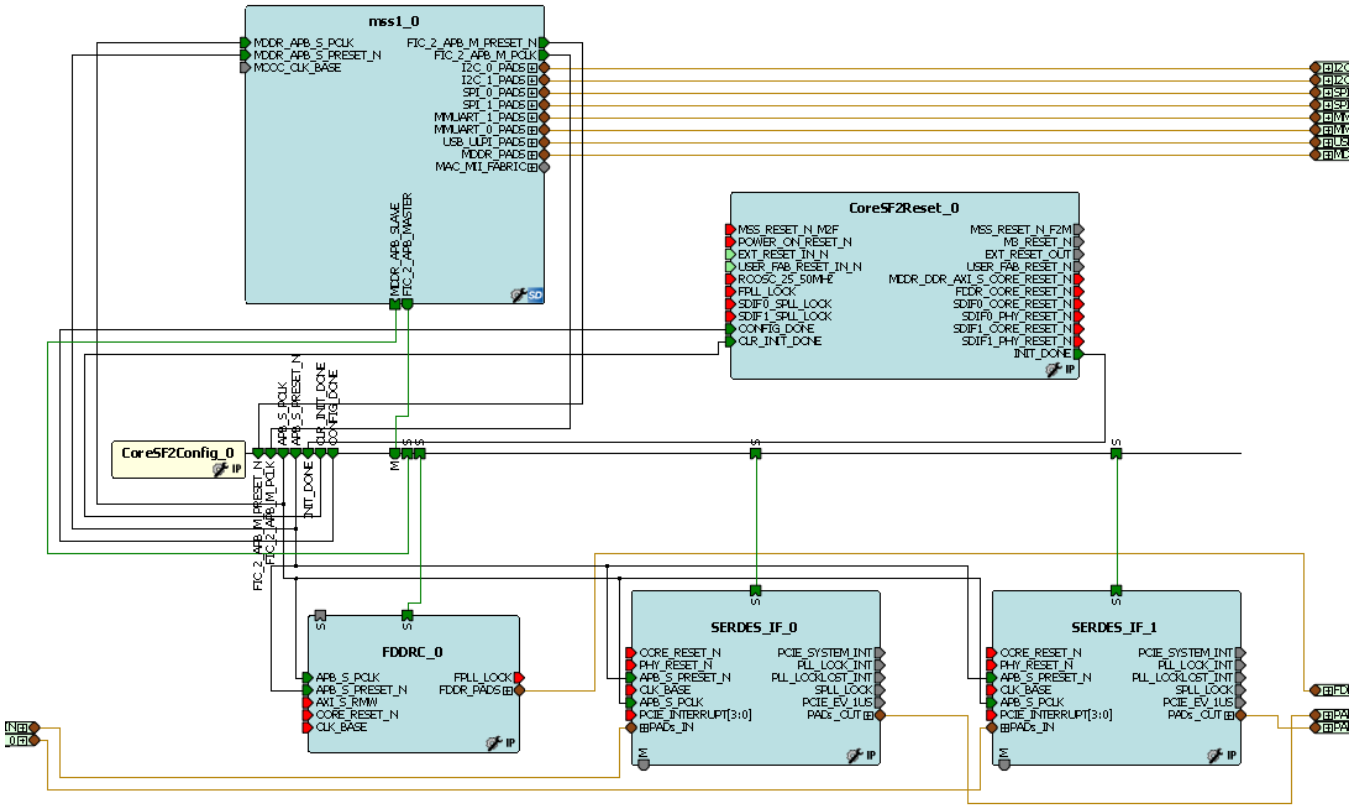

Figure 1 Connecting CoreSF2Config in SmartDesign

Configuring CoreSF2Config in SmartDesign

The CoreSF2Config GUI is shown in Figure 2. Check boxes allow selection of peripheral blocks that will be in use. If a peripheral block is not in use, the ports related to that block do not appear for connection on the CoreSF2Config symbol.

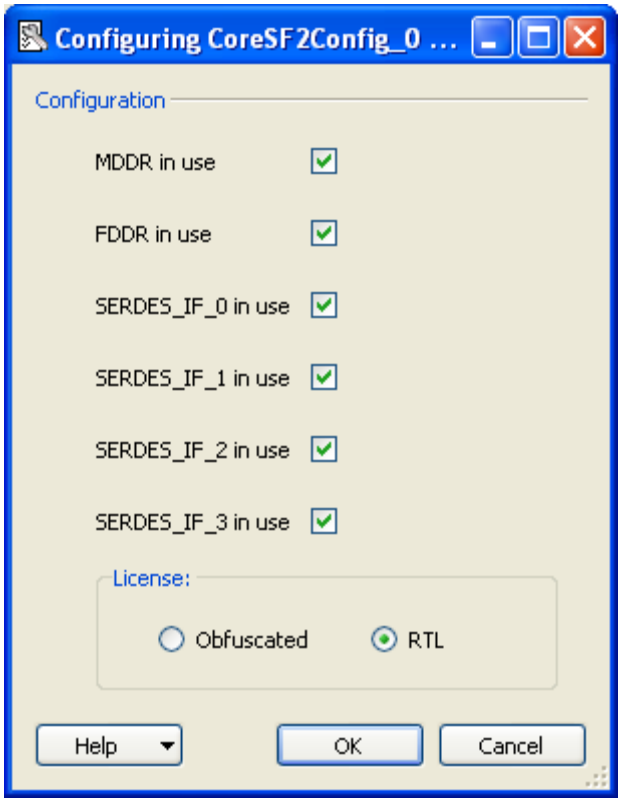

Figure 2 CoreSF2Config Configuration GUI

Memory Map

In the SmartFusion2 MSS memory map, accesses in the address range 0x40020800 to 0x4002FFFF are propagated to the FIC_2_APB_MASTER interface of the MSS. Table 2 shows the address ranges for the peripheral blocks when CoreSF2Config is mastered by the FIC_2_APB_MASTER interface.

Table 2 CoreSF2Config Address Map

Address Range	Description
0x40020800 – 0x40020FFF	MDDR
0x40021000 – 0x400217FF	FDDR
0x40022000 – 0x40023FFF	Internal control and status registers, described under Control and Status Registers section.
0x40024000 – 0x40027FFF	Reserved
0x40028000 – 0x4002A3FF	SERDESIF_0
0x4002C000 – 0x4002E3FF	SERDESIF_1
0x40030000 – 0x400323FF	SERDESIF_2
0x40034000 – 0x400363FF	SERDESIF_3

Control and Status Registers

Control Register 1

Address : 0x40022000
Access : Read/write
Reset state : 0x00000000

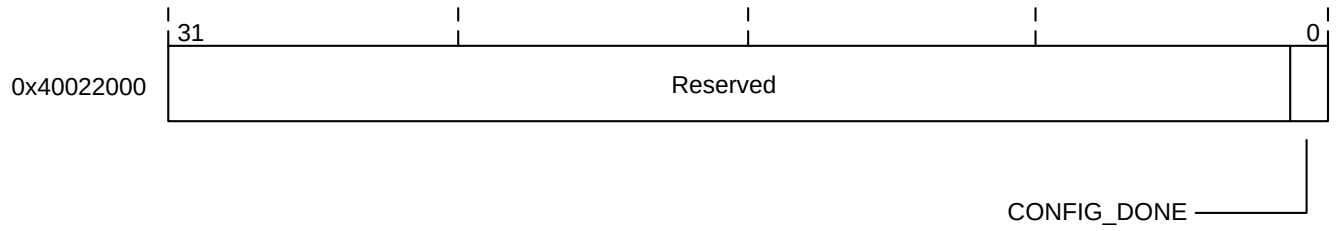

Figure 3 Control Register 1

Table 3 describes the fields of Control Register 1.

Table 3 Control Register 1 Bit Assignments

Bits	Field	Function
[31:1]	-	Reserved
[0]	CONFIG_DONE	Controls the CONFIG_DONE output of the core.

Status Register

Address : 0x40022004
Access : Read only
Reset state : 0x00000000

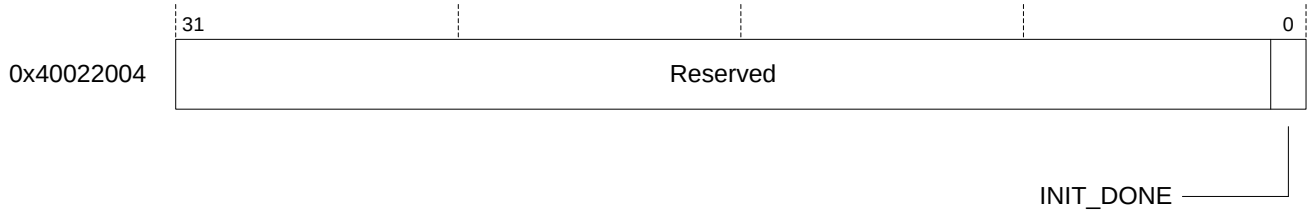

Figure 4 Status Register

Table 4 describes the fields of the Status Register.

Table 4 Status Register Bit Definitions

Bits	Field	Function
[31:1]	-	Reserved
[0]	INIT_DONE	Indicates the logic level on the INIT_DONE input to the core. Normally, this input is connected to the INIT_DONE output of CoreSF2Reset.

Control Register 2

Address : 0x40022008
Access : Read/write
Reset state : 0x00000000

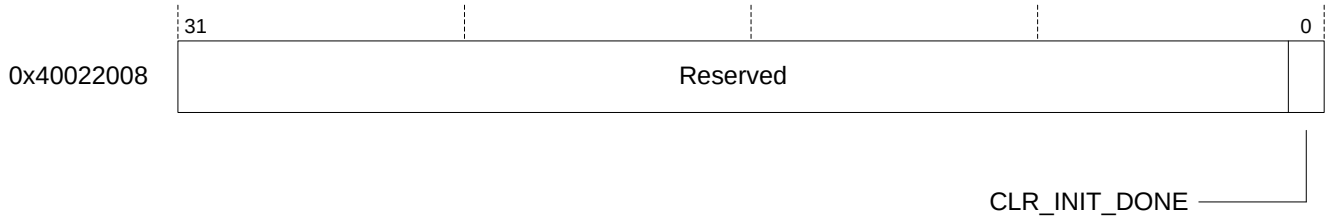

Figure 5 Control Register 2

Table 5 describes the fields of Control Register 2.

Table 5 Control Register 2 Bit Definitions

Bits	Field	Function
[31:1]	-	Reserved
[0]	CLR_INIT_DONE	Controls the CLR_INIT_DONE output of the core. Writing ‘1’ to this bit causes the CLR_INIT_DONE output to be asserted. When a falling edge is detected on the INIT_DONE input, this bit will automatically be cleared and the CLR_INIT_DONE output will be de-asserted.

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Visit the Microsemi SoC Products Group Customer Support website for more information and support (http://www.microsemi.com/soc/support/search/default.aspx). Many answers available on the searchable web resource include diagrams, illustrations, and links to other resources on website.

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You can browse a variety of technical and non-technical information on the Microsemi SoC Products Group home page, at http://www.microsemi.com/soc/.

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