CoreAHBLSRAM v2.0

Handbook

Microsemi

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Introduction

General Description

CoreAHBLSRAM v2.0 provides access to the embedded large SRAM (LSRAM) and small SRAM (uSRAM) blocks present on SmartFusion®2 system-on-chip (SoC) field programmable gate array (FPGA) family devices through AHB-Lite slave interface. It facilitates convenient access to SRAM by AHB masters.

Various configuration parameters or generics apply to CoreAHBLSRAM to control the amount of memory it provides access to, and to the data width of the core.

Core Version

This handbook applies to CoreAHBLSRAM v2.0.

Supported Families

- SmartFusion2 SoC FPGA devices

Functional Block Description

CoreAHBLSRAM consists of three major functional blocks: AHBL slave interface logic, SRAM control logic, and SRAM block instances as shown in Figure 1.

The IP core selects either the LSRAM (RAM1Kx18) or the uSRAM (RAM64x18) based on the configurable parameter 'SEL_RAM_TYPE'.

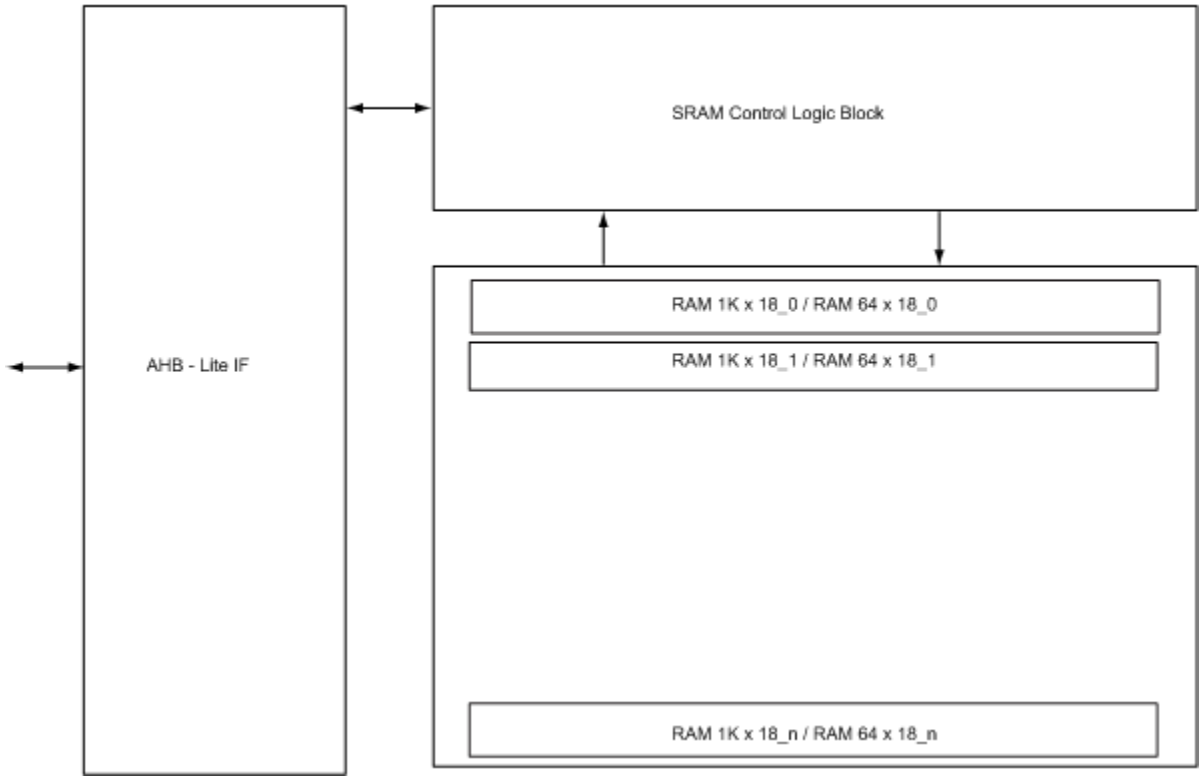

Figure 1 CoreAHBLSRAM Block Diagram

AHB-Lite Interface

The core implements standard AHB-Lite slave interface, which provides word, half-word, and byte accesses. Read and write accesses on the AHB slave interface gets converted into corresponding transfers on the LSRAM or uSRAM.

SRAM Control Logic

The SRAM control logic block converts the AHB-Lite read/write transactions into the corresponding transactions on the LSRAM/uSRAM memory block. The core provides configurable parameters to select LSRAM or uSRAM. It also has the ability to merge blocks of memory based on the requirement.

The SRAM memory size can be configured from 2048 bytes to 139264 bytes (considering only 68 RAM1Kx18 LSRAMs) in steps of 2048 bytes for LSRAMs, and 128 bytes to 9216 bytes in steps of 128 bytes for uSRAMs.

Each of these SRAMs contains an SII (system IP) interface which allows access by the System Controller.

It (core) also supports the ‘BUSY’ output signal from the RAM macros to provide access to the SII interface. The RAM macro asserts the BUSY signal if the SII interface requests for access to the RAM macros. If any AHB transaction is in progress, it is allowed to complete successfully. Then the HREADY signal is pulled low, thereby preventing any further transactions on the AHB bus. When the BUSY signal is de-asserted again, the AHB bus transactions can continue normally.

SRAM Block

There are 69 LSRAMs and 72 uSRAMs available in the SmartFusion2 SoC FPGA device family.

Note: Only 68 LSRAMs are used for optimal utilization of the fabric memories and thereby improve the performance of the design. Hence, one LSRAM block remains unused in M2S050 device.

The SRAM memory begins at address offset 0x0000 and continues to an upper limit which depends on the configuration of the core.

The AHB-Lite interface supports transfer sizes of word (32-bit), half-word (16-bit), and byte (8-bit). The internal configuration of the SRAMs is always fixed to support maximum data width (that is, 32-bit data width). Each LSRAM lowest configuration (2Kx8) is 16 Kbits that is 2 Kbytes. It is logically possible to merge multiple LSRAMs into one large LSRAM. The maximum density in the M2S050 device is 139,264 bytes that can be achieved by using 68 blocks of LSRAM (that is, 68 x {2048x8} = 139,264 bytes).

In order to support the AHB-Lite Transfer Sizes (using HSIZE) of byte (8-bit) writes, half-word (16-bit) writes, and word (32-bit) writes, the core logic configures the memory to support byte writes, where each byte has its own separate write enable signal.

For each uSRAM, the lowest configuration is 128x8. It is logically possible to merge multiple uSRAMs into one large uSRAM. The maximum density in the M2S050 device is 9,216 bytes that can be achieved by using 72 blocks of uSRAM (that is 72 x {128x8} = 9,216 bytes).

Tool Flows

Licensing

CoreAHBLSRAM is licensed in two ways. Depending on license tool flow, functionality may be limited.

Obfuscated

Complete RTL code is provided for the core, allowing the core to be instantiated with the SmartDesign. Simulation, synthesis, and layout can be performed within Libero® System-on-Chip (SoC). The RTL code for the core is obfuscated[1] and some of the testbench source files are not provided; they are instead precompiled into the compiled simulation library.

RTL

Complete RTL source code is provided for the core and testbenches.

SmartDesign

CoreAHBLSRAM is preinstalled in the SmartDesign IP Deployment design environment. An example of the instantiated view is shown in Figure 2. The core can be configured using the configuration graphical user interface (GUI) within the SmartDesign, as shown in Figure 3.

For information on using the SmartDesign to instantiate and generate cores, refer to the Using DirectCore in Libero® SoC User's Guide.

Figure 2 SmartDesign CoreAHBLSRAM Instance View

1 *Obfuscated means the RTL source files have had formatting and comments removed, and all instance and net names have been replaced with random character sequences.*

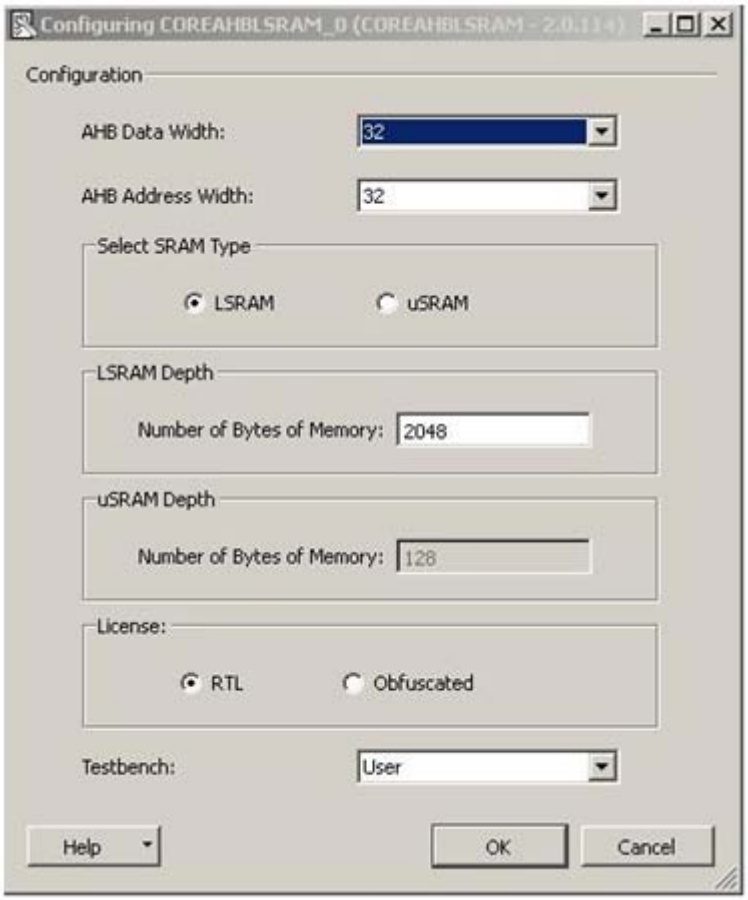

Figure 3 SmartDesign CoreAHBLSRAM Configuration Window

Simulation Flows

The user testbench for CoreAHBLSRAM is included in all releases.

To run simulations, select the User Testbench flow within the SmartDesign and click **Save & Generate** on the **Generate** pane. The user testbench is selected through the Core Testbench Configuration GUI.

When SmartDesign generates the Libero SoC project, it will install the user testbench files.

To run the user testbench, set the design root to the CoreAHBLSRAM instantiation in the Libero SoC design hierarchy pane and click the **Simulation** icon in the Libero SoC design flow window. This invokes the ModelSim® and automatically runs the simulation.

User Testbench

An example user testbench is included with CoreAHBLSRAM as shown in Figure 4.

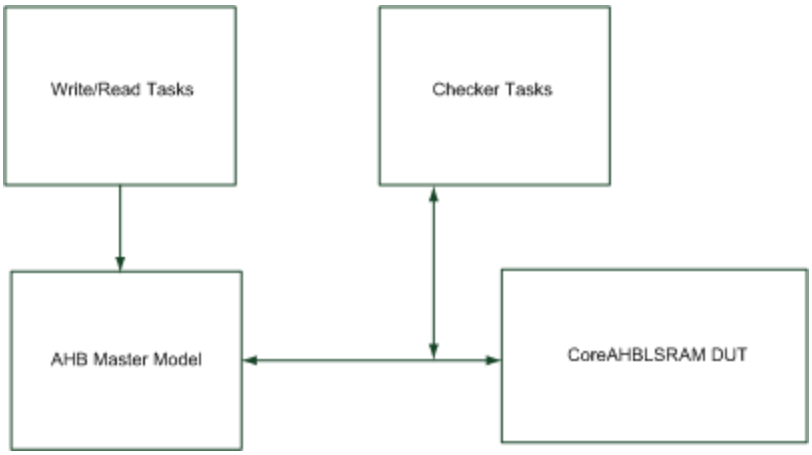

Figure 4 User Testbench

As shown in Figure 4, the user testbench instantiates a Microsemi DirectCore CoreAHBLSRAM DUT. The AHBLSRAM master model tasks drive write/read transactions to the DUT. The DUT in turn performs write and read to the SRAM memories which are instantiated inside the DUT. The checker model tasks checks and determines whether or not the transaction is successful and displays the result.

Synthesis in Libero SoC

Click the **Synthesis** icon in Libero SoC. The **Synthesis** window displays the Synplicity® project. Set Synplicity to use the Verilog 2001 standard, if Verilog is being used. To run Synthesis, select the **Run** icon.

Place-and-Route in Libero SoC

Click the **Layout** icon in the Libero SoC to invoke Designer. CoreAHBLSRAM requires no special place-and-route settings.

Core Interfaces

Signal descriptions for CoreAHBLSRAM are defined in Table 1 .

Table 1. Signal Descriptions

Port Name	Width	Direction	Description
AHBL Slave Interface Ports			
HCLK	1	In	AHB clock. All the AHB signals inside the block are clocked on the rising edge.
HRESETn	1	In	AHB Reset. This signal is active low. Asynchronous assertion and synchronous de-assertion. This is used to reset AHB registers in the block.
HSEL	1	In	AHBL slave select. This signal indicates that the current transfer is intended for the selected slave.
HADDR	18	In	AHBL address. 32-bit address on the AHBL interface. For LSRAM, only [17:0] bits are valid.
HWRITE	1	In	AHBL write. Where HIGH indicates that the current transaction is a write. Where LOW indicates that the current transaction is a read.
HREADYIN	1	In	When high, the HREADY signal indicates to the master and all slaves, that the previous transfer is complete.
HREADYOUT	1	Out	When high, the HREADYOUT signal indicates that a transfer has been completed on the bus. This signal can be driven low to extend a transfer.
HTRANS	2	In	AHBL transfer type. Indicates the transfer type of the current transaction. b00 = IDLE b01 = BUSY b10 = NONSEQUENTIAL b11 = SEQUENTIAL
HSIZE	3	In	AHBL transfer size. Indicates the size of the current transfer (8/16/32/64 bit transactions only) bx00 = 8 bit (byte) transaction bx01 = 16 bit (half-word) transaction bx10 = 32 bit (word) transaction bx11 = 64 bit (double-word) transaction
HBURST	3	In	AHBL Burst type b000 = Single Note: Only Single Length Burst is permitted.

Port Name	Width	Direction	Description
HWDATA	AHB_DWIDTH	In	AHBL write data. Write data from the AHBL master to the AHBL slave.
HRESP	1	Out	AHBL response status. When driven high at the end of a transaction, it indicates that the transaction was completed with errors. When driven low at the end of a transaction, it indicates that the transaction was completed successfully.
HRDATA	AHB_DWIDTH	Out	AHBL read data. Read data from the AHBL slave to the AHBL master.

Core Parameters

CoreAHBLSRAM Configurable Options

There are a number of configurable options that apply to CoreAHBLSRAM as shown in Table 2. If a configuration other than the default is required, select the configuration dialog box in SmartDesign to select appropriate values for the configurable options.

Table 2. CoreAHBLSRAM Configuration Options

Name	Valid Range	Description
FAMILY	19	Must be set to the required FPGA family: 19: SmartFusion2 device
AHB_AWIDTH	32	A 32-bit System AHB address bus.
AHB_DWIDTH	32	Write/Read data bus on AHB side.
LSRAM_NUM_LOCATIONS_DWIDTH32	2 k to 139 k in steps of 2 k	Number of memory locations 2 k, 4 k, 6 k,.....,139 k (1 k = 1024 location) This is valid only for LSRAM memory configuration
USRAM_NUM_LOCATIONS_DWIDTH32	128 to 9 k	Number of memory locations 128, 256,.....,9 k (in steps of 128) This is valid only for uSRAM memory configuration.
SEL_SRAM_TYPE	0 or 1	Used to select the fabric memory type 0: Select RAM1Kx18 LSRAM memory 1: Select RAM64x18 uSRAM memory

Register Map and Descriptions

CoreAHBLSRAM do not contain any registers.

Ordering Information

Ordering Codes

CoreAHBLSRAM can be ordered through a local Sales Representative. It can be ordered using the following number scheme: CoreAHBLSRAM-XX, where XX is listed in.

Table 3. Ordering Codes

XX	Description
OM	RTL for Obfuscated RTL—multiple use license
RM	RTL for RTL source — multiple-use license

Product Support

Microsemi SoC Products Group backs its products with various support services, including Customer Service, Customer Technical Support Center, a website, electronic mail, and worldwide sales offices. This appendix contains information about contacting Microsemi SoC Products Group and using these support services.

Customer Service

Contact Customer Service for non-technical product support, such as product pricing, product upgrades, update information, order status, and authorization.

From North America, call **800.262.1060**
From the rest of the world, call **650.318.4460**
Fax, from anywhere in the world **650. 318.8044**

Customer Technical Support Center

Microsemi SoC Products Group staffs its Customer Technical Support Center with highly skilled engineers who can help answer your hardware, software, and design questions about Microsemi SoC Products. The Customer Technical Support Center spends a great deal of time creating application notes, answers to common design cycle questions, documentation of known issues and various FAQs. So, before you contact us, please visit our online resources. It is very likely we have already answered your questions.

Technical Support

Visit the Microsemi SoC Products Group Customer Support website for more information and support (http://www.microsemi.com/soc/support/search/default.aspx). Many answers available on the searchable web resource include diagrams, illustrations, and links to other resources on website.

Website

You can browse a variety of technical and non-technical information on the Microsemi SoC Products Group home page, at http://www.microsemi.com/soc/.

Contacting the Customer Technical Support Center

Highly skilled engineers staff the Technical Support Center. The Technical Support Center can be contacted by email or through the Microsemi SoC Products Group website.

Email

You can communicate your technical questions to our email address and receive answers back by email, fax, or phone. Also, if you have design problems, you can email your design files to receive assistance. We constantly monitor the email account throughout the day. When sending your request to us, please be sure to include your full name, company name, and your contact information for efficient processing of your request.

The technical support email address is soc_tech@microsemi.com.

My Cases

Microsemi SoC Products Group customers may submit and track technical cases online by going to My Cases.

Outside the U.S.

Customers needing assistance outside the US time zones can either contact technical support via email (soc_tech@microsemi.com) or contact a local sales office. Sales office listings can be found at www.microsemi.com/soc/company/contact/default.aspx.

ITAR Technical Support

For technical support on RH and RT FPGAs that are regulated by International Traffic in Arms Regulations (ITAR), contact us via soc_tech_itar@microsemi.com. Alternatively, within My Cases, select **Yes** in the ITAR drop-down list. For a complete list of ITAR-regulated Microsemi FPGAs, visit the ITAR web page.

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