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Release Notes
CoreSGMII v3.3

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51300127. 5.0 9/20

1 Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

1.1 Revision 5.0

Added PolarFire® SoC support.

1.2 Revision 4.0

Updated changes related to CoreSGMII v3.2.

1.3 Revision 3.0

Updated changes related to CoreSGMII v3.1.

1.4 Revision 2.0

Updated changes related to CoreSGMII v3.0.

1.5 Revision 1.0

Revision 1.0 was the first publication of this document. Created for CoreSGMII v2.0.

Contents

Tables

2 CoreSGMII v3.3

2.1 Overview

These release notes accompany the production release of CoreSGMII v3.3. This document provides details about the features, enhancements, system requirements, supported families, implementations, and known issues and workarounds.

2.2 Features

- Full-duplex support for 1000 Mbps operation
- Full and half-duplex support for 10/100 Mbps operation
- GMII for interfacing to a MAC
- MDIO interface to configure and monitor
- Implements 8b/10b encoding and decoding
- Clause 37 Auto-Negotiation
- Ten Bit Interface
- Comma alignment

2.3 Interfaces

IEEE 802.3 gigabit media independent interface (G/MII), MDIO interface, and Ten Bit Interface.

2.4 Delivery Types

CoreSGMII is available in two modes:

- Evaluation (Free)
- Obfuscated (Licensable)

2.5 Supported Families

- PolarFire® SoC
- PolarFire®
- RTG4™
- IGLOO®2
- SmartFusion®2

2.6 Supported Tool Flows

- CoreSGMII v3.3 requires Libero® System-on-Chip (SoC) software v11.7.3.
- Microsemi® SoC Products Group Libero software v11.7.3 can be used with CoreSGMII.

Note: CoreSGMII is compatible with Libero System-on-Chip (SoC).

2.7 Installation Instructions

The CoreSGMII CPZ file must be installed into Libero software. This is done automatically through the Catalog update function in Libero, or the CPZ file can be manually added using the **Add Core** catalog feature. Once the CPZ file is installed in Libero, the core can be configured, generated, and instantiated within SmartDesign for inclusion in the Libero project. For more information, see the *Knowledge Based article*.

To know how to create SmartDesign project using the IP cores, refer to *Libero SoC documents page* and use the latest SmartDesign user guide.

2.8 Documentation

This release contains a copy of the *CoreSGMII Handbook*. The handbook, describes the core functionality and gives step-by-step instructions on how to simulate, synthesize, and place-and-route this core, and also implementation suggestions. Refer to *Libero SoC documents page* for instructions on obtaining IP documentation.

For updates and additional information, visit the Intellectual Property pages on the Microsemi SoC Products Group website: visit:

http://www.microsemi.com/products/fpga-soc/design-resources/ip-cores.

2.9 Supported Test Environments

The following test environments are supported:

- Verilog user testbench

2.10 Resolved Issues in the v3.3 Release

There were no software action requests (SARs) resolved. PolarFire SoC support is added.

2.11 Resolved Issues in the v3.2 Release

Table 1 • **Resolved Issues in the v3.2 Release**

SAR Number	Changes
87216	To add support for RTG4 family.

2.12 Resolved Issues in the v3.1 Release

Table 2 • **Resolved Issues in the v3.1 Release**

SAR Number	Changes
77385	Add RX_SLIP output port and remove the barrel shift word aligner for the PolarFire case.
82706	CoreSGMII needs to be updated for RX SLIP enable or disable support.

2.13 Resolved Issues in the v3.0 Release

Table 3 • **Resolved Issues in the v3.0 Release**

SAR Number	Changes
75226	Support for a single 125MHz TBI receive clock.
75233	To add support for PolarFire family.

2.14 Discontinued Features and Devices

62.5 MHz PMA clocks have been replaced with 125 MHz PMA clock.

2.15 Known Limitations and Workarounds

There are no known limitations and workarounds.