CoreUARTapb v5.2 Release Notes

This is the production release for the CoreUARTapb IP core. These release notes describe the features and enhancements for CoreUARTapb IP v5.2. They also contain information about system requirements, supported families, implementations, and known issues and workarounds.

Features

CoreUARTapb is a highly configurable core and has the following features:

- Asynchronous mode to interface with industry standard UART
- Optional transmit and receive FIFOs
- APB interface
- Fixed and programmable modes of operation

Delivery Types

CoreUARTapb is licensed in two ways: Obfuscated and RTL.

Obfuscated

Complete RTL code is provided for the core, enabling the core to be instantiated with SmartDesign. Simulation, Synthesis, and Layout can be performed with Libero® Integrated Design Environment (IDE). The RTL code for the core is obfuscated.

RTL

Complete RTL source code is provided for the core and testbenches.

Supported Families

- IGLOO®
- IGLOOe
- IGLOO PLUS
- ProASIC®3
- ProASIC3E
- ProASIC3L
- SmartFusion®
- SmartFusion2
- ProASIC PLUS®
- Fusion
- Axcelerator®
- RTAX-S
- SX-A
- RTSX-S

Supported Tool Flows

This version of the core requires Libero IDE v11.0 or later.

Installation Instructions

For RTL and Obfuscated versions of the core, the FLEXlm license must be installed before the core can be exported. Refer to the Libero IDE online help for further instructions regarding core installation and licensing.

Documentation

This release contains a copy of the *CoreUARTapb Handbook*. The handbook describes the core functionality and gives implementation suggestions.

For updates and additional information about the software, devices, and hardware, visit the Intellectual Property pages on at http://www.microsemi.com/soc.

Supported Test Environments

The following test environments are supported for CoreUARTapb:

- Verilog user testbench
- VHDL user testbench

New Features and Devices

The following new features and devices are included in the v5.2 release:

- Support for SmartFusion2 devices

Release History

Table 1 provides the release history of CoreUARTapb.

Table 1 • **Release History of CoreUARTapb**

Version	Date	Changes
5.2	September 2012	Added support for SmartFusion2 devices.
5.1	March 2012	Fractional baud value feature added to give extra precision. This feature can be fixed or programmable.
4.2	October 2010	Maintenance release. Fixed performance SAR 20741, usability SAR 18238, and other minor changes.
4.1	July 2009	Maintenance release. Fixed major SAR No. 19041 and others (see Table 4 on page 3). Changed testbench to AMBA DirectCore BFM-based version.
4.0	February 2009	Widened baud value. Added framing error status register bit.
3.1	May 2007	Initial version of the core

Resolved Issues in the v5.2 Release

No additional SARs were resolved in the CoreUARTapb v5.2 release.

Resolved Issues in the v5.1 Release

Table 2 lists the software action requests (SARs) that were resolved in the CoreUARTapb v5.1 release.

Table 2 • **Resolved Issues in the CoreUARTapb v4.2 Release**

SAR No.	Description
37390	Addition of the fractional baud value feature

Resolved Issues in the v4.2 Release

Table 3 lists the software action requests (SARs) that were resolved in the CoreUARTapb v4.2 release.

Table 3 • **Resolved Issues in the CoreUARTapb v4.2 Release**

SAR No.	Description
22254	CoreUARTapb Spirit Definition for port PCLK changed to IN type instead of INOUT.
18238	CoreUART and CoreUARTapb can be instantiated in the same design without module name conflicts.
20741	Performance improvement for continuous transmission when TX FIFO enabled; there is no longer a 3-bit delay between byte transmissions.
22093	Added tied-off AMBA3 APB signals: PREADY and PSLVERR.
28297	BFM overflow test fixed in user testbench.

Resolved Issues in the v4.1 Release

Table 4 lists the software action requests (SARs) that were resolved in the CoreUARTapb v4.1 release.

Table 4 • **Resolved Issues in the CoreUARTapb v4.1 Release**

SAR No.	Description
19342	Framing error is cleared on byte receive in FIFO mode.
19282	FIFO overflow error has been fixed.
19041	RXRDY in FIFO mode fixed.
18382	Fixed BAUD_VALUE of up to 8,191 is now allowed (13-bit baud value).

Resolved Issues in the v4.0 Release

Table 5 lists the software action requests (SARs) that were resolved in the CoreUARTapb v4.0 release.

Table 5 • **Resolved Issues in the CoreUARTapb v4.0 Release**

SAR No.	Description
12177	Added URL resource links to CoreUARTapb package.
11848	Core naming rules fixed
11849	Device name fixed for SX-A in handbook.
11928	Fixed FIFO error during synthesis for IGLOO family.
12126	Fixed RXRDY assertion bug, whereby RXRDY is asserted when RX stays low for an entire byte. This is fixed by adding a FRAMING_ERR signal to indicate a missing stop bit.
11605	Added missing memory map information.
11673	Corrected baud rate equation in CoreUARTapb Handbook.
11715	Fixed VHDL testbench error.
11866	Fixed missing source file for IGLOO family.

Resolved Issues in the v3.1 Release

No issues were resolved in the v3.1 release.

Known Issues and Workarounds

There are no known limitations or workarounds in the CoreUARTapb v5.2 release.

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