RN0053
Release Notes
CoreCORDIC v4.1

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1 Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

1.1 Revision 4.0

Added PolarFire® SoC support.

1.2 Revision 3.0

As listed in Table 1, page 8.

1.3 Revision 2.0

As listed in Table 2, page 8.

1.4 Revision 1.0

The first publication of this document.

Contents

Tables

2 CoreCORDIC v4.1

This document accompanies the production release of CoreCORDIC v4.1 IP core. It describes the features, enhancements, system requirements, supported families, implementations, known issues and workarounds, and resolved issues of previous version.

2.1 Key Features

CoreCORDIC has the following key features:

- Parameterizable RTL generator
- Functional modes:
  - General vector rotation
  - Conversion from Polar to Rectangular co-ordinates
  - Translation from Rectangular to Polar co-ordinates
  - Sine and Cosine calculation
  - Arctangent (angle) calculation
- Configurable 8 to 48 bits input and output data bit resolution
- Automatic or user-controllable precision of internal calculations up to 48 bits
- Variety of output rounding options:
  - Truncation
  - Convergent rounding (round to nearest even)
  - Symmetric rounding (round to positive or negative infinity)
  - Round up (round to positive infinity)
- Word-serial architecture for smaller area
- Parallel architecture for high throughput
- Configurable number of iterations up to 48
- Synchronous design using a single clock

2.2 Supported Interfaces

CoreCORDIC does not have any standard interface available.

2.3 Delivery Types

CoreCORDIC is distributed with Libero® System-on-Chip (SoC) or Integrated Design Environment (IDE) design software. Complete hardware description language (HDL) source code is provided for the core and testbenches.

Note: CoreCORDIC is compatible with both Libero IDE and Libero SoC. Unless specified otherwise, this document uses the common name Libero to identify Libero IDE and Libero SoC.

2.4 Supported Families

CoreCORDIC v4.1 supports the following families:

- PolarFire® SoC
- PolarFire®
- SmartFusion®2
- IGLOO®2
- IGLOO®
- IGLOOe
- IGLOOPLUS
- RTG4™
- ProASIC®3
- ProASIC3E
- ProASIC3L
- ProASICPLUS
- SmartFusion®
- Fusion
- Axcelerator®
- RTAX-S/SL and RTAX-DSP

2.5 Supported Tool Flows

CoreCORDIC v4.1 supports the following tool flows:

- CoreCORDIC v4.1 requires the Libero software v9.1 or later.
- Supports Windows® and Linux operating systems.

2.6 Installation Instructions

The CoreCORDIC CPZ file must be installed into Libero software. This is done automatically through the Catalog update function in Libero, or the CPZ file can be manually added using the **Add Core** catalog feature. Once the CPZ file is installed in Libero, the core can be configured, generated, and instantiated within SmartDesign for inclusion in the Libero project. For more information, see the *Knowledge Based article*.

To know how to create SmartDesign project using the IP cores, refer to *Libero SoC documents page* and use the latest SmartDesign user guide.

2.7 Documentation

This release contains a copy of the *CoreCORDIC Handbook*. The handbook, describes the core functionality and gives step-by-step instructions on how to simulate, synthesize, and place-and-route this core, and also implementation suggestions. Refer to *Libero SoC documents page* for instructions on obtaining IP documentation.

For updates and additional information, visit the Intellectual Property pages on the Microsemi SoC Products Group website: visit:

http://www.microsemi.com/products/fpga-soc/design-resources/ip-cores.

2.8 Supported Test Environments

CoreCORDIC v4.1 supports the following test environments:

- VHDL user testbench
- Verilog user testbench

2.9 Resolved Issues in the v4.1 Release

There were no software action requests (SARs) resolved. PolarFireSoC support is added.

2.10 Resolved Issues in the v4.0 Release

Table 1 shows SARs resolved in the CoreCORDIC v4.0 release.

Table 1 • **Resolved SARs in CoreCORDIC v4.0**

SAR No.	Description
26547	Provide support for the core to follow SmartDesign flow.
29075	Eliminate synthesis failure due to RTL parameter mismatch.
34711	Expose only valid core ports to a user.
34712	Simplify the core use flow.
35321, 34940	Prevent a possible mismatch between RTL module parameters/entity generics.
43062, 50809	Provide better user interface to avoid user's confusion.
34658	Connect synchronous reset line to all CORDIC registers.
55916	Extend CORDIC support to cover recently emerged FPGA families.
57144	Support for negative input X values.

2.11 Resolved Issues in the v3.0 Release

Table 2 shows SARs resolved in the CoreCORDIC v3.0 release.

Table 2 • **Resolved SARs in CoreCORDIC v3.0**

SAR	Description
13497	Generated core does not seem to match up with the datasheet pin descriptions.
19458	CoreCORDIC for Verilog requires Package Directory.
19459	Remove package directory dependency for VHDL.
20132	CoreCORDIC in Word Serial mode has RTL and Doc mismatches.

2.12 Known Limitations and Workarounds

There are no known limitations or workarounds in the CoreCORDIC v4.1 release.