CoreAHBLSRAM v2.0 Release Notes

This release note accompanies the production release for CoreAHBLSRAM v2.0 IP core. This is the first production release of CoreAHBLSRAM. This document provides details about the features, supported families, system requirements, implementations, and known limitations and workarounds.

Features

CoreAHBLSRAM is a highly configurable core that provides the following features:

- Configurable memory size. Memory size can be configured from 2048 bytes to 139264 bytes, in steps of 2K bytes for LSRAMs (RAM1Kx18)
- Configurable memory size. Memory size can be configured from 512 bytes to 9216 bytes in steps of 512 bytes for uSRAMs (RAM64x18)
- Configurable parameter to access either LSRAM or uSRAM memory
- Ability to logically merge multiple SRAM blocks to form large SRAMs or uSRAMs
- AHB interface with data width of 32-bits
- Support to BUSY output signal from the RAM macros to provide access to the SII interface

Delivery Types

CoreAHBLSRAM is licensed in two ways: Obfuscated and RTL.

Obfuscated

Complete RTL code is provided for the core, enabling the core to be instantiated with SmartDesign. Simulation, synthesis, and layout can be performed with Libero® System-on-Chip (SoC). The RTL code for the core is obfuscated.

RTL

Complete RTL source code is provided for the core and testbenches.

Supported Families

- SmartFusion2 (M2S050T) device.

Supported Tool Flows

Use Libero SoC v11.0 or later with the CoreAHBLSRAM release.

Installation Instructions

For the RTL version of the core, the FlexLM license must be installed before the core can be exported.

Refer to the Libero SoC online help for instructions on core installation and licensing.

Documentation

This release contains a copy of the CoreAHBLSRAM Handbook, which describes the core functionality, gives step-by-step instructions on how to simulate, synthesize, and place-and-route this core, and provides implementation suggestions.

For updates and additional information about the software, devices, and hardware, visit the Intellectual Property pages on the Microsemi web site at:

www.microsemi.com/soc.

Supported Test Environments

- Verilog user testbench
- VHDL user testbench

Discontinued Features and Devices

This is the first production release of CoreAHBLSRAM.v2.0.

Known Limitations and Workarounds

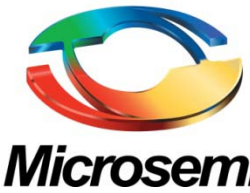
This is the first production release of CoreAHBLSRAM.v2.0.

Release History

There are no resolved issues in the CoreAHBLSRAM v2.0 release; this is the first production release of CoreAHBLSRAM v2.0.

Table 1. Release History

Version	Date	Changes
2.0	January 2013	Initial release



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