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Release Notes
CorePCIe_AHBLtoAXI v2.0

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1 Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

1.1 Revision 1.0

The first publication of this document. Created for CorePCIe_AHBLtoAXI v2.0.

Contents

2 CorePCIe_AHBLtoAXI v2.0

2.1 Overview

These release notes accompany the production release of CorePCIe_AHBLtoAXI v2.0. This document provides details about the features, enhancements, system requirements, supported families, implementations, and known issues and workarounds.

2.2 Features

The CorePCIe_AHBLtoAXI IP core provides an interface (bridge) between the AHBL domain and AXI domain. The IP core is an AHBL slave and an AXI master. The core allows an AHBL bus system to be connected to an AXI bus enabling an AHBL master to communicate with an AXI slave.

The IP core is recommended to be used with SmartFusion®2, IGLOO®2, and RTG4™ PCIe AXI Slave to connect to an AHBL master or AHBL sub-system.

The following features are supported in CorePCIe_AHBLtoAXI:

- Compliant to AMBA 3 AHB-Lite and AMBA 3 AXI specifications
- Provides an interface between the AHBL domain and the AXI domain
- AHBL and AXI domains are synchronous (common clock for both AHBL and AXI)
- Generates only single-beat increment burst AXI transactions
- Converts 32-bit AHBL write/read transactions into 64-bit AXI write/read transactions, respectively
- Controls the bus responses from AXI-Slave to AHBL-Master

The following features are not supported in CorePCIe_AHBLtoAXI:

- Protection (HPROT) and lock (HMASTLOCK) signal is not supported on the AHB interface
- Protection (AWPROT/ARPROT) and cached (AWCACHE/ARCACHE) transfers are not supported on the AXI interface
- Locked transfers are not supported on the AXI interface (ARLOCK and AWLOCK outputs are tied low)

2.3 Delivery Types

Core is freely available. Complete clear RTL source code is provided.

2.4 Supported Families

- IGLOO2
- SmartFusion2
- RTG4

2.5 Supported Tool Flows

Core requires Libero® v11.0 or later.

2.6 Installation Instructions

The core must be installed into Libero software. This is done automatically through the Catalog update function in Libero, or the CPZ file can be manually added using the **Add Core** catalog feature. Once the CPZ file is installed in Libero, the core can be configured, generated, and instantiated within SmartDesign for inclusion in the Libero project. For more information, see the *Knowledge Based article*.

To know how to create SmartDesign project using the IP cores, refer to the *SmartDesign User guide*.

2.7 Documentation

This release contains a copy of the *CorePCIe_AHBLtoAXI Handbook*. The handbook, describes the core functionality and gives step-by-step instructions on how to simulate, synthesize, and place-and-route this core, and implementation suggestions. Refer to the *Libero SoC Online Help* for instructions on obtaining IP documentation.

For updates and additional information, visit the Intellectual Property pages on the Microsemi SoC Products Group website: visit:

http://www.microsemi.com/products/fpga-soc/design-resources/ip-cores.

2.8 Supported Test Environments

No testbench is provided with the core.

2.9 Discontinued Features and Devices

There are no discontinued features and devices.

2.10 Known Limitations and Workarounds

There are no known limitations and workarounds.