RN0059
Release Notes
CoreAHBLite v5.5

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1 Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

1.1 Revision 12.0

Added PolarFire® SoC support. Updated changes related to CoreAHBLite v5.5.

1.2 Revision 11.0

Updated changes related to CoreAHBLite v5.4.

1.3 Revision 10.0

Updated changes related to CoreAHBLite v5.3. Added information about PolarFire® support.

1.4 Revision 9.0

Updated changes related to CoreAHBLite v5.2. Added information about IGLOO®2 and RTG4™ support.

1.5 Revision 8.0

Updated changes related to CoreAHBLite v5.0. Added two more master interfaces. CoreAHBLite can now support a total of four masters.

1.6 Revision 7.0

Updated changes related to CoreAHBLite v4.0.

A greater range of memory space configurations is now supported. Slave slot size can range from 256 bytes to 256 Mbytes.

Mode with 16 x 64 Kbyte slots along with one huge (2 GByte) slot is still supported, but initialization interfaces located from 0x00040000 - 0x0004FFFF are no longer supported in this mode.

Combining of slave slots is now possible. This allows multiple regions of the memory map to be accessed through a single slave interface (S16). This feature may be useful while accessing MSS resources in the SmartFusion or SmartFusion2 device.

1.7 Revision 6.0

Updated changes related to CoreAHBLite v3.1. Added capability for memory maps to be altered in SmartDesign to reflect the value of the MODE_CFG parameter.

1.8 Revision 5.0

Updated changes related to CoreAHBLite v3.0. Added another memory configuration mode. Added huge slot capability and Init/Config client support.

1.9 Revision 4.0

Updated changes related to CoreAHBLite v2.0. Added multi-master capability and additional ports to satisfy multi-master capability.

1.10 Revision 3.0

Updated changes related to CoreAHBLite v1.3. Minor updates.

1.11 Revision 2.0

Updated changes related to CoreAHBLite v1.2. Minor updates.

1.12 Revision 1.0

Revision 1.0 was the first publication of this document. Created for CoreAHBLite v1.1.

2 CoreAHBLite v5.5 Release Notes

This document accompanies the release of CoreAHBLite v5.5. It describes the features and enhancements of CoreAHBLite v5.5. It also contains the information on system requirements, supported families, implementations, known issues and workarounds, and resolved issues with the previous version.

2.1 Features

CoreAHBLite has the following features:

- Supports up to four masters
- Supports up to 16 slaves (up to 17 in one mode, if a huge slave is in use)
- Address space per slave varies from 256 bytes to 256 MB (Huge slave occupies 2 GB)
- Supports allocation of slave slots to a “combined region” slave interface in most modes
- Allows access to slave slots to be enabled on a per master basis. All masters have equal priority (round-robin arbitration scheme)
- Supports remapping feature for master 0 interface

2.2 Interfaces

CoreAHBLite v5.5 supports four AHB-Lite master interfaces and up to 16 AHB-Lite slave interfaces (up to 17 slave interfaces are supported in one mode when the huge slave is in use).

Microsemi recommends using SmartDesign to connect and configure CoreAHBLite v5.5 while creating a system design.

2.3 Delivery Types

No license is required to use the core.

2.3.1 RTL

Complete RTL source code is provided for the core.

2.4 Supported Families

CoreAHBLite supports the following families:

- PolarFire® SoC
- PolarFire®
- RTG4™
- SmartFusion®2
- IGLOO®2
- SmartFusion®
- IGLOO®
- IGLOO®e
- IGLOO® PLUS
- Fusion®
- ProASIC®3
- ProASIC®3E
- ProASIC®3L
- Axcelerator®
- RTAX-S

2.5 Supported Tool Flows

Use Libero Design software v8.6 or later with the CoreAHBLite v5.5 release.

2.6 Installation Instructions

The CoreAHBLite CPZ file must be installed into Libero software. This is done automatically through the Catalog update function in Libero, or the CPZ file can be manually added using the **Add Core** catalog feature. Once the CPZ file is installed in Libero, the core can be configured, generated, and instantiated within SmartDesign for inclusion in the Libero project. For more information, see the *Knowledge Based article*.

To know how to create SmartDesign project using the IP cores, refer to *Libero SoC documents page* and use the latest SmartDesign user guide.

2.7 Documentation

This release contains a copy of the *CoreAHBLite Handbook*. The handbook, describes the core functionality and gives step-by-step instructions on how to simulate, synthesize, and place-and-route this core, and also implementation suggestions. Refer to *Libero SoC documents page* for instructions on obtaining IP documentation.

For updates and additional information, visit the Intellectual Property pages on the Microsemi SoC Products Group website: visit:

http://www.microsemi.com/products/fpga-soc/design-resources/ip-cores.

2.8 Known Issues and Workarounds

There are no known issues in CoreAHBLite v5.5.

2.9 Resolved Issues in the v5.5 Release

There were no software action requests (SARs) resolved. PolarFireSoC support is added.

2.10 Resolved Issues in the v5.4 Release

Table 1 • **Resolved SARs in CoreAHBLite v5.4 Release**

SAR	Description
87186	Core not working in burst mode.
105585	Mirrored slave to Mirrored master enhancement.

2.11 Resolved Issues in the v5.3 Release

Table 2 • **Resolved SARs in CoreAHBLite v5.3 Release**

SAR	Description
83890	HTRANS bit0 is connected to “0” for all slaves at top level.
56427	Check hdl errors out on testbench created by system builder.
87186	Core not working in burst mode.
54034	Need more information on AMBA AHBLite protocol specification.

2.12 Resolved Issues in the v3.1 Release

Table 3 • **Resolved SARs in CoreAHBLite v3.1 Release**

SAR	Description
23409	XPATH equations needed to differentiate mode memory maps.

2.13 Resolved Issues in the v3.0 Release

Table 4 • **Resolved SARs in CoreAHBLite v3.0 Release**

SAR	Description
14960	Validation should warn if all slots are disabled.
12612	Core now supports 60 MHz operations.
17753	File components.vhd need to be packaged using logical library COREAHBLITE_LIB.
14958	Clock and reset signals should be tagged as mandatory.
14666	Remap input has no default value in SmartDesign.
19750	Mirrored slave HMASTLOCK_S* outputs need to be brought out at the top-level.

2.14 Resolved Issues in the v2.0 Release

The v2.0 release is an updated version of the previous release, with new I/O signals and some modified I/O signals.