SmartFusion2 CMSIS Hardware Abstraction Layer Release Notes

Version 2.3

Changes since previous version

The primary purpose of this release is to add support for SoftConsole v4.0.

The release also addresses a number of SARs listed in the table below. This mainly involves changes to linker scripts and startup code. Also, some more explanatory detail has been added to linker scripts, GDB scripts and the user guide.

All Integrated Development Environments

- Copying and filling of memory on startup now handles non-word aligned sections.

Softconsole v4.0

- Renamed all .s source files to .S. This change is required to allow compilation.
- Modified debug-in-microsemi-smartfusion2-esram.ld to remove remapping of eSRAM to location 0x00000000. The remap is unnecessary for this linker script and has negative side effects, whereby accesses to some unimplemented memory locations in the Cortex-M3 code region (0x00000000-0x1FFFFFFF) using the SoftConsole debugger, cause the processor to hang for Libero designs without the MDDR enabled.

Softconsole v3.4

- Modified debug-in-microsemi-smartfusion2-esram.ld to remove remapping of eSRAM to location 0x00000000. The remap is unnecessary for this linker script and has negative side effects, whereby accesses to some unimplemented memory locations in the Cortex-M3 code region (0x00000000-0x1FFFFFFF) using the SoftConsole debugger, cause the processor to hang for Libero designs without the MDDR enabled.
- When debugging from external DDR memory, bundled gdb scripts for SoftConsole v3.4 now verify DDR status register after initialization of DDR before continuing. This is the correct sequence and conforms to CMSIS, Keil and IAR DDR initialization sequence. This change is a result of code review.

  Note: No adverse effect was observed when status register was not checked.

IAR Embedded Workbench

- Register description files for IAR and Keil are now bundled with CMSIS HAL for use in the Keil and IAR debuggers. They can be obtained from the example project files associated with Smatfusion2 CMSIS HAL and copied to Keil or IAR environments as required. The files give detailed descriptions of each register in the Smartfusion2 and allow easy reading and writing (if write enabled) to each register from the debugger.

Keil-MDK

- Register description file update. See IAR detail above.

Other

- Added a description to the user's guide of how to generate and copy debugger scripts to Softconsole v3.4, Keil and IAR.
- Added problem solving section to the User Guide.
- Added preprocessor symbol (MSCC_NO_RELATIVE_PATHS) to facilitate simple transfer of files to Keil CMSIS-Pack which requires a flat structure. This has no impact on use outside the Keil CMSIS-Pack environment.

Resolved issues in version 2.3

Driver issues are tracked as software action requests (SAR).

SAR #	SAR Resolution
60738	Correct invalid heap size computed by Softconsole. This was addressed by adding the keyword ABSOLUTE to the linker scripts.
60741	If sections were not aligned on 4 word boundaries (where word = 32bit), potentially crash or incorrect initialization could occur on startup. Modified linker scripts for Softconsole so sections are aligned as expected.
66764	Modified SoftConsole linker scripts to allow setting a minimum heap size. This ensures an error is generated if the heap size is below the minimum defined amount. This defined value can be found and adjusted at the start of the linker script.
66747	Determined process stack support was not required. Removed support as it was consuming memory and confusing.
66751	Corrected production code linker script when program was being copied and run from external memory. Previously this configuration would crash as all expected data was not available to startup code. All required code/data now available to startup code.
66828	It was determined cache must be turned off to allow reliable debugging. This is now done by the debug scripts. A note has also been added to the user's guide to warn programmers not to enable cache in firmware when debugging – with an example of how to achieve this using precompile switch.
66831	There was no example GBD, Keil or IAR script to allow debugging in DDR memory in the evaluation kit. These have been added.
67208	Previously there was an error in debug script that limited access to external DDR memory in the Dev. kits to 256MB. Debug scripts relating to debugging from external memory have been modified to allow access. Note: The linker scripts are generic and limit access to 64MB as this memory amount is common across all kits. The amount of memory on each Microsemi kit is now detailed in the linker scripts and the scripts can be edited if access to full memory range is required for a particular board.

Version 2.2

Changes since previous version

- Added support for memory single bit error correction and double error bit detection (SECDED). Relevant memory content is initialized during the system initialization in order to set the error correction codes (ECC) used for error detection and correction.

  Note: Enabling SECDED in your design will have an impact on the system's startup time. This is noticeable when starting a debug session with SECDED enabled on large external DDR memory. It may look like the debugger is unresponsive while the memory is initialized when the debug session starts.

- Added support for M2S090 dual PCIe controller configuration. This requires configuration data generated by Libero 11.4 and later.
- Added support for debugging application running in DDR memory connected to the MDDR memory controller.

Resolved issues in version 2.2

Driver issues are tracked as software action requests (SAR).

SAR #	SAR Resolution
44041	Modified SoftConsole linker scripts to make use of DDR memory connected to the MDDR memory controller.
44770	Corrected several assertions and UART redirection issues with the HAL files bundled with the SmartFusion2 CMSIS-HAL
44771	Corrected various register descriptions errors in m2sxxx.h.
53854	Added missing SERDES configuration register base addresses for SERDES blocks found on large SmartFusion2 devices.
58298	Fixed a bug which resulted in the incorrect PMA ready bit being polled as part of the PCIe controller configuration.
58338	PMA ready is now polled for the first PCIe lane of each link. The information regarding which lane to poll is derived from configuration data generated by Libero 11.4 and later.
58339	The correct PMA ready for a PCIe link is being polled through the use of #define generated as part of the Libero configuration.
58893	The second PCIe controller of the M2S090 is now correctly reset as part of the system's initialization.

Version 2.1

This is the first production release of the SmartFusion2 CMSIS Hardware Abstraction Layer.

SmartFusion2 CMSIS Hardware Abstraction Layer source code SVN revision numbers

The table below lists the SVN revision number of the files making up the SmartFusion2 CMSIS Hardware Abstraction Layer. These revision numbers can be seen at the top of each source file. They can be used to identify the version of driver used in an existing project.

Tool Chain Independent Files

File	SVN revision		
	Version 2.1	Version 2.2	Version 2.3
CMSIS/m2sxxx.h	5267	6526	6526
CMSIS/system_m2sxxx.h	5280	5280	5280
CMSIS/system_m2sxxx.c	5280	6687	7375
CMSIS/mss_assert.h	5279	6422	6422
CMSIS/sys_init_cfg_types.h	4410	4410	4410
CMSIS/hw_reg_io.h	5263	5263	5263
hal/hal.h	5258	5258	5258
hal/hal_assert.h	5274	5274	7375
hal/hw_reg_access.h	5258	5258	5258
hal/CortexM3/cortex_nvic.h	5257	5257	5257
hal/CortexM3/cortex_nvic.c	5259	5259	7375

SoftConsole specific files

File	SVN revision		
	Version 2.1	Version 2.2	Version 2.3
CMSIS/startup_gcc/debug-in-external-ram.ld	5269	6692	n/a
debug-in-microsemi-smartfusion2-external-ram.ld	n/a	n/a	7349
CMSIS/startup_gcc/debug-in-microsemi-smartfusion2-envm.ld	5269	6693	7419
CMSIS/startup_gcc/debug-in-microsemi-smartfusion2-esram.ld	5269	6693	7419
CMSIS/startup_gcc/newlib_stubs.c	5269	6665	6665
CMSIS/startup_gcc/production-execute-in-place.ld	5269	6693	7454
CMSIS/startup_gcc/production-relocate-executable.ld	5269	6691	7419
CMSIS/startup_gcc/startup_m2sxxx.s	5269	6676	7413

hal/CortexM3/GNU/cpu_types.h	5258	5258	5258
hal/CortexM3/GNU/hal.S	5258	6667	6667
hal/CortexM3/GNU/hw_macros.h	5258	5258	5258
hal/CortexM3/GNU/hw_reg_access.S	5258	6667	6667

Note: *hal.s* and *hw_reg_access.s* were renamed to *hal.S* and *hw_reg_access.S* (please note difference in lower case "s" and upper case "S") in version 2.2 of the SmartFusion2 CMSIS-HAL.

IAR Embedded Workbench specific files

File	SVN revision		
	Version 2.1	Version 2.2	Version 2.3
CMSIS/startup_iar/startup_m2sxxx.s	5268	6270	7413
CMSIS/startup_iar/write.c	4948	6704	7375
CMSIS/startup_iar/read.c	4948	6704	7375
CMSIS/startup_iar/low_level_init.c	n/a	6717	7375
CMSIS/startup_iar/vector_table.c	n/a	6270	6270
CMSIS/startup_iar/default_irqs.c	n/a	6270	6270
CMSIS/startup_iar/smartfusion2_esram_debug.icf	n/a	6698	7419
CMSIS/startup_iar/smartfusion2_envm.icf	n/a	6698	7419
CMSIS/startup_iar/smartfusion2_mddr_debug.icf	n/a	6698	7419
CMSIS/startup_iar/smartfusion2_envm_to_mddr.icf	n/a	6698	7419
hal/CortexM3/EWARM/cpu_types.h	5258	5258	5258
hal/CortexM3/EWARM/hal.s	5258	5258	5258
hal/CortexM3/EWARM/hw_macros.h	5258	5258	5258
hal/CortexM3/EWARM/hw_reg_access.s	5258	5258	5258

Keil-MDK specific files

File	SVN revision		
	Version 2.1	Version 2.2	Version 2.3
CMSIS/startup_arm/startup_m2sxxx.s	5280	6656	7419
CMSIS/startup_arm/retarget.c	4949	6704	7375
CMSIS/startup_arm/low_level_init.c	n/a	6703	7375
CMSIS/startup_arm/smartfusion2_esram_debug.sct	n/a	6656	7419
CMSIS/startup_arm/smartfusion2_execute_in_place.sct	n/a	6656	7419
CMSIS/startup_arm/smartfusion2_mddr_debug.sct	n/a	6656	7419

CMSIS/startup_arm/smartfusion2_relocate_to_external_ram.sct	n/a	6656	7419
hal/CortexM3/Keil/cpu_types.h	5258	5258	5258
hal/CortexM3/Keil/hal.s	5261	5261	5261
hal/CortexM3/Keil/hw_macros.h	5258	5258	5258
hal/CortexM3/Keil/hw_reg_access.s	5258	5258	5258