RN0236

Release Notes

MIV_RV32 v3.0

Released

October 2020

Contents

1 Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

1.1 Revision 2.0

Revision 2.0 of this document was published in October 2020. The following is a summary of changes.

- Changed the core name to MIV_RV32 from MIV_RV32IMC. This configuration neutral name allows for future expansion of support for additional RISC-V ISA extensions.

1.2 Revision 1.0

Revision 1.0 is the first publication of this document published in March 2020.

2 MIV_RV32 v3.0 Release Notes

2.1 Overview

These release notes are issued with the production release of MIV_RV32 v3.0. This document provides details about the features, enhancements, system requirements, supported families, implementations, and known issues and workarounds of the IP.

2.2 Features

MIV_RV32 has the following features:

- Designed for low power FPGA soft-core implementations
- Supports the RISC-V standard RV32I ISA with optional M and C extensions
- Availability of Tightly Coupled Memory, with size defined by address range
- TCM APB Slave (TAS) to TCM
- Boot ROM feature to load an image and run from memory
- External, Timer and Soft Interrupts
- Up to six optional external interrupts
- Vectored and non-vectored interrupt support
- Optional on-chip debug unit with a JTAG interface
- AHBL, APB3, and AXI3/AXI4 optional external bus interfaces

2.3 Delivery Types

No license is required to use MIV_RV32. Complete RTL source code is provided for the core.

2.4 Supported Families

- PolarFire SoC®
- PolarFire RT®
- PolarFire®
- RTG4™
- IGLOO®2
- SmartFusion®2

2.5 Installation Instructions

The MIV_RV32 CPZ file must be installed into Libero software. This is done automatically through the Catalog update function in Libero, or the CPZ file can be manually added using the Add Core catalog feature. Once the CPZ file is installed in Libero, the core can be configured, generated, and instantiated within a design for inclusion in the Libero project.

See the Libero SoC Online Help for further instructions on core installation, licensing, and general use.

2.6 Documentation

This release contains a copy of the MIV_RV32 Handbook and RISC-V Specification documents. The handbook describes the core functionality and gives step-by-step instructions on how to simulate, synthesize, and place-and-route this core, and also implementation suggestions. See the Libero SoC Online Help for instructions on obtaining IP documentation.

A design guide is also included which walks through an example Libero design for PolarFire®.

For updates and additional information about the software, devices, and hardware, visit the Intellectual Property pages on the Microsemi SoC Products Group website:

http://www.microsemi.com/products/fpga-soc/design-resources/ip-cores

More information can also be obtained from *MI-V embedded ecosystem*.

2.7 Supported Test Environments

No testbench is provided with MIV_RV32.

The MIV_RV32 RTL can be used to simulate the processor executing a program using a standard Libero generated testbench.

2.8 Discontinued Features and Devices

None.

2.9 Known Limitations and Workarounds

The following are the limitations and workaround applicable to the MIV_RV32 v3.0 release.

1. The TCM is limited to a maximum size of 256 Kb.
2. To initialize the TCM in PolarFire using the system controller, a local parameter **l_cfg_hard_tcm0_en**, in the **miv_rv32_opsrv_cfg_pkg.v** file should be changed to 1’b1 prior to synthesis. See section 2.7 in MIV_RV32 v3.0 Handbook.
3. Debugging over GPIO using FlashPro 5 should be limited to 10 MHz maximum.
4. Please note the JTAG_TRSTN input is now active low. In previous versions, this input was active high.

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