CoreAHBLite v5.2 Release Notes

This document accompanies the release of CoreAHBLite v5.2. It describes the features and enhancements of CoreAHBLite v5.2. It also contains the information on system requirements, supported families, implementations, known issues and workarounds, and resolved issues of previous version.

Features

CoreAHBLite has the following features:

- Supports four masters
- Supports up to 16 slaves (up to 17 in one mode, if the huge slave is in use)
- Address space per slave varies from 256 bytes to 256 MB (Huge slave occupies 2 GB)
- Supports allocation of slave slots to a “combined region” slave interface in most modes
- Allows access to slave slots to be enabled on a per master basis. All masters have equal priority (round-robin arbitration scheme)
- Supports remapping feature for master 0 interface

Interfaces

CoreAHBLite v5.2 supports four AHB-Lite master interfaces and up to 16 AHB-Lite slave interfaces (up to 17 slave interfaces are supported in one mode when the huge slave is in use).

Microsemi recommends using SmartDesign to connect and configure CoreAHBLite v5.2 while creating a system design.

Delivery Types

CoreAHBLite v5.2 is licensed in two ways, obfuscated or register transfer level (RTL).

Obfuscated

Complete RTL code is provided for the core, allowing the core to be instantiated with SmartDesign. Simulation, synthesis, and layout can be performed within Libero® System-on-Chip (SoC). The RTL code for the core is obfuscated.

RTL

Complete RTL source code is provided for the core.

Supported Families

CoreAHBLite supports the following families:

- SmartFusion®2
- SmartFusion®
- Microsemi Fusion®
- IGLOO®
- IGLOO®e
- IGLOO™ PLUS
- ProASIC®3

- ProASIC®3E
- ProASIC®3L
- Axcelerator®
- RTAX-S
- IGLOO®2
- RTG4™

Supported Tool Flows

Use Libero v8.6 or later with CoreAHBLite v5.2 release.

Installation Instructions

CoreAHBLite v5.2 is available through the Libero SoC IP Catalog. Download it from a remote web-based repository into your local vault. In the Libero software instantiate, configure, connect, and generate the core using the SmartDesign tool.

New Features and Devices

- Additional memory space configuration options have been added. Slave slot size can now vary from 256 bytes to 256 Mbytes.
- Slave slots can now be combined, allowing multiple areas of the memory space to be accessed through the S16 slave interface. This feature is useful while accessing microcontroller subsystem (MSS) resources in SmartFusion or SmartFusion2 devices.

Discontinued Features and Devices

CoreAHBLite v3.0 and v3.1 provided 16 initialization interfaces when configured in a particular mode. These interfaces can be addressed at fixed locations (from 0x00040000 to 0x0004FFFF) in the CoreAHBLite memory map. These initialization interfaces are not supported in CoreAHBLite v4.0 and later versions.

Known Issues and Workarounds

There are no known issues in CoreAHBLite v5.2.

Release History

Table 1 Release History

Version	Date	Changes
5.2	November 2014	Added IGLOO2 and RTG4 support.
5.0	November 2013	Added two more master interfaces. CoreAHBLite can now support a total of four masters.
4.0	March 2013	A greater range of memory space configurations are now supported. Slave slot size can range from 256 bytes to 256 Mbytes. Mode with 16 x 64 Kbyte slots along with one huge (2 GByte) slot is still supported, but initialization interfaces located from 0x00040000 – 0x0004FFFF are no longer supported in this mode. Combining of slave slots is now possible. This allows multiple regions of the memory map to be accessed through a single slave interface (S16). This feature may be useful while accessing MSS resources in the SmartFusion or SmartFusion2 device.
3.1	February 2010	Added capability for memory maps to be altered in SmartDesign to reflect the value of the

Version	Date	Changes
		MODE_CFG parameter.
3.0	November 2009	Added another memory configuration mode. Added huge slot capability and Init/Config client support.
2.0	March 2009	Added multi-master capability and additional ports to satisfy multi-master capability.
1.3	August 2007	Minor updates.
1.2	January 2006	Minor updates.
1.1	November 2005	First production release.

Resolved Issues in the v3.1 Release

Table 2 Resolved SARs in CoreAHBLite v3.1 Release

SAR	Description
23409	XPATH equations needed to differentiate mode memory maps.

Resolved Issues in the v3.0 Release

Table 3 Resolved SARs in CoreAHBLite v3.0 Release

SAR	Description
14960	Validation should warn if all slots are disabled.
12612	Core now supports 60 MHz operation.
17753	File components.vhd needs to be packaged using logical library COREAHBLITE_LIB.
14958	Clock and reset signals should be tagged as mandatory.
14666	Remap input has no default value in SmartDesign.
19750	Mirrored slave HMASTLOCK_S* outputs need to be brought out at top level.

Resolved Issues in the v2.0 Release

The v2.0 release is an updated version of the previous release, with new I/O signals and some modified I/O signals.

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