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CoreTBItoEPCS v2.2 Release Notes

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1 Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

1.1 Revision 4.0

Updated section Delivery Types.

1.2 Revision 3.0

Updated changes related to CoreTBItoEPCS v2.2.

1.3 Revision 2.0

Updated changes related to CoreTBItoEPCS v2.1.

1.4 Revision 1.0

Revision 1.0 was the first publication of this document. Created for CoreTBItoEPCS v2.0.

Contents

2 Preface

2.1 Purpose

These release notes accompany the production release of CoreTBItoEPCS v2.2. This document provides details about the features, enhancements, system requirements, supported families, implementations, and known issues and workarounds.

2.2 Intended Audience

FPGA designers using Libero® System-on-Chip (SoC).

3 CoreTBItoEPCS v2.2 Release Notes

3.1 Overview

These release notes accompany the production release of CoreTBItoEPCS v2.2. This document provides details about the features, enhancements, system requirements, supported families, implementations, and known issues and workarounds.

3.2 Features

CoreTBItoEPCS implements an Rx/Tx TBI interface and Rx/Tx External PCS interfaces and has the following features:

- TBI and EPCS clocks are asynchronous to each other.
- TBI clock frequency = 62.5 MHz and EPCS clock frequency = 125 MHz.
- Data on TBI (TCGF/RCGF) bus comes with double data rate.
- TBI data width is 10 bits.
- EPCS data width is 20 bits, but only 10 bits are used depending, on the TX_UPPER_EPCS/RX_UPPER_EPCS parameter/generic.
- This bridge accepts data from TBI only after PHY is ready (EPCS_READY), assuming that TBI will not send data until the PHY is ready.

3.3 Delivery Types

CoreTBItoEPCS is licensed free.

3.3.1 RTL

Complete Verilog and VHDL RTL source code is provided for the core and testbenches.

3.4 Supported Families

- IGLOO®2
- SmartFusion®2

3.5 Supported Tool Flows

- CoreTBItoEPCS v2.2 requires Libero® System-on-Chip (SoC) software v11.6.
- Microsemi® SoC Products Group Libero software v11.6 can be used with CoreTBItoEPCS.

Note: CoreTBItoEPCS is compatible with Libero System-on-Chip (SoC).

3.6 Installation Instructions

The CoreTBItoEPCS CPZ file must be installed into Libero software. This is done automatically through the Catalog update function in Libero, or the CPZ file can be manually added using the **Add Core** catalog feature. Once the CPZ file is installed in Libero, the core can be configured, generated, and instantiated within SmartDesign for inclusion in the Libero project.

Refer to the *Libero SoC Online Help* for further instructions on core installation, licensing, and general use.

3.7 Documentation

This release contains a copy of the *CoreTBItoEPCS Handbook*. The handbook, describes the core functionality and gives step-by-step instructions on how to simulate, synthesize, and place-and-route this core, and also implementation suggestions. Refer to the *Libero SoC Online Help* for instructions on obtaining IP documentation.

For updates and additional information about the software, devices, and hardware, visit the Intellectual Property pages on the Microsemi SoC Products Group website: visit:

http://www.microsemi.com/products/fpga-soc/design-resources/ip-cores.

3.8 Supported Test Environments

The following test environments are supported:

- Verilog user testbench
- VHDL user testbench

3.9 Resolved History

Table 1 lists the release history for CoreTBItoEPCS.

Table 1 • **Release History**

Version	Date	Changes
2.2	September 2016	Updated CoreTBItoEPCS v2.2 Handbook.
2.1	March 2014	Support for IGLOO2 added.
2.0	December 2012	Initial version of the core.

3.10 Resolved Issues in the v2.2 Release

There were no SARs were resolved in the v2.2 release.

3.11 Resolved Issues in the v2.1 Release

Table 2 • **Resolved Issues in the v2.1 Release**

SAR Number	Changes
55717	Updated the core packing format from CCZ to CPZ.
53341	VHDL: Some processes are not sensitive to the clock edge when they should be.

3.12 Resolved Issues in the v2.0 Release

As this is the initial version there were no SARs were resolved in the v2.0 release.

3.13 Discontinued Features and Devices

There are no discontinued features or devices.

3.14 Known Limitations and Workarounds

There are no known limitations and workarounds.