RN0044

CorePCIF_AHB v4.3 Release Notes

Microsemi
a Microchip company

Microsemi Headquarters
One Enterprise, Aliso Viejo,
CA 92656 USA
Within the USA: +1 (800) 713-4113
Outside the USA: +1 (949) 380-6100
Sales: +1 (949) 380-6136
Fax: +1 (949) 215-4996
Email: sales.support@microsemi.com
www.microsemi.com

About Microsemi

Microsemi, a wholly owned subsidiary of Microchip Technology Inc. (Nasdaq: MCHP), offers a comprehensive portfolio of semiconductor and system solutions for aerospace & defense, communications, data center and industrial markets. Products include high-performance and radiation-hardened analog mixed-signal integrated circuits, FPGAs, SoCs and ASICs; power management products; timing and synchronization devices and precise time solutions, setting the world's standard for time; voice processing devices; RF solutions; discrete components; enterprise storage and communication solutions, security technologies and scalable anti-tamper products; Ethernet solutions; Power-over-Ethernet ICs and midspans; as well as custom design capabilities and services. Learn more at www.microsemi.com.

51300044-11/9.20

1 Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

1.1 Revision 11.0

Added PolarFire® SoC support.

1.2 Revision 10.0

Updated changes related to CorePCIF_AHB v4.2.

1.3 Revision 9.0

Updated changes related to CorePCIF_AHB v4.1.

1.4 Revision 8.0

Updated changes related to CorePCIF_AHB v4.0.

1.5 Revision 7.0

Updated changes related to CorePCIF_AHB v3.7.

1.6 Revision 6.0

Updated changes related to CorePCIF_AHB v3.6.

1.7 Revision 5.0

Updated changes related to CorePCIF_AHB v3.5.

1.8 Revision 4.0

Updated changes related to CorePCIF_AHB v3.4.

1.9 Revision 3.0

Updated changes related to CorePCIF_AHB v3.3.

1.10 Revision 2.0

Updated changes related to CorePCIF_AHB v3.2.

1.11 Revision 1.0

Revision 1.0 was the first publication of this document. Created for CorePCIF_AHB v3.1.

Contents

2 CorePCIF_AHB v4.3 Release Notes

2.1 Overview

These release notes accompany the production release of CorePCIF_AHB v4.3. This document provides details about the features, enhancements, system requirements, supported families, implementations, and known issues and workarounds.

2.2 Features

CorePCIF_AHB is a highly configurable core, including the following features:

- Implements a PCI to AHB bridge
- Allows transfers to be initiated from the PCI or AHB side
- Supports asynchronous clocks
- Direct Master functions
- Built-in DMA controller
- Interrupt capability
- CardBus support
- Configurable user testbench
- Hot-swap extended capabilities support for compact PCI

2.3 Interfaces

The CorePCIF_AHB core supports PCI specification v2.3 and an AHB interface.

2.4 Delivery Types

The CorePCIF_AHB core is licensed in two ways: Obfuscated and RTL.

2.4.1 Evaluation

Precompiled simulation libraries are provided, allowing the core to be instantiated in SmartDesign and simulated in Libero. The design may not be synthesized, as source code is not provided.

2.4.2 Obfuscated

Complete RTL code is provided for the core, enabling the core to be instantiated with SmartDesign. Simulation, synthesis, and layout can be performed with Libero software. The RTL code for the core is obfuscated.

2.4.3 RTL

Complete RTL source code is provided for the core and testbenches.

2.5 Supported Families

- PolarFire® SoC
- PolarFire®
- RTG4™
- SmartFusion®2
- IGLOO®2
- SmartFusion®
- IGLOO®
- IGLOO®e
- Fusion
- ProASIC®3
- ProASIC®3E
- ProASIC®3L

2.6 Supported Tool Flows

CorePCIF_AHB v4.3 requires Libero v9.0 or later.

Note: CorePCIF is compatible with Libero Integrated Design Environment (IDE), Libero System-on-Chip (SoC), and Libero System-on-Chip (SoC) PolarFire. Unless specified otherwise, this document uses the name Libero to identify Libero IDE, Libero SoC, and Libero SoC PolarFire.

2.7 Installation Instructions

The CorePCIF_AHB CPZ file must be installed into Libero software. This is done automatically through the Catalog update function in Libero, or the CPZ file can be manually added using the **Add Core** catalog feature. Once the CPZ file is installed in Libero, the core can be configured, generated, and instantiated within SmartDesign for inclusion in the Libero project. For more information, see the *Knowledge Based article*.

To know how to create SmartDesign project using the IP cores, refer to *Libero SoC documents page* and use the latest SmartDesign user guide.

2.8 Documentation

This release contains a copy of the *CorePCIF_AHB Handbook*. The handbook, describes the core functionality and gives step-by-step instructions on how to simulate, synthesize, and place-and-route this core, and also implementation suggestions. Refer to *Libero SoC documents page* for instructions on obtaining IP documentation.

For updates and additional information, visit the Intellectual Property pages on the Microsemi SoC Products Group website: visit:

http://www.microsemi.com/products/fpga-soc/design-resources/ip-cores.

2.9 Supported Test Environments

- Verilog user testbench
- VHDL user testbench

2.10 Resolved History

Table 1 lists the release history for CorePCIF_AHB.

Table 1 • **Release History**

Version	Date	Changes
4.3	September 2020	• Added PolarFire SoC support.
4.2	October 2018	• Updated the family specific libraries in the obfuscated version of the core.
4.1	November 2017	• Added support for RTG4 and PolarFire devices families. • Resolved SARs listed in Table 2.
4.0	December 2013	• Added support for SmartFusion2 family devices.
3.7	December 2010	• Resolved SARs listed in Table 3. • SmartFusion support added
3.6	June 2009	• Resolved SARs listed in Table 4.
3.5	November 2008	• Resolved SARs listed in Table 5. • ProASIC3L support added.
3.4	April 2008	• Resolved SARs listed in Table 6.
3.3	March 2008	• Resolved SARs listed in Table 7. • Additional parameters to control global usage.
3.2		• There was no v3.2 release of CorePCIF_AHB.
3.1	January 2007	• First Production release.

2.11 Resolved Issues in v4.3 Release

There were no software action requests (SARs) resolved. PolarFireSoC support is added.

2.11.1 Resolved Issues in the v4.1 Release

Table 2 lists the Software Action Requests (SARS) that were resolved in the CorePCIF_AHB v4.1 release.

Table 2 • **Resolved Issues in the v4.1 Release**

SAR Number	Description
89836	Resolved simulation failing in evaluation version. Updated pre-compiled library provided with simulation version.
89754	Resolved blackbox inferring in synthesis for VHDL version of the core in RTG4, SF2 and IGLOO2 families. Added device library in the family specific file-set for RTG4, SF2 and IGLOO2.
89627	Added RTG4 support.
56730	Updated supported families list of Handbook and Release Notes.
29667	Updated HB with information related to DMA transfers.

2.11.2 Resolved Issues in the v3.7 Release

Table 3 lists the Software Action Requests (SARS) that were resolved in the CorePCIF_AHB v3.7 release.

Table 3 • **Resolved SARs in the CorePCIF_AHB v3.7 Release**

SAR	Description
25204	Corrected Pin assignment in PDC constraint file.
26167	MEMORY_WIDTH parameter was changed to MEMORY_SIZE in the handbook.
27873	Resolved the read followed by write issue on the AHB bus in CorePCIF_AHB.
28199	Resolved Issue in buffer memory read/write when transferring data in the boundary offset.

2.11.3 Resolved Issues in the v3.6 Release

Table 4 lists the Software Action Requests (SARS) that were resolved in the CorePCIF_AHB v3.6 release.

Table 4 • **Resolved SARs in the CorePCIF_AHB v3.6 Release**

SAR	Description
14404	Added USE_REGISTERS parameter support for all families, allowing logic tiles rather than RAM blocks to be used for the internal memory. The number of logic tiles used is based on the core configuration.
14964	If a DMA transfer is terminated with a target abort during the last data transfer, the core fails to set the DMA error bits in the DMA status register and retries the transfer. The core has been modified to set the DMA error bits and stop the DMA transfer.
14967	The testbench master incorrectly deasserts IRDYN during a disconnect cycle. The testbench master has been modified to deassert IRDY a cycle earlier.
4888 13972 13971 11775	Core packaging has been updated to improve usability in SmartDesign.

2.11.4 Resolved Issues in the v3.5 Release

Table 5 lists the Software Action Requests (SARs) that were resolved in the CorePCIF_AHB v3.5 release.

Table 5 • **Resolved SARs in the CorePCIF_AHB v3.5 Release**

SAR	Description
76225 77144	When using ProASIC3-based families, the internal RAM block used as a data FIFO now uses positive clock edges on both the read and write side of the RAM.
76987	The core has been modified so that the CLKBIBUF FPGA library cell is only used when the core generates the PCI clock. In other cases a CLKBUF is used.
77283	The GUI incorrectly grayed out the Use Global Resources options for TRDYN and IRDYN based on the Master and target selections. They were swapped over. This has been fixed.
77693	The CM8DXE2 module is no longer used and has been removed.
78605 78620 78625	Several small changes were made to the core catalog and packaging data to correct operation in Libero IDE v8.4.
79022	When GNTN is deasserted prior to FRAMEN assertion and the core only has a single word to transfer, the core deasserts REQN. This is not a violation of the PCI specification but can cause a data starvation issue, depending on the PCI arbiter behavior. The core has been modified so REQN is not deasserted in this case.
75266	Link to datasheet in catalog display changed to link to handbook.
78633	Handbook updated to clearly show BAR0 is used to access buffer memory and BAR1 the DMA control registers.

2.11.5 Resolved Issues in the v3.4 Release

Table 6 lists the Software Action Requests that were resolved in the CorePCIF_AHB v3.4 release.

Table 6 • **Resolved SARs in the CorePCIF_AHB v3.4 Release**

SAR	Description
75086 75725	It is possible for the DMA master to incorrectly restart a DMA read when RD_BUSY_MASTER is asserted and FIFO recovery is disabled. This can lead to the core stalling the PCI bus if the backend does not respond to the backend read request. This is corrected in this release.
75726	The del_buffer.vhd/v files have been modified to reduce the number of warnings generated by Synplicity. No functional changes have been made.

2.11.6 Resolved Issues in the v3.3 Release

Table 7 lists the Software Action Requests (SARs) that were resolved in the CorePCIF_AHB v3.3 release.

Table 7 • **Resolved SARs in the CorePCIF_AHB v3.3 Release**

SAR	Description
65066 65089 68247 73988 74414	Configuration GUI updates were organized so that unnecessary entries are grayed out. Also various parameter rules were added.
66197 67848	Core packaging meta-data (family names) were corrected to allow cores to be correctly filtered in the IP catalog.
68152	Core packaging memory map information was added.
74725	Added additional generics for global reset control on TRDY and IRDY.
74994	DMA data transfers from the memory buffer will fail if the target function is disabled and memory buffer enabled. This has been fixed and the tests updated to explicitly verify the DMA transfers.

2.11.7 Resolved Issues in the v3.2 Release

The release following v3.1 was v3.3. There is no v3.2 Release of CorePCIF_AHB.

2.11.8 Resolved Issues in the v3.1 Release

This is the first production release of CorePCIF_AHB. CorePCIF_AHB allows an AHB bus system to be connected to a PCI bus. CorePCIF_AHB is built on top of the CorePCIF core. The CorePCIF release note included with this release describes the revision history for the base CorePCIF core.

2.12 Known Issues and Workarounds

Table 8 lists the known issues and the associated SARs.

Table 8 • **Known Issues and Associated SARs**

SAR	Description
61217	When importing the core into Libero from CoreConsole, the constraints file may not be correctly installed in the Libero project. The constraints files must be manually installed. In the Libero file manager, right-click on the constraints section, and then import all the constraint files located in the *liberoproject/coreconsole/ccproject/CorePCIF/constraints* directory.