CoreGPIO v3.0 Release Notes

This is the production release for the CoreGPIO IP core. These release notes describe the features and enhancements for CoreGPIO v3.0. They also contain information about system requirements, supported families, implementations, and known issues and workarounds.

Features

CoreGPIO provides an advanced peripheral bus (APB) register-based interface to up to 32 general purpose inputs and 32 general purpose outputs. The input logic contains a simple 3-stage synchronization circuit and the output is set synchronously. Each bit can be set to either a fixed or register-based configuration via top-level parameters, including input type, interrupt type/enable, and output enable.

Key Features

CoreGPIO v3.0 has the following key features:

- Advanced microcontroller bus architecture (AMBA) 2 APB support, forward compatibility with AMBA 3 APB
- 8-, 16-, or 32-bit APB data width
- 1 to 32 bits of I/O for all APB-width configurations
- Fixed or configurable interrupt generation:

  Negative edge

  Positive edge

  Both edges

  Level high

  Level low
- Parameter-configurable for single-interrupt signal or up to 32-bit wide interrupt bus
- Fixed or configurable I/O type (input, output, or both)
- Configurable output enable (internal or external implementation)

Interfaces

CoreGPIO is available with an AMBA APB register interface.

Documentation

This release contains a copy of the *CoreGPIO Handbook*, which describes the core functionality, gives step-by step instructions on how to simulate, synthesize, and place-and-route the core, and includes implementation suggestions.

For updates and additional information about the software, devices, and hardware, visit the Intellectual Property pages on the Actel website at http://www.actel.com.

Delivery Types

CoreGPIO is licensed in two ways: Obfuscated and RTL.

Obfuscated

Complete RTL code is provided for the core, enabling the core to be instantiated with SmartDesign. Simulation, Synthesis, and Layout can be performed with Actel Libero® Integrated Design Environment (IDE). The RTL code for the core is obfuscated.

RTL

Complete RTL source code is provided for the core and testbenches. A license is required, contact Actel to obtain a license.

Supported Families

- IGLOO®
- IGLOOe
- IGLOO nano
- IGLOO PLUS
- ProASIC®3
- ProASIC3 nano
- ProASIC3L
- Fusion
- ProASIC PLUS®
- Axcelerator®
- RTAX-S

Supported Tool Flows

This version should be used with Libero® Integrated Design Environment (IDE) v8.5 SP1 or later.

Installation Instructions

The CoreGPIO CCZ file must be installed into Libero IDE. Within Libero IDE, click the **Add Core** button in the Catalog to locate and install a local CCZ file, or use the automatic web update feature in Libero IDE. Once the CCZ file is installed in Libero IDE, the core can be instantiated, configured, and generated within SmartDesign for inclusion in your Libero IDE project. Refer to the Libero IDE online help for further instructions on core installation, licensing, and general use.

Release History

Table 1 provides the release history of CoreGPIO.

Table 1 · CoreGPIO Release History

Version	Date	Changes
3.0	August 09	Updated for Libero IDE v8.5. Fixed issues as described in Table 2 on page 3. Added variable APB data width support. Added per-bit configurability. Added interrupt generation. Added output enable.
2.0	July 08	Minor fixes.
1.2	August 07	Added support for GPIO widths other than 8 bits.
1.0	December 05	First production release.

Resolved Issues in the v3.0 Release

Table 2 lists the software action requests (SARs) that were resolved in the CoreGPIO v3.0 release.

Table 2 · Resolved Issues in the v3.0 Release

SAR Number	Description
11663 11759	Added 8-, 16-, 32-bit mode to testbench.
11959	Added handbook to core package.
11593	Split VHDL package and VHDL top-level entity.
11805	Added support for reset value configuration.
11689 11475	Added support for 8-, 16-, and 32-bit mode in core.

Resolved Issues in the v2.0 Release

No resolved issues in the v2.0 release.

Resolved Issues in the v1.2 Release

No resolved issues in the v1.2 release.

Known Limitations and Workarounds

There are no known limitations or workarounds in the CoreGPIO v3.0 release.

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