

M2S150
Release Notes
FIL-HSP-IP_M2S
February 2018



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1 **Revision History**

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

1.1 **Revision 1.0**

Revision 1.0 was published in February 2018. It was the first publication of this document.

2 FIL-HSP-IP M2S150-ADV-DEVKIT Release Information

The FIL-HSP-IP core is designed to be used for Matlab design development and verification on real hardware using the Mathworks FPGA-in-Loop (FIL) simulation methodology on Microsemi SmartFusion2™ SoC FPGA Advanced development kit (M2S150-ADV-DEV-KIT).

2.1 Key Features

The key supported features are as follows:

- Provides connectivity between Mathworks Simulink and SmartFusion2 Advanced Development kit over Ethernet.
- Supports Ethernet speed of up to 1 Gbps.

2.2 Supported Device Families

The features are supported on SmartFusion2 M2S150TS-1FC1152.

2.3 Resource Utilization

The following table lists the resource utilization of FIL-HSP-IP, implemented in the SmartFusion 2 SOC FPFA device.

Table 1 • Resource Utilization

FPGA Elements	Used	Total	Percentage
4 LUT	3709	146124	2.54%
DFF	1686	146124	1.15%
IO Registers	0	1716	0%
Logic Elements	3935	146124	2.69%

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