RN0068
Release Notes
CoreAHBtoAPB3 v3.2

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1 Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

1.1 Revision 4.0

Added PolarFire® SoC support.

1.2 Revision 3.0

Added RTG4™ and IGLOO®2 support.

1.3 Revision 2.0

The following is a summary of the changes made in this document.

- Added explicit support for more device families.
- Width of HADDR and PADDR address bus ports increased from 24 bits to 32 bits.

1.4 Revision 1.0

The first publication of this document.

Contents

2 CoreAHBtoAPB3 v3.2

These release notes accompany the production release of CoreAHBtoAPB3 v3.2. This document provides details about the features, enhancements, system requirements, supported families, implementations, and known issues and workarounds.

2.1 Features

- Creates a bridge between advanced microcontroller bus architecture (AMBA®) advanced high-performance bus (AHB or AHB-Lite) and advanced peripheral bus (APB)
- Connects automatically to CoreAHB/CoreAHBLite and CoreAPB3 in SmartDesign
- Complies with AMBA 3 APB

2.2 Interfaces

CoreAHBtoAPB3 v3.2 supports an AHB or AHB-Lite slave interface connected to an AHB or AHB-Lite mirrored slave interface (as found on, for example, CoreAHB or CoreAHBLite) as well as an AMBA3 APB master interface that connects to an AMBA 3 APB mirrored master interface (as found on, for example, CoreAPB3).

2.3 Delivery Types

CoreAHBtoAPB3 is licensed in two ways: Obfuscated or register transfer level (RTL).

2.3.1 Obfuscated

Complete RTL code is provided for the core, allowing the core to be instantiated with SmartDesign. Simulation, synthesis, and layout can be performed within Libero® System-on-Chip (SoC). The RTL code for the core is obfuscated.

2.3.2 RTL

Complete RTL source code is provided for the core.

2.4 Supported Families

- PolarFire® SoC
- PolarFire®
- SmartFusion®2
- SmartFusion®
- Microsemi Fusion®
- IGLOO®
- IGLOOe
- IGLOO PLUS
- ProASIC®3
- ProASIC3E
- ProASIC3L
- Axcelerator®
- RTAX-S
- IGLOO®2
- RTG4™

2.5 Supported Tool Flows

Libero software v8.6 or later supports CoreAHBtoAPB3 v3.2.

2.6 Installation Instructions

The CoreAHBtoAPB3 CPZ file must be installed into Libero software. This is done automatically through the Catalog update function in Libero, or the CPZ file can be manually added using the **Add Core** catalog feature. Once the CPZ file is installed in Libero, the core can be configured, generated, and instantiated within SmartDesign for inclusion in the Libero project. For more information, see the *Knowledge Based article*.

To know how to create SmartDesign project using the IP cores, refer to *Libero SoC documents page* and use the latest SmartDesign user guide.

2.7 Documentation

This release contains a copy of the *CoreAHBtoAPB3 Handbook*. The handbook, describes the core functionality and gives step-by-step instructions on how to simulate, synthesize, and place-and-route this core, and also implementation suggestions. Refer to *Libero SoC documents page* for instructions on obtaining IP documentation.

For updates and additional information, visit the Intellectual Property pages on the Microsemi SoC Products Group website: visit:

http://www.microsemi.com/products/fpga-soc/design-resources/ip-cores.

2.8 Known Issues and Workarounds

There are no known issues for CoreAHBtoAPB3 v3.2.

2.9 Resolved Issues in the v3.2 Release

There were no software action requests (SARs) resolved. PolarFire SoC support is added.