

RN0003
Release Notes
CoreUART v5.7



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1 Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

1.1 Revision 14.0

Added PolarFire® SoC support.

1.2 Revision 13.0

Added support for PolarFire®.

1.3 Revision 12.0

Updated handbook for v5.5 core release.

1.4 Revision 11.0

Added support for RTG4™.

1.5 Revision 10.0

Added support for IGLOO®2 devices.

1.6 Revision 9.0

Added support for SmartFusion®2 devices.

1.7 Revision 8.0

A programmable option for fractional baud value was added to give extra precision.

1.8 Revision 7.0

Maintenance release. Fixed performance SAR 20741, usability SAR 18238, and other minor changes.

1.9 Revision 6.0

Maintenance release. Fixed major SAR No. 19041, and others (see Table 5).

1.10 Revision 5.0

The following is a summary of the changes made in this revision.

- Widened baud value
- Added Framing error functionality

1.11 Revision 4.0

The following is a summary of the changes made in this revision.

- Added support for IGLOO and Fusion devices
- Removed synchronous mode

1.12 Revision 3.0

Added TX and RX FIFOs

1.13 Revision 2.0

Added support for ProASIC3 devices.

1.14 Revision 1.0

The first publication of this document.

Contents

1	Revision History	3
1.1	Revision 14.0	3
1.2	Revision 13.0	3
1.3	Revision 12.0	3
1.4	Revision 11.0	3
1.5	Revision 10.0	3
1.6	Revision 9.0	3
1.7	Revision 8.0	3
1.8	Revision 7.0	3
1.9	Revision 6.0	3
1.10	Revision 5.0	3
1.11	Revision 4.0	3
1.12	Revision 3.0	3
1.13	Revision 2.0	3
1.14	Revision 1.0	4
2	CoreUART v5.7	7
2.1	Features	7
2.2	Delivery Types	7
2.2.1	Obfuscated	7
2.2.2	RTL	7
2.3	Supported Families	7
2.4	Supported Tool Flows	7
2.5	Installation Instructions	7
2.6	Documentation	8
2.7	Supported Test Environments	8
2.8	New Features and Devices	8
2.9	Resolved Issues in the v5.7 Release	8
2.10	Resolved Issues in the v5.6 Release	8
2.11	Resolved Issues in the v5.5 Release	8
2.12	Resolved Issues in the v5.4 Release	8
2.13	Resolved Issues in the v5.3 Release	8
2.14	Resolved Issues in the v5.2 Release	8
2.15	Resolved Issues in the v5.1 Release	9
2.16	Resolved Issues in the v4.2 Release	9
2.17	Resolved Issues in the v4.1 Release	9
2.18	Resolved Issues in the v4.0 Release	9
2.19	Resolved Issues in the v3.1 Release	10
2.20	Known Issues and Workarounds	10

Tables

Table 1	Resolved Issues in the CoreUART v5.5 Release	8
Table 2	Resolved Issues in the CoreUART v5.1 Release	9
Table 3	Resolved Issues in the CoreUART v4.2 Release	9
Table 4	Resolved Issues in the CoreUART v4.1 Release	9
Table 5	Resolved Issues in the CoreUART v4.0 Release	9
Table 6	Resolved Issues in the CoreUART (previous releases)	10

2 CoreUART v5.7

This is the production release for the CoreUART IP core. These release notes describe the features and enhancements for CoreUART IP v5.7. They also contain information about system requirements, supported families, implementations, and known issues and workarounds.

2.1 Features

CoreUART is a highly configurable core and has the following features:

- Asynchronous mode to interface with industry standard UART
- Optional Transmit and Receive FIFOs

2.2 Delivery Types

No license needed.

2.2.1 Obfuscated

Complete RTL code is provided for the core, enabling the core to be instantiated with SmartDesign. Simulation, Synthesis, and Layout can be performed with Libero[®] System-on-Chip (SoC). The RTL code for the core is obfuscated.

2.2.2 RTL

Complete RTL source code is provided for the core and testbenches.

2.3 Supported Families

- PolarFire[®] SoC
- PolarFire[®]
- RTG4[™]
- IGLOO[®]2
- SmartFusion[®]2
- SmartFusion[®]
- IGLOO[®]
- IGLOOe
- IGLOO PLUS
- ProASIC[®]3
- ProASIC3E
- ProASIC3L
- Fusion
- ProASICPLUS[®]
- Axcelerator[®]
- RTAX-S
- SX-A
- RTSX-S

2.4 Supported Tool Flows

This version of the core requires Libero v8.6 or later.

2.5 Installation Instructions

The CoreUART CPZ file must be installed into Libero software. This is done automatically through the Catalog update function in Libero, or the CPZ file can be manually added using the **Add Core** catalog feature. Once the CPZ file is installed in Libero, the core can be configured, generated, and instantiated within SmartDesign for inclusion in the Libero project. For more information, see the [Knowledge Based article](#).

To know how to create SmartDesign project using the IP cores, refer to *Libero SoC documents page* and use the latest SmartDesign user guide.

2.6 Documentation

This release contains a copy of the *CoreUART Handbook*. The handbook, describes the core functionality and gives step-by-step instructions on how to simulate, synthesize, and place-and-route this core, and also implementation suggestions. Refer to *Libero SoC documents page* for instructions on obtaining IP documentation.

For updates and additional information, visit the Intellectual Property pages on the Microsemi SoC Products Group website: visit:

<http://www.microsemi.com/products/fpga-soc/design-resources/ip-cores>.

2.7 Supported Test Environments

The following test environments are supported for CoreUART:

- Verilog user testbench
- VHDL user testbench

2.8 New Features and Devices

The following new features and devices are included in the v5.7 release:

- Support for PolarFire SoC added

2.9 Resolved Issues in the v5.7 Release

There were no software action requests (SARs) resolved. PolarFire SoC support is added.

2.10 Resolved Issues in the v5.6 Release

No additional SARs were resolved in the v5.6 release.

2.11 Resolved Issues in the v5.5 Release

Table 1 lists the SARs that were resolved in the CoreUART v5.5 release.

Table 1 • Resolved Issues in the CoreUART v5.5 Release

SAR No.	Description
66586	Baudval zero is not supported, to be updated in the handbook.

2.12 Resolved Issues in the v5.4 Release

No additional SARs were resolved in the v5.4 release.

2.13 Resolved Issues in the v5.3 Release

No additional SARs were resolved in the v5.3 release.

2.14 Resolved Issues in the v5.2 Release

No additional SARs were resolved in the v5.2 release.

2.15 Resolved Issues in the v5.1 Release

Table 2 lists the software action requests (SARs) that were resolved in the CoreUART v5.1 release.

Table 2 • Resolved Issues in the CoreUART v5.1 Release

SAR No.	Description
37390	Addition of the fractional baud value feature

2.16 Resolved Issues in the v4.2 Release

Table 3 lists the software action requests (SARs) that were resolved in the CoreUART v4.2 release.

Table 3 • Resolved Issues in the CoreUART v4.2 Release

SAR No.	Description
18238	CoreUART and CoreUARTapb can be instantiated in the same design without module name conflicts.
20741	Performance improvement for continuous transmission when TX FIFO enabled; there is no longer a 3-bit delay between byte transmissions.

2.17 Resolved Issues in the v4.1 Release

Table 4 lists the software action requests (SARs) that were resolved in the CoreUART v4.1 release.

Table 4 • Resolved Issues in the CoreUART v4.1 Release

SAR No.	Description
19342	Framing error is cleared on byte receive in FIFO mode.
19282	FIFO overflow error has been fixed.
19041	RXRDY in FIFO mode fixed.

2.18 Resolved Issues in the v4.0 Release

Table 5 lists the software action requests (SARs) that were resolved in the CoreUART v4.0 release.

Table 5 • Resolved Issues in the CoreUART v4.0 Release

SAR No.	Description
12177	Added URL resource links to CoreUART package.
11848	Core naming rules fixed.
11849	Device name fixed for SX-A in handbook.
11928	Fixed FIFO error during synthesis for IGLOO family.
12126	Fixed RXRDY assertion bug, whereby RXRDY is asserted when RX stays low for an entire byte. This is fixed by adding a FRAMING_ERR signal to indicate a missing stop bit.

2.19 Resolved Issues in the v3.1 Release

Table 6 lists the software action requests (SARs) that were resolved in previous releases of CoreUART.)

Table 6 • Resolved Issues in the CoreUART (previous releases)

SAR No.	Description
59866	Changed the received_full signal name to rxrdy in order match its functionality.
54173	Added explanation for the default parameters in the handbook.
61666	Modified the FIFO flags to match the programmed FIFO level signals.

2.20 Known Issues and Workarounds

There are no known limitations or workarounds in the CoreUART v5.7 release.