CoreSPI v3.0 Release Notes

This is the production release for the CoreSPI IP core. These release notes describe the features and enhancements of the core. They also contain information about system requirements, supported families, implementations, and known issues and workarounds.

Features

The Serial Peripheral Interface (SPI) allows high-speed synchronous serial data transfer between microprocessors/microcontrollers and peripheral devices. CoreSPI core implements the Serial Peripheral Interface, which can operate as a Master, a Slave, or both Master and Slave.

Key features of CoreSPI are as follows:

- Full duplex, synchronous, 8-bit serial data transfer
- High bit rates
- Master or Slave mode or both Master and Slave
- Bit rates generated in Master mode: 1/2, 1/4, 1/8, 1/16, 1/32, 1/64, 1/128, and 1/256 of f_{PCLK}
- Bit rates supported in Slave mode: $f_{PCLK} \leq f_{PCLK}/2$
- 8 Slave Select lines.
- MSB first or LSB first data transfer
- Fully synchronous design with one clock domain

Interfaces

CoreSPI contains an APB interface for direct register access via the APB bus, which is typically connected to one of the Actel soft processor cores (CoreMP7, Core8051s, or CoreABC). It also contains the Serial Peripheral Interface (SPI) for serial data transfers.

Delivery Types

The CoreSPI core is licensed in three ways: Evaluation, Obfuscated, and RTL.

Evaluation

Allows simulation of CoreSPI using Actel Libero® Integrated Design Environment (IDE) or Model*Sim*.®

Obfuscated

Complete RTL code is provided for the core, enabling the core to be instantiated with CoreConsole. Simulation, Synthesis, and Layout can be performed with Actel Libero IDE. The RTL code for the core is obfuscated, and some of the testbench source files are not provided.

RTL

Complete RTL source code is provided for the core and testbenches.

Supported Families

- Fusion
- IGLOO™/e
- ProASIC®3/E
- ProASIC PLUS®
- Axcelerator®
- RTAX-S

Supported Tool Flows

Use CoreConsole v1.2.1 and Libero IDE v7.3 or later with this CoreSPI release.

Installation Instructions

The CoreSPI CCZ file must be installed using CoreConsole. Using **Actions** > **Add to database** in CoreConsole, locate and install the CCZ file. Then shut down and restart CoreConsole (this should be done when no CoreConsole project is open). Once installed in CoreConsole, the core can be instantiated, configured, and exported to Libero IDE. For the RTL and Obfuscated versions of the core, the FlexLM license must be installed and CoreConsole restarted before the core can be exported. Consult CoreConsole online help for further instructions with core installation and licensing.

Documentation

This release contains a copy of the *CoreSPI Handbook*, which describes the core functionality, gives step-by-step instructions on how to simulate, synthesize, and place-and-route this core, and includes implementation suggestions. The documentation can be viewed by right-clicking the **Core Selection** pane in CoreConsole after the core has been installed. For updates and additional information about

the software, devices, and hardware, visit the Intellectual Property pages on the Actel website at http://www.actel.com.

Supported Test Environments

The following test environments are supported for CoreSPI:

- VHDL user testbench
- Verilog user testbench
- VHDL full verification testbench
- Verilog full verification testbench

Discontinued Features

The Special Function Register (SFR) interface has been removed for this version of the core (CoreSPI v3.0).

New Features

An APB interface has been added in place of the SFR interface from previous versions of the core.

Resolved Issues in the v3.0 Release

Table 1 lists the Software Action Requests (SARs) that were resolved in the CoreSPI v3.0 release.

Table 1. Resolved SARs in the CoreSPI v3.0 Release

SAR	Description
67221	An APB interface has been added and the SFR interface has been removed for use with CoreConsole in bus-centric designs.
61318	CoreSPI was missing ProASIC3 libraries for the verification testbench (v2.1), but the testbench no longer requires family-specific libraries (v3.0).

Known Issues and Workarounds

There are no known issues for this release of CoreSPI (v3.0).

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