

**RN0239**  
**Release Notes**  
**CoreAXItoAXIConnect v2.0**



---

a  **MICROCHIP** company



a  MICROCHIP company

**Microsemi Headquarters**

One Enterprise, Aliso Viejo,  
CA 92656 USA

Within the USA: +1 (800) 713-4113

Outside the USA: +1 (949) 380-6100

Sales: +1 (949) 380-6136

Fax: +1 (949) 215-4996

Email: [sales.support@microsemi.com](mailto:sales.support@microsemi.com)

[www.microsemi.com](http://www.microsemi.com)

©2020 Microsemi, a wholly owned subsidiary of Microchip Technology Inc. All rights reserved. Microsemi and the Microsemi logo are registered trademarks of Microsemi Corporation. All other trademarks and service marks are the property of their respective owners.

Microsemi makes no warranty, representation, or guarantee regarding the information contained herein or the suitability of its products and services for any particular purpose, nor does Microsemi assume any liability whatsoever arising out of the application or use of any product or circuit. The products sold hereunder and any other products sold by Microsemi have been subject to limited testing and should not be used in conjunction with mission-critical equipment or applications. Any performance specifications are believed to be reliable but are not verified, and Buyer must conduct and complete all performance and other testing of the products, alone and together with, or installed in, any end-products. Buyer shall not rely on any data and performance specifications or parameters provided by Microsemi. It is the Buyer's responsibility to independently determine suitability of any products and to test and verify the same. The information provided by Microsemi hereunder is provided "as is, where is" and with all faults, and the entire risk associated with such information is entirely with the Buyer. Microsemi does not grant, explicitly or implicitly, to any party any patent rights, licenses, or any other IP rights, whether with regard to such information itself or anything described by such information. Information provided in this document is proprietary to Microsemi, and Microsemi reserves the right to make any changes to the information in this document or to any products and services at any time without notice.

### About Microsemi

Microsemi, a wholly owned subsidiary of Microchip Technology Inc. (Nasdaq: MCHP), offers a comprehensive portfolio of semiconductor and system solutions for aerospace & defense, communications, data center and industrial markets. Products include high-performance and radiation-hardened analog mixed-signal integrated circuits, FPGAs, SoCs and ASICs; power management products; timing and synchronization devices and precise time solutions, setting the world's standard for time; voice processing devices; RF solutions; discrete components; enterprise storage and communication solutions, security technologies and scalable anti-tamper products; Ethernet solutions; Power-over-Ethernet ICs and midspans; as well as custom design capabilities and services. Learn more at [www.microsemi.com](http://www.microsemi.com).

# 1 Revision History

---

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

## 1.1 Revision 1.0

This is the first publication of this document. Created for CoreAXItoAXIConnect v2.0.

# Contents

---

1	Revision History	3
1.1	Revision 1.0	3
2	CoreAXItoAXIConnect	5
2.1	Key Features	5
2.2	Delivery Types	5
2.2.1	Register Transfer Level (RTL)	5
2.3	Supported Families	5
2.4	Supported Tool Flows	5
2.5	Installation Instructions	5
2.6	Documentation	5
2.7	Known Issues and Workarounds	5
2.8	Resolved Issues	5

## 2 CoreAXItoAXIConnect

---

This release notes accompanies the production release of CoreAXItoAXIConnect IP Core. This document provides details about the features, system requirements, supported families, implementations, and known issues and workarounds.

### 2.1 Key Features

This IP is used as a connector between the two CoreAXI4Interconnect modules. An AXI to AXI Connector that connects a slave interface of one CoreAXI4Interconnect module with the master interface of another CoreAXI4Interconnect module with no intervening logic.

### 2.2 Delivery Types

CoreAXItoAXIConnect is licence free.

#### 2.2.1 Register Transfer Level (RTL)

The complete RTL source code is provided for the core.

### 2.3 Supported Families

The following list of families support are supported:

- PolarFire® SoC
- PolarFire®
- SmartFusion®2
- IGLOO®2
- RTG4™

### 2.4 Supported Tool Flows

Requires Libero® System-on-Chip (SoC) v12.2 or later.

### 2.5 Installation Instructions

The CoreAXItoAXIConnect CPZ file must be installed into Libero software. This is done automatically through the Catalog update function in Libero, or the CPZ file can be manually added using the **Add Core** catalog feature. Once the CPZ file is installed in Libero, the core can be configured, generated, and instantiated within SmartDesign for inclusion in the Libero project. For more information, see the *Knowledge Based article*.

To know how to create SmartDesign project using the IP cores, refer to the *SmartDesign User guide*.

### 2.6 Documentation

This release contains a copy of the CoreAXItoAXIConnect Handbook. The handbook describes the core functionality and gives step-by-step instructions on how to simulate, synthesize, and place-and-route this core and implementation suggestions.

For updates and additional information, visit the Intellectual Property pages on the Microsemi SoC Products Group website: visit:

<http://www.microsemi.com/products/fpga-soc/design-resources/ip-cores>.

### 2.7 Known Issues and Workarounds

There are no known limitations and workarounds for CoreAXItoAXIConnect.

### 2.8 Resolved Issues

No SARs - Initial Release.