CoreAHBLite v5.2

Handbook

Microsemi

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Introduction

Core Overview

CoreAHBLite implements an advanced microcontroller bus architecture (AMBA) AHB-Lite bus interconnect fabric. CoreAHBLite provides four master interfaces and can accommodate up to 16 slave interfaces. Each slave interface can be enabled or disabled for each master using the configuration graphical user interface (GUI) of the core. Slave interfaces that are not enabled do not appear for connection on the CoreAHBLite symbol and are optimized away during the synthesis. Similarly, if no slave interfaces are selected for a given master, then that master interface is disabled and optimized away during the synthesis.

CoreAHBLite supports the following memory space scenarios:

- 16 64 KB slave slots, some reserved space, and 1 huge 2 GB slave slot
- 4 GB address space apportioned into 16 slave slots, each of size 256 MB
- 256 MB address space apportioned into 16 slave slots, each of size 16 MB
- 16 MB address space apportioned into 16 slave slots, each of size 1 MB
- 1 MB address space apportioned into 16 slave slots, each of size 64 KB
- 64 KB address space apportioned into 16 slave slots, each of size 4 KB
- 4 KB address space apportioned into 16 slave slots, each of size 256 B

For all cases except the first option listed above, it is possible to allocate one or more slave slots to a **combined region** slave interface. When some slave slots have been assigned to the **combined region**, an additional slave interface becomes available for connection. This feature allows a number of (possibly noncontiguous) regions of the memory space to be associated with a single slave interface. This may be useful, in a SmartFusion®2 system-on-chip (SoC) field programmable gate array (FPGA) device, where a master located in the FPGA fabric wants to access a number of resources in the microcontroller subsystem (MSS) through a single slave interface.

The first memory space configuration listed above is useful in a SmartFusion® SoC FPGA device. The 16 64 KB slave slots occupy a total address space of 16*64*1024 = 2^{20} bytes and this suits the 20-bit address bus provided in the interface from the SmartFusion MSS to the FPGA fabric. The huge (2 GB) slave slot is useful in the opposite direction, that is, when a master based in the FPGA fabric needs to access resources in the SmartFusion MSS device.

CoreAHBLite provides a remapping facility for its master 0 connection. When remapping is enabled (by holding the REMAP_M0 input of the core High), slave slots 0 and 1 are swapped over from the viewpoint of master 0. This feature is typically used to swap memory resources between slots 0 and 1 when a processor is connected to the master 0 interface.

A block diagram of CoreAHBLite is shown in Figure 1. A typical application using CoreAHBLite is shown in Figure 2.

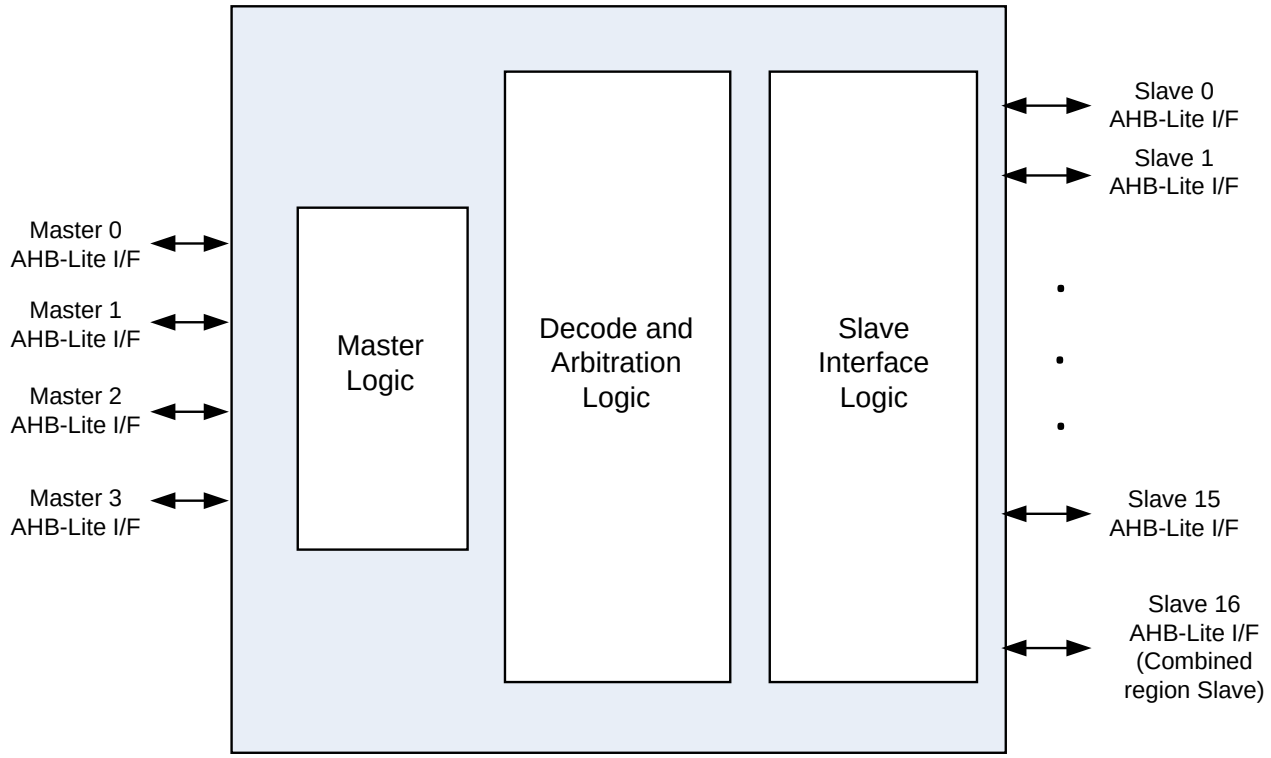

Figure 1 CoreAHBLite Block Diagram

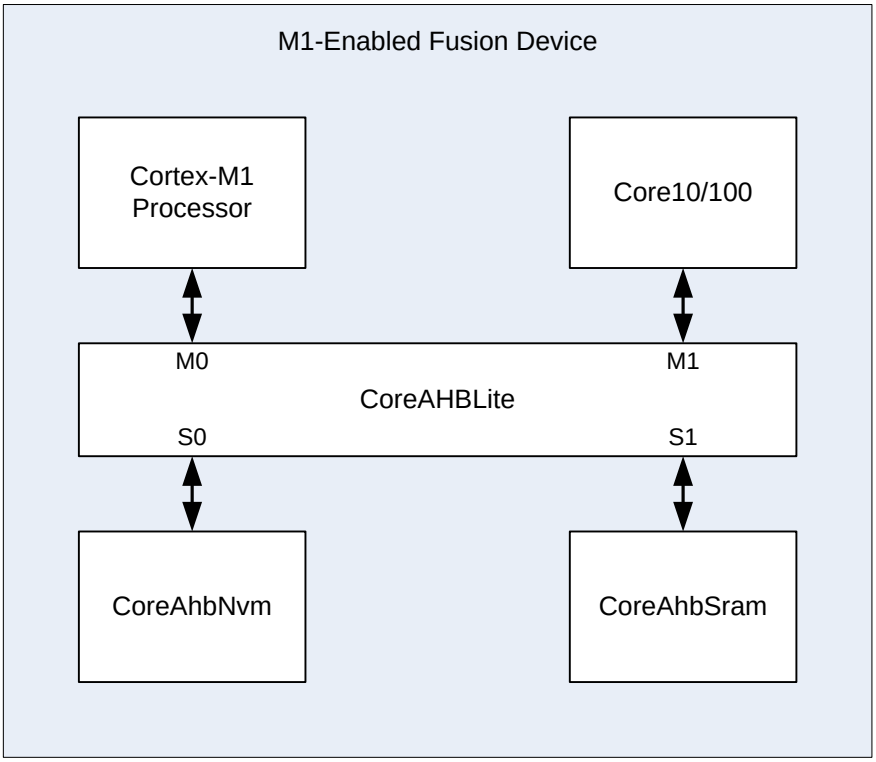

Figure 2 CoreAHBLite Typical Application

Key Features

Following are the key features of CoreAHBLite:

- Supports four masters
- Supports up to 16 slaves (up to 17 in one mode, if the huge slave is in use)
- Address space per slave varies from 256 bytes to 256 MB (huge slave occupies 2 GB.)
- Supports allocation of slave slots to a **combined region** slave interface in most modes
- Enable access to any slave slot on a per master basis
- Equal priority for all masters (round-robin arbitration scheme)
- Supports remapping feature for master 0 interface

Supported Families

The following families are supported in this version:

- SmartFusion®2
- SmartFusion®
- Microsemi Fusion®
- IGLOO®, IGLOOe, and IGLOO PLUS
- ProASIC®3, ProASIC3E, ProASIC3L
- ProASIC PLUS®
- Axcelerator®
- RTAX-S
- IGLOO®2
- RTG4™

Core Version

This handbook supports CoreAHBLite v5.2.

Supported Interfaces

CoreAHBLite supports four AHB-Lite master interfaces and up to 16 AHB-Lite slave interfaces (up to 17 slave interfaces are supported in one mode when the huge slave is in use).

Microsemi® recommends using the SmartDesign tool to connect and configure CoreAHBLite while creating a system design.

Utilization and Performance

Utilization and performance data is provided in Table 1, Table 2, and Table 3. The data is indicative only. CoreAHBLite is a bus component that interconnects between master and slave devices. The overall device utilization and performance of a system is very much system dependent.

Table 1 CoreAHBLite Device Utilization and Performance (minimum configuration, 1 master and 1 slave)

Family	FPGA Resources			Utilization		Performance (MHz)
	Sequential	Combinatorial	Total	Device	%	
SmartFusion2	67	176	243	M2S150T	0.17	250
IGLOO2	67	175	242	M2GL150T	0.17	250
RTG4	64	173	237	RT4G150	0.15	132
IGLOO/e	31	146	177	M1AGLE3000V2	< 1%	76
ProASIC3/E	31	134	165	M1A3P1000	< 1%	108
ProASIC3L	31	134	165	M1A3P1000L	< 1%	89
Fusion	31	134	165	M1AFS1500	< 1%	105
ProASIC^{PLUS}	33	136	169	APA1000	< 1%	91
Axcelerator	35	91	126	AX1000	< 1%	121
RTAX-S	35	91	126	RTAX1000S	< 1%	116

Table 2 CoreAHBLite Device Utilization and Performance (typical configuration, 1 master and 4 slaves)

Family	FPGA Resources			Utilization		Performance (MHz)
	Sequential	Combinatorial	Total	Device	%	
SmartFusion2	110	568	678	M2S150T	0.47	198
IGLOO2	110	562	672	M2GL150T	0.46	198
RTG4	90	552	642	RT4G150	0.42	103
IGLOO/e	71	391	462	M1AGLE3000V2	< 1%	49
ProASIC3/E	70	374	444	M1A3P1000	2%	105
ProASIC3L	70	364	434	M1A3P1000L	2%	72
Fusion	70	364	434	M1AFS1500	1%	91
ProASIC^{PLUS}	80	529	609	APA1000	1%	70
Axcelerator	79	300	379	AX1000	2%	94
RTAX-S	79	300	379	RTAX1000S	2%	88

Table 3 CoreAHBLite Device Utilization and Performance (two masters and 16 slaves)

Family	FPGA Resources			Utilization		Performance (MHz)
	Sequential	Combinatorial	Total	Device	%	
SmartFusion2	315	1983	2298	M2S150T	1.58	178
IGLOO2	354	2203	2557	M2GL150T	1.75	152
RTG4	272	2086	2358	RT4G150	1.55	90
IGLOO/e	190	3222	3412	M1AGLE3000V2	5%	28
ProASIC3/E	187	3053	3240	M1A3P1000	13%	71
ProASIC3L	193	3056	3249	M1A3P1000L	13%	57
Fusion	181	3238	3419	M1AFS1500	9%	61
ProASIC^{PLUS}	200	3683	3883	APA1000	7%	47
Axcelerator	292	1721	2013	AX1000	11%	103
RTAX-S	292	1721	2013	RTAX1000S	11%	81

Interface Description

Configuration Parameters

The register transfer level (RTL) code for CoreAHBLite has parameters for configuring the core. While working with the core in the SmartDesign tool, a configuration GUI is used to set the values of these parameters. CoreAHBLite parameters are described in Table 4.

Table 4 CoreAHBLite Configuration Parameters

Parameter Name	Valid Range	Default	Description
MEMSPACE	0 to 6	0	0: 16 64 KB slots, reserved space, and 1 huge (2 GB) slot beginning at address 0x80000000 1: 4 GB addressable space apportioned into 16 slave slots, each of size 256 MB 2: 256 MB addressable space apportioned into 16 slave slots, each of size 16 MB 3: 16 MB addressable space apportioned into 16 slave slots, each of size 1 MB 4: 1 MB addressable space apportioned into 16 slave slots, each of size 64 KB 5: 64 KB addressable space apportioned into 16 slave slots, each of size 4 KB 6: 4 KB addressable space apportioned into 16 slave slots, each of size 256 B
HADDR_SHG_CFG	0 or 1	1	This parameter is only relevant when MEMSPACE = 0. 0: HADDR_S16[31] tied low, huge slave address range is 0x00000000 - 0x7FFFFFFF from slave perspective. 1: HADDR_S16[31] tied high, huge slave address range is 0x80000000 - 0xFFFFFFFF from slave perspective.
M0_AHBSLOT0ENABLE	0 or 1	0	0: Disables slave 0 for master 0 1: Enables slave 0 for master 0
M0_AHBSLOT1ENABLE	0 or 1	0	0: Disables slave 1 for master 0 1: Enables slave 1 for master 0
…	…	…	…
M0_AHBSLOT15ENABLE	0 or 1	0	0: Disables slave 15 for master 0 1: Enables slave 15 for master 0
M0_AHBSLOT16ENABLE	0 or 1	0	0: Disables slave 16 for master 0 1: Enables slave 16 for master 0 (Slave 16 is the combined region slave or huge slave.)
M1_AHBSLOT0ENABLE	0 or 1	0	0: Disables slave 0 for master 1 1: Enables slave 0 for master 1

Parameter Name	Valid Range	Default	Description
M1_AHBSLOT1ENABLE	0 or 1	0	0: Disables slave 1 for master 1 1: Enables slave 1 for master 1
…	…	…	…
M1_AHBSLOT15ENABLE	0 or 1	0	0: Disables slave 15 for master 1 1: Enables slave 15 for master 1
M1_AHBSLOT16ENABLE	0 or 1	0	0: Disables slave 16 for master 1 1: Enables slave 16 for master 1 (Slave 16 is the combined region slave or huge slave.)
M2_AHBSLOT0ENABLE	0 or 1	0	0: Disables slave 0 for master 2 1: Enables slave 0 for master 2
M2_AHBSLOT1ENABLE	0 or 1	0	0: Disables slave 1 for master 2 1: Enables slave 1 for master 2
…	…	…	…
M2_AHBSLOT15ENABLE	0 or 1	0	0: Disables slave 15 for master 2 1: Enables slave 15 for master 2
M2_AHBSLOT16ENABLE	0 or 1	0	0: Disables slave 16 for master 2 1: Enables slave 16 for master 2 (Slave 16 is the combined region slave or huge slave.)
M3_AHBSLOT0ENABLE	0 or 1	0	0: Disables slave 0 for master 3 1: Enables slave 0 for master 3
M3_AHBSLOT1ENABLE	0 or 1	0	0: Disables slave 1 for master 3 1: Enables slave 1 for master 3
…	…	…	…
M3_AHBSLOT15ENABLE	0 or 1	0	0: Disables slave 15 for master 3 1: Enables slave 15 for master 3
M3_AHBSLOT16ENABLE	0 or 1	0	0: Disables slave 16 for master 3 1: Enables slave 16 for master 3 (Slave 16 is the combined region slave or huge slave.)
SC_0	0 or 1	0	This parameter is only relevant when MEMSPACE > 0. This parameter can be used to assign slave slot 0 to the combined region. 0: Slave slot 0 is not assigned to the combined region. Slave interface 0 is available for connection, if enabled. 1: Slave slot 0 is assigned to the combined region. Slave interface 16 is available for connection, if enabled, but slave interface 0 is not available for connection.

Parameter Name	Valid Range	Default	Description
SC_1	0 or 1	0	This parameter is only relevant when MEMSPACE > 0. This parameter can be used to assign slave slot 1 to the combined region. 0: Slave slot 1 is not assigned to the combined region. Slave interface 1 is available for connection, if enabled. 1: Slave slot 1 is assigned to the combined region. Slave interface 16 is available for connection, if enabled, but slave interface 1 is not available for connection.
…	…	…	…
SC_15	0 or 1	0	This parameter is only relevant when MEMSPACE > 0. This parameter can be used to assign slave slot 15 to the combined region. 0: Slave slot 15 is not assigned to the combined region. Slave interface 15 is available for connection, if enabled. 1: Slave slot 15 is assigned to the combined region. Slave interface 16 is available for connection, if enabled, but slave interface 15 is not available for connection.

Ports

The ports present on CoreAHBLite are listed in Table 5.

Table 5 CoreAHBLite Ports

Port Name	Type	Description
HRESETN	Input	AHB-Lite reset, active low asynchronous reset.
HCLK	Input	AHB-Lite clock signal. All AHB-Lite interface signals are synchronous to the rising edge of this clock.
HADDR_M0[31:0]	Input	AHB-Lite address bus for master 0.
HMASTLOCK_M0	Input	AHB-Lite locked sequence indication for master 0.
HSIZE_M0[2:0]	Input	AHB-Lite transfer size for master 0. Indicates the size of the transfer. Only byte, half-word and word transactions are supported.
HTRANS_M0[1:0]	Input	AHB-Lite transfer type for master 0. Indicates the type of the current transfer: 00: Idle 01: Busy 10: Non-sequential 11: Sequential
HWRITE_M0	Input	AHB-Lite write indication for master 0. High for a write, Low for a read.
HWDATA_M0[31:0]	Input	AHB-Lite write data for master 0.
HBURST_M0[2:0]	Input	AHB-Lite burst type for master 0. Indicates if the transfer forms part of a burst.
HPROT_M0[3:0]	Input	AHB-Lite protection control for master 0. The protection control signals provide additional information about a bus access and are primarily intended for use by a module that wishes to implement some level of protection. These signals are not passed to the slave interface.
HRESP_M0[1:0]	Output	AHB-Lite transfer response for master 0: 00: Okay 01: Error 10: Retry 11: Split HRESP_M0[1] is tied low internally. HRESP_M0[0] = 0 indicates an Okay response and HRESP_M0[0] = 1 indicates an Error response.
HRDATA_M0[31:0]	Output	AHB-Lite read data for master 0.
HREADY_M0	Output	AHB-Lite ready signal for master 0. When asserted, this signal indicates that a transfer has finished on the bus. This signal may be driven low to extend a transfer.
REMAP_M0	Input	Remap signal for master 0. When this signal is High, slots 0 and 1 are swapped over in the memory space from the viewpoint of master 0.
HADDR_M1[31:0]	Input	AHB-Lite address bus for master 1.
HMASTLOCK_M1	Input	AHB-Lite locked sequence indication for master 1.
HSIZE_M1[2:0]	Input	AHB-Lite transfer size for master 1. Indicates the size of the transfer. Only byte, half-word, and word transactions are supported.
HTRANS_M1[1:0]	Input	AHB-Lite transfer type for master 1. Indicates the type of the current transfer: 00: Idle 01: Busy 10: Non-sequential 11: Sequential
HWRITE_M1	Input	AHB-Lite write indication for master 1. High for a write, Low for a read.

Port Name	Type	Description
HWDATA_M1[31:0]	Input	AHB-Lite write data for master 1.
HBURST_M1[2:0]	Input	AHB-Lite burst type for master 1. Indicates if the transfer forms part of a burst.
HPROT_M1[3:0]	Input	AHB-Lite protection control for master 1. The protection control signals provide additional information about a bus access and are primarily intended for use by a module that wishes to implement some level of protection. These signals are not passed to the slave interface.
HRESP_M1[1:0]	Output	AHB-Lite transfer response for master 1: 00: Okay 01: Error 10: Retry 11: Split HRESP_M1[1] is tied low internally. HRESP_M1[0] = 0 indicates an Okay response and HRESP_M1[0] = 1 indicates an Error response.
HRDATA_M1[31:0]	Output	AHB-Lite read data for master 1.
HREADY_M1	Output	AHB-Lite ready signal for master 1. When asserted, this signal indicates that a transfer has finished on the bus. This signal may be driven low to extend a transfer.
HADDR_M2[31:0]	Input	AHB-Lite address bus for master 2.
HMASTLOCK_M2	Input	AHB-Lite locked sequence indication for master 2
HSIZE_M2[2:0]	Input	AHB-Lite transfer size for master 2. Indicates the size of the transfer. Only byte, half-word and word transactions are supported.
HTRANS_M2[1:0]	Input	AHB-Lite transfer type for master 2. Indicates the type of the current transfer: 00: Idle 01: Busy 10: Non-sequential 11: Sequential
HWRITE_M2	Input	AHB-Lite write indication for master 2. High for a write, Low for a read.
HWDATA_M2[31:0]	Input	AHB-Lite write data for master 2.
HBURST_M2[2:0]	Input	AHB-Lite burst type for master 2. Indicates if the transfer forms part of a burst.
HPROT_M2[3:0]	Input	AHB-Lite protection control for master 2. The protection control signals provide additional information on a bus access and are primarily intended for use by a module that wishes to implement some level of protection. These signals are not passed to the slave interface.
HRESP_M2[1:0]	Output	AHB-Lite transfer response for master 2: 00: Okay 01: Error 10: Retry 11: Split HRESP_M0[1] is tied low internally. HRESP_M0[0] = 0 indicates an Okay response and HRESP_M0[0] = 1 indicates an Error response.
HRDATA_M2[31:0]	Output	AHB-Lite read data for master 2.
HREADY_M2	Output	AHB-Lite ready signal for master 2. When asserted, this signal indicates that a transfer has finished on the bus. This signal may be driven Low to extend a transfer.
HADDR_M3[31:0]	Input	AHB-Lite address bus for master 3.
HMASTLOCK_M3	Input	AHB-Lite locked sequence indication for master 3.

Port Name	Type	Description
HSIZE_M3[2:0]	Input	AHB-Lite transfer size for master 3. Indicates the size of the transfer. Only byte, half-word and word transactions are supported.
HTRANS_M3[1:0]	Input	AHB-Lite transfer type for master 3. Indicates the type of the current transfer: 00: Idle 01: Busy 10: Non-sequential 11: Sequential
HWRITE_M3	Input	AHB-Lite write indication for master 3. High for a write, Low for a read.
HWDATA_M3[31:0]	Input	AHB-Lite write data for master 3.
HBURST_M3[2:0]	Input	AHB-Lite burst type for master 3. Indicates if the transfer forms part of a burst.
HPROT_M3[3:0]	Input	AHB-Lite protection control for master 3. The protection control signals provide additional information about a bus access and are primarily intended for use by a module that wishes to implement some level of protection. These signals are not passed to the slave interface.
HRESP_M3[1:0]	Output	AHB-Lite transfer response for master 3: 00: Okay 01: Error 10: Retry 11: Split HRESP_M0[1] is tied low internally. HRESP_M0[0] = 0 indicates an Okay response and HRESP_M0[0] = 1 indicates an Error response.
HRDATA_M3[31:0]	Output	AHB-Lite read data for master 3.
HREADY_M3	Output	AHB-Lite ready signal for master 3. When asserted, this signal indicates that a transfer has finished on the bus. This signal may be driven low to extend a transfer.
HRDATA_S0[31:0]	Input	AHB-Lite read data from slave 0.
HREADYOUT_S0	Input	AHB-Lite ready signal from slave 0.
HRESP_S0[1:0]	Input	AHB-Lite transfer response from slave 0.
HSEL_S0	Output	AHB-Lite slave 0 select.
HADDR_S0[31:0]	Output	AHB-Lite address bus for slave 0.
HSIZE_S0[2:0]	Output	AHB-Lite transfer size for slave 0.
HTRANS_S0[1:0]	Output	AHB-Lite transfer type for slave 0.
HWRITE_S0	Output	AHB-Lite write indication for slave 0.
HWDATA_S0[31:0]	Output	AHB-Lite write data for slave 0.
HMASTLOCK_S0	Output	AHB-Lite master locked sequence indication for slave 0.
HREADY_S0	Output	AHB-Lite ready signal to slave 0.
HBURST_S0[2:0]	Output	AHB-Lite burst type indication to slave 0.
HPROT_S0[3:0]	Output	AHB-Lite protection control to slave 0.
…	…	…
HRDATA_S15[31:0]	Input	AHB-Lite read data from slave 15.
HREADYOUT_S15	Input	AHB-Lite ready signal from slave 15.
HRESP_S15[1:0]	Input	AHB-Lite transfer response from slave 15.
HSEL_S15	Output	AHB-Lite slave 15 select.
HADDR_S15[31:0]	Output	AHB-Lite address bus for slave 15.
HSIZE_S15[2:0]	Output	AHB-Lite transfer size for slave 15.

Port Name	Type	Description
HTRANS_S15[1:0]	Output	AHB-Lite transfer type for slave 15.
HWRITE_S15	Output	AHB-Lite write indication for slave 15.
HWDATA_S15[31:0]	Output	AHB-Lite write data for slave 15.
HMASTLOCK_S15	Output	AHB-Lite master locked sequence indication for slave 15.
HREADY_S15	Output	AHB-Lite ready signal to slave 15.
HBURST_S15[2:0]	Output	AHB-Lite burst type indication to slave 15.
HPROT_S15[3:0]	Output	AHB-Lite protection control to slave 15.
HRDATA_S16[31:0]	Input	AHB-Lite read data from slave 16 (combined region slave or huge slave).
HREADYOUT_S16	Input	AHB-Lite ready signal from slave 16 (combined region slave or huge slave).
HRESP_S16[1:0]	Input	AHB-Lite transfer response from slave 16 (combined region slave or huge slave).
HSEL_S16	Output	AHB-Lite select for slave 16 (combined region slave or huge slave).
HADDR_S16[31:0]	Output	AHB-Lite address bus for slave 16 (combined region slave or huge slave).
HSIZE_S16[2:0]	Output	AHB-Lite transfer size for slave 16 (combined region slave or huge slave).
HTRANS_S16[1:0]	Output	AHB-Lite transfer type for slave 16 (combined region slave or huge slave).
HWRITE_S16	Output	AHB-Lite write indication for slave 16 (combined region slave or huge slave).
HWDATA_S16[31:0]	Output	AHB-Lite write data for slave 16 (combined region slave or huge slave).
HMASTLOCK_S16	Output	AHB-Lite master locked sequence indication for slave 16 (combined region slave or huge slave).
HREADY_S16	Output	AHB-Lite ready signal to slave 16 (combined region slave or huge slave).
HBURST_S16[2:0]	Output	AHB-Lite burst type indication to slave 16 (combined region slave or huge slave).
HPROT_S16[3:0]	Output	AHB-Lite protection control to slave 16 (combined region slave or huge slave).

Note: All signals in this table are active high unless otherwise stated.

Licensing

CoreAHBLite is licensed in two ways, Obfuscated or RTL.

Obfuscated

Complete RTL code is provided for the core, allowing the core to be instantiated with the SmartDesign tool. Simulation, synthesis, and layout can be performed within Libero® System-on-Chip (SoC). The RTL code for the core is obfuscated.

RTL

Complete RTL source code is provided for the core.

SmartDesign

CoreAHBLite is available through the Libero SoC IP Catalog. Download it from a remote web-based repository and install into your local vault to make it ready to use. Once installed in the Libero software, you can instantiate, configure, connect, and generate the core using the SmartDesign tool.

Configuring CoreAHBLite in SmartDesign

The CoreAHBLite configuration GUI takes up a large amount of screen area when it is sized to show all configuration options. Figure 3 shows the top portion of the configuration GUI and Figure 4 shows the bottom portion.

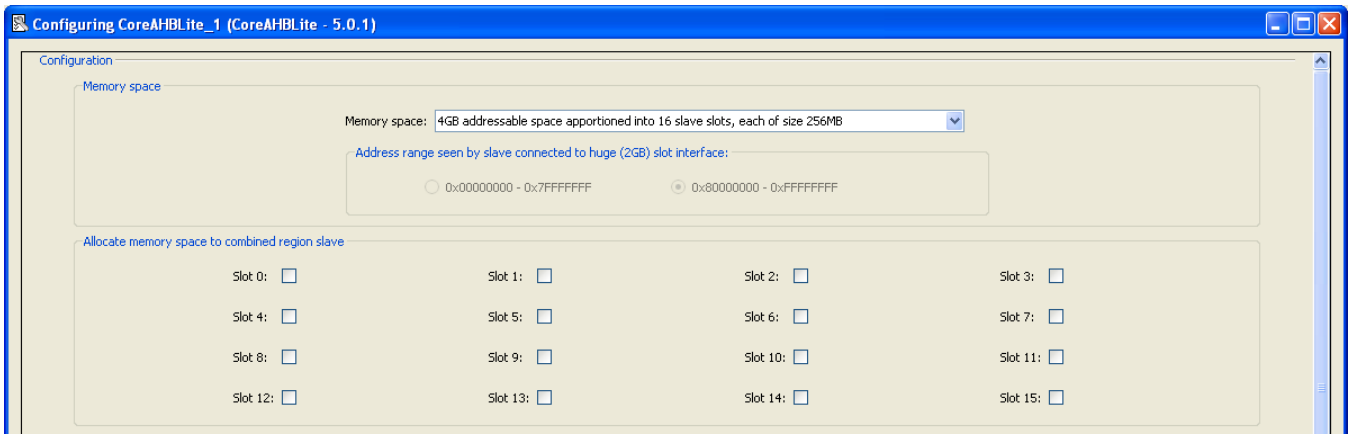

Figure 3 CoreAHBLite Configuration GUI (Top Portion)

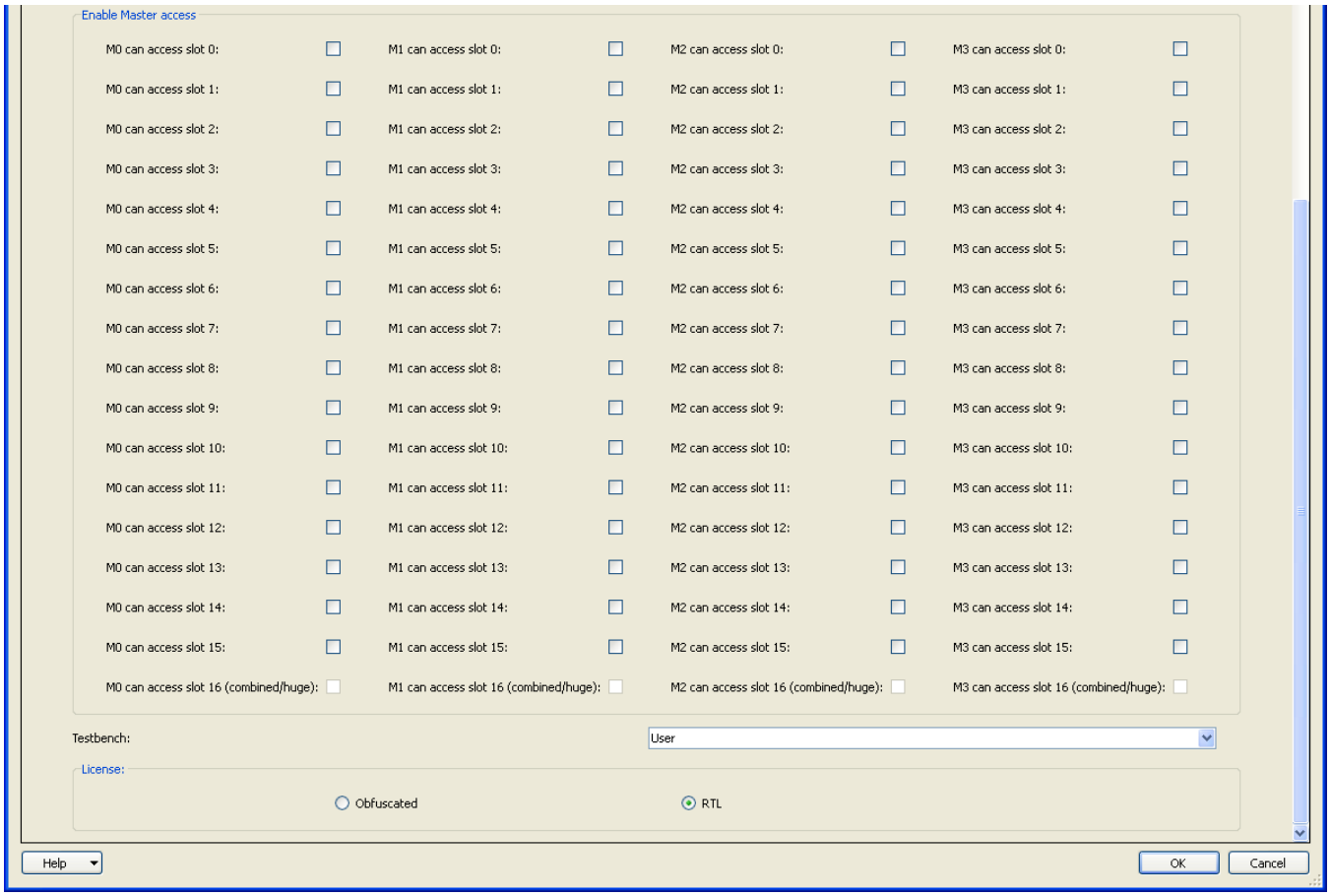

Figure 4 CoreAHBLite Configuration GUI (Bottom Portion)

The configuration options displayed in the configuration GUI correspond with the configuration parameters listed in Table 4.

For some of the configuration options, tool tips pop up when the mouse pointer hovers over the option in the configuration GUI. These tooltips explain a little more about the related options. The following paragraphs describe the configuration options available for CoreAHBLite with reference to the configuration GUI.

Memory Space Configuration

A drop-down list provides seven possible options for the memory space configuration. The first option on the list is "*16 64 KB slots, plus reserved space, plus 1 huge (2 GB) slot beginning at address 0x80000000*". This setting is typically used in a SmartFusion device. The 16 64 KB slots consume a total address space of 16*64*1024 = 2^{20} bytes and can be addressed using the 20-bit address bus that comes from the SmartFusion MSS to the FPGA fabric. The huge (2 GB) slave is typically used by a fabric based master to access resources in the SmartFusion MSS. Slot 16 is used for the huge slave.

The other options in the drop-down list provide for a memory space that is evenly divided into 16 slots. The total address space consumed by these 16 slots decreases as you descend the list of options. The number of address bits of relevance decreases as the address space reduces.

When the memory space is set to "*16 64 KB slots, plus reserved space, plus 1 huge (2 GB) slot beginning at address 0x80000000*", a further configuration option is enabled. This option allows you to choose the address range for the huge slave, as seen by the slave connected to the huge slave interface. The huge slave always appears at 0x80000000 – 0xFFFFFFFF from the master's point of view, but the slave itself can be presented with an address range of either 0x00000000 – 0x7FFFFFFF or 0x80000000 – 0xFFFFFFFF. Essentially, this configuration option controls bit 31 of the huge slave address bus.

Combining Slave Slots

For all memory space configurations, where the total space is evenly divided into 16 slots, one or more slave slots can be assigned to a **combined region** by selecting the checkboxes in the **Allocate memory space to combined region slave** panel of the configuration GUI.

Note: The slave slot combination is not supported when the memory space is set to “16 64 KB slots, plus reserved space, plus 1 huge (2 GB) slot beginning at address 0x80000000”.

When some slots have been allocated to a combined region, an additional slave interface, labeled S16, is displayed for connection on the CoreAHBLite symbol in SmartDesign. Combining slave slots provide a means to access a region larger than the size of a slot through a single slave interface. If slots are combined, they do not necessarily have to be contiguous in the memory space. If a slave slot is allocated to the combined region, then its corresponding interface is no longer available for connection separately.

Figure 5 shows an example, memory map where slot combining is used. In this example, an AHB-Lite master can access slaves based at addresses 0x00000000, 0xA0000000, 0xB0000000, and 0xC0000000 through individual slave interfaces of CoreAHBLite as shown in Figure 5. Additionally, any access from the master with an address in the ranges 0x40000000 – 0x4FFFFFFF or 0x60000000 – 0x6FFFFFFF results in accessing the S16 slave interface of CoreAHBLite.

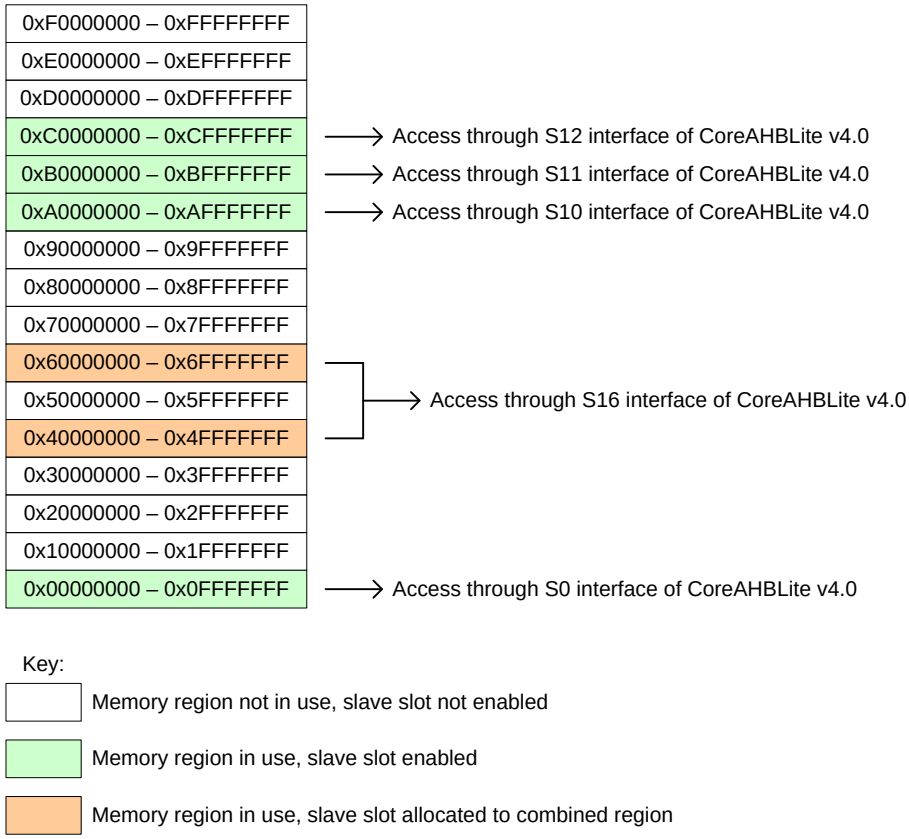

Figure 5 Example Memory Map Showing Use of Slot Combining

Enabling of Slave Slots

In the **Enable Master access** panel of the configuration GUI, check boxes are provided to enable or disable access to each slave slot. Access to slave slots can be configured on a per master basis. The enable checkbox for any slot assigned to the combined region is grayed out since it is not possible to connect a slave to such a slot. If a slot is disabled its corresponding interface does not appear for connection on the CoreAHBLite symbol in the SmartDesign tool. The checkboxes for enabling master access to the **combined region** slave interface (S16) are available to check if some slots are allocated to the combined region.

Memory Map

There are no addressable resources within CoreAHBLite itself. The core divides the address space seen by a master into a number of slave slots. Table 6 shows the memory map for CoreAHBLite when the memory space is set to "*16 64 KB slots, plus reserved space, plus 1 huge (2 GB) slot beginning at address 0x80000000*". For other memory space settings, refer to Table 7 that shows the allocation of space to each slave slot.

When the memory space is set to other than "*16 64 KB slots, reserved space, and 1 huge (2 GB) slot beginning at address 0x80000000*", it is possible to combine slots to create a portion of the memory map that can be accessed through an additional **combined region** slave interface. This interface is labeled S16 on the CoreAHBLite symbol in the SmartDesign tool.

Table 6 Memory Map When Memory Space is set to "16 64 KB slots, reserved space, and 1 huge (2 GB) slot beginning at address 0x80000000"

Resource	Address Space
Slave 0	0x00000000 – 0x0000FFFF
Slave 1	0x00010000 – 0x0001FFFF
Slave 2	0x00020000 – 0x0002FFFF
Slave 3	0x00030000 – 0x0003FFFF
Slave 4	0x00040000 – 0x0004FFFF
Slave 5	0x00050000 – 0x0005FFFF
Slave 6	0x00060000 – 0x0006FFFF
Slave 7	0x00070000 – 0x0007FFFF
Slave 8	0x00080000 – 0x0008FFFF
Slave 9	0x00090000 – 0x0009FFFF
Slave 10	0x000A0000 – 0x000AFFFF
Slave 11	0x000B0000 – 0x000BFFFF
Slave 12	0x000C0000 – 0x000CFFFF
Slave 13	0x000D0000 – 0x000DFFFF
Slave 14	0x000E0000 – 0x000EFFFF
Slave 15	0x000F0000 – 0x000FFFFF
(Reserved)	0x00100000 – 0x7FFFFFFF
Huge slave (Slave 16)	0x80000000 – 0xFFFFFFFF

Note: The slave connected to the huge slave interface (S16) can see an address range of either 0x80000000 – 0xFFFFFFFF or 0x00000000 – 0x7FFFFFFF depending on how the core is configured. From the master's point of view, the huge slave always appears in the range 0x80000000 – 0xFFFFFFFF.

Table 7 Memory Map for a Range of Memory Space Settings other than “16 64 KB slots, reserved space, and 1 huge (2 GB) slot beginning at address 0x80000000”

Total address space:	**4 GB**	**256 MB**	**…**	**64 KB**	**4 KB**
Resource	**Address Space**				
Slave 0	0x00000000 – 0x0FFFFFFF	0x00000000 – 0x00FFFFFF		0x00000000 – 0x0000FFFF	0x00000000 – 0x00000FFF
Slave 1	0x10000000 – 0x1FFFFFFF	0x01000000 – 0x01FFFFFF		0x00010000 – 0x0001FFFF	0x00001000 – 0x00001FFF
Slave 2	0x20000000 – 0x2FFFFFFF	0x02000000 – 0x02FFFFFF		0x00020000 – 0x0002FFFF	0x00002000 – 0x00002FFF
Slave 3	0x30000000 – 0x3FFFFFFF	0x03000000 – 0x03FFFFFF		0x00030000 – 0x0003FFFF	0x00003000 – 0x00003FFF
Slave 4	0x40000000 – 0x4FFFFFFF	0x04000000 – 0x04FFFFFF		0x00040000 – 0x0004FFFF	0x00004000 – 0x00004FFF
Slave 5	0x50000000 – 0x5FFFFFFF	0x05000000 – 0x05FFFFFF		0x00050000 – 0x0005FFFF	0x00005000 – 0x00005FFF
Slave 6	0x60000000 – 0x6FFFFFFF	0x06000000 – 0x06FFFFFF		0x00060000 – 0x0006FFFF	0x00006000 – 0x00006FFF
Slave 7	0x70000000 – 0x7FFFFFFF	0x07000000 – 0x07FFFFFF		0x00070000 – 0x0007FFFF	0x00007000 – 0x00007FFF
Slave 8	0x80000000 – 0x8FFFFFFF	0x08000000 – 0x08FFFFFF		0x00080000 – 0x0008FFFF	0x00008000 – 0x00008FFF
Slave 9	0x90000000 – 0x9FFFFFFF	0x09000000 – 0x09FFFFFF		0x00090000 – 0x0009FFFF	0x00009000 – 0x00009FFF
Slave 10	0xA0000000 – 0xAFFFFFFF	0x0A000000 – 0x0AFFFFFF		0x000A0000 – 0x000AFFFF	0x0000A000 – 0x0000AFFF
Slave 11	0xB0000000 – 0xBFFFFFFF	0x0B000000 – 0x0BFFFFFF		0x000B0000 – 0x000BFFFF	0x0000B000 – 0x0000BFFF
Slave 12	0xC0000000 – 0xCFFFFFFF	0x0C000000 – 0x0CFFFFFF		0x000C0000 – 0x000CFFFF	0x0000C000 – 0x000CFFF
Slave 13	0xD0000000 – 0xDFFFFFFF	0x0D000000 – 0x0DFFFFFF		0x000D0000 – 0x000DFFFF	0x0000D000 – 0x0000DFFF
Slave 14	0xE0000000 – 0xEFFFFFFF	0x0E000000 – 0x0EFFFFFF		0x000E0000 – 0x000EFFFF	0x0000E000 – 0x0000EFFF
Slave 15	0xF0000000 – 0xFFFFFFFF	0x0F000000 – 0x0FFFFFFF		0x000F0000 – 0x000FFFFF	0x0000F000 – 0x0000FFFF

Ordering Information

Ordering Codes

CoreAHBLite v5.2 can be ordered through Microsemi local Sales Representative. It should be ordered using the following number scheme: CoreAHBLite-XX, where XX is listed in Table 8.

Table 8 Ordering Codes

XX	Description
OM	RTL for Obfuscated RTL—multiple use license
RM	RTL for RTL source — multiple-use license

List of Changes

The following table lists critical changes that were made in each revision of the document.

Date	Change	Page
November 2014	Updated for v5.2 of CoreAHBLite. Added SmartFusion2, IGLOO2, and RTG4 utilization results.	N/A
November 2013	Updated for v5.0 of CoreAHBLite. Two master interfaces have been added, up to four masters are supported by v5.0.	N/A
February 2013	Updated to suit v4.0 of CoreAHBLite.	N/A

Product Support

Microsemi SoC Products Group backs its products with various support services, including Customer Service, Customer Technical Support Center, a website, electronic mail, and worldwide sales offices. This appendix contains information about contacting Microsemi SoC Products Group and using these support services.

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From North America, call **800.262.1060**
From the rest of the world, call **650.318.4460**
Fax, from anywhere in the world **650. 318.8044**

Customer Technical Support Center

Microsemi SoC Products Group staffs its Customer Technical Support Center with highly skilled engineers who can help answer your hardware, software, and design questions about Microsemi SoC Products. The Customer Technical Support Center spends a great deal of time creating application notes, answers to common design cycle questions, documentation of known issues and various FAQs. So, before you contact us, please visit our online resources. It is very likely we have already answered your questions.

Technical Support

Visit the Microsemi SoC Products Group Customer Support website for more information and support (http://www.microsemi.com/soc/support/search/default.aspx). Many answers available on the searchable web resource include diagrams, illustrations, and links to other resources on website.

Website

You can browse a variety of technical and non-technical information on the Microsemi SoC Products Group home page, at http://www.microsemi.com/soc/.

Contacting the Customer Technical Support Center

Highly skilled engineers staff the Technical Support Center. The Technical Support Center can be contacted by email or through the Microsemi SoC Products Group website.

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You can communicate your technical questions to our email address and receive answers back by email, fax, or phone. Also, if you have design problems, you can email your design files to receive assistance. We constantly monitor the email account throughout the day. When sending your request to us, please be sure to include your full name, company name, and your contact information for efficient processing of your request.

The technical support email address is soc_tech@microsemi.com.

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Outside the U.S.

Customers needing assistance outside the US time zones can either contact technical support via email (soc_tech@microsemi.com) or contact a local sales office. Sales office listings can be found at www.microsemi.com/soc/company/contact/default.aspx.

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