CoreAHBLSRAM v2.2 Release Notes

This document accompanies the production release of CoreAHBLSRAM v2.2. It describes about the features, enhancements, system requirements, supported families, implementations, known issues, and workarounds.

Features

CoreAHBLSRAM is a highly configurable core that provides the following features:

- Configurable memory size. Memory size can be configured from 2048 bytes to 139264 bytes, in steps of 2K bytes for LSRAMs (RAM1Kx18)
- Configurable memory size. Memory size can be configured from 128 bytes to 9216 bytes in steps of 128 bytes for USRAMs (RAM64x18)
- Configurable parameter to utilize either LSRAM or USRAM memory
- Merges multiple SRAM blocks to form large SRAMs or USRAMs
- AHB interface with data width of 32-bits

Delivery Types

A license is not required for using CoreAHBLSRAM v2.2. The complete hardware description language (HDL) source code is provided for the core and testbenches.

Supported Families

- RTG4™
- IGLOO®2
- SmartFusion®2

Supported Tool Flows

This version must be used with Libero® System-on-Chip (SoC) software v11.0 or later.

Installation Instructions

Within the Libero SoC software, click **Add Core** in the Catalog to locate and install a local CPZ file, or use the automatic web update feature in Libero SoC. After the CPZ file is installed in the Libero SoC, the core can be instantiated, configured, and generated within SmartDesign for inclusion in the Libero SoC project.

For more information about core installation, licensing, and general use, refer to the *Libero SoC Online Help.*

Documentation

This release contains a copy of the *CoreAHBLSRAM Handbook*. The handbook describes the core functionality and gives step-by-step instructions on how to simulate, synthesize, and place-and-route this core, and also implementation suggestions. Refer to the *Libero SoC Online Help* for instructions on obtaining IP documentation.

For more information about Microsemi Intellectual Property, visit http://www.microsemi.com/products/fpga-soc/design-resources/ip-cores. For updates and additional information about Microsemi software, FPGAs, and hardware, visit http://www.microsemi.com.

Supported Test Environments

CoreAHBLSRAM v2.2 supports Verilog user testbench.

Release History

Table 1 lists the release history for CoreAHBLSRAM.

Table 1. Release History

Version	Date	Changes
2.2	March 2016	Fixed bugs and issues as described in Table 2
2.1	December 2014	Added RTG4 and IGLOO2 support
2.0	January 2013	Initial release

Resolved Issues in the v2.2 Release

Table 2. Resolved Issues in the v2.2 Release

SAR Number	Changes
47113	CoreAHBLSRAM simulation results in collisions
69268	Simulation warning messages from CoreAHBLSRAM core
71128	AHBLSRAM doesnot support Burst Transactions
71061	CoreAHBLSRAM utilizes block RAM inefficiently
73458	Configurator allows invalid sizes to be entered without any warning

Resolved Issues in the v2.1 Release

Table 3. Resolved Issues in the v2.1 Release

SAR Number	Changes
43499	The RTL license option was present even when there were no RTL licenses available
50360	Request to change the field name in the GUI (LSRAM Depth)
52379	Duplicate Modules
58550	CoreAHBLSRAM v2.0 only support SmartFusion2

Discontinued Features and Devices

There are no discontinued features or devices.

Known Limitations and Workarounds

There are no known limitations and workarounds.

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