RN0223
Release Notes
CoreUHD_SDITX v2.1

Microsemi
a Microchip company

Microsemi Headquarters
One Enterprise, Aliso Viejo,
CA 92656 USA
Within the USA: +1 (800) 713-4113
Outside the USA: +1 (949) 380-6100
Sales: +1 (949) 380-6136
Fax: +1 (949) 215-4996
Email: sales.support@microsemi.com
www.microsemi.com

About Microsemi

Microsemi, a wholly owned subsidiary of Microchip Technology Inc. (Nasdaq: MCHP), offers a comprehensive portfolio of semiconductor and system solutions for aerospace & defense, communications, data center and industrial markets. Products include high-performance and radiation-hardened analog mixed-signal integrated circuits, FPGAs, SoCs and ASICs; power management products; timing and synchronization devices and precise time solutions, setting the world's standard for time; voice processing devices; RF solutions; discrete components; enterprise storage and communication solutions, security technologies and scalable anti-tamper products; Ethernet solutions; Power-over-Ethernet ICs and midspans; as well as custom design capabilities and services. Learn more at www.microsemi.com.

51300223. 2.0 9/20

1 Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

1.1 Revision 2.0

Updated changes related to CoreUHD_SDITX v2.1.

1.2 Revision 1.0

Revision 1.0 was the first publication of this document. Created for CoreUHD_SDITX v2.0.

Contents

1 Revision History . . . 3
1.1 Revision 2.0 . . . 3
1.2 Revision 1.0 . . . 3
2 CoreUHD_SDITX . . . 6
2.1 Overview . . . 6
2.2 Features . . . 6
2.3 Delivery Types . . . 6
2.4 Supported Families . . . 6
2.5 Supported Tool Flows . . . 6
2.6 Installation Instructions . . . 7
2.7 Documentation . . . 7
2.8 Supported Test Environments . . . 7
2.9 Resolved Issues in the v2.1 Release . . . 7
2.10 Discontinued Features and Devices . . . 7
2.11 Known Limitations and Workarounds . . . 7

Tables

Table 1 Resolved Issues in the v2.1 Release 7

2 CoreUHD_SDITX

2.1 Overview

This release notes provides details about the features, enhancements, system requirements, supported families, implementations, and known issues and workarounds.

2.2 Features

CoreUHD_SDITX DirectCore IP is a Serial Digital Interface (SDI) Framer. The core accepts the raw video data and performs the framing of the SDI data stream.

CoreUHD_SDITX has the following features:

- Compliant with SMPTE ST 292-1 (HD-SDI) standard.
- Compliant with SMPTE ST 424 (3G-SDI) standard.
- Compliant with SMPTE ST 2081-1 (6G-SDI) standard.
- Compliant with SMPTE ST 2082-1 (12G-SDI) standard.
- Supports data rates 1.485 Gb/s and 1.485/1.001 Gb/s for HD-SDI standard.
- Supports data rates 2.97 Gb/s and 2.97/1.001 Gb/s for 3G-SDI standard.
- Supports data rates 5.94 Gb/s and 5.94/1.001 Gb/s for 6G-SDI standard.
- Supports data rates 11.88 Gb/s and 11.88/1.001 Gb/s for 12G-SDI standard.
- Performs generation and insertion of Line Number (LN) packets.
- Performs generation and insertion of CRC packets.
- Performs generation and insertion of Video Payload Identification (VPID) packets.
- Performs insertion of sync-bits in timing reference words in 12G-SDI and 6G-SDI standards.
- Performs scrambling and NRZI encoding.

2.3 Delivery Types

CoreUHD_SDITX is available in two versions:

- **Evaluation:** Evaluation version is available for free and supports 4 hours of the functionality on silicon while operating at 12G-SDI, 6G-SDI and 3G-SDI data rates and 8 hours of the functionality on silicon while operating at HD-SDI data rate.
- **Obfuscated:** Obfuscated version is license locked and is available only with Libero Platinum license.

2.4 Supported Families

- PolarFire® SoC
- PolarFire®

2.5 Supported Tool Flows

CoreUHD_SDITX v2.1 requires Libero v12.0 or higher.

2.6 Installation Instructions

The CoreSDITX CPZ file must be installed into Libero software. This is done automatically through the Catalog update function in Libero, or the CPZ file can be manually added using the **Add Core** catalog feature. Once the CPZ file is installed in Libero, the core can be configured, generated, and instantiated within SmartDesign for inclusion in the Libero project. For more information, see the *Knowledge Based article*.

To know how to create SmartDesign project using the IP cores, refer to the *SmartDesign User guide*.

2.7 Documentation

This release contains a copy of the *CoreSDITX Handbook*. The handbook, describes the core functionality and gives step-by-step instructions on how to simulate, synthesize, and place-and-route this core, and also implementation suggestions. Visit *https://www.microsemi.com/product-directory/design-resources/1750-libero-soc#documents* page for the latest version and instructions on obtaining IP documentation.

For updates and additional information, visit the Intellectual Property pages on the Microsemi SoC Products Group website: visit:

http://www.microsemi.com/products/fpga-soc/design-resources/ip-cores.

2.8 Supported Test Environments

VHDL user testbench is provided with the core.

2.9 Resolved Issues in the v2.1 Release

Table 1 • **Resolved Issues in the v2.1 Release**

SAR Number	Description
SAR112756	Added support for HD-SDI standard and 3G-SDI standard (both Level A and Level B mappings)
SAR110815	Resolved duplicate modules issue while using multiple instances of the core in Libero.

2.10 Discontinued Features and Devices

There are no discontinued features and devices.

2.11 Known Limitations and Workarounds

There are no known limitations and workarounds.