CoreReset_PF v2.1

Handbook

Microsemi

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Introduction

CoreReset_PF will allow synchronization of the resets to the user-specified clock domain into which each reset is feeding, so that while assertion is asynchronous, negation is synchronous to the clock. A diagram of CoreReset_PF shown in Figure 1.

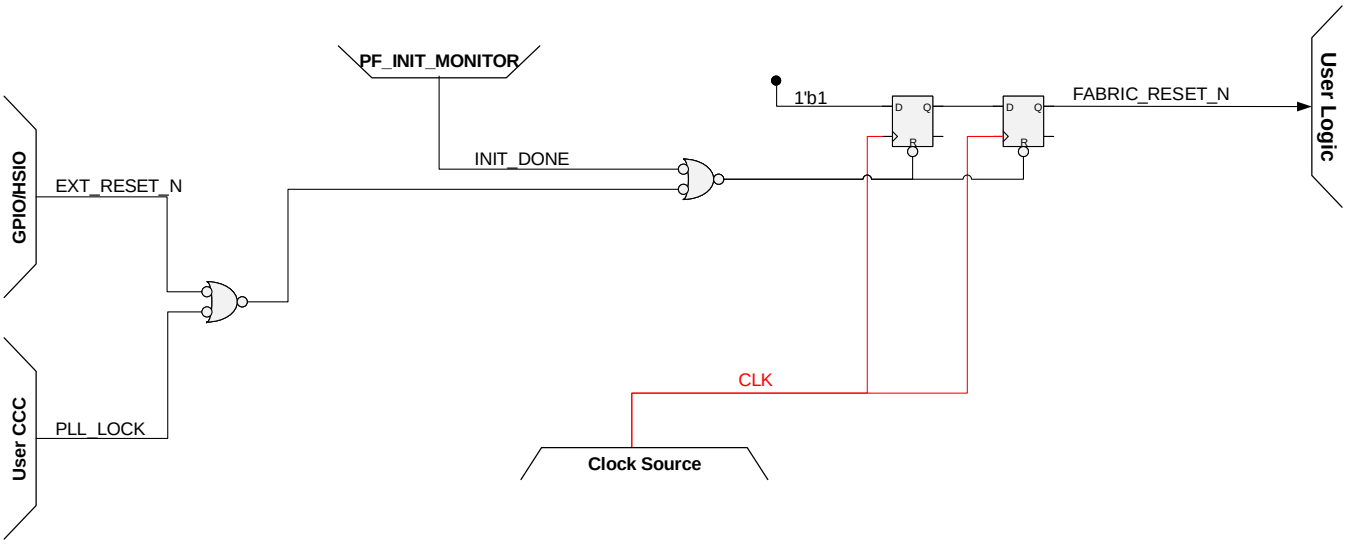

Figure 1 CoreReset_PF Block Diagram

Key Features

Following are the key features:

- Generates a reset which is asserted asynchronously by one of multiple potential sources and which negates scynchronously to a specified clock. This ensures that recovery time of downstream logic is met and that all flip flops come out of reset in the same clock period.
- Multiple reset can be used such as external gpio, phase lock loop lock or init done in conjunction with the master reset from the system controller (via CORESYSSERVICES_PF).

Supported Families

This version of CoreReset_PF supports the following FPGA families:

- PolarFire

Core Version

This handbook supports CoreReset_PF version 2.1.

Utilization and Performance

CoreReset_PF has been implemented for the PolarFire device family. A summary of the implementation data for CoreReset_PF is listed in Table 1.

Table 1 CoreReset_PF Device Utilization and Performance

Family	Tiles			Utilization		Performance MHz
	Sequential	Combinatorial	Total	Device	Total %	
PolarFire	2	3	5	MPF300T	0.000012	160

Note: Data in this table were achieved using default synthesis and layout settings . Top-level parameters/generics were left at their default values.

Design Description

I/O Signals

The port signals for the CoreReset_PF macro are shown in Figure 2 and defined in Table 2.

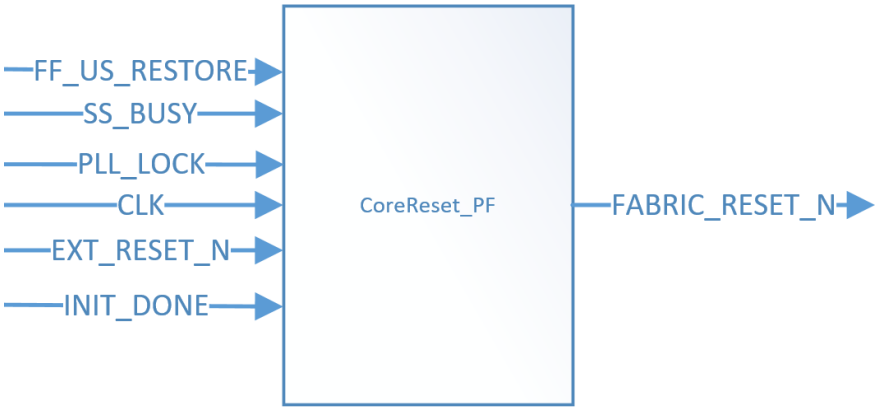

Figure 2 CoreReset_PF I/O Signal Diagram

Table 2 CoreReset_PF I/O Signal Descriptions

Port Name	Type	Description
EXT_RESET_N	In	Active low reset input from GPIO or HSIO. Optional, if not used this must be tied high.
CLK	In	Clock input from system, recovered or different clock domain.
PLL_LOCK	In	PLL Lock signal from Clock Conditioning Circuit. Optional, only used in systems which need to support flash freeze. If not used, must be tied low.
FF_US_RESTORE	In	Optional. Only used in the systems which need to support flash freeze. If not used, must be tied low.
SS_BUSY	In	When asserted, reset from PLL_LOCK or EXT_RESET_N are ignored. This ensures that no reset occurs whilst PLL is re-acquiring lock during flash freeze exit. Optional
INIT_DONE	In	When signal asserts the initialization of the device is complete. This signal should be connected to one of the PF_INIT_MONITOR signals. These signal come from the system controller and must be used as they provide the master reset for the system.
FABRIC_RESET_N	Out	This is the output reset, which may be used to reset user logic in the fabric. It is an active low reset, which asserts asynchronously, but negates synchronously to CLK.

Notes:

1. *All signals are active High (logic 1) unless otherwise noted.*

Tool Flows

Licensing

CoreReset_PF is license free.

RTL

Complete RTL source code is provided for the core and testbenches.

SmartDesign

CoreReset_PF is preinstalled in the SmartDesign IP Deployment design environment. For information on using the SmartDesign to instantiate and generate cores, refer to the *Using DirectCore in Libero SoC User Guide*.

Figure 3 CoreReset_PF Full I/O View

Simulation Flows

The User Testbench for CoreReset_PF is included in all releases.

To run simulations, select the **User Testbench** flow within **SmartDesign CoreReset_PF** configuration GUI, right-click the canvas, and select **Generate Design**.

When SmartDesign generates the design files, it will install the user testbench files.

To run the user testbench, Set the design root to the CoreReset_PF instantiation in the Libero® System-on-Chip (SoC) design hierarchy pane and click the Simulation icon in the Libero SoC Design Flow window. This will invoke ModelSim® and automatically run the simulation.

Synthesis in Libero SoC

After setting the design root appropriately for your design, click the **Synthesis** icon in the Libero SoC. The Synthesis window appears, displaying the Synplicity® project. Set Synplicity to use the Verilog 2001 standard if Verilog is being used. To run Synthesis, click the **Run** icon.

Place-and-Route in Libero SoC

After setting the design root appropriately for the design, and after running Synthesis, click the **Layout** icon in the Libero SoC software to invoke Designer. CoreReset_PF requires no special place-and-route settings.

List of Changes

The following table lists critical changes that were made in each revision of the document.

Table 3 List of changes

Date	Change	Page
1st December 2017	Updated core version to 2.1	N/A

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