HB0870
Handbook
CoreUHD_SDITX v2.1

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1 Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

1.1 Revision 2.0

Updated for CoreUHD_SDITX v2.1.

1.2 Revision 1.0

This was the first publication of this document. Created for CoreUHD_SDITX v2.0.

2 Introduction

2.1 Overview

CoreUHD_SDITX DirectCore IP is a Serial Digital Interface (SDI) Framer. Core supports 1.5 Gigabits per second SDI (HD-SDI), 3 Gigabits per second SDI (3G-SDI), 6 Gigabits per second SDI (6G-SDI), and 12 Gigabits per second SDI (12G-SDI) SDI standards defined by the Society of Motion Picture and Television Engineers (SMPTE).

2.2 Features

Core has the following features:

- Compliant with SMPTE ST 292-1 (HD-SDI) standard.
- Compliant with SMPTE ST 424 (3G-SDI) standard.
- Compliant with SMPTE ST 2081-1 (6G-SDI) standard.
- Compliant with SMPTE ST 2082-1 (12G-SDI) standard.
- Supports data rates 1.485 Gb/s and 1.485/1.001 Gb/s for HD-SDI standard.
- Supports data rates 2.97 Gb/s and 2.97/1.001 Gb/s for 3G-SDI standard.
- Supports data rates 5.94 Gb/s and 5.94/1.001 Gb/s for 6G-SDI standard.
- Supports data rates 11.88 Gb/s and 11.88/1.001 Gb/s for 12G-SDI standard.
- Performs generation and insertion of Line Number (LN) packets.
- Performs generation and insertion of CRC packets.
- Performs generation and insertion of Video Payload Identification (VPID) packets.
- Performs insertion of sync-bits in timing reference words in 12G-SDI and 6G-SDI standards.
- Performs scrambling and NRZI encoding.

2.3 Core Version

This handbook is for CoreUHD_SDITX version 2.1.

2.4 Supported Families

- PolarFire® SoC
- PolarFire®

2.5 Device Utilization and Performance

Device Utilization and Performance data is provided in Table 1, page 3 for the supported device families. The data described in this table is only indicative. The overall device utilization and performance of the core is system dependent.

Table 1 • **Device Utilization and Performance**

Family (Device)	Configuration Parameters		Utilization (Logic Elements)				Performance (MHz)
	TX_SDI_STD	TX_SDI_DW	Sequential (DFF)	Combinatorial (4LUT)	Total	%	TX_CLK Frequency
PolarFire (MPF300T)	3	20	461	734	1195	0.20	198
	4	40	869	1435	2304	0.38	168
	5	80	1645	2954	4599	0.77	197
PolarFire SoC (MPFS250T)	3	20	537	810	1347	0.26	167
	4	40	945	1533	2478	0.48	169
	5	80	1712	3064	4776	0.94	184

Note: The data in this table is achieved using typical synthesis and layout settings. Frequency (MHz) was set to 100 and the speed grade was -1.

3 Interface

3.1 Configuration Parameters

The following table describes the configurable parameter/generic of the Core. All the parameters/generics are integer types.

Table 2 • **Parameter/Generic Descriptions**

Parameter Name	Valid Range	Default	Description
TX_SDI_STD	3, 4, 5	5	**SDI STANDARD** Configure the core for required SDI standard. • 3 – HD-SDI and 3G-SDI • 4 – 6G-SDI • 5 – 12G-SDI
TX_SDI_DW	20, 40, 80	80	**SDI DATA WIDTH** Configure the data width of the parallel SDI data stream on the transceiver interface of the core. • 20 – Select 20-bits in HD-SDI and 3G-SDI standard (when TX_SDI_STD parameter is set to 3) • 40 – Select 40-bits in 6G-SDI standard (when TX_SDI_STD parameter is set to 4) • 80 – Select 80-bits in 12G-SDI standard (when TX_SDI_STD parameter is set to 5)

3.2 Ports

All the input and output ports of the core are listed in the following table.

Table 3 • **Input and Output Signals**

Port	Width	Direction	Description
Clock and Reset			
TX_CLK	1	Input	Transmit clock input. All input signals are required to be clocked on rising edge to this clock. All the output signals are clocked on rising edge of this clock. Recommended to connect to LANE***x***_TX_CLK of Transceiver. The required clock frequency is 148.5 (/1.001) MHz when data streams are transmitted at 12G-SDI, 6G-SDI, or 3G-SDI data rate. The required clock frequency is 74.25 (/1.001) MHz when data streams are transmitted at HD-SDI data rate.
TX_RESETN	1	Input	Active low asynchronous reset input. The reset input is required to be synchronous to clock TX_CLK.
Transceiver Interface			
TX_SDI_DATA	TX_SDI_DW	Output	Transmit data to Transceiver. SDI data stream output. Recommended to connect to LANE***x***_TX_DATA of Transceiver.
TX_CLK_STABLE	1	Input	Transmit Clock Stable from the Transceiver. The core resets whenever TX_CLK_STABLE is not asserted. Recommended to connect to LANE***x***_TX_CLK_STABLE of Transceiver.
Data Stream Inputs			
TX_DATA_DS1	10	Input	Data Stream 1 input. DS1 in 12G-SDI, 6G-SDI, 3G-SDI, and HD-SDI standards.
TX_DATA_DS2	10	Input	Data Stream 2 input. DS2 in 12G-SDI, 6G-SDI, 3G-SDI and HD-SDI standards.
TX_DATA_DS3	10	Input	Data Stream 3 input. DS3 in 12G-SDI and 6G-SDI standards.
TX_DATA_DS4	10	Input	Data Stream 4 input. DS4 in 12G-SDI and 6G-SDI standards.
TX_DATA_DS5	10	Input	Data Stream 5 input. DS5 in 12G-SDI standard.
TX_DATA_DS6	10	Input	Data Stream 6 input. DS6 in 12G-SDI standard.
TX_DATA_DS7	10	Input	Data Stream 7 input. DS7 in 12G-SDI standard.
TX_DATA_DS8	10	Input	Data Stream 8 input. DS8 in 12G-SDI standard.
Line Number Inputs			
TX_LN_DS1	11	Input	Line number to be inserted in DS1 data stream.
TX_LN_DS2	11	Input	Line number to be inserted in DS2 data stream.
TX_LN_DS3	11	Input	Line number to be inserted in DS3 data stream.
TX_LN_DS4	11	Input	Line number to be inserted in DS4 data stream.
TX_LN_DS5	11	Input	Line number to be inserted in DS5 data stream.
TX_LN_DS6	11	Input	Line number to be inserted in DS6 data stream.
TX_LN_DS7	11	Input	Line number to be inserted in DS7 data stream.
TX_LN_DS8	11	Input	Line number to be inserted in DS8 data stream.
VPID Data Inputs			

Table 3 • **Input and Output Signals *(continued)***

Port	Width	Direction	Description
TX_VPID_DS1	32	Input	VPID data bytes to be inserted in DS1 data stream.
TX_VPID_DS2	32	Input	VPID data bytes to be inserted in DS2 data stream.
TX_VPID_DS3	32	Input	VPID data bytes to be inserted in DS3 data stream.
TX_VPID_DS4	32	Input	VPID data bytes to be inserted in DS4 data stream.
TX_VPID_DS5	32	Input	VPID data bytes to be inserted in DS5 data stream.
TX_VPID_DS6	32	Input	VPID data bytes to be inserted in DS6 data stream.
TX_VPID_DS7	32	Input	VPID data bytes to be inserted in DS7 data stream.
TX_VPID_DS8	32	Input	VPID data bytes to be inserted in DS8 data stream.
VPID Line Number Inputs			
TX_VPID_LN_DS1	11	Input	Line number for VPID insertion in DS1 data stream.
TX_VPID_LN_DS2	11	Input	Line number for VPID insertion in DS2 data stream.
TX_VPID_LN_DS3	11	Input	Line number for VPID insertion in DS3 data stream.
TX_VPID_LN_DS4	11	Input	Line number for VPID insertion in DS4 data stream.
TX_VPID_LN_DS5	11	Input	Line number for VPID insertion in DS5 data stream.
TX_VPID_LN_DS6	11	Input	Line number for VPID insertion in DS6 data stream.
TX_VPID_LN_DS7	11	Input	Line number for VPID insertion in DS7 data stream.
TX_VPID_LN_DS8	11	Input	Line number for VPID insertion in DS8 data stream.
Control Inputs			
TX_INSERT_LN	1	Input	Input to enable or disable line number insertion is in the data stream. When high, core inserts line number (LN) packets in each data stream, generated from line number data provided on the line number input port of the respective data stream. When low, line number packets are not inserted in SDI data stream, instead data available on the data stream is retained. This input must remain high for the complete duration of the line for which the LN packet insertion is required.
TX_INSERT_CRC	1	Input	Input to enable or disable CRC insertion in the data stream. When high, core inserts CRC packets in each data stream, generated from the data input of respective data streams. When low, CRC packets are not inserted in SDI data stream instead data available on the data stream is retained. This input must remain high for the complete duration of the line for which the CRC packet insertion is required.
TX_INSERT_VPID	1	Input	Input to enable or disable VPID insertion in the data stream. When high, core inserts VPID packets in each data stream, generated from the VPID byte provided on the VPID data input of respective data streams. When low, VPID packets are not inserted in SDI data stream instead data available on the data stream is retained. This input must remain high for the complete duration of the line for which VPID insertion is required.
Status Outputs			

Table 3 • **Input and Output Signals *(continued)***

Port	Width	Direction	Description
TX_DS_MUX	1	Output	This output signal indicates the data stream multiplex type of the input data streams. If this output is low, when the core is operating at 12G-SDI or 6G-SDI data rates, then it indicates Type1 multiplex is detected on the input data streams (one instance of TRS Words, Line Number Words, CRC Words, etc in each data stream). If this output is high, when the core is operating at 12G-SDI or 6G-SDI data rates, it indicates Type2 multiplex is detected on the input data streams (two instances of TRS Words, Line Number Words, CRC Words, etc in each data stream). If this output is low, when the core is operating at 3G-SDI data rate, then it indicates 3G-SDI Level A mapping is detected on the input data stream. If this output is high, when the core is operating at 3G-SDI data rate, then it indicates 3G-SDI Level B mapping is detected on the input data stream. This output shall be ignored when the core is operating at the HD-SDI data rate. Once multiplex type/mapping type is detected, the output remains unchanged until there is change in multiplex type/mapping type on the input data stream.
TX_TRS	1	Output	This output signal indicates that data on the SDI data stream output is first TRS word of the SDI data stream.
TX_BAD_TRS	1	Output	This output indicates that the TRS information on the SDI data stream is not valid TRS as mentioned in SMPTE standard. This output goes high whenever bad TRS is detected. This does not affect the data stream framing performed by the core.

Note: x can be 0, 1, 2, and 3.

Note: All the ports with suffix _DS1 and _DS2 are available in HD-SDI standard, 3G-SDI standard, 6G-SDI standard, and 12G-SDI standard.

Note: All the ports with suffix _DS3 and _DS4 are available in both 6G-SDI standard and 12G-SDI standard.

Note: All the ports with suffix _DS5, _DS6, _DS7, and _DS8 are available only in 12G-SDI standard.

Note: The VPID Data Inputs are 32-bit each. Bits [7:0] is the Byte1, Bits [15:8] is the Byte2, Bits [23:16] is the Byte3, Bits [31:24] is the Byte4.

4 Functional Description

CoreUHD_SDITX is SDI Framer. The core accepts the raw video data and performs the framing of the SDI data stream. The framing is performed as per the SMPTE SDI protocol specification for the SDI standard configured.

As per the SMPTE 6G-SDI and 12G-SDI specifications the individual data streams of the SDI data stream can be of either Type1 multiplex type or Type2 multiplex type based on the image mapping standards.

- **Type1 multiplex:** Each data stream has a single instance of TRS words, Line Numbers, CRC Words and so on.
- **Type2 multiplex:** Each data stream has two instances of TRS words, Line Numbers, CRC Words and so on.

The core is capable of accepting both Type1 and Type2 multiplex SDI data stream. The core detects the type of the multiplexing and reports it on the TX_DS_MUX output.

In case of the Type2 multiplex data streams, the core performs LN insertion, VPID insertion and CRC generation and insertion on both channels of the multiplexed data stream.

As per the SMPTE 3G-SDI image mapping specification two types of mappings are specified.

- **Level A mapping:** Each data stream has a single instance of TRS words, Line Numbers, CRC Words, and so on (This is similar to Type 1 multiplexing present in 12G-SDI and 6G-SDI).
- **Level B mapping:** Each data stream has two instances of TRS words, Line Numbers, CRC Words, and so on (This is similar to Type 2 multiplexing present in 12G-SDI and 6G-SDI).

The core is capable of accepting both Level A and Level B mapped SDI data stream. The core detects the type of mapping and reports it on the TX_DS_MUX output.

In the case of the Level B multiplex data streams, the core performs LN insertion, VPID insertion, and CRC generation and insertion on both channels of the multiplexed data stream.

Figure 1 • **CoreUHD_SDITX block diagram in HD-SDI and 3G-SDI Standard**

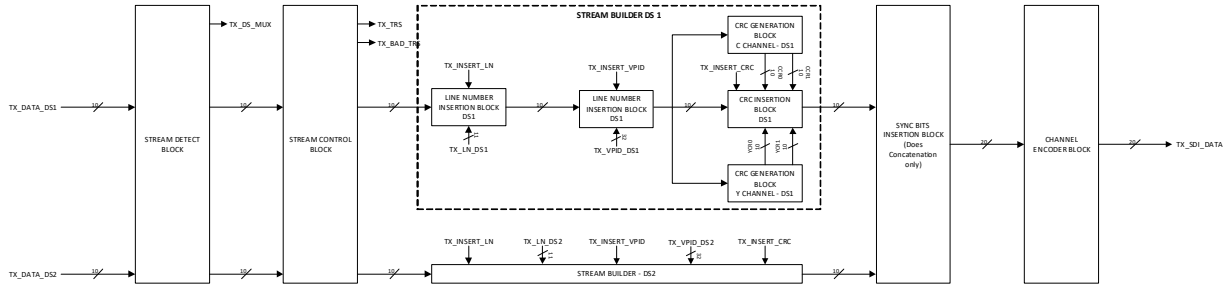


Figure 2 • **CoreUHD_SDITX Block Diagram in 6G-SDI Standard**

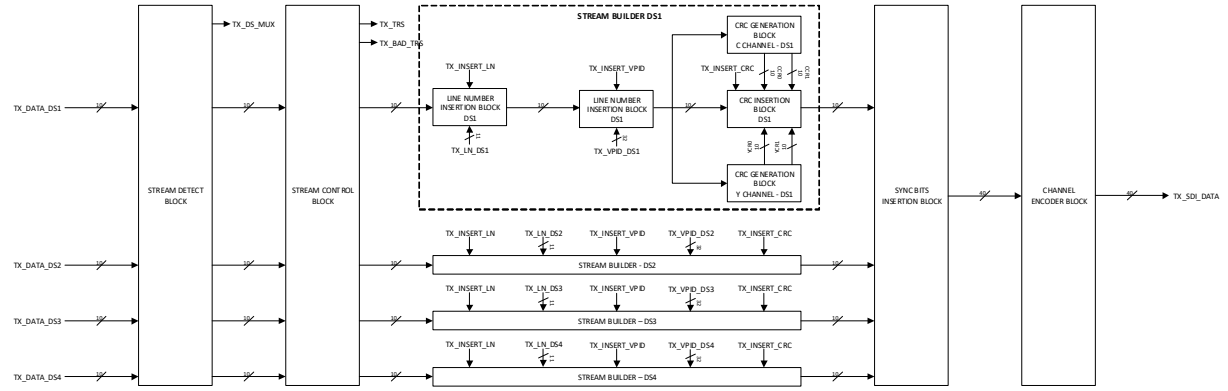
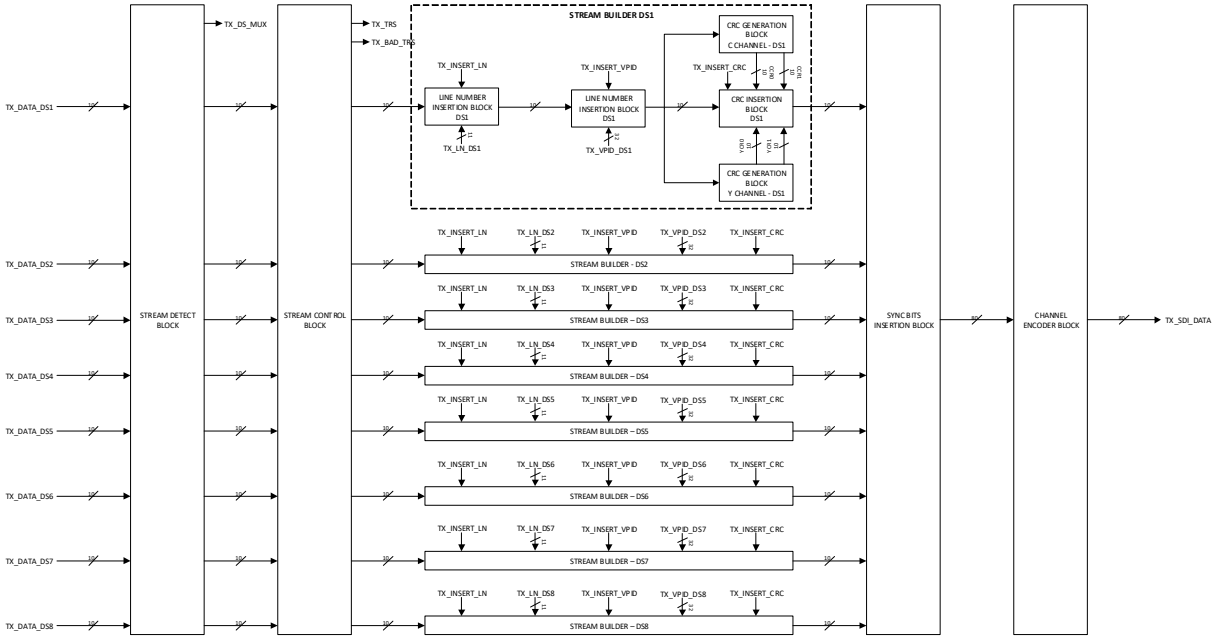


Figure 3 • **CoreUHD_SDITX Block Diagram in 12G-SDI Standard**



The functional blocks of the core are described in the following sections:

4.1 Stream Detect Block

Stream Detect Block detects the timing reference words in the input data streams and generates the control signals required for the stream control block.

The block generates a signal to indicate the first word of the timing reference words. Also, the block detects the multiplex type of the data stream input based on the timing reference words.

4.2 Stream Control Block

Stream Control Block generates the control signals for the line number insertion block, VPID insertion block, CRC generation block, CRC insertion block and syncs bits insertion block.

The block generates TX_TRS status signal indicating the first word of TRS is output on TX_SDI_DATA output signal. Also the block detects, if a bad TRS signal is available on the input data streams.

4.3 Line Number Insertion Block

Line Number Insertion Block encodes the line number input into LN0 and LN1 line number packets as defined in the SMPTE specification. The encoded line number packets LN0 and LN1 are inserted into the data stream at the appropriate positions as defined in the SMPTE specification.

The block performs the line number packet insertion in the data stream if the TX_INSERT_LN input is high. This signal shall be high for the complete duration of the line for which line number packets insertion is required. If this signal is low, the block does not perform the line number insertion.

4.4 VPID Insertion Block

The VPID Insertion Block inserts the VPID packets into the data stream at the appropriate positions as recommended in the SMPTE specification. The user defined words of VPID packets are encoded from the VPID bytes input. Along with the user defined words, the block inserts the ancillary data flags, the data identification, the secondary data identification, the data count packets and the checksum words which are part of VPID packet. The VPID packets are inserted in the line number provided on the VPID line number input for each frame.

The block performs the line number packet insertion in the data stream if the TX_INSERT_VPID input is high. This signal shall be high for the complete duration of the frame for which VPID packets insertion is required. If this signal is low, the block does not perform the VPID insertion.

4.5 CRC Generation Block

CRC Generation Block computes the CRC value for each line of the input data stream. The CRC computation is as per CRC polynomial specified in the SMPTE specification.

CRC(X) = $\mathbf{X^{18} + X^5 + X^4 + 1}$

The 18-bit CRC is generated and encoded to form CR0 and CR1 CRC packets as defined in the SMPTE specification.

4.6 CRC Insertion Block

CRC Insertion Block inserts the CR0 and CR1 CRC packets into the data stream, at the appropriate positions as defined in the SMPTE specification.

The block performs the CRC packet insertion in the data stream if the TX_INSERT_CRC input is high. This signal shall be high for the complete duration of the line for which line number packets insertion is required. If this signal is low, the block does not perform the CRC insertion.

4.7 Sync Bits Insertion Block

Sync Bits Insertion Block performs the sync bit insertion on the 10-bit 3FF and 10-bit 000 timing reference words. The two LSB of 3FF word is replaced by 01b and that of 000 word is replaced by 10b.

The block inserts the sync bits only on the required timing reference signals as defined in SMPTE SDI specification retaining the 3FF 000 000 sequence which is required for the receiver to achieve synchronization and word alignment. The sync bits insertion depends on the SDI standard, and the input data stream multiplexing type. The core performs sync bits insertion only in 12G-SDI standard and 6G-SDI standard.

4.8 Channel Encoder Block

Channel Encoder Block performs the scrambled NRZI encoding on the concatenated SDI data stream. The channel encoding is performed as per the polynomials specified in the SMPTE specification.

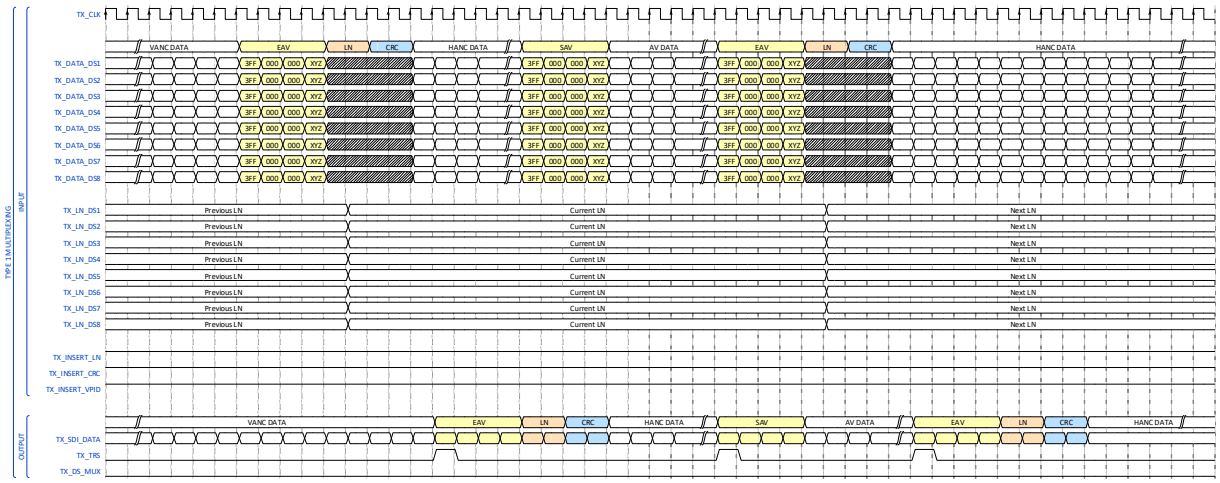
G1(X) = $\mathbf{X^9 + X^4 + 1}$ and $\mathbf{G_2(X) = X + 1}$

5 Timing Diagrams

5.1 Type1 Multiplex Data Stream

The following figure shows the timing diagram for 12G-SDI standard and 6G-SDI standard Type1 10-bit multiplex data stream. Refer the following timing diagram for HD-SDI standard and 3G-SDI standard - Level A mapping.

Figure 4 • **Timing Diagram for Type1 10-bit Multiplex Data Stream**



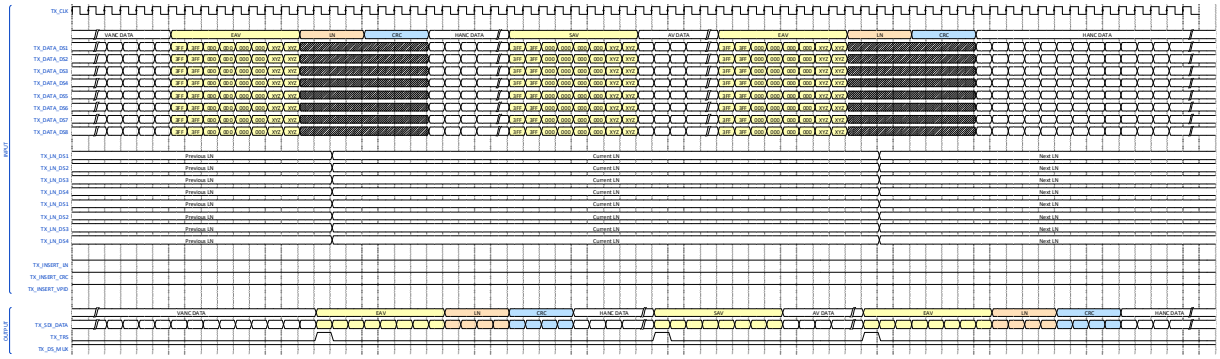
Note: In 6G-SDI standard, ignore the ports with suffix _DS5, _DS6, _DS7, and _DS8.

Note: In HD-SDI standard and 3G-SDI standard - Level A mapping, ignore the ports with suffix _DS3, _DS4, _DS5, _DS6, _DS7, and _DS8.

5.2 Type2 Multiplex Data Stream

The following figure shows the timing diagram for 12G-SDI standard and 6G-SDI standard Type2 10-bit multiplex data stream. Refer the following timing diagram for 3G-SDI standard - Level B mapping.

Figure 5 • **Timing Diagram for Type2 10-bit Multiplex Data Stream**



Note: In 6G-SDI standard, ignore the ports with suffix _DS5, _DS6, _DS7, and _DS8.

Note: In 3G-SDI standard - Level B mapping, ignore the ports with suffix _DS3, _DS4, _DS5, _DS6, _DS7, and _DS8.

6 Tool Flow

6.1 License

Core is available in two versions:

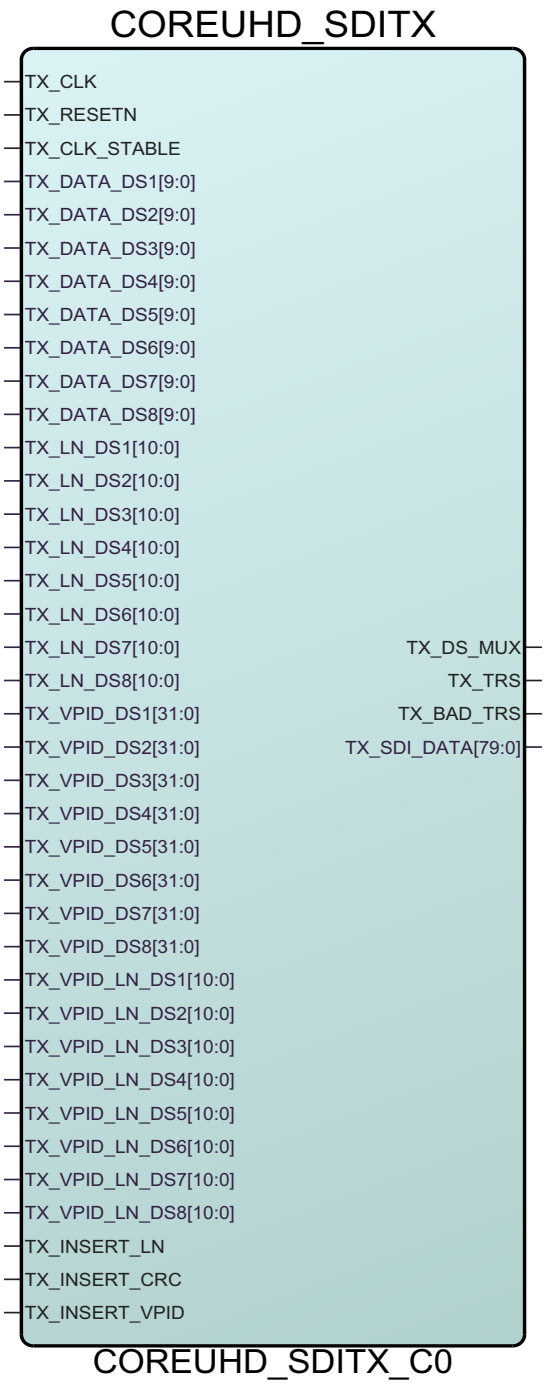
- **Evaluation:** Evaluation version is available for free and supports 4 hours of the functionality on silicon while operating at 12G-SDI, 6G-SDI, and 3G-SDI data rates, and 8 hours of the functionality on silicon while operating at HD-SDI data rate.
- **Obfuscated:** Obfuscated version is license locked and is available only with Libero Platinum license.

6.2 Using core in Libero SmartDesign

Core is pre-installed in the SmartDesign IP deployment design environment or Core is downloaded from the online repository.

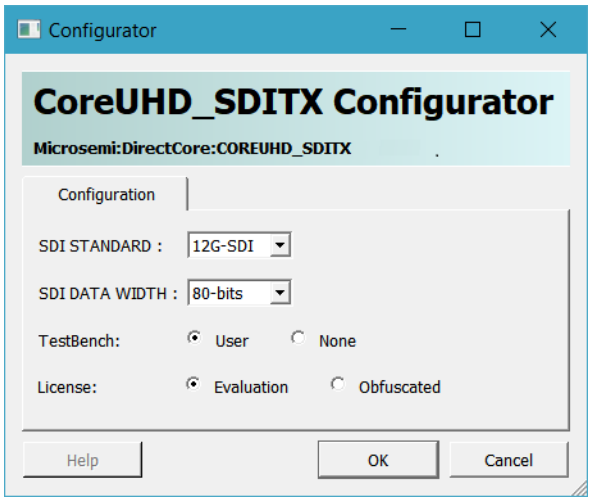
An example of the core instantiated in Libero SmartDesign is shown in the following figure.

Figure 6 • **Core Instance Full I/O View in SmartDesign**



The core can be configured using the configuration GUI in the SmartDesign, as shown in the following figure.

Figure 7 • **Configuring the Core in SmartDesign**



For more information on using the SmartDesign to instantiate and generate cores, refer to the *Using DirectCore in Libero® SoC User Guide*.

6.3 Simulation Flows

The User Testbench is provided along with the core.

To run the user testbench simulations, do the following steps:

1. Select **User** option for the Testbench flow in the **Core Configuration** window. When SmartDesign generates the design files, it also generates the user testbench files.
2. Set the design root to the core instantiation in the Libero design hierarchy pane and
3. Click **Simulation** in the Libero **Design Flow** window. This invokes ModelSim and automatically runs the user testbench simulation.

6.4 Synthesis in Libero

To run synthesis on the core, do the following steps:

1. Set the design root to the IP component instance.
2. Run the **Synthesis** tool from the Libero **Design Flow** pane.

6.5 Place-and-Route in Libero

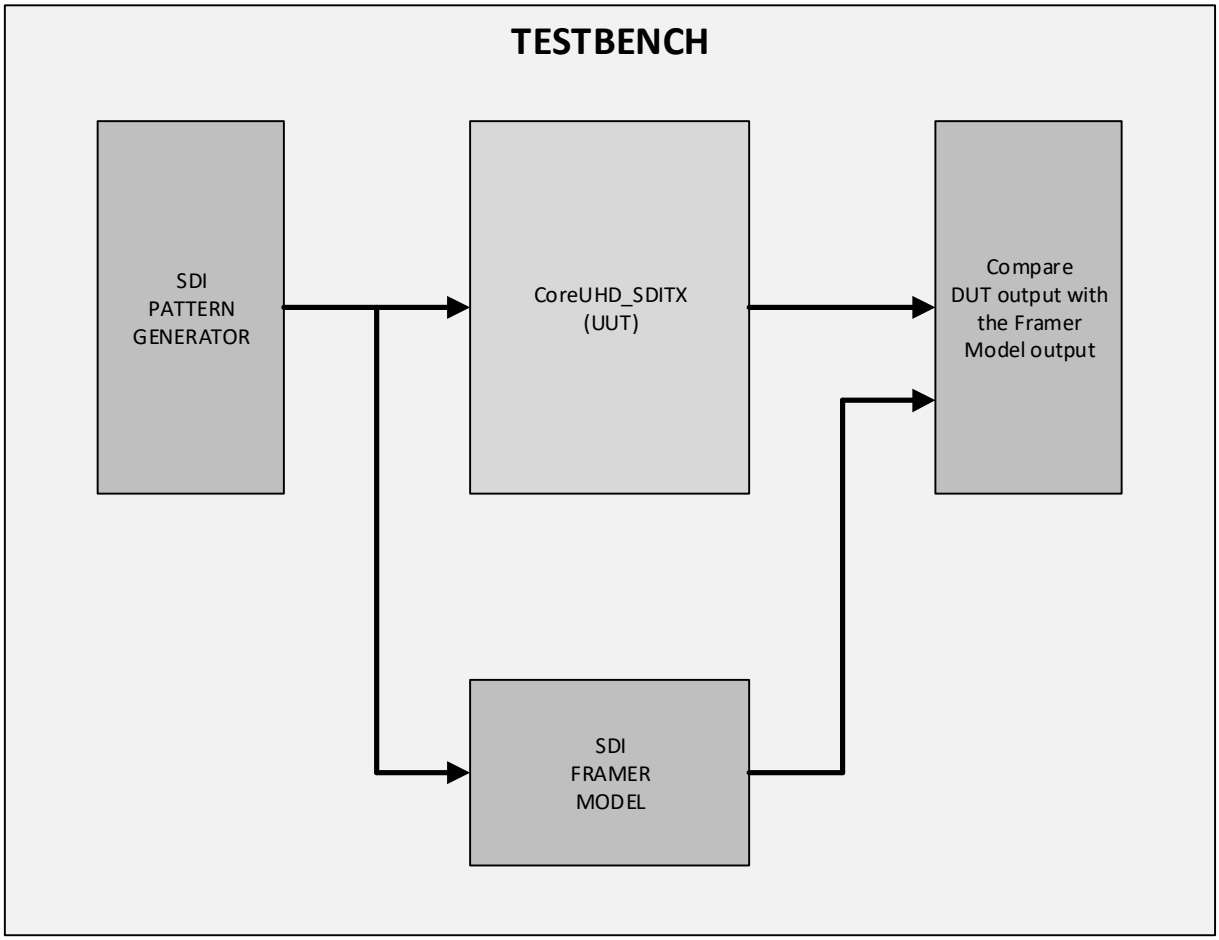
When the design is synthesized:

1. Run the **Place-And-Route** tool from the Libero **Design Flow** pane.

7 Testbench

UserTtestbench is provided with the core that verifies a few of the features.

Figure 8 • **User Testbench**



The user testbench has instance of the core - Unit Under Test (UUT), an SDI Pattern Generator, an SDI Framer Model, and a data comparator module.

The testbench configures the SDI Pattern Generator, UUT, and the SDI Framer Model with the parameters for which the core is being configured from configurator GUI.

The pattern generator generates the data streams, line number data, VPID data, VPID line number data, and control signals required to connect to the UUT, and the SDI Framer Model based on the configured standard.

The UUT performs the framing of the raw video into the SDI data stream. The SDI Framer Model also performs the framing of the raw video into the SDI data stream. The SDI data output of both UUT and SDI Framer Model is provided as inputs to the data comparator module.

The data comparator checker compares the SDI data output from the UUT with the SDI data output from the SDI Framer Model. The module reports if there is any data mismatch between the output of the UUT and SDI Framer Model.

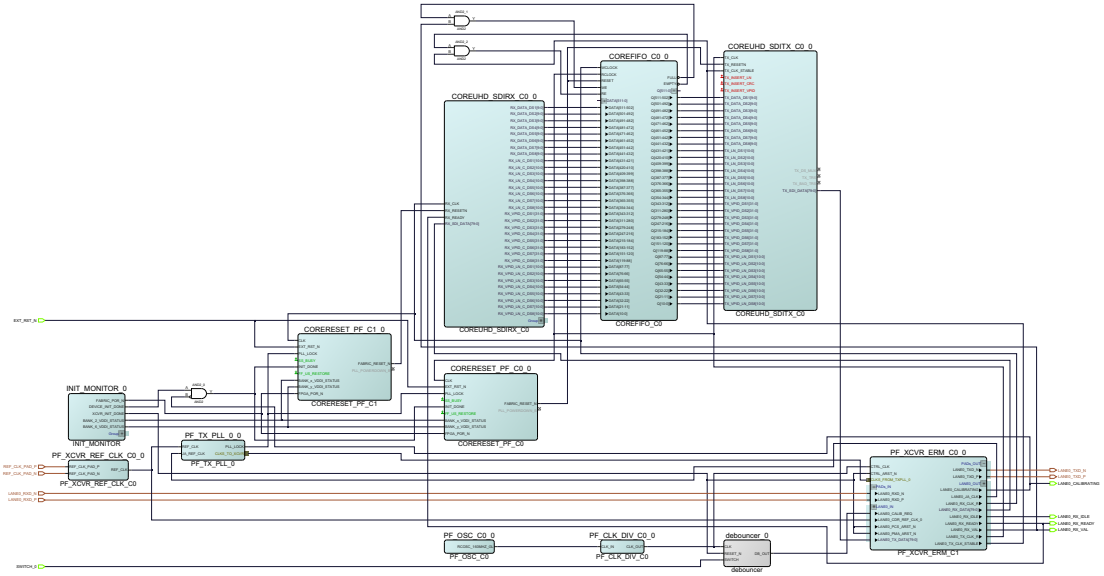
8 System Integration

In this example design:

- CoreUHD_SDIRX (COREUHD_SDIRX_C0_0) is configured in required SDI standard (HD-SDI and 3G-SDI/6G-SDI/12G-SDI). This core de-frames the SDI data stream into raw video data.
- CoreUHD_SDITX (COREUHD_SDITX_C0_0) is configured in required SDI standard (HD-SDI and 3G-SDI/6G-SDI/12G-SDI) same as COREUHD_SDIRX_C0_0. COREUHD_SDITX_C0_0 frames the raw data into SDI data stream.
- In HD-SDI standard, PF_XCVR_ERM (PF_XCVR_ERM_C0_0) is configured for data rate of 1485 Mbps in PMA mode with Receiver Calibration set to “CDR”, 20-bit interface data width, and 148.5 MHz reference clock.
- In 3G-SDI standard, PF_XCVR_ERM (PF_XCVR_ERM_C0_0) is configured for data rate of 2970 Mbps in PMA mode with Receiver Calibration set to “CDR”, 20-bit interface data width, and 148.5 MHz reference clock.
- In 6G-SDI standard, PF_XCVR_ERM (PF_XCVR_ERM_C0_0) is configured for data rate of 5940 Mbps in PMA standard with Receiver Calibration set to “CDR”, 40-bit interface data width, and 148.5 MHz reference clock.
- In 12G-SDI standard, PF_XCVR_ERM_C0_0 is configured for data rate of 11880 Mbps in PMA mode with Receiver Calibration set to “On Demand and First Lock”, 80-bit interface data width, and 148.5 MHz reference clock.
- XCVR_INIT_DONE signal of PF_INIT_MONITOR (INIT_MONITOR_0) is connected to PCS_RST_N, PMA_RST_N, and CTRL_ARST_N reset inputs of PF_XCVR_ERM_C0_0.
- LANE0_CDR_REF_CLK_0 input of PF_XCVR_ERM_C0_0 is driven by 148.5 MHz clock from REF_CLK of PF_XCVR_REF_CLK (PF_XCVR_REF_CLK_C0_0).
- CTRL_CLK (ERM clock) of PF_XCVR_ERM_C0_0 is driven by 40MHz clock generated from 160 MHz clock driven by OSC (PF_OSC_C0_0) using clock divider (PF_CLK_DIV_C0_0). This is applicable only for 6G-SDI and 12G-SDI data rates.
- The JA_CLK port of the PF_XCVR_ERM_C0_0 is enabled for jitter cleaning purpose.The value of JA PLL reference clock frequency in TX_PLL configurator should be the same as RX JA clock frequency in the Transceiver configurator.
- PF_TXPLL (PF_TX_PLL_0_0) is configured in jitter cleaning mode. REF_CLK of PF_XCVR_REF_CLK_C0_0 drives the REF_CLK input of PF_TX_PLL_0_0. JA_CLK port of the PF_XCVR_ERM_C0_0 drives the JA_REF_CLK input port of PF_TX_PLL_0_0.
- FABRIC_RESET_N from CoreRESET_PF (CORERESET_PF_C0_0) is connected to TX_RESETN input of COREUHD_SDITX_C0_0. FABRIC_RESET_N from CoreRESET_PF (CORERESET_PF_C1_0) is connected to RX_RESETN input of COREUHD_SDIRX_C0_0.
- RX_CLK of COREUHD_SDIRX_C0_0 is driven from LANE0_RX_CLK_R of PF_XCVR_ERM_C0_0 and TX_CLK of COREUHD_SDITX_C0_0 is driven from LANE0_TX_CLK_R of PF_XCVR_ERM_C0_0.
- The raw video data from COREUHD_SDIRX_C0_0 is looped back onto COREUHD_SDITX_C0_0 through CoreFIFO (COREFIFO_C0_0).
- The TX_INSERT_LN, TX_INSERT_CRC, and TX_INSERT_VPID inputs of COREUHD_SDITX_C0_0 are tied high, enabling insertion of LN packets, CRC packets and VPID packets.
- The C channel line number outputs, the C channel VPID data outputs, and the C channel VPID line number outputs of COREUHD_SDIRX_C0_0 are connected to the respective line number inputs, VPID inputs, and VPID line number inputs of COREUHD_SDITX_C0_0.

Note: Based on the image format transmitted, user can connect either C channel line number outputs, VPID outputs, and VPID line number outputs or Y channel line number outputs, VPID outputs, and VPID line number outputs from COREUHD_SDIRX_C0_0 to the line number inputs, the VPID inputs, and the VPID line number inputs of COREUHD_SDITX_C0_0.

Figure 9 • **System Integration**



9 References

- SMPTE ST 292-1 - 1.5 Gb/s Signal/Data Serial Interface
- SMPTE ST 424 - 3 Gb/s Signal/Data Serial Interface
- SMPTE ST 2081-1 - 6 Gb/s Signal/Data Serial Interface
- SMPTE ST 2082-1 - 12 Gb/s Signal/Data Serial Interface
- SMPTE ST 352 - Payload Identification Codes for Serial Digital Interface
- *UG0667 - Microsemi PolarFire FPGA User Guide*