CoreI2C v7.0 Release Notes

This is the production release for CoreI2C. These release notes describe the features and enhancements. They also contain information about system requirements, supported families, implementations, and known issues and workarounds.

Features

Intended Use

CoreI2C provides an APB-driven serial interface, supporting I^2C, SMBus, and PMBus data transfers. Several Verilog/VHDL parameters are available to minimize FPGA fabric area for a given application. CoreI2C also allows for multiple I^2C channels, reusing logic across channels to reduce overall tile count.

Key Features

- Conforms to the Philips Inter-Integrated Circuit (I^2C) v2.1 Specification (7-bit addressing format at 100 Kbps and 400 Kbps data rates)
- Supports SMBus v2.0 Specification
- Supports PMBus v1.1 Specification
- Data transfers up to at least 400 kbps nominally; faster rates can be achieved depending on external load and/or I/O pad circuitry
- Modes of operation configurable to minimize size
- Advanced Peripheral Bus (APB) register interface
- Multi-master collision detection and arbitration
- Own address and general call address detection
- Second Slave address decode capability
- Data transfer in multiples of bytes
- SMBus timeout and real-time idle condition counters
- IPMI 3 ms SCL low timeout
- Optional SMBus signals, SMBSUS_N and SMBALERT_N, controllable via APB IF
- Configurable spike suppression width
- Multiple channel configuration option

Interfaces

CoreI2C is available with an AMBA APB register interface.

Delivery Types

CoreI2C is licensed in two ways: Obfuscated and RTL.

Obfuscated

Complete RTL code is provided for the core, enabling the core to be instantiated with CoreConsole. Simulation, Synthesis, and Layout can be performed with Libero® Integrated Design Environment (IDE). The RTL code for the core is obfuscated, and some of the testbench source files are not provided. They are precompiled into the compiled simulation library instead.

RTL

Complete RTL source code is provided for the core and testbenches.

Supported Families

- IGLOO®
- IGLOOe
- IGLOO PLUS
- ProASIC®3
- ProASIC3E
- ProASIC3L
- Fusion
- ProASIC PLUS®
- Axcelerator®
- RTAX-S
- SmartFusion

Supported Tool Flows

CoreI2C requires SmartDesign and Actel Libero IDE v8.6 and later.

Installation Instructions

Use Libero® Integrated Design Environment (IDE) to install the CoreFFT CPZ.

Within Libero IDE, click the **Add Core** button in the Catalog window to locate and install a local CPZ file, or use the automatic web update feature in Libero IDE. Once the *.cpz file is installed in Libero IDE, the core can be configured, generated, and instantiated within SmartDesign for inclusion in your Libero IDE project.

Documentation

The release contains a copy of the *CoreI2C Handbook*. The handbook describes the core functionality and gives step-by-step instructions on how to simulate, synthesize, and place-and-route this core, as well as implementation suggestions.

For updates and additional information about the software, devices, and hardware visit the Intellectual Property pages on the Actel website at www.actel.com.

Supported Test Environments

The following test environments are supported:

- VHDL user testbench
- Verilog user testbench

Known Limitations and Workarounds

There are no known limitations or workarounds with the CoreI2C v7.0 release.

Release History

Table 1 provides the release history of CoreI2C.

Table 1 · CoreI2C Release History

Version	Date	Changes
7.0	June, 2011	Interrupt generation after STOP bit is sent. I2C slave 2nd address capability functionality corrected (SAR 30964). Operation details for Master mode example updated.
6.0	Nov. 2009	Remove 50 µs SMBus idle condition check (not required). Multiple channel mode, up to 16 I^2C/SMBus channels on a single APB interface. Improved tile utilization.
5.0	Nov. 2008	Added the ability to further reduce tile count by hardwiring some configuration parameters. Added IPMI SCL low timeout functionality. Added second slave address capability. Configurable spike suppression width.
4.0	Aug. 2008	Start hold timing violation corrected. Serviced many software action requests (SARs). SMBus/PMBus functionality added to v4.0. IGLOO/e device support added. Added synthesis constraint to prevent Synopsys® tile error when using FSM compiler. Added Master Transmit and Slave Receive modes to reduce tile counts for write-only applications.
3.0	Nov. 2007	Switched from SFR to APB interface.
2.1	Jan. 2005	Discontinued support of Actel A54SX and eX families.
2.0	Aug. 2003	Initial release.

Resolved Issues in the v7.0 Release

Table 2 lists the Software Action Requests (SARs) that were resolved in the CoreI2C v7.0 release.

Table 2 · Resolved Issues in the v7.0 Release

SAR	Description
25023	A pending Master Tx aborts (NACK) concurrent Slave Rx.
25400	SMBus Timeout Issue During Master TX/RX transaction.
25401	IPMI timeout issue during Master TX/RX transactions.
29537	Generate an interrupt after STOP bit is set.
30964	I2C slave 2nd address capability doesn't work.

Resolved Issues in the v6.0 Release

Table 3 lists the Software Action Requests (SARs) that were resolved in the CoreI2C v6.0 release.

Table 3 · Resolved Issues in the v6.0 Release

SAR	Description
20288	Remove 50 µS SMBus idle condition check (not required).

Resolved Issues in the v5.0 Release

Table 4 lists the Software Action Requests (SARs) that were resolved in the CoreI2C v5.0 release.

Table 4 · Resolved Issues in the v5.0 Release

SAR	Description
78614	Fixed GlitchReg Value parameter.
78611	Required SMBus Optional Signal Interrupts.
78608	3 ms IPMI timeout required.
78610	IPMI extra Slave Address mode
78609	Fixed Slave Address mode for decreasing tile count
78613	Changed I2CCLK and I2CDAT signals to SCL/SDA.
78612	Fixed Baud Rate (saves about 50 tiles)
78560	The SMBUS signals float when not in use

Resolved Issues in the v4.0 Release

Table 5 lists the Software Action Requests (SARs) that were resolved in the CoreI2C v4.0 release.

Table 5 · Resolved Issues in the v4.0 Release

SAR	Description
78449	Device/family metadata issues - v4.0.106.
78444	Added synthesis constraint to prevent Synplicity tile error.
78443	Added SMBus functionality.
78220	CCZ verification: Synthesis warnings
77968	Request for a Master Transmit, Slave Receive mode to reduce tile counts for IPMI or any write-only application
77967	Start hold timing violation corrected.
69300	The handbook needs to describe the open drain I/O.
68890	CoreI2C simulation in Evaluation mode
68382	Utilization in VHDL is about two times that of Verilog.
68111	SPIRIT description missing link between APBslave i/f and RegisterMap
67496	CoreI2C shows up under non-AMBA bus list.
67475	The link to the datasheet for CoreI2C in CoreConsole does not work.
67474	Block diagram for CoreI2C does not show BCLK.
67450	CoreConsole does not generate C code for I^2C.
66806	Update the Data Transfers rate.
66574	Request to show the open drain configuration in the handbook.
65986	Data should be labeled PWDATA instead of PRDATA.
62885	Link to datasheet in core description is broken.

Resolved Issues in the v3.0 Release

Table 6 lists the Software Action Requests (SARs) that were resolved in the CoreI2C v3.0 release.

Table 6. Resolved Issues in the v3.0 Release

SAR	Description
62412	An APB interface has been added and the SFR interface has been removed for use with CoreConsole in bus-centric designs.
57330	The datasheet provided with previous versions of the core incorrectly described serdati as “serial clock input.” The datasheet has since been superseded by a handbook, which accurately describes the serial data input (I2CDATI).

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