CorePWM v4.1 Release Notes

This is the production release for CorePWM. These release notes describe the features and enhancements. They also contain information about system requirements, supported families, implementations, and known issues and workarounds.

Features

Intended Use

CorePWM is a general purpose, multi-channel pulse width modulator (PWM) module for motor control, tone generation, battery charging, heating elements, and more.

In General Purpose PWM mode, duty cycle updates can be performed asynchronously or synchronously, based on parameter selection. In synchronous mode, all channels are updated at the beginning of the PWM period, which is useful for motor control and can be used to keep a constant dead band space between channel waveforms. Asynchronous mode is relevant to applications such as LED control, where synchronous updates are not required. Asynchronous mode lowers the area size, reducing shadow register requirements.

In addition to the general purpose PWM modes, there is a "Low Ripple DAC" mode that creates a minimum period pulse train whose High/Low average is that of the chosen duty cycle. When used with a low-pass filter (such as a simple RC circuit), a DAC can be created with far better bandwidth and ripple performance than a standard PWM algorithm can achieve. This type of DAC is ideally suited for fine tuning of power supply output levels.

CorePWM also provides support for tachometer monitoring of 3- and 4-wire fans. Incoming tachometer data is read by the firmware through the APB interface to calculate fan speed.

Key Features

- Configuration updates for all channels can be synchronized to the beginning of the PWM period, allowing precise updates and maintaining phase alignments between channels
- Configurable resolution based on the APB bus width
- Low-cost PWM solution with up to 16 separate PWM digital outputs, configurable via a register interface
- For DAC applications: Optional, per-channel Low Ripple DAC mode, allowing for greater resolution output of a given filter
- Low-cost TACHOMETER solution with up to 16 separate TACH digital inputs, configurable via a register interface
- All PWM outputs are double-edge-controlled
- Per-channel fixed register option for lower tile count
- Edge control based on a configurable PWM period with prescaler value and 0% to 100% duty cycle capability
- Set High, set Low, and Toggle Edge-Control modes
- Can be programmed on-the-fly from a microcontroller, such as Core8051s, CoreABC
- Can be used to perform open or closed-loop margining of power supplies

Interfaces

CorePWM is available with an AMBA APB register interface.

Delivery Types

CorePWM is licensed in two ways: Obfuscated and RTL.

Obfuscated

Complete RTL code is provided for the core, enabling the core to be instantiated with SmartDesign. Simulation, Synthesis, and Layout can be performed with Actel Libero® Integrated Design Environment (IDE). The RTL code for the core is obfuscated, and some of the testbench source files are not provided. They are pre-compiled into the compiled simulation library instead.

RTL

Complete RTL source code is provided for the core and testbenches.

Supported Families

- IGLOO®/e
- ProASIC®3/E/L
- Fusion
- ProASIC PLUS®
- Axcelerator®
- RTAX-S
- RTAX-DSP

Supported Tool Flows

Requires Libero IDE v8.6 or later.

Installation Instructions

The CorePWM CCZ file must be installed into Libero IDE. Within Libero IDE, click the **Add Core** button in the Catalog to locate and install a local CCZ file, or use the automatic web update feature in Libero IDE. Once the CCZ file is installed in Libero IDE, the core can be instantiated, configured, and generated within SmartDesign for inclusion in your Libero IDE project. Refer to the Libero IDE online help for further instructions on core installation, licensing, and general use.

Documentation

The release contains a copy of the *CorePWM Handbook*. The handbook describes the core functionality, gives step-by-step instructions on how to simulate, synthesize, and place-and-route the core, and includes implementation suggestions.

For updates and additional information about the software, devices, and hardware, visit the Intellectual Property pages on the Actel website at http://www.actel.com.

Supported Test Environments

The following test environments are supported:

- VHDL user testbench
- Verilog user testbench

Discontinued Features and Devices

No features have been discontinued in the v4.1 CorePWM release.

New Features and Devices

- Modified TACH logic to remove any dependency on PWM_STRETCH
- Modified SmartDesign configuration to support the number of PWM and TACH channels as independent values

Release History

Table 1 provides the release history of CorePWM.

Table 1 · Release History of CorePWM

Version	Date	Changes
4.1	February 2010	Modified the TACHMODE operation implementation.
4.0	November 2009	Added center-aligned PWM and TACH interface support.
3.0	August 2008	Added Low Ripple DAC mode and changed the configurable number of PWM outputs from 1 to 16.
2.0	April 2006	First production release.

Resolved Issues in the v4.1 Release

Table 2 lists the Software Action Requests (SARs) that were resolved in the CorePWM v4.1 release.

Table 2 · Resolved Issues in the v.4.1 Release

SAR	Description
22676	Modified the implementation of TACHMODE operation when set to "0".

Resolved Issues in the v4.0 Release

Table 3 lists the Software Action Requests (SARs) that were resolved in the CorePWM v4.0 release.

Table 3 · Resolved Issues in the v.4.0 Release

SAR	Description
19605	Added center-aligned PWM support.

Resolved Issues in the v3.0 Release

Table 4 lists the Software Action Requests (SARs) that were resolved in the CorePWM v3.0 release.

Table 4 · Resolved Issues in the v.3.0 Release

SAR	Description
78524	Added configurable number of outputs, from 1 to 16.
78523	Added Low Ripple DAC mode.
78522	Added configurable resolution based on the APB bus.
61834	In version 2.0 of CorePWM, the PWM_NUM parameter is fixed at 8 due to previous CoreConsole limitations. This issue has been fixed.

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