UG0646

User Guide

Display Enhancement

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Microsemi

Power Matters.™

Contents

1 Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

1.1 Revision 3.0

In revision 3.0 of this document, the Resource Utilization section and the Resource Utilization Report were updated. For more information, see Resource Utilization (see page 6).

1.2 Revision 2.0

The following is a summary of changes in revision 2.0 of this document.

- Updated the Top-Level Block Diagram of Display Enhancement Inputs and Outputs figure and the Input and Output Ports of the Display Enhancement Module table. For more information, see Top-Level Block Diagram of Display Enhancement Inputs and Outputs (see page 3) and Input and Output Ports of the Display Enhancement Module (see page 4) for clock parameter name change (SAR 75773).
- Added the Testbench section as per SAR 75773. For more information, see Testbench (see page 6) .

1.3 Revision 1.0

Revision 1.0 is the first publication of this document.

2 Introduction

Display Enhancement module enables you to adjust the brightness, contrast, saturation, and hue of the final video display to personal preferences. These adjustments are done on YCbCr color space as calculations are simpler compared to RGB domain.

The following equations are for adjusting brightness, contrast, saturation, and hue values on Y, Cb, and Cr:

EQ1: Y' = ((Y – 16)×C) + B +16

EQ2: Cb" = (((Cb – 128)×Cos(H) + (Cr – 128)×Sin(H))×C×S) + 128

EQ3: Cr" = (((Cr – 128)×Cos(H) – (Cr – 128)×Sin(H))×C×S) + 128

Where,
B = Brightness constant
C = Contrast constant
S = Saturation constant
H = Hue angle

In EQ1, input Y value is subtracted by number 16 to position the black level at zero. It removes the DC offset, therefore adjusting the contrast does not vary the black level. Multiply the YCbCr pixel values by a constant to adjust the contrast. If Cb and Cr are not adjusted, color shift will result whenever the contrast is changed. The brightness value is added or subtracted from the contrast adjusted Y value. Brightness control is done after the contrast control to avoid introducing a varying DC offset due to contrast adjustment. The value 16 is added to bring back the black level at 16.

In EQ2 and EQ3, inputs Cb and Cr values are subtracted by 128 to position the range about zero. The subtraction of Cb and Cr values by 128 can result in negative values which needs to addressed. The hue value is adjusted by mixing the Cb and Cr values, as shown in EQ2 and EQ3. Saturation and Contrast values are adjusted by multiplying the hue mixed Cb and Cr values by a pair of constants, and then by adding 128 to resultant Cb and Cr.

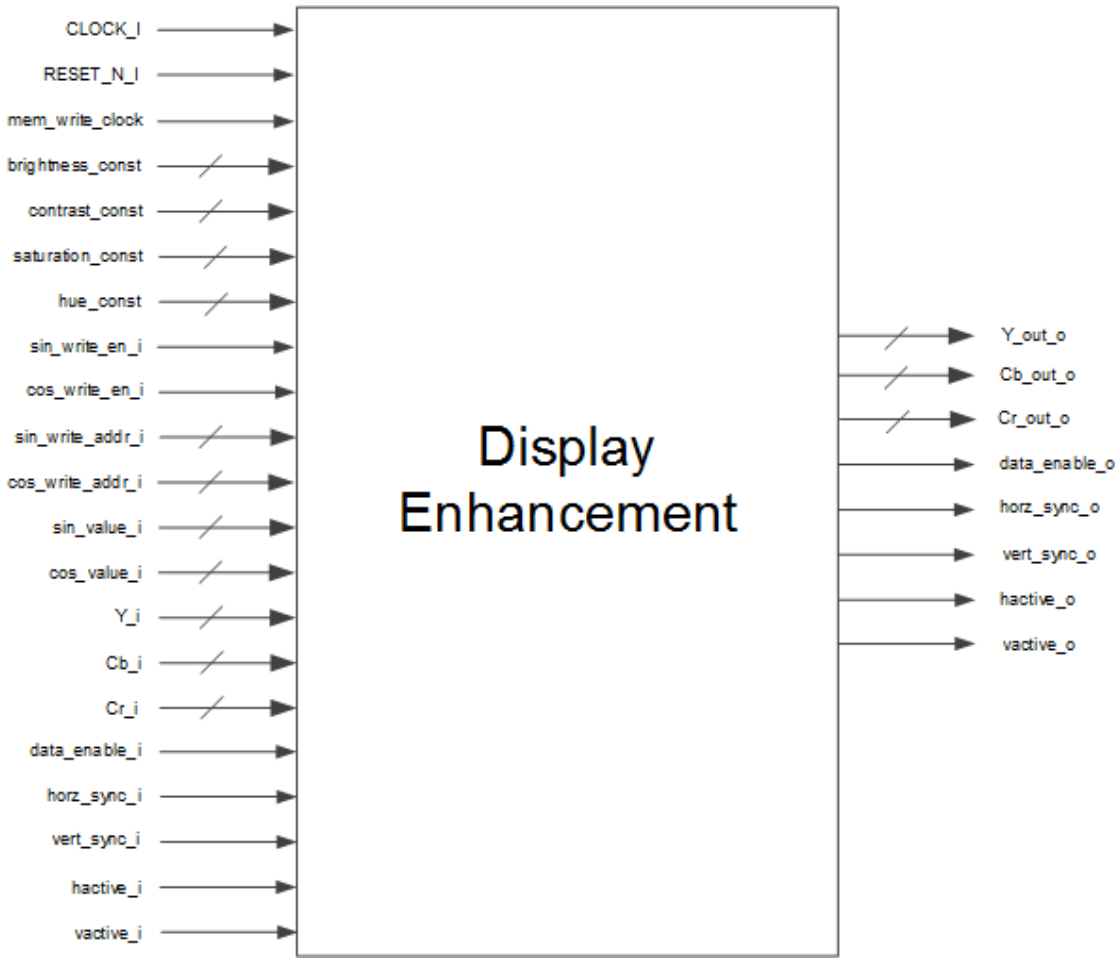
3 Hardware Implementation

3.1 Design Description

The display enhancement module performs the adjustment of brightness, contrast, saturation, and hue as per the equations mentioned in the Design Description section. The module takes YCbCr inputs and outputs the resultant YCbCr after computation. It receives signed values of brightness, contrast, saturation, and hue as inputs from an external controller. It also takes data enable, horizontal, and vertical sync signals as inputs, and pipelines them to match the converted video data outputs.

The following figure shows the top-level input and output signals of the display enhancement module.

Figure 1 • Top-Level Block Diagram of Display Enhancement Inputs and Outputs



3.2 Inputs and Outputs

The following table lists the input and output ports of the display enhancement module.

Table 1 • Input and Output Ports of the Display Enhancement Module

Signal Name	Direction	Width	Description
RESET_N_I	Input	–	Active low asynchronous reset signal to design
VIDEO_CLOCK_I	Input	–	System clock input
mem_write_clock	Input	–	Sine-cosine memory write clock
Y_i	Input	[(g_YCbCr_DATA_BIT_WIDTH -1) : 0]	Luma input value
Cb_i	Input	[(g_YCbCr_DATA_BIT_WIDTH -1) : 0]	Cb input value
Cr_i	Input	[(g_YCbCr_DATA_BIT_WIDTH -1) : 0]	Cr input value
data_enable_i	Input	–	Video data enable input
horz_sync_i	Input	–	Horizontal sync signal
vert_sync_i	Input	–	Vertical sync signal
brightness_i	Input	[(g_B_C_SAT_CONSTANT_WIDTH-1): 0]	Input brightness constant
contrast_i	Input	[(g_B_C_SAT_CONSTANT_WIDTH-1): 0]	Input contrast constant
saturation_i	Input	[(g_B_C_SAT_CONSTANT_WIDTH-1): 0]	Input saturation constant
hue_i	Input	[(g_HUE_CONSTANT_WIDTH -1):0]	Input hue angle constant
sin_write_en_i	Input	–	Sine memory write enable
cos_write_en_i	Input	–	Cosine memory write enable
sin_write_addr_i	Input	[7:0]	Sine memory write address
cos_write_addr_i	Input	[7:0]	Cosine memory write address
sin_value_i	Input	[(g_SIN_COS_DWIDTH-1):0]	Input sine value
cos_value_i	Input	[(g_SIN_COS_DWIDTH-1):0]	Input cosine value
hactive_i	Input	–	Horizontal active input
vactive_i	Input	–	Vertical active input
Y_out_o	Output	[(g_YCbCr_DATA_BIT_WIDTH -1) : 0]	Resultant luma output value
Cb_out_o	Output	[(g_YCbCr_DATA_BIT_WIDTH -1) : 0]	Resultant Cb output value
Cr_out_o	Output	[(g_YCbCr_DATA_BIT_WIDTH -1) : 0]	Resultant Cr output value
data_enable_o	Output	–	Video data enable output
horz_sync_o	Output	–	Horizontal sync signal
vert_sync_o	Output	–	Vertical sync signal
hactive_o	Output	–	Horizontal active output
vactive_o	Output	–	Vertical active output

For hue adjustments, the sine and cosine values for angles ranging from 0° to 180° are received from an external controller, which are stored in the block's internal ram buffers. The –180° to –1° angle values are calculated by performing required manipulation on the corresponding sine and cosine values of the absolute value of the angle from the ram buffer.

The following table lists the input value range for every adjustment parameter.

Table 2 • Input Value Range for Adjustment Parameters

Value Range	Parameters
Brightness	–128 to 127
Contrast	–128 to 127
Saturation	–128 to 127
Hue	–180°to 180°

In the display enhancement module, the Y, Cb, and Cr values for each pixel are sign extended to perform all the sign calculations. It checks the overflow and underflow conditions by saturating the final luma Y value in 16–235 range and Cb and Cr values in 16–240 range.

3.3 Configuration Parameters

The following table lists the configuration parameters used in the hardware implementation of the display enhancement module. These parameters are generic and can be varied based on the application requirement.

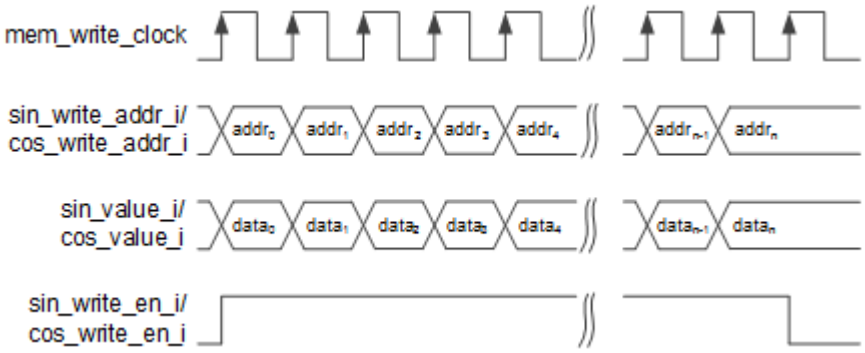
Table 3 • Configuration Parameters of the Display Enhancements

Name	Description
g_B_C_SAT_CONSTANT_WIDTH	Brightness, contrast, and saturation constants data bit width
g_YCbCr_DATA_BIT_WIDTH	YCbCr data bit width
g_HUE_CONSTANT_WIDTH	Hue degree data bit width
g_SIN_COS_DWIDTH	Data width of sine and cosine values for the hue degree value
g_SIN_COS_MEM_DEPTH	Depth of the memory storing the sine and cosine values for the hue degree value

3.4 Timing Diagrams

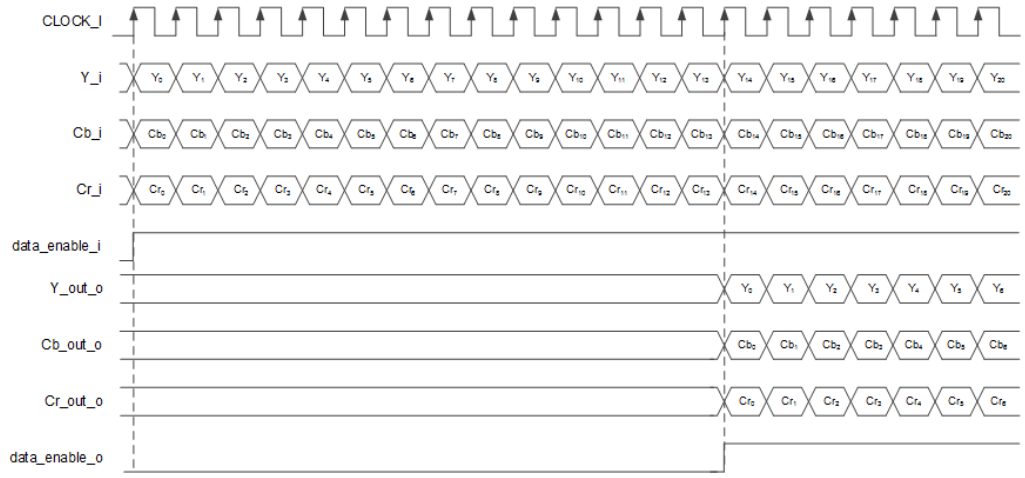
The following figure shows writing of sine and cosine values into the internal memory. It shows the connection between address inputs sin_write_addr_i/cos_write_addr_i, data inputs sin_value_i/ cos_value_i, and write Eeable Inputs sin_write_en_i/cos_write_en_i.

Figure 2 • Timing Diagram



The following figure shows the connection between the YCbCr and data_enable inputs and the corresponding YCbCr and data_enable output.

Figure 3 • Timing Diagram of the YCbCr Input and YCbCr Output for the Display Enhancement Module



3.5 Testbench

A testbench is provided to check the functionality of display enhancement core. The following table lists the parameters that can be configured according to application.

Table 4 • Configuration Parameters

Name	Description
CLKPERIOD	Clock period
HEIGHT	Height of the image
WIDTH	Width of the image
WRITE_CLK	Clock period of Sine-Cosine memory write clock
DATA_BIT_WIDTH	RGB data bit width
WAIT	Delay between two lines of input (Image)
IMAGE_FILE_NAME	Input (image) file name

3.6 Resource Utilization

The display enhancement block is implemented on an M2S150T SmartFusion®2 System-on-Chip (SoC) FPGA in the FC1152 package) and PolarFire FPGA (MPF300TS_ES - 1FCG1152E package).

Table 5 • Resource Utilization of Display Enhancement Module

Resource	Usage
DFFs	1010
4-input LUTs	520
MACC	9
RAM1Kx18	2
RAM64x18	0

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