RN0032
Release Notes
CorePWM v4.5

Microsemi
a Microchip company

Microsemi Headquarters
One Enterprise, Aliso Viejo,
CA 92656 USA
Within the USA: +1 (800) 713-4113
Outside the USA: +1 (949) 380-6100
Sales: +1 (949) 380-6136
Fax: +1 (949) 215-4996
Email: sales.support@microsemi.com
www.microsemi.com

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1 Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

1.1 Revision 9.0

Added PolarFire® SoC support.

1.2 Revision 8.0

The following is a summary of the changes made in this revision.

- Added RTG4 information in Supported Families and Utilization and Performance Tables.
- Updated core version to 4.4 in Core Version.

1.3 Revision 7.0

Added support for PolarFire®.

1.4 Revision 6.0

Added support for RTG4™.

1.5 Revision 5.0

Updated handbook with the supported new families and added support for a separate PWM clock.

1.6 Revision 4.0

Modified the TACHMODE operation implementation.

1.7 Revision 3.0

Added center-aligned PWM and TACH interface support.

1.8 Revision 2.0

Added Low Ripple DAC mode and changed the configurable number of PWM outputs from 1 to 16.

1.9 Revision 1.0

Initial release.

Contents

Tables

2 CorePWM v4.5

This is the production release for CorePWM. These release notes describe the features and enhancements. They also contain information about system requirements, supported families, implementations, and known issues and workarounds.

2.1 Features

2.1.1 Intended Use

CorePWM is a general purpose, multi-channel pulse width modulator (PWM) module for motor control, tone generation, battery charging, heating elements, and more.

In General Purpose PWM mode, duty cycle updates can be performed asynchronously or synchronously, based on parameter selection. In synchronous mode, all channels are updated at the beginning of the PWM period, which is useful for motor control and can be used to keep a constant dead band space between channel waveforms. Asynchronous mode is relevant to applications such as LED control, where synchronous updates are not required. Asynchronous mode lowers the area size, reducing shadow register requirements.

In addition to the general purpose PWM modes, there is a “Low Ripple DAC” mode that creates a minimum period pulse train whose High/Low average is that of the chosen duty cycle. When used with a low-pass filter (such as a simple RC circuit), a DAC can be created with far better bandwidth and ripple performance than a standard PWM algorithm can achieve. This type of DAC is ideally suited for fine tuning of power supply output levels.

CorePWM also provides support for tachometer monitoring of 3- and 4-wire fans. Incoming tachometer data is read by the firmware through the APB interface to calculate fan speed.

2.1.2 Key Features

- Configuration updates for all channels can be synchronized to the beginning of the PWM period, allowing precise updates and maintaining phase alignments between channels
- Configurable resolution based on the APB bus width
- Low-cost PWM solution with up to 16 separate PWM digital outputs, configurable via a register interface
- For DAC applications: Optional, per-channel Low Ripple DAC mode, allowing for greater resolution output of a given filter
- Low-cost TACHOMETER solution with up to 16 separate TACH digital inputs, configurable via a register interface
- All PWM outputs are double-edge-controlled
- Per-channel fixed register option for lower tile count
- Edge control based on a configurable PWM period with prescaler value and 0% to 100% duty cycle capability
- Set High, set Low, and Toggle Edge-Control modes
- Can be programmed on-the-fly from a microcontroller, such as Core8051s, CoreABC, or the Fusion backbone
- Can be used to perform open or closed-loop margining of power supplies

2.2 Interfaces

CorePWM is available with an AMBA APB register interface.

2.3 Delivery Types

CorePWM is license free.

2.3.1 RTL

Complete RTL source code is provided for the core and testbenches.

2.4 Supported Families

- PolarFire® SoC
- PolarFire®
- RTG4™
- SmartFusion®2
- IGLOO®2
- IGLOO®/e
- ProASIC®3/E/L
- Fusion
- ProASIC PLUS®
- Axcelerator®
- RTAX-S
- RTAX-DSP
- SmartFusion®

2.5 Supported Tool Flows

Requires Libero IDE v8.6 or later.

2.6 Installation Instructions

The CorePWM CPZ file must be installed into Libero software. This is done automatically through the Catalog update function in Libero, or the CPZ file can be manually added using the **Add Core** catalog feature. Once the CPZ file is installed in Libero, the core can be configured, generated, and instantiated within SmartDesign for inclusion in the Libero project. For more information, see the *Knowledge Based article*.

To know how to create SmartDesign project using the IP cores, refer to *Libero SoC documents page* and use the latest SmartDesign user guide.

2.7 Documentation

This release contains a copy of the *CorePWM Handbook*. The handbook, describes the core functionality and gives step-by-step instructions on how to simulate, synthesize, and place-and-route this core, and also implementation suggestions. Refer to *Libero SoC documents page* for instructions on obtaining IP documentation.

For updates and additional information, visit the Intellectual Property pages on the Microsemi SoC Products Group website: visit:

http://www.microsemi.com/products/fpga-soc/design-resources/ip-cores.

2.8 Supported Test Environments

The following test environments are supported:

- VHDL user testbench
- Verilog user testbench

2.9 Resolved Issues in v4.5 Release

There were no software action requests (SARs) resolved. PolarFire SoC support is added.

2.10 Resolved Issues in v4.4 Release

There are no resolved issues with the CorePWM v4.4 release.

2.11 Resolved Issues in v4.3 Release

There are no resolved issues with the CorePWM v4.3 release.

2.12 Resolved Issues in v4.2 Release

Table 1, page 8 lists the Software Action Requests (SARs) that were resolved in the CorePWM v4.2 release.

Table 1 • **Resolved Issues in the v.4.2 Release**

SAR	Description
32275	Enhancement request for dual APB and PWM clock.
36469	Stop Tach ports from generating when in PWM only mode.
26900	Add control in configuration GUI to prevent error configuration (APB_DWIDTH > PWM_NUM).
46409	Port tie offs incorrect due to packager port ranges.

2.13 Resolved Issues in v4.1 Release

Table 2, page 8 lists the SARs that were resolved in the CorePWM v4.1 release.

Table 2 • **Resolved Issues in the v.4.1 Release**

SAR	Description
22676	Modified the implementation of TACHMODE operation when set to "0".

2.14 Resolved Issues in v4.0 Release

Table 3, page 8 lists the Software Action Requests (SARs) that were resolved in the CorePWM v4.0 release.

Table 3 • **Resolved Issues in the v.4.0 Release**

SAR	Description
19605	Added center-aligned PWM support.

2.15 Resolved Issues in v3.0 Release

Table 4, page 8 lists the Software Action Requests (SARs) that were resolved in the CorePWM v3.0 release.

Table 4 • **Resolved Issues in the v.3.0 Release**

SAR	Description
78524	Added configurable number of outputs, from 1 to 16.
78523	Added Low Ripple DAC mode.
78522	Added configurable resolution based on the APB bus.
61834	In version 2.0 of CorePWM, the PWM_NUM parameter is fixed at 8 due to previous CoreConsole limitations. This issue has been fixed.